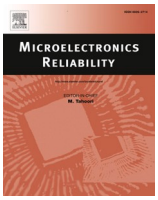
Microelectronics Reliability 150 (2023) 115131

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Impact of high-temperature operating lifetime tests on the stability of 0.15 μm AlGaN/GaN HEMTs: A temperature-dependent analysis

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ARTICLE INFO

Keywords:
GaN
HEMT
Millimiter-wave
HTOL
Threshold voltage shift
Trapping
Hot-electrons
Reliability

ABSTRACT

We present a detailed analysis of the effect of low- and high-temperature operating lifetime (LTOL and HTOL) carried out on 0.15 μm GaN HEMTs for RF applications. Based on several stress experiments carried out at different temperature levels, a) we demonstrate the existence of two degradation modes consisting, respectively, in the negative and positive shift in the threshold voltage; b) temperature-dependent I-V measurements indicate that no modification in the Schottky barrier height takes place after stress; c) the negative V_{TH} shift is ascribed to the temperature- and field-assisted de-trapping of electrons from the passivation/AlGaN stack under the gate, consistent with previous reports; d) the positive V_{TH} shift, which only occurs at high temperature levels, is ascribed to the trapping of hot electrons, possibly at the AlGaN/SiN interface.

1. Introduction

The high electron mobility transistor (HEMT) based on AlGaN/GaN heterostructures is considered a key device for high-power, high-frequency radio frequency (RF) applications. However, the performance of these devices can be adversely affected by the high-temperature operating environment [1,2], leading to a parametric shift of the main parameters, which worsens the performance of transistors over time.

Understanding the underlying mechanisms is critical for the reliable operation of these devices at high power densities and temperatures. Standard tests that investigate the effects of both temperature and electric field on the reliability of silicon devices have been applied also to wide-bandgap semiconductor devices [3]. Many published works investigated the effects of both temperature and bias on the performances of AlGaN/GaN HEMT. Most of them consist in long-term stresses with a duration of thousands of hours in which the first interim characterization measurement can be found after 1 h from the start of the test [4–6]. Only few reports evaluated the behavior of the devices in the first hours of operation with great accuracy.

In this article, we study the effect of both temperature and electric field on 0.15 μm AlGaN/GaN HEMT for RF application through short-term low- and high- temperature operating lifetime (LTOL and HTOL) tests. Specifically, we analyzed the changes in the main device parameters (e.g., threshold voltage, saturation current, on-resistance) of the devices over time by performing interim DC characterizations already after 1 s of stress.

The obtained results show a non-monotonic behavior of the threshold voltage (V_{TH}). In absence of a Schottky barrier height (SBH) modification, these parametric shifts may be related to de-trapping/trapping phenomena occurring, respectively, under the gate stack and at the AlGaN/passivation interface.

The results presented in this paper provide a valuable contribution to understanding of the high-temperature parametric shift of AlGaN/GaN HEMTs, which is crucial for ensuring the reliable operation of these devices in harsh high-power and high-frequency RF applications [7,8].

2. Tested devices & methods

A simplified example of the device under test (DUT) structure is visible in Fig. 1.

The devices analyzed are on-wafer AlGaN/GaN HEMTs with two fingers having a gate width Wg = 2 × 35 μm and gate length Lg = 150 nm. The gate-to-source and gate-to-drain distances are respectively Lgs = 0.8 μm and Lgd = 1.5 μm, resulting in an asymmetric structure. A

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https://doi.org/10.1016/j.microrel.2023.115131
Received 31 May 2023; Received in revised form 28 June 2023; Accepted 13 July 2023
Available online 1 October 2023

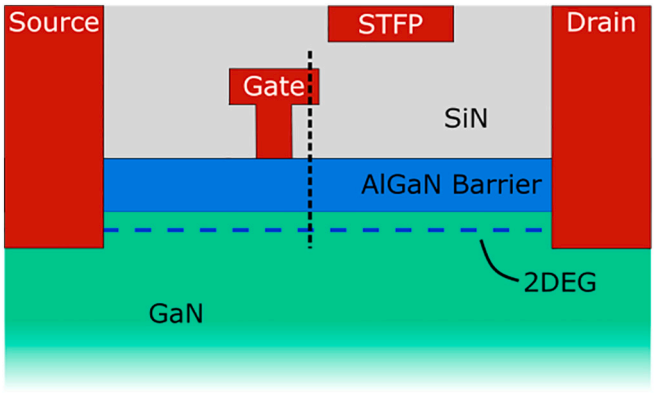


Fig. 1. Simplified structure of the DUT where only one finger is shown.

Table 1
Stress parameters for the LTOL and the HTOL test.

T [°C]	Vds [V]	Vgs [V]	Time [h]
RT	20	−2.59	400
55	20	−2.64	68
80	20	−2.61	24
140	20	−2.65	24
200	20	−2.76	14
250	20	−2.86	24

source-terminated field plate (STFP) is also used to obtain a better distribution of the electric field. A SiN passivation was deposited by plasma-enhanced chemical vapor deposition (PECVD), while gate foot etching is performed by CF4 plasma. Being a two-finger device, the layout also features an air bridge.

We performed low-temperature operating lifetime tests (LTOL) at four different baseplate temperatures: room temperature (RT), 55 °C, 80 °C, and 140 °C. HTOL was performed at 200 °C and 250 °C.

Every test was performed with an applied drain bias of $V_{DS} = 20$ V, for all samples, the gate bias V_{GS} was adjusted to obtain an initial drain-source current equal to $I_{DS} = 100$ mA/mm.

To determine the value of V_{GS}, we performed, at the chosen baseplate temperature, five I_{DS}-V_{GS} characterizations at $V_{DS} = 20$ V with a current compliance of 100 mA/mm, and selected the last V_{GS} value before compliance is reached at the fifth measurement. The number of five I_{DS}-V_{GS} was chosen to obtain a stable V_{GS} value, since variations are observed if the compliance current value is applied for long periods of time.

The DC parameters of the device are collected at the chosen baseplate temperature, after exponentially longer stress periods (e.g., 1, 2, 5, 10, 60, 120, 300, 600 s), with a delay of 120 s between the end of the stress phases and the electrical characterization. The delay time was introduced to allow device cool down before characterization. Previous experiments on the same devices showed that 120 s are enough for the device to return to the baseplate temperature after the stress segment. The drain and the gate stress current were measured during the full duration of the stress.

3. Results & discussion

The stress parameters to which the devices have been subjected are listed in Table 1. As can be observed, the V_{GS} value necessary to obtain the initial $I_{DS} = 100$ mA/mm condition decreases with temperature. This is explained considering the temperature dependence of the threshold voltage, which shows a negative shift with increasing temperature [9].

The variation of the drain-to-source current I_{DS} obtained during the LTOL (Fig. 2a) shows two phases: a fast increase and a slow decrease, the latter only visible at 80 °C and 140 °C and for longer stress periods

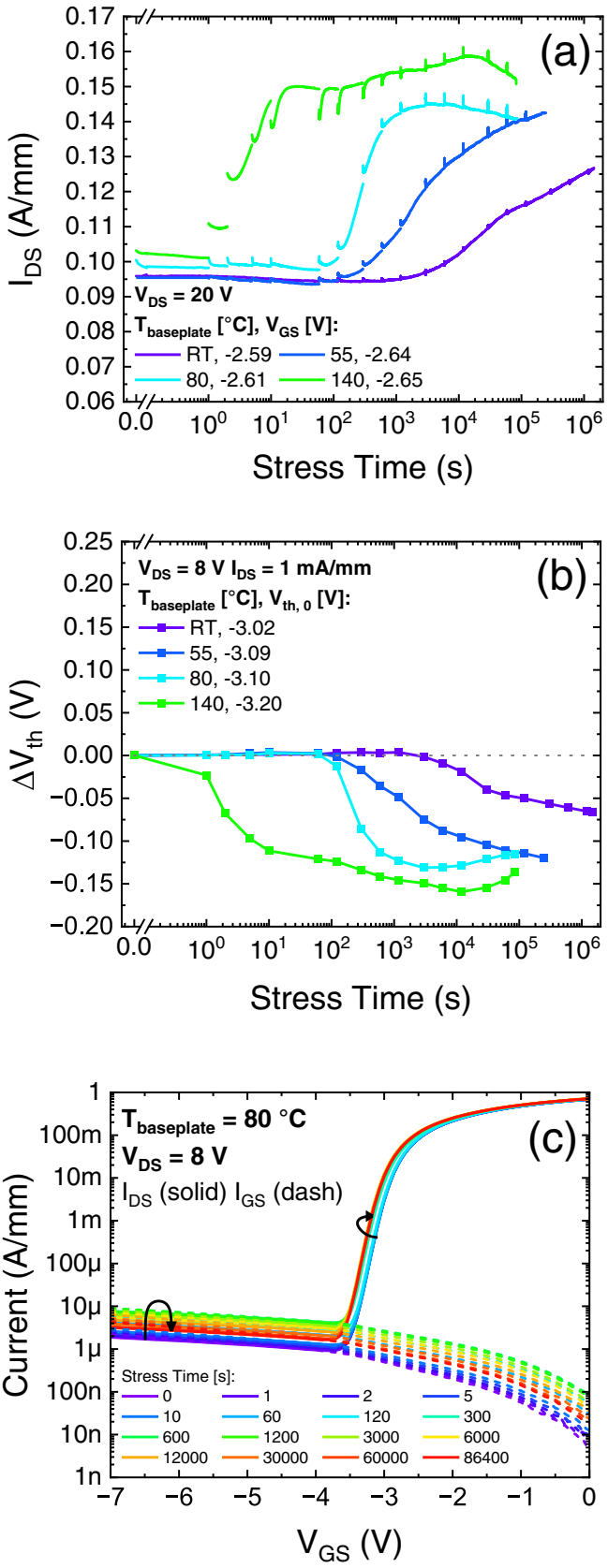
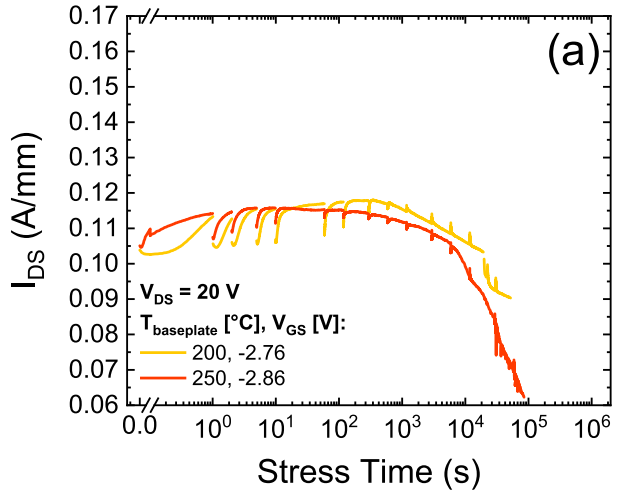
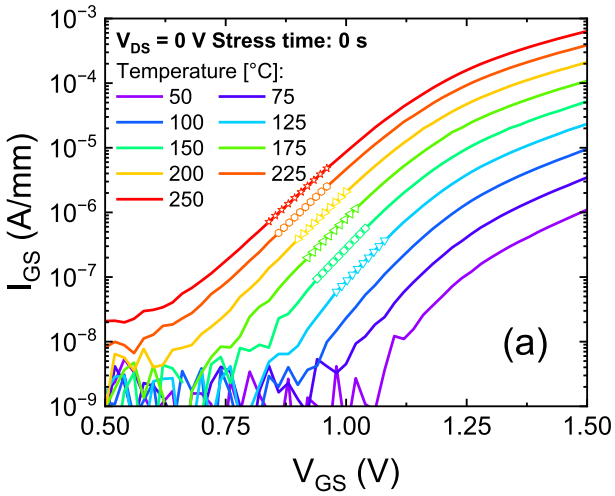
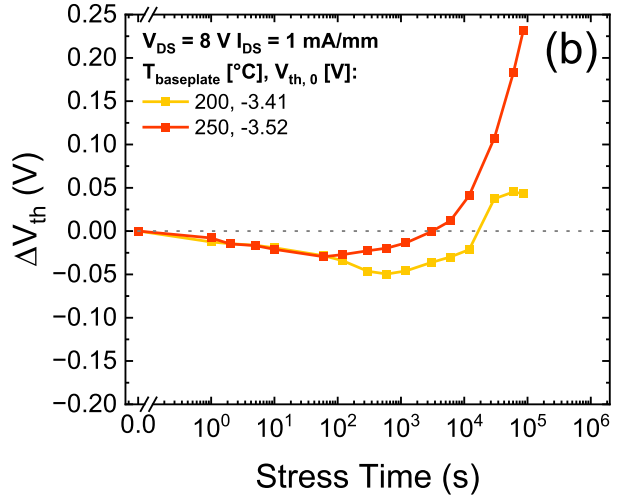
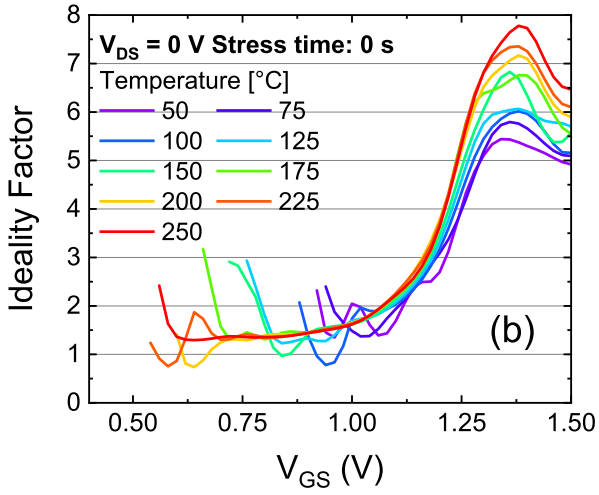


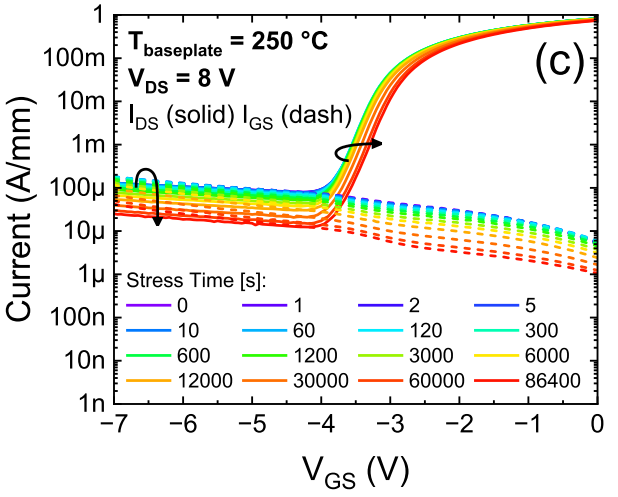
Fig. 2. a) Evolutions of the drain-to-source current during the LTOL stress test. b) Corresponding variation of the threshold voltage. c) Example of low temperature drain and gate current vs. gate voltage taken at $V_{DS} = 8$ V; the corresponding V_{TH} is taken at $I_{DS} = 1$ mA/mm.











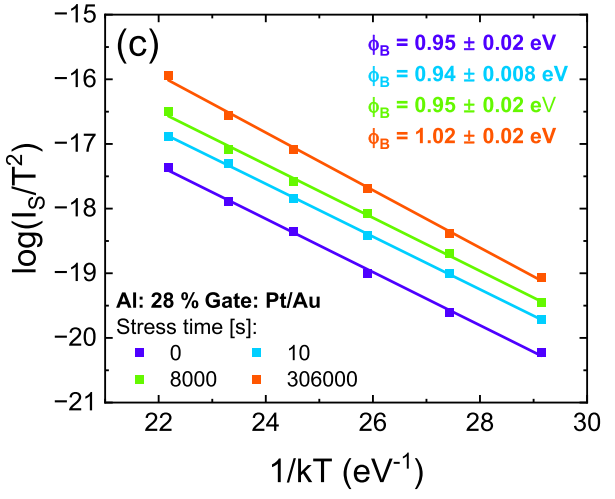


Fig. 3. a) Evolutions of the drain-to-source current during the HTOL stress test. b) Corresponding variation of the threshold voltage. c) Example of high temperature drain and gate current vs. gate voltage taken at V_{DS} = 8 V; the corresponding V_{TH} is taken at I_{DS} = 1 mA/mm.

Fig. 4. a) Example of temperature I-V curves obtained before the HTOL test. The fitting regions were decided considering stable regions of the (b) ideality factor. (c) Resulting SBH values during the stress. A negligible variation is obtained.

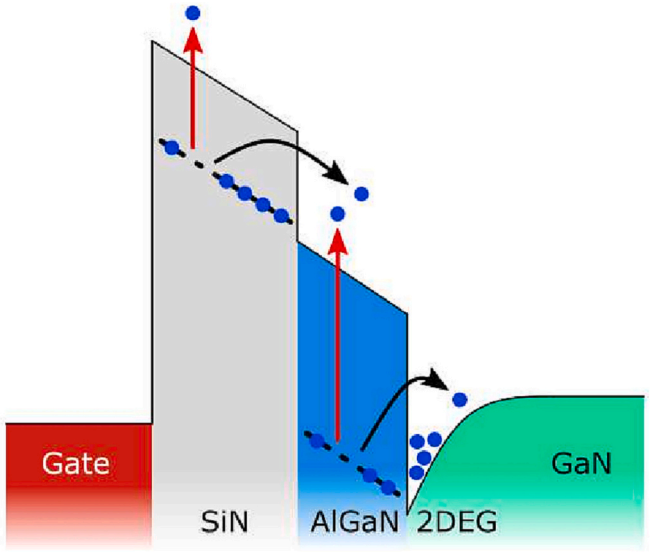


Fig. 5. Band diagram at the gate stack (exact position is highlighted in Fig. 1 as a black dashed line). Temperature- and field-assisted electron de-trapping are represented respectively by red and black arrows.

(10^3–10^4 s).

It may be reasonable to say that the degradation phase should also be observed at RT and 55 °C for longer stress periods, given the apparent onset of a plateau.

From the drain current vs. gate voltage characteristics (Figs. 2c and 3c), we extracted the threshold voltage V_{TH} value, corresponding to the value at which $I_{DS} = 1$ mA/mm is reached, imposing $V_{DS} = 8$ V. The obtained threshold voltage shift $\Delta V_{TH} = V_{TH,stressed} - V_{TH,unstressed}$ (Fig. 2b) demonstrate that the initial rise of I_{DS} is correlated with a negative shift of V_{TH}, while the current reduction to a positive shift.

The results of the HTOL tests show behaviors similar to the ones observed during the LTOL tests, with the two phases clearly visible. The initial increase in drain current (Fig. 3a) is further accelerated, while the maximum reached current values in both HTOL have decreased by 45 mA/mm, with respect to the 140 °C LTOL curve. The negative I_{DS} shift starts much earlier (300 s at 250 °C); thus, we can observe a net negative shift of the drain current. The corresponding V_{TH} shifts (Fig. 3b) are negative in the first current phase and positive during the second phase as in the LTOL. In particular: the observed negative shifts decrease by more than 100 mV, which explains the lower current increase in the first phase; a great positive shift of more than 250 mV (at 250 °C) is responsible for the slower reduction phase.

Taking into account the results obtained in [10] which relate the drain current variation to the degradation of the evolution of the SBH, we evaluated the barrier height during the HTOL test at 250 °C. We applied the thermionic emission model as in [11] to the diode characteristics taken at different temperatures (from 25 °C to 250 °C with a step of 25 °C) at four different time points during stress (0, 10, 8000, 306,000 s).

The diode curves (Fig. 4a) are linearly fitted in the voltage regions at which the ideality factor (Fig. 4b) results in being more stable and near unity. With the intercept values obtained from the linear fit, it is possible to build an Arrhenius plot (Fig. 4c), whose slope is directly proportional to the SBH. Results show that the SBH remains at a stable value of 0.94 eV throughout the HTOL test.

These results are consistent with [12], in which the current variations appear to occur without gate stack degradation. We observed that the first phase of degradation is recoverable, and hence we propose that a temperature- and field-assisted electron de-trapping phenomenon is responsible for it. In particular, we assume that the de-trapping is to be located at the AlGaN/passivation interface [13,14] (Fig. 5).

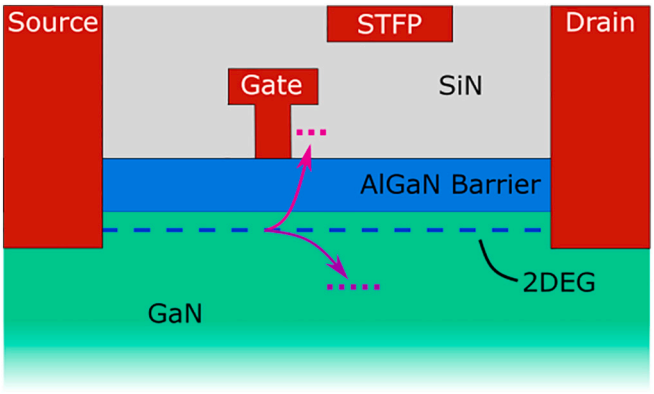


Fig. 6. Visual representation of the trapping location of hot electrons during the second phase of the HTOL.

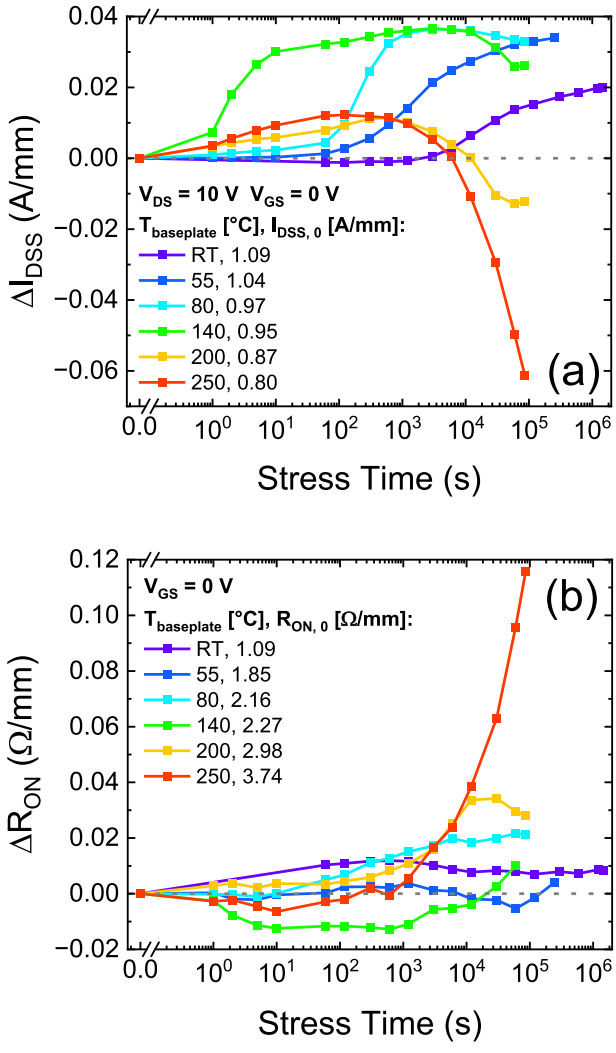


Fig. 7. a) Saturation current and b) on-resistance. Values were extrapolated from the output characteristics. For the on resistance, we linearly fitted the current value in the device linear region.

Regarding the second phase of degradation, we supposed, based on the results presented in [9] that the positive shift in threshold voltage is due to the gradual trapping of hot electrons in the passivation [15] or the GaN buffer layer [16] (Fig. 6), possibly near the gate foot or under the gate head. This would lead to a gradual increase in the threshold

voltage, with a very slow recovery, consistent with the results of the measurements. Changes in the transverse field induced by trapping may also be possible.

To further support our hypothesis, we extracted the evolution of the saturation current I_{DSS} and the on-resistance R_{ON} during the tests. In the former case (Fig. 7a), we observed an initial increase in the current, consistent with the increased 2DEG density caused by the de-trapping phenomena, followed by a slow decrease which can be related to the decrease in the 2DEG density caused by the hot electron trapping effect. Regarding the R_{ON} (Fig. 7b), we observed an increase over longer periods of time. This is consistent with the trapping phenomenon in the gate-to-drain access region [17].

4. Conclusions

In this paper, we investigate the parametric degradation of 0.15 μm AlGaN/GaN HEMT when subjected to short-term LTOL and HTOL. We observed two separate phases in the evolution of the drain current. The first fast increase phase, which is accelerated by temperature, corresponds to a negative shift of the threshold voltage value. We did not find evidence of variation in the SBH. Given the recoverable nature of the phenomenon, we attributed it to a temperature- and field-assisted de-trapping of electrons from the AlGaN/passivation stack, below the gate head. The following slow degradation phase, visible only at high temperatures, is related to a strong positive shift of the threshold voltage and has been ascribed to a slow trapping of hot electrons, possibly in the AlGaN/SiN interface.

CRediT authorship contribution statement

All authors contributed equally to this work.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

Acknowledgment

This activity was supported by project iRel40. iRel40 is a European co-funded innovation project that has been granted by the ECSEL Joint Undertaking (JU) under grant agreement No 876659. The funding of the project comes from the Horizon 2020 research program and participating countries. National funding is provided by Germany, including the Free States of Saxony and Thuringia, Austria, Belgium, Finland, France, Italy, the Netherlands, Slovakia, Spain, Sweden, and Turkey. This project is co-funded by the Ministry of Economic Development in Italy.

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