UNIVERSITA' DI PADOVA  FACOLTA' DI INGEGNERIA

Dipartimento di Ingegneria dell'Informazione

Scuola di Dottorato di Ricerca in Ingegneria dell'Informazione
Indirizzo: Ingegneria informatica ed elettronica industriale

Ciclo XX

Analysis and Implementation of Digital Control Architectures for DC-DC Switching Converters

Dottorando: Luca Corradini

Supervisore: Prof. Simone Buso

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Abstract

Power electronics for consumer applications represents a typical example of engineering tradeoff between costs, performances, system complexity, efficiency and robustness. In this context, control of Switched Mode Power Supplies (SMPS) has been traditionally achieved through analog means with dedicated integrated circuits (ICs). Analog compensation is well known among power electronics engineers and provides the designer with an excellent tool for maximizing the performances/cost ratio. However, as power systems are becoming increasingly complex and often composed of smaller interacting units, the classical concept of control has gradually evolved into the more general problem of *power management*. Beside the basic control function, a number of additional features are often required such as communication capabilities between diffrerent power converters, smart power management for efficiency maximization in critical applications like portable equipments, a certain degree of *programmability* of the compensation characteristics, or even intelligent solutions for *automatic tuning* of the compensator to the specific power processor.

Though at the time of writing analog control ICs for power converters are still dominating the market, in these last years *digital* control solutions have been receiving increasing attention from both the scientific and industrial communities. Digital control in power electronics is potentially able to meet the aforementioned requirements of modern power supply systems and electronic equipments due to the versatility and programmability inherent in the digital approach. On the other hand, a digital controller finds its major weakness in the achievable closed-loop dynamic performances. Analog-to-digital conversion times, computational delays and sampling-related delays strongly limit the small-signal closed-loop bandwidth of a digitally controlled SMPS; quantization effects bring other severe constraints not known to analog solutions.

For these reasons, intensive scientific research activity is addressing the problem of making digital compensators stronger competitors against their analog counterparts in terms of achievable dynamic performances.

The work of this dissertation finds its origin in the outlined context. Maily focusing on low-voltage, high-current applications, two topics related to digital control of DC-DC converters are discussed. The *multiple sampling technique* is a non-conventional control approach which allows for analog-like performances to be achieved in terms of small-signal control bandwidth. The multiple sampling approach is analysed theoretically and experimentally validated, confirming its effectiveness in pushing the dynamic performances of a digitally controlled power supply. Secondly, a robust, low-complexity *autotuning technique* for Proportional-Integral-Derivative (PID) digital compensators is proposed, investigated in detail and experimentally validated.

Finally, in the conclusions the main results of the Ph.D. activity are summarized, and possible developments for future works are outlined.

Abstract

L'elettronica di potenza impiegata in applicazioni *consumer* costituisce un tipico esempio di compromesso ingegneristico fra costi, prestazioni, complessità, efficienza nonché robustezza del sistema. In quest'ambito, il controllo di convertitori a commutazione è tradizionalmente ottenuto per via analogica tramite l'impiego di integrati dedicati. Tecniche di compensazione analogiche sono ben note fra i progettisti e costituiscono un eccellente strumento di massimizzazione del rapporto prestazioni/costi. Tuttavia, mano a mano che i sistemi di potenza sono diventati più complessi e spesso costituiti a loro volta da sotto-sistemi fra loro interagenti, il classico concetto di controllo si è gradualmente evoluto nella più generale tematica del *power management*. Oltre alla funzione basilare del controllo, sempre più spesso sono richieste funzionalità addizionali quali capacità di comunicazione fra i diversi convertitori, strategie di gestione intelligente del convertitore al fine di massimizzare l'efficienza complessiva – questo di particolare importanza nelle applicazioni portatili – nonché un certo grado di programmabilità delle caratteristiche della compensazione, fino ad arrivare a soluzioni per la *taratura automatica* dei parametri del controllore stesso.

Sebbene attualmente il mercato sia ancora dominato dai controllori integrati analogici, negli ultimi anni soluzioni di controllo integrato *digitale* hanno ricevuto attenzione via via crescente sia da parte della comunità scientifica che da parte del mondo industriale. Potenzialmente, il controllo digitale appare capace di soddisfare le esigenze sopra menzionate, in primo luogo grazie alla intrinseca programmabilità e versatilità del digitale stesso. D'altro canto, il punto debole più evidente di un controllore digitale risiede nelle prestazioni dinamiche a catena chiusa con esso ottenibili. I tempi finiti di conversione analogico-digitale, i ritardi di calcolo così come i ritardi associati al campionamento pongono limiti severi alla massima banda di

controllo ottenibile in un convertitore controllato digitalmente. Ulteriori limitazioni sono poste dagli effetti di quantizzazione.

Per le ragioni sopra esposte, la realizzazione di controllori digitali in grado di essere competitivi rispetto alle classiche soluzioni analogiche in termini di prestazioni dinamiche è materia di intensa attività scientifica nonché interesse industriale.

Questo lavoro di tesi si inquadra nel contesto così delineato. Con particolare riferimento alle applicazioni per basse tensioni ed elevate correnti, verranno discusse due tematiche legate al controllo digitale di convertitori continua-continua. La tecnica del *multi-campionamento* è una strategia di campionamento non convenzionale che consente di ottenere prestazioni dinamiche vicine all'analogico in termini di banda di controllo a catena chiusa. L'approccio del multi-campionamento è studiato nel dettaglio da un punto di vista teorico nonché verificato sperimentalmente, confermandone l'efficacia. In secondo luogo, è dettagliatamente discussa e verificata sperimentalmente una tecnica ad elevata robustezza e bassa complessità per l'*auto-taratura* di controllori Proporzionali-Integrali-Derivativi (PID) digitali.

Infine, nelle conclusioni sono riassunti i principali risultati dell'attività di dottorato, nonché venogono delineati alcuni possibili sviluppi per lavori futuri.

Acknowledgments

"It's always a good idea to say thank you to the people that give you money"

Words of wisdom heard during a conference

I would like to warmly thank my advisors Prof. Simone Buso and Prof. Paolo Mattavelli for their invaluable support and guide during my PhD activity, as well as the entire Power Electronics Group (PEL) of the Department of Information Engineering at the University of Padova. It has been a great opportuninty for me to work in this stimulating and prolific research group and together with such brilliant minds and personalities. As I would like to acknowledge my past and present collegues and friends in the PEL group, Benoit Bidoggia, Luisa Coppola, Enrico Orietti, Vladimir Scarpa, Elisabetta Tedeschi and Rosa Paola Venturini. My acknowledgments also go to Erik Della Monica, Daniele Trevisan, Prof. Stefano Saggini and Walter Stefanutti from the University of Udine.

This work and PhD fellowship have been entirely sponsored by Infineon Technologies AG. I would like to thank all the guys in the Padova Design Center, and in particular Dr. Giovanni Capodivacca and Dr. Giuseppe Bernacchia. Their knowledge as experienced industry designers greatly helped me in my professional path.

Part of my PhD activity has been carried out at the Colorado Power Electronics Center (CoPEC), University of Colorado at Boulder. It has been a real honor for me to have the chance to work for Prof. Dragan Maksimović and Prof. Regan Zane during my eight months research period in Colorado, and a huge opportunity to grow both professionally and personally. I thank them both for their warm hospitality and for pushing me to give the best.

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Mari Shirazi deserves a very special acknowledgment. I have been working with her on the autotuning project during my whole time in Boulder, and we often found ourselves facing the same stresses and frustrations, when – as it always happens during a project – things were not going as we expected. As well as we did share the same relief and happiness when seeing our efforts awarded by experimental success. And though she definitely tried to kill me by making me climb over Boulder’s mountains (“Come on Luca let’s go for a hike!”), I got fully repaid by convincing her in watching a horror movie (“Come on Mari let’s watch this!”). Now seriously, she is one of the most hard-working, honest and true persons I have ever met in my whole life.

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Finally my thanks go to my parents, who always encouraged me in doing what I like and always supported me in pursuing my interests and passions.

Luca Corradini

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Chapter I

Introduction

Control of switched mode power supplies (SMPS) intended for consumer market has been traditionally achieved through analog means. Nowadays, analog control ICs are available at low price and for a variety of power applications and converter topologies. These controllers typically integrate one or more error amplifiers, modulation circuitry, a temperature-compensated voltage reference, overvoltage/overcurrent protections as well as soft-start, standby and automatic shutdown features. Depending on the power rating, gate drivers and power switches may be integrated or left as off-chip components. Surrounding passive circuitry is used to program the controller behavior, define the shape of the compensator transfer function and provide feedback and sensing interfaces between the chip and the power converter.

Companies like Infineon Technologies, ST Microelectronics, Intersil, Linear, Maxim, National Semiconductor – just to mention few of them – offer broad lines of inexpensive analog ICs for SMPS control, which cover low-power solutions for

portable applications, general purpose adjustable step-up/step-down converters as well as specific control ICs for low-voltage, high-current converters intended for modern microprocessors power supply. At the time of writing (fall 2007) these analog solutions are widespread in the market of consumer applications and strongly dominate the scene.

Digital solutions, on the other hand, are fairly common in environments where *intelligent* control strategies for power management are required and fully justify the increased cost of a digital control system. Main advantages of a digital control system over an analog solution are represented by the high degree of programmability and computational power, the reduced need for external passive components and the consequent decreased sensitivity to tolerances and other sources of parametric variations, the possibility to implement complex control strategies as well as to easily switch through different modes of operation, targeting for highest efficiency or optimized dynamic performances. System monitoring functions are of extreme importance for high-reliability applications and their implementation strongly point to digital solutions able to collect and process environmental data. Self-tuning, also known as *autotuning* functions allow a digital compensator to adapt its parameters to the specific power plant under control, eliminating the need for manual design or calibration and enhancing controller modularity and versatility.

Examples in which digital controllers find natural employment include industrial environments, where the complexity and number of interconnected subsystems often demand sophisticated and “smart” control decisions whose algorithmic nature is not prone to analog implementations, or mission-critical applications like aircraft or spacecraft power supply systems, where reliability is a major concern. Another typical high-reliability demanding environment is represented by the distributed power system employed, for instance, in a server application.

Depending on the specific requirements and cost/performance tradeoffs, the hardware platform for the digital control system may be based on application-specific integrated circuits (ASICs), microcontrollers, digital signal processors (DSPs) or microcomputers. In all the described applications the increased cost for a digital control system has negligible impact on the overall project, and is furthermore justified by the savings that come from the increased system robustness and reliability.

In recent years, however, digital solutions have been proposed in the market of consumer applications. Point-of-load power supplies employed in desktop/laptop computers are examples, along with digital control ICs for multiphase converters employed in voltage regulation modules (VRMs). In this context the competition with analog solutions leads to reconsider the previous statements concerning cost and performances tradeoffs. Rather than pointing to expensive microcontroller or DSP platforms, digital solutions for consumer applications are more prone to ASIC implementations which integrate A/D conversion and pulse-width modulation resources, control hardware, conventional protection circuitry and – depending on the application – communication, system monitoring and autotuning functions.

Design of a digital control IC with analog-like performances in terms of dynamic capabilities, area and power consumption is a challenging issue. Leaving apart mixed-signal solutions, pure digital systems for SMPS control invariantly require fast A/D converters and optimized digital pulse-width modulators (DPWMs). Accuracy comparable to analog controllers is achieved only by means of sufficient bit resolution and/or dedicated signal processing provisions. These factors all point to increase the overall area consumption. As far as the dynamic performances are concerned, loop gain delays due to A/D conversion, computational time and DPWM phase lag contribute to lower the ceiling of maximum achievable control bandwidth. Other limitations

specifically encountered in digital system include reaction times of the digital controller, which are limited by the sampling rate, as well as quantization phenomena such as limit cycle oscillations.

Digital power also brings with it a certain *"cultural shock"* among circuit designers that must not be neglected. Building blocks of analog ICs for SMPS control – operational amplifiers, bandgap references, oscillators, sensing circuitry etc… – represent standard solutions in the world of analog design and the different companies have developed, across the years, a well-established *know-how* in the design and layout steps. The same cannot be stated for digital solutions, which still require a certain amount of knowledge not always owned or correctly mastered by traditional power IC designers. For similar reasons, experienced digital designers may not have an in-depth knowledge of power conversion systems.

On the other hand, advantageous aspects of digital control exist that do not have analog counterparts, many of them have been mentioned previously. In general, digital control wins where the algorithmics of the operation is too complex for analog implementations. No analog controller exhibits the same degree of programmability and versatility as a digital controller does. Compensator parameters can be stored in a nonvolatile memory and loaded in a programmable controller at system power-on. This way, different sets of pre-calculated parameters can be run for many environmental conditions on the same control hardware. More evolved *tuning algorithms* literally perform an *automatic design* of the compensator parameters through a number of online measurements and post-processing operations.

Different control laws can be adopted over time by the same control structure, depending on the particular situation. A typical example is efficiency maximization in a converter switching from heavy-load to light-load operation. Detection of this transition

allows to choose the most suitable control strategy in order to track the point of highest efficiency, this being of utmost importance for portable and battery-operated equipments.

From these considerations, real breakthrough of digital control in consumer power electronics will come from cost-effective solutions featuring capabilities not available in analog ICs. The research for hardware, power and area optimization in digital ICs for SMPS control has stimulated the scientific community over the recent years, leading to the achievement of increasingly improved performances.

1.1. Research Background

For the reasons discussed in the introduction, digital control in power electronics has gained increased attention from the scientific community over the last years [1-4]. All the main contributions to digital solutions for SMPS presented in literature aim to demonstrate control approaches with minimum hardware resources and reduced complexity [5-23].

Feasibility of completely *integrated* digital controllers was demonstrated for the first time in [5-6], in which innovative solutions for the main constituents of a digital controller, namely the compensator, the A/D converter and the digital pulse-width modulator, were presented. Based on a look-up table structure, the PID compensator employed in [5] presented reduced complexity. Delay-line and windowed ADCs were used in these works for fast conversion times and small area requirements. A ring oscillator-MUX DPWM was implemented in [6], while in [5] a hybrid counter/delay line architecture was considered as a suitable tradeoff between resolution, area and power consumption. Further works in the area exploited ring-oscillator ADCs [8,10]

and other hybrid DPWM structures. Further examples of DPWM architectures can be found in [24-27].

Along with solutions aimed to an increasingly deeper integration, the research activity also focused on exporting control approaches widespread in the analog world into the digital domain, an example being the investigation and development of digital current-mode control techniques [13,15,20]. More recently, the concept of *continuous time digital signal processing* has been proposed in [23] as a mean to dramatically push the dynamic performances.

One of the most intense and interesting research activities concerns the development and implementation of hardware-effective *autotuning techniques* for digital compensators [45-56]. Results presented in literature indeed point to a number of viable approaches for robust and repeatable autotuning. Moreover, identification approaches have been presented which allow for system *health monitoring* functions to be implemented [57-59], which enhance the controller with fault detection features and can as well be employed to undertake *preventing* actions against possible future faults.

Beside purely digital control solutions, *mixed-signal* controllers are worth to be mentioned [31-35]. These approaches combine simple integrated analog blocks and digital provisions with the aim to achieve analog-like dynamic performances, but still retaining the advantages of digital systems like programmability, low passive component count and control robustness.

Modeling also represents a primary research line concern in the field of digital power. Though conventional SMPS analog models are well known by engineers, correct modeling of a digitally controlled switching converter is often unclear to many designers and subject to errors and misconceptions, leading to difficulties in both understanding the behavior of the system and properly designing its controller.

Important contributions to the correct modeling of digitally controlled SMPS have been proposed in the literature [60-64]. A unique phenomenon of digital control is represented by limit cycling oscillations (LCOs). Being originated from quantization effects operating in a feedback system, these phenomena present intrinsic modeling difficulties. Many research groups have faced the problem through different approaches [65-69], presenting general guidelines for avoiding the onset of LCOs in a digitally controlled SMPS.

1.2. State of the Art Technology

After having outlined the status of the research, a brief overview of some digital control ICs currently available on the market allows to better complete the picture.

Intersil's ISL6595 digital multiphase controller represents a typical example in the field of voltage regulation modules (VRM) control for microprocessors power supply. This 3.3V-operated IC provides voltage control and current sharing for up to six interleaved phases with switching frequencies programmable from 100 kHz to 2 MHz. An I^2C digital interface allows the programming of the PID compensator parameters as well as the shape of the loadline, making the IC compatible with Intel as well as AMD microprocessors. Current sensing is provided with an on-chip calibration function. Off-chip drivers are required. A nonlinear technique – ATR, Active Transient Response – is employed to optimize dynamic performances during load transients.

The PX7510-20 and PX75222-42 ICs by Primarion are a line of digital controllers for Point-of-Load Converters intended for single or multiple output, single or multi-phase topologies. Multiphase operation can also be acheved by synchronization of multiple ICs. Control and monitoring functions are provided through the PMBus™ industry standard interface. Again the chip is equipped with a non-volatile memory

(NVM) which allows for the main control parameters and behavior to be online programmed.

Linear's LTC7510 digital POL controller provides similar features. Interestingly, this chip implements a 4x oversampling PID control. The subject of increasing the sampling frequency with respect to the converter switching frequency represents a main study in this work, as will be outlined in the next Section.

Silicon Labs Si8250 digital power supply controller represents perhaps one of the most advanced and powerful ICs available on the market. Intended for DC-DC as well as AC-DC applications, it is based on a dedicated DSP filter engine for control purposes and employs a 50 MIPS CPU for system managements functions.

It is clear from this brief overview that companies involved in the digital power strongly point to highly programmable products with high degree of interfacing and online configuration capabilities.

1.3. The Work of this Dissertation

The entire work and PhD fellowship have been sponsored by Infineon Technologies AG – Padova Design Center. The author would like to thank collaborators and friends at Infineon Technologies for their support and valuable suggestions.

This work treats two topics related to the digital control of DC-DC switching converters, namely *multiple sampling* and *autotuning*.

In Chapter II the main concepts of digital control in power electronics are summarized. The main topics of this work are then treated in Chapters III to V and will be introduced in the following subsections.

The methodology adopted in this work for experimental testing of the various described techniques largely employed FPGA-based development platforms interfaced

with power stage boards. Field-Programmable Gate Arrays devices (FPGAs) represent excellent and versatile tools for rapid prototyping and verification of digital circuits [70-83], and are extensively used in the literature of SMPS digital control.

1.3.1. Multiple Sampling

Multiple sampling [38-44] represents a non-conventional sampling strategy in which the control sampling frequency is kept higher than the converter switching frequency. Though sometimes employed in commercial digital ICs, a detailed analysis of the multiple sampling technique has never been proposed in the literature. In this work it is demonstrated how the increased sampling frequency brings to a significant reduction of the DPWM small-signal phase lag, thus breaking the bandwidth limitations usually found in digitally controlled SMPS and allowing for analog-like performances to be achieved. A small-signal model for multi-sampled modulators and converters is developed in Chapter III and experimentally validated, confirming these assessments.

The analysis then proceeds in investigating the major drawbacks of the multiple sampling technique, which have been identified in the injection of switching frequency harmonics into the feedback loop, a phenomenon which has been found to trigger non-linear effects and unexpected system behaviors. The most relevant aspect of this phenomenon is the onset of control *dead bands* in the static transcharacteristic of a multi-sampled pulse-width modulator. These dead bands represent sets of operating points for which the modulator gain is *zero*, and therefore make any small-signal control action totally uneffective. This phenomenon has a severe impact on the closed-loop behavior, as proper steady-state and dynamic regulation may be compromised.

A nonlinear model is proposed in Chapter III which fully characterizes the open-loop and closed-loop steady state operation of a multi-sampled modulator. Presence of sampling induced dead bands is explained through the discussed model. Simulations

and experimental tests are also proposed as a further evidence of the validity of the conclusions.

Given these considerations, multiple sampling technique turns out to be a viable approach only if suitable provisions are undertaken to mitigate or eliminate the aforementioned nonlinear phenomena. Thus, strictly connected with the analysis and modeling of multiple-sampled systems is the investigation of *PWM linearization techniques* aimed to restore the linearity of multi-sampled modulators. Different approaches have been proposed in the literature during this PhD activity [40,42,44], the most relevant of which are illustrated in detail in Chapter IV.

An interesting conclusion that was drawn while developing and experimentally testing the PWM linearization techniques was the evident superiority, in terms of *intrinsic linearity*, of triangular modulators with respect to trailing edge or leading edge PWM schemes. Multi-sampled systems based on triangular modulations are found to be much less prone to exhibit strong nonlinearities, resulting in an overall better behavior which allows to fully exploit the main benefits of the multiple sampling strategy. Proofs of the superior performances of triangular modulators are reported in this work, along with quantitative analysis derived from the developed models.

1.3.2. Autotuning

Part of the PhD activity has been carried out at the *Colorado Power Electronics Center (CoPEC)*, at the University of Colorado at Boulder, Department of Electrical and Computer Engineering, under the supervision of Prof. Dragan Maksimović and Prof. Regan Zane.

The activity was mainly developed as a comparative analysis of different autotuning techniques for digitally controlled Point-of-Load (POL) converters having wide range of capacitive loads. Two tuning approaches were identified and investigated in terms of

complexity, performance, tuning capabilities and robustness. The *System-ID tuning technique*, which finds its bases on cross-correlation methods for system identification [45-48], has been developed by CoPEC student and friend Mariko Shirazi. The technique identifies the entire frequency response of the converter through injection of a pseudo-random binary sequence (PRBS) and further post-processing operations. Once the control-to-output frequency response is identified, a tuning algorithm is enabled to automatically design a digital PID compensator. Tuning targets are expressed in terms of phase margin, gain margin and desired control bandwidth. Provisions aimed to avoid the onset of steady-state limit cycling were also considered.

As a second tuning technique, the *relay-feedback approach* was considered and investigated by the author. The concept of relay feedback, well known in the industrial field and reproposed in [51] as a viable solution for self-tuning of digitally controlled SMPS, was developed with provisions specifically aimed to handle the wide range of capacitive loads dictated by the application. The technique induces amplitude-limited oscillations in the system and performs the identification of the power converter parameters through repeated frequency measurements. A tuning algorithm iteratively adjusts the parameters of the PID compensator until specified tuning targets – formulated as before – are met.

Both investigated methods were HDL coded and successfully tested and validated on experimental FPGA-controlled point-of-load prototype converters. The results of the analysis are reported in [52].

The study of the relay-feedback autotuning has been carried out as a part of this PhD activity during my research time period at Boulder, and further investigated at the Department of Information Engineering of Padova, Italy, where additional provisions were studied and tested for enhanced robustness and tuning accuracy. The description of

the relay-based tuning approach is reported in Chapter V along with implementation details and experimental results confirming the validity and modest hardware requirements of the technique.

Finally, Chapter VI draws the main conclusions summarizing the relevant results achieved by the PhD activity. Proposals for future works and subjects for further investigations are also outlined.

Chapter II

Principles Of Digital Control In Power Electronics

This chapter provides an overall introduction to the digital control of a power processing system based on a DC-DC switching converter. A typical control architecture is first discussed from a system-level point of view, where the analog power processing system represents the plant whose dynamics is to be controlled in order to fulfill the power delivery requirements dictated by the application, while the digital system has as its first objective that of achieve the required regulation of the converter state variables through negative feedback. Depending on the specific application, secondary functions may include system monitoring and diagnostics, communications and self-tuning features.

Analog and digital systems are interfaced by means of A/D and D/A converters; among these, state variables A/D conversion and the Digital Pulse Width Modulator represent the most important from the control viewpoint. A first discussion on sampling strategies will also be initiated in Section 2.2, while an in-depth analysis will be proposed in Chapter III.

Correct small-signal z-domain modeling is mandatory for an effective digital compensator design. Section 2.3 of this Chapter is devoted to the purpose of deriving the discrete-time equivalent model of the power plant as well as to express the system loop gain. Simulation examples will be provided to appreciate the accuracy of the discrete-time models.

Quantization effects are of unique importance in a digital control system, as they do not have an analog counterpart. Limit cycle oscillations represent the most typical – and undesired – quantization effect in a digital feedback system. A brief survey of quantization sources is carried out in Section 2.4, along with a discussion of limit cycle oscillations and some basic criteria proposed in the literature for their reduction or suppression.

2.1. System-Level Overview Of A Digital Control Architecture For A DC-DC SMPS

Figure 2.1.1 illustrates a structural description of a DC-DC digitally controlled power converter. The following scenario can always be drawn: an electronic equipment, here designated as *load*, draws an average power P_o and requires a tightly regulated

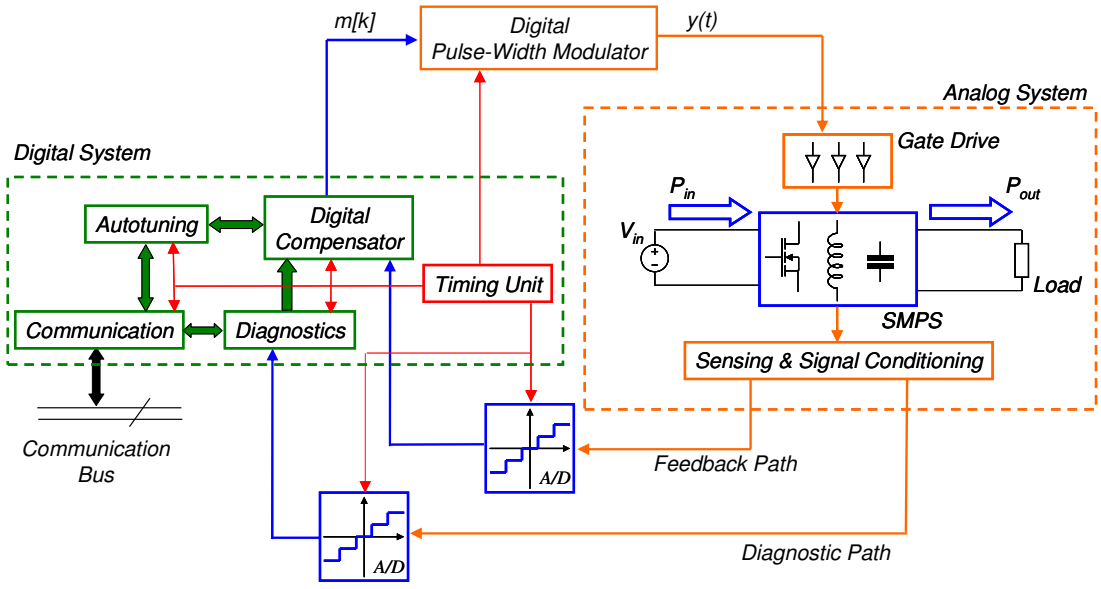

Fig. 2.1.1 – System-level architecture of a digitally controlled SMPS

voltage V_o in order to operate properly, while an unregulated (or poorly regulated) DC voltage source V_{in} is available. A Switched Mode Power Supply (SMPS) is thus employed as a power processor in order to perform a high-efficiency power conversion from the input power source V_{in} to the load. A negative feedback loop based on a digital compensator stabilizes V_o with respect to variations of the input voltage (*line regulation*) and of the output current drawn by the load itself (*load regulation*).

In a digital control loop one or more converter state variables are sampled and quantized by means of Analog to Digital Converters (ADCs). Adequate signal sensing and analog conditioning circuitry is usually required before the conversion to take place. The discretized information is processed by the digital compensator through its *control algorithm*, which calculates the discrete-time control signal *m[k]* on a sampling cycle basis. *Pulse-width modulated* (PWM) converters will be considered in this work, where the control signal modulates the converter duty cycle.

As in analog control schemes, the PWM modulator plays a key role in interfacing the control system to the switching converter. In a digitally controlled power converter, the *Digital Pulse Width Modulator* (DPWM) acts as a digital to analog converter (D/A), as its function is to translate the digital sequence *m[k]* produced by the compensator in an analog PWM signal *y(t)* suitable for driving the SMPS power switches.

As modern power switches require several amps of sourcing/sinking capability from the gate signal during the switching transitions, *gate drivers* are usually present as an interface between the DPWM and the power converter; the function of the gate drivers is to enhance the driving capabilities of the PWM signal *y(t)* by increasing its power level, as well as to perform proper *voltage level conversion*.

Beside its control function, the digital system may include *diagnostics*, *communication* and *self-tuning* capabilities. These features will be briefly discussed in

Subsection 2.1.2., while Chapter V will be entirely devoted to the subject of *self-tuning digital compensators*, as well as to the development, implementation and experimental validation of a specific tuning technique.

The following subsections present a more detailed description of the main constituents of a digitally controlled power converter.

2.1.1. Analog System

The DC-DC power converter, along with the gate driving and the analog sensing/conditioning circuitry, represents the analog system. This section provides a brief overview of these constituents mainly focused to their system-level modeling in terms of s-domain transfer functions.

i. Power Converter

The power processing function performed by the switching converter represents the fundamental role of the analog system. The conventional modeling approach for SMPS employed in power electronics is based on *averaging* and *linearizing* the behavior of the nonlinear, time-variant switching converter to achieve a linear, time-invariant description of its low-frequency, small-signal dynamics, i.e. for frequencies well below the switching frequency f_s and for small deviations with respect to the steady-state quiescent point. This analysis has the major objective of identifying the analog signals of interest from the control point of view and establishing the existing relationships among them.

A number of *independent input signals* can be identified as those signals that are imposed externally and affect the converter state variables as well as its outputs. These include the converter input voltage perturbation $\hat{v}_{in}(t)$ and the converter load current perturbation $\hat{\imath}_o(t)$. In some cases the load current is not considered as an input signal,

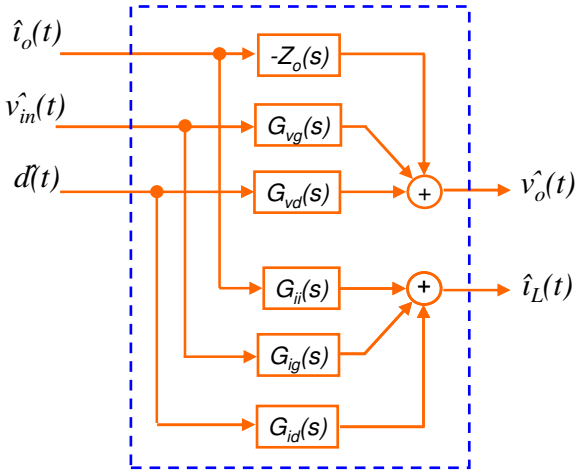

Fig. 2.1.2 – s-domain transfer functions of a DC-DC switching converter

and an explicit load relationship is formulated by assuming, for instance, a resistive load R_o.

In pulse-width modulated SMPS the most important input signal is represented by:

$$d(t) \equiv \frac{1}{T_s}\int_{t-T_s}^{t} y(\tau)d\tau = D + \hat{d}(t)\,, \qquad (2.1.1)$$

i.e. the low-frequency content of the pulse-width modulator output signal $y(t)$. While $\hat{v}_{in}(t)$ and $\hat{\imath}_o(t)$ represent *disturbances* from the control design point of view, (2.1.1) plays the role of the analog control signal. Its relationship with the digital control signal perturbation $\hat{m}[k]$ will be examined in Section 2.2 as well as in Chapter III.

State variables $x_i(t)$ are the analog quantities that define the state of the switching converter. In general, the state vector is composed by the set of capacitor voltages and inductor currents.

Output signals represent the analog quantities to be sensed and/or monitored for regulation or diagnostic purposes. As mentioned in the introduction, the converter output voltage $\hat{v}_o(t)$ is a signal typically targeted for tight regulation when supplying a load. Average or peak current-mode controllers sense the converter inductor current $\hat{\imath}_L(t)$ for both regulation and over-current protection purposes. Multi-phase buck converters

typically employed as low-voltage, high current Voltage Regulation Modules (VRMs) for modern microprocessors power supply invariantly require the sensing of the phase currents to ensure current sharing and proper droop resistance emulation.

We shall describe the power converter as illustrated in Fig. 2.1.2; the control-to-output and control-to-inductor current transfer functions $G_{vd}(s)$ and $G_{id}(s)$ are defined, along with the audiosusceptibility $G_{vg}(s)$, the input voltage-to inductor current transfer function $G_{ig}(s)$, the open-loop output impedance $Z_o(s)$ and the load current-to-inductor current transfer function $G_{ii}(s)$. Explicit expressions of these transfer functions depend on the topology considered. Moreover, depending on the particular situation, one or more of these transfer functions may be neglected for the purpose of analysis.

Please note that the output voltage and the inductor current themselves represent state variables for the converter. For this reason we will often talk about sensing and/or sampling of the converter state variables, without much distinction between state variables and output signals.

ii. Sensing and Signal Conditioning

Analog signal conditioning is normally required when sensing the converter signals for control and monitoring purposes. Basic operations on sensed signals include level-shifting and amplification for suitable interfacing with the ADCs analog input voltage range. Analog circuitry based on wide bandwidth operational amplifiers is commonly employed for voltage and current sensing along the feedback path. Filtering is usually limited to frequencies well beyond the converter switching frequency, in order not to introduce unacceptable phase losses around the desired closed-loop bandwidth. For this reason, aliasing effects usually occur during the A/D conversion of the analog variables, affecting the spectra of the digitized sequences. Depending on the sampling frequency,

these effects influence the closed-loop behavior of the converter in different ways. More detailed analyses will be carried out in Section 2.2 and in Chapter III.

Small signal-wise, the analog sensing and conditioning circuitry can be modeled by means of an s-domain transfer function $H_{sense}(s)$. Depending on the desired modeling accuracy, H_{sense} may be described by a pure gain or by a magnitude and phase-varying frequency response.

iii. Gate Drivers

To fully exploit modern power MOSFETs capability of achieving short turn-on and turn-off times, suitable gate driving circuitry is usually required. Gate drivers supply high-current turn-on and turn-off driving commands and operate the necessary voltage level conversion between the DPWM output signal $y(t)$ and the power switches. A typical driving problem is represented by the high-side switch of a synchronous buck converter, whose source is not grounded and varies between 0V and V_{in} during the converter operation. Bootstrap techniques are often employed by the gate drivers to obtain a suitable gate-to-source driving voltage. In synchronous converters another typical driving challenge is represented by the cross-conduction phenomenon, i.e. both switches conducting at the same time during the switching transitions. Beside being a possible cause of failures, the cross-conduction degrades the converter efficiency. To overcome this problem a suitable *dead-time* has to be introduced by the driving circuitry between the turn-off of one switch and the other switch turn-on.

A gate driver delivers the turn-on or turn-off command to the power switches with a certain delay $\Delta t_G'$ with respect to the incoming input signal $y(t)$. The actual turn-on or turn-off of the power switch exhibits a further propagation delay $\Delta t_G''$. From the control point of view the overall propagation delay $\Delta t_G = \Delta t_G' + \Delta t_G''$ generates a lag in the loop gain phase response given by:

$$\Delta\varphi_G(f) = -2\pi f \Delta t_G \tag{2.1.2}$$

Modern integrated drivers exhibit propagation delays on the order of 20-50ns. Common values for the closed-loop bandwidth f_c in analog control lie between one tenth to one fifth of the converter switching frequency f_s, these being upper limits also for conventional digital control schemes. Thus, evaluation of (2.1.2) at $f = f_c$ yields:

$$\Delta\varphi_G(f_c) = -2\pi\alpha\frac{\Delta t_G}{T_s}, \tag{2.1.3}$$

with α ranging from 0.1 to 0.2. The gate driving delay impact on the loop gain phase response is evaluated once the switching frequency is specified. As long as f_s ranges within few hundreds of kHz, it is easily seen from (2.1.3) that negligible phase lags are originated from the gate driving circuitry. Contribution (2.1.3) is therefore usually neglected with respect to other, more important terms originated from A/D conversion, computational and PWM modulation delays that will be considered in the following Sections. However, when high-frequency converters are considered, operating at switching frequencies on the order of several MHz, (2.1.3) may become significant and must be included to correctly account for the total loop gain phase behavior.

2.1.2. Digital System and A/D – D/A Interfaces

By *digital system* we mean that part of the power processing loop in which the information is processed via numerical ways. It includes the digital compensator as well as diagnostic, communication and self-tuning functions. Analog-to-Digital and Digital-to-Analog interfaces exist to allow the digital system exchange information with the power converter and the surrounding analog world. This Section presents an overview of these units, focusing on those system-level aspects of primary importance from the control point of view.

i. Analog to Digital Conversion

The sampling and quantization of the converter state variables – after sensing and proper conditioning is performed – serves the purpose of both providing feedback signals for the compensator and the necessary monitoring function for other features of the digital system like diagnostics or autotuning.

Analog-to-Digital Converters operating a linear, or *uniform* quantization will be considered in this context, meaning that the quantization levels are equally spaced within the ADC analog input voltage range. The ADC resolution, expressed by the length n_{AD} of the output binary word, and the ADC *full sale range FSR* define the ADC voltage quantization step:

$$\Delta q_{AD} \equiv \frac{FSR}{2^{n_{AD}}} \tag{2.1.4}$$

From a system-level point of view, there are two main aspects to be considered in selecting the A/D converter, namely its resolution n_{AD} and its conversion time Δt_{AD}.

The ADC resolution can be selected once the dynamic range *DR* required to the sampled signal within the digital domain is known; for an input signal uniformly distributed between 0 and a the resulting signal-to-noise ratio is:

$$SNR_{dB} = 6.02 n_{AD} - 20 \log_{10}\left(\frac{FSR}{a}\right), \tag{2.1.5}$$

where SNR_{dB} is expressed in decibels. From the condition $SNR_{dB} > DR$ the required ADC resolution is found. Please note that equation (2.1.5) does not account for noise sources different from quantization noise and which may cause the effective number of bits to differ from n_{AD}.

The selection of the quantization step is based on regulation accuracy in both static and dynamic conditions. Quantization effects such as the possible onset of limit cycle

oscillations usually also come into play when selecting the proper A/D resolution. These aspects will be addressed in Section 2.4.

As an example, let us consider a low-voltage application in which the output voltage is regulated up to 1.5V with a ±0.5% DC regulation accuracy. The maximum allowed quantization step is thus Δq_{AD} = 15mV, to which corresponds a minimum ADC dynamic range $DR = 20log_{10}(1.5V/15mV) = 40dB$. From (2.1.5) and assuming FSR = 2V, the minimum number of bits is n_{AD} = 8. This reasoning only accounts for steady-state regulation accuracy; in practice a higher number of bits will be required to achieve suitable dynamic responses.

Digitally controlled SMPS usually require high conversion rate ADCs in spite of the relatively low sampling rate of the converter state variables, which may be equal to the switching frequency or few times higher (see Section 2.2 for a discussion on sampling strategies). In fact, the A/D conversion time Δt_{AD} is of extreme importance when the ADC is operated within a feedback loop, as any delay time translates into a phase lag that limits the achievable closed-loop bandwidth:

$$\Delta\varphi_{AD}(f) = -2\pi f \Delta t_{AD} \tag{2.1.6}$$

The term of comparison is represented by the converter switching period T_s, as discussed for gate driving delays: at a given closed loop bandwidth f_c defined as some fraction α of the converter switching frequency f_s, evaluation of (2.1.6) yields:

$$\Delta\varphi_{AD}(f_c) = -2\pi\alpha\frac{\Delta t_{AD}}{T_s}, \tag{2.1.7}$$

Negligible values of (2.1.7) are achieved for conversion rates in the order of tens of megasamples per second. Please note that pipeline ADCs are not always suitable for SMPS control applications, as their high conversion rate does not necessarily imply a small conversion time.

Beside these system-level discussions, additional application-specific considerations have to be made in order to identify the most suitable A/D converter. In fully integrated digital controllers the use of area efficient ADCs is usually mandatory. Power consumption is also of primary concern especially in portable applications and it limits both the A/D sampling rate and the A/D resolution. An in-depth discussion of these issues is out of the scope of the present work. A number of solutions have been proposed in the literature [5-10], to which the interested reader is addressed.

ii. Digital Pulse Width Modulator

In any digital control scheme a *control algorithm* or *control law* is employed to process data sampled from the analog plant and produce the discrete-time control signal *m[k]* used to achieve the desired control action. In pulse-width modulated SMPS this action is obtained by modulating the duty cycle of the power switches activity. Thus, *m[k]* inherently represents the desired duty ratio. However, the information carried by *m[k]* has to be delivered to the power converter switches as an on/off signal *y(t)*. The digital pulse width modulator (DPWM) thus acts as the necessary interface between the digital compensator and the power converter [24-27].

Strictly speaking, the DPWM performs a D/A conversion from the digital input *m[k]* to the modulated analog waveform *y(t)*. It is characterized by its resolution, i.e. the number of bits n_{DA} of the input digital word. Each of the possible 2^{nDA} values of the digital input is mapped by the DPWM to a unique duty ratio. Thus, once the switching period is specified, a *time quantization* can be associated to a particular DPWM:

$$\Delta q_{t,DA} \equiv \frac{T_s}{2^{n_{DA}}}, \tag{2.1.8}$$

which represents the smallest turn-on time variation the DPWM is able to generate.

Considerations related to quantization effects and limit cycling phenomena discussed in Section 2.4 suggest that the DPWM resolution should be selected as high as possible, limitations being posed by area and power consumption. In this work we will often assume an infinitesimal time quantization step, i.e. an infinite resolution, meaning that the validity of the discussed results will be compromised when coarse time quantizations are considered.

As in the case of ADCs, the choice of a particular DPWM architecture in an integrated digital controller is affected by both area and power constraints. An interesting survey of DPWM architectures and tradeoffs among resolution, silicon area and power consumption is given in [25].

An in-depth discussion of the behavior of digital pulse width modulators in relation with the adopted sampling strategy will be initiated in Section 2.2 and extended in Chapter III.

iii. Digital Compensator

In both analog and digital control of SMPS the compensator objective is to perform a signal processing function on the sensed converter state variables in order to produce a control action on the plant.

The basic operation of a digital compensator works on a sampling-cycle basis starting from the acquisition of an input digital sample *e[k]* – often recognized as the *error* between the regulated variable and the control setpoint – and terminating with the computed digital control sample *m[k]*, available after a certain *computational delay* Δt_{calc} which depends on the control law complexity as well as on its hardware implementation.

Linear control laws represent the most important class of signal processing functions employed in digital control of SMPS. They relate *m[k]* to *e[k]* by means of a linear, constant coefficients difference equation of the type:

$$m[k] = -\sum_{i=1}^{n} a_i m[k-i] + \sum_{j=0}^{m} b_j e[k-j], \qquad m \le n \tag{2.1.9}$$

Control laws of the type (2.1.9) are of particular importance because they simply involve additions and multiplications. These operations are readily available in microcontroller or DSP-based platforms, or can be implemented as hardwired logic in an integrated digital controller using standard adders and multipliers blocks. Equation (2.1.9) includes the important subclass of Proportional-Integral-Derivative (PID) digital compensators. An overview of digital PIDs is given in Appendix A.

Nonlinear control actions can also be performed [28-30], generally aimed to achieve better dynamic performances in closed-loop operation. These may include anti-windup provisions as well as nonlinear proportional and integral actions.

More generally, a digital compensator presents programmability and versatility features not usually found in analog control that allow for *different* control laws to be implemented and adopted as a function of particular boundary conditions, opening the possibility to *intelligent* control strategies. A typical example has been proposed in [8], where efficiency maximization in a low-power application was obtained by changing the control strategy when switching from heavy-load to light-load conditions and viceversa. For these reasons, the action of a digital compensator can be better described by a *control algorithm* rather than by a simple linear or nonlinear signal processing operation.

iv. Diagnostics, Communication and Autotuning

Beside its control function, the digital system may be provided with a number of features aimed to enhance the robustness of the power conversion, as well as its integration and interfacing capabilities with the surrounding world.

Diagnostic functions are common in high-reliability applications. Examples are given by distributed power systems for server applications, aircraft and spacecraft power systems and military applications. The need for high-reliability invariantly requires fault detection features, if not fault prediction capabilities. Diagnostics is the set of monitoring activities aimed to periodically check the health of the power system and eventually activate signaling mechanisms when the onset of critical situations is detected.

Communication functions allow the digital system to interact with the surrounding world, exchanging information about the converter status as well as receiving commands and programming instructions. Whenever a centralized diagnostic monitor is present in a distributed power system, communication buses allow the collection of health information of different subsystems. In some cases the communication may occur between the converter and the load, as it happens between modern microprocessors and VRM modules.

Autotuning is a feature that allows a digital system to automatically tune its digital compensator parameters. This function is one of the most interesting possibilities offered by digital techniques and allows for great performance optimization. Beside optimizing the SMPS control from a dynamic point of view by determining the most suitable compensator for a given power plant, self-tuning features greatly enhance the versatility of a digital control system and its robustness with respect to process parametric variations, these being well known weak points in conventional analog

controllers. Chapter V is entirely devoted to the analysis and experimental evaluation of a particular tuning technique.

The functions briefly summarized in this Subsection are quite common in high-reliability and mission-critical applications where digital controllers are employed. On the other hand, low-cost and low-control complexity requirements dictated by the market of consumer applications make these provisions by no means widespread. For this reason, hardware-effective solutions for diagnostics and intelligent autotuning features are of great scientific interest and many publications have been and are being proposed in the literature [45-56, 57-59].

2.2. *Sampling Strategies*

The sampling strategy is related to two main aspects of the analog to digital conversion of the converter state variables, namely *how many samples* should be acquired per switching period and *where* the sampling instants should be allocated in time within the switching period. A third important aspect, related to the quantization step, will be addressed in Section 2.4. As far as the first aspect is addressed, classical digital control schemes often employ a sampling frequency equal to the switching frequency. This method will be denoted as *single sampling* approach. A second approach, the study of which constitutes one of the main contributions of this work, is to use a sampling frequency greater than the switching frequency. An extensive study of the *multiple sampling* technique is presented in Chapter III. In the following Subsections the main relevant aspects of single and multiple sampling will be summarized.

We will use the notation (N,Δt) to denote a specific sampling strategy. The first number, N, defines the sampling frequency and represents the integer number of samples acquired per switching period, or *multisampling factor*:

$$f_{sampling} = Nf_s \tag{2.2.1}$$

The second number represents the delay time between the first sampling instant with respect to the beginning of the switching period. Expressing these concepts mathematically, the set of the sampling instants corresponding to the sampling strategy (N,Δt) is:

$$t_{sampling}(k) = \Delta t + k\frac{T_s}{N}, \qquad k \in \mathrm{Z}, \tag{2.2.2}$$

where the time origin has been assumed to be aligned to the beginning of a switching period. We will make use of k as running index to denote the time

dependence of any discrete-time sequence obtained through sampling of an analog signal by means of a given sampling strategy. The particular sampling strategy will be clear from the context.

Let us now consider an analog signal $x(t)$, and let $X(f)$ be its Fourier transform. If the discrete-time sequence $x_s[k]$ is obtained from $x(t)$ by means of the sampling strategy $(N,\Delta t)$, the Discrete Fourier Transform $X_s(f)$ of $x_s[k]$ is related to $X(f)$ by the well known sampling relationship:

$$X_s(f) = \sum_{m=-\infty}^{+\infty} X(f - mNf_s) e^{j2\pi(f-mNf_s)\Delta t} \tag{2.2.3}$$

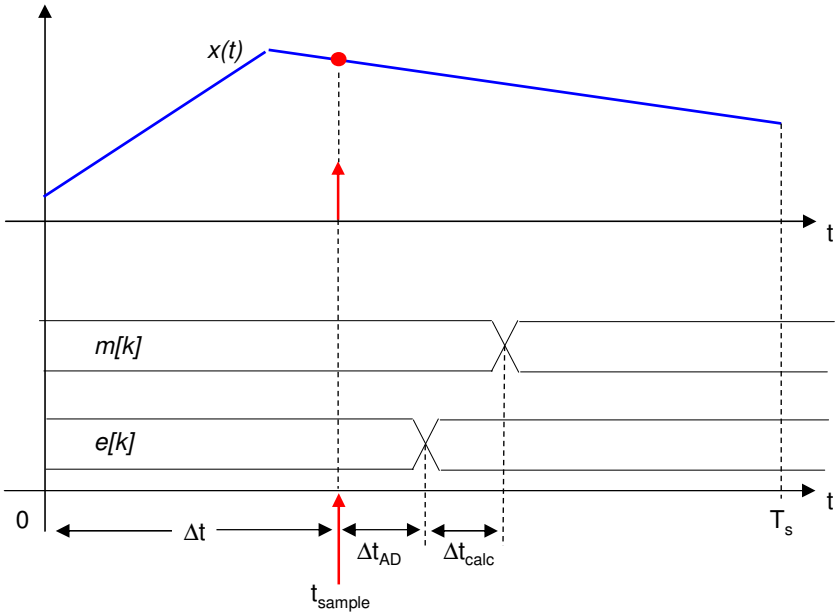

Fig. 2.2.1 – Typical timing diagram of a single-sampling strategy (1,Δt)

2.2.1. Single Sampling Approach

Single sampling strategies are of the form (1,Δt); a typical timing diagram of a single sampled digital controller is shown in Fig. 2.2.1. The converter state variable *x(t)* is sampled in $t=t_{sample}$. The next sample of the digital error signal *e[k]* is available to the digital compensator once the A/D conversion is completed; the A/D conversion time is indicated as Δt_{AD} in Fig. 2.2.1. The digital compensator then calculates the control signal *m[k]* with some computational delay Δt_{calc}. The resulting value is latched by the digital pulse-width modulator into its internal registers to generate the next PWM pulse.

In single sampling approaches the most relevant *aliasing effect* affecting the resulting discrete-time sequence is represented by a DC level corruption. For (1,Δt) strategies (2.2.3) yields:

$$X_s(f) = \sum_{m=-\infty}^{+\infty} X(f - mf_s) e^{j2\pi(f-mf_s)\Delta t} \qquad (2.2.4)$$

Thus:

$$X_s(0) = \sum_{m=-\infty}^{+\infty} X(mf_s) e^{j2\pi(mf_s)\Delta t} \tag{2.2.5}$$

In DC-DC converters a systematic offset in the output voltage or current regulation can result from (2.2.5) if the sampling instant position Δt is not chosen properly.

As an example, let us consider a 12V-1.5V application requiring the average output voltage to be regulated to within ±0.5% of the nominal voltage. If a 20mV peak-to-peak triangular (i.e. ESR-dominated) switching ripple is superimposed to the output voltage, a (1,0) sampling strategy would yield $X_s(0)=X(0)$-10mV, bringing the output voltage out of the regulation window. Though any systematic offset could be digitally compensated by adjusting the digital reference, a cleaner solution is to place the sampling instant in order to sample the analog waveform where it is close to its average value. In the preceding example, where a triangular ripple is observed at the converter output, it is common practice to sample the output voltage either in the middle of the turn-on or in the middle of the turn-off switching phases. In trailing edge modulations, $(1,DT_s/2)$ or $(1,(1+D)T_s/2)$ strategies are adopted on this purpose, while (1,0) or $(1,T_s/2)$ strategies are employed if triangular modulations are used. Please note that with triangular modulations the sampling strategy that achieves the correct average value sampling does not depend on the converter operating point.

In low-voltage applications running at $D<<1$, sampling in the middle of the turn-off phase is usually preferred as it places the sampling instant sufficiently far from switching transitions that could inject unacceptable switching noise into the feedback loop.

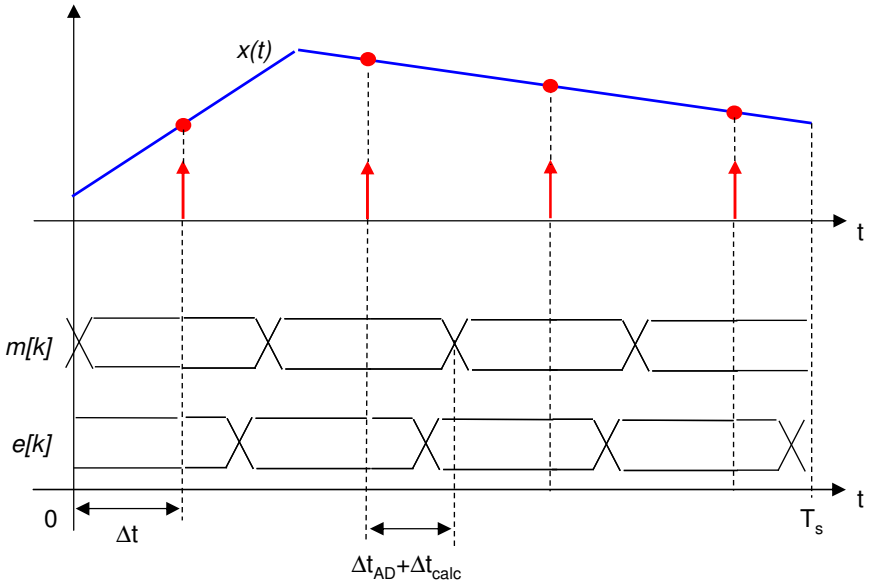

Fig. 2.2.2 – Typical timing diagram of a (4,Δt) multiple sampling strategy

2.2.2. *Multiple Sampling Approach*

In multiple sampling strategies more than one sample is acquired and processed at each switching period. Figure 2.2.2 illustrates an example of timing diagram of a (4,Δt) sampling strategy.

When employing the multiple sampling the DC level of the sampled sequence is less affected by aliasing effects, as higher order harmonics of the analog signal are now superimposing at $f=0$. However, *switching frequency harmonics* of the type $f_j = jf_s$, $1<j\leq N-1$, are now sampled and become integral part of the spectrum of $x_s[k]$, as pointed out by (2.2.3). This *switching frequency ripple injection* represents the major drawback found in multiple sampling strategies, as it represents a source of disturbances for the digital compensator and the feedback loop. The subject will be extensively addressed in Chapter III.

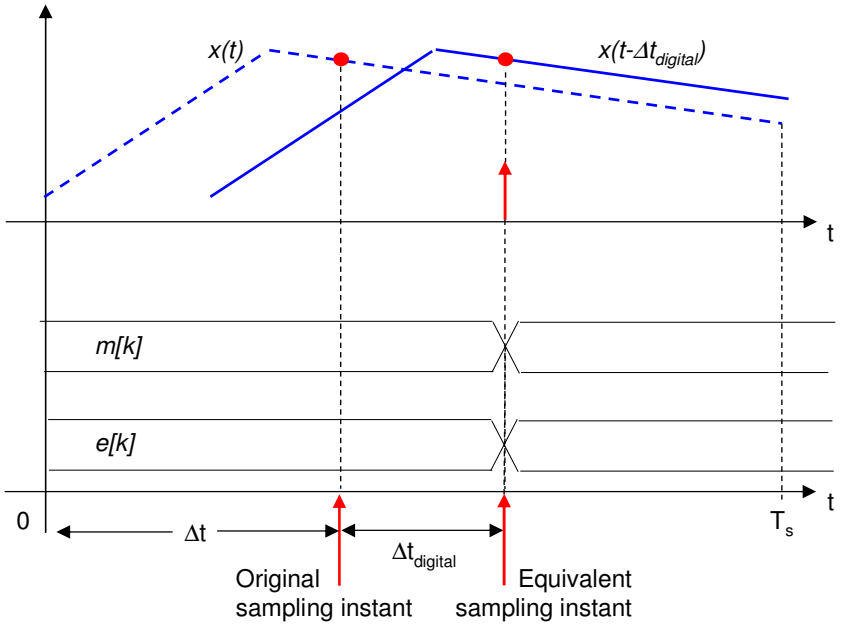

Fig. 2.2.3 – Equivalent modeling of digital delays

2.2.3. *Modeling of Digital Delays*

The A/D conversion time Δt_{AD} and the computational delay Δt_{calc} of the digital compensator represent delay times which occur in the digital domain. However, for modeling purposes it is more convenient to represent these delays in the analog domain and treat the A/D conversion and the compensator as if they were delay-free.

Referring to Fig. 2.2.1, it is sufficient to delay the analog waveform by $\Delta t_{AD} + \Delta t_{calc}$ seconds and shift the sampling event of the same quantity. More formally, a $(N,\Delta t)$ sampling strategy in which a delay $\Delta t_{digital}$ occurs in the digital processing of the information is equivalent to a $(N, \Delta t + \Delta t_{digital})$ strategy in which the digital system is delay-free, provided that the analog waveforms are delayed by $\Delta t_{digital}$ before the sampling occurs. Figure 2.2.3 illustrates the concept. The analog signal $x(t)$ is delayed

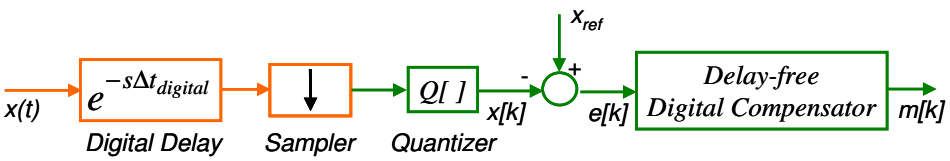

Fig. 2.2.4 – Block diagram model accounting for digital delays

by $\Delta t_{digital} = \Delta t_{AD} + \Delta t_{calc}$ and then sampled. The error waveform $e[k]$ and the modulating signal $m[k]$ are now updated instantly, thus keeping full equivalence with Fig. 2.2.1. Figure 2.2.4 illustrates the block diagram corresponding to this modeling approach.

2.3. Discrete-Time Modeling Of Digitally Controlled SMPS

In this section we will focus on the modeling of the control loop. Thus, referring back to Fig. 2.1.1, we will focus on the systems and elements found along the feedback path. As a case study, a voltage-mode control scheme will be first considered and discussed in Subsection 2.3.1. The modeling concepts presented can be nevertheless extended to more complex control schemes; a digital current-mode control example will be given at the end of this Section.

Special care has to be paid when modeling the small-signal behavior of the pulse-width modulator. Subsection 2.3.2 is devoted to the purpose of summarizing the main dynamic characteristics of analog and digital pulse-width modulators. For an extended and detailed analysis, please refer to Chapter III.

The ultimate goal of this section is the derivation of the *discrete-time equivalent model* of a digitally controlled DC-DC converter. This subject will be addressed in Subsection 2.3.3.

2.3.1. Voltage Mode Control Loop

Figure 2.3.1 illustrates a voltage-mode control loop at a small-signal transfer function level. The power converter reacts, through its control-to-output transfer function $G_{vd}(s)$, to the analog control signal $\hat{d}(t)$, which represents the small-signal content of the PWM waveform produced by the pulse-width modulator, as defined in (2.1.1). An additional term, not shown in Fig. 2.3.1, may be included to model the gate driving delay Δt_G, as discussed in Section 2.1.1. Alternatively, one may think of having the gate driving delay modeled in the transfer function $G_{vd}(s)$ itself.

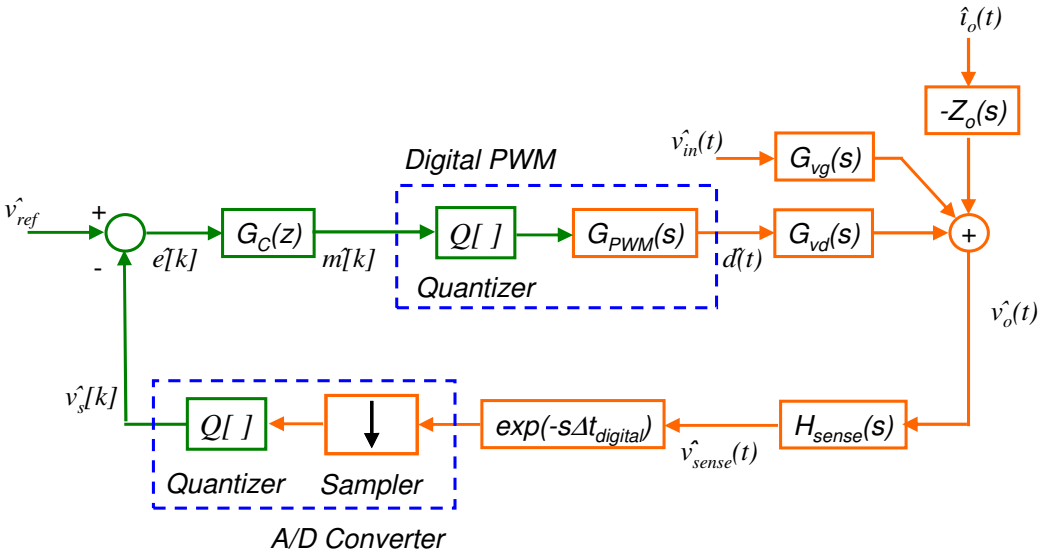

Fig. 2.3.1 – Block Diagram Of a Voltage Mode Digital Control Loop

The converter output current $\hat{i}_o(t)$ and the converter input voltage $\hat{v}_{in}(t)$ represent disturbances that superimpose on the output voltage $\hat{v}_o(t)$ through the converter open-loop output impedance $Z_o(s)$ and the open-loop audiosusceptibility $G_{vg}(s)$ respectively.

The analog sensing and conditioning circuitry for the converter output voltage $\hat{v}_o(t)$ has been described in Fig. 2.3.1 by means of an overall transfer function $H_{sense}(s)$; its output signal $\hat{v}_{sense}(t)$ is then sampled and quantized to a digital sequence $\hat{v}_s[k]$. Please note that in Fig. 2.3.1 the overall digital delay $\Delta t_{delay} = \Delta t_{AD} + \Delta t_{calc}$ has been modeled in the analog domain, as described in Section 2.2.

A *single-sampling* strategy will be assumed here; as discussed in Section 2.2, this means that the sampling frequency $f_{sampling}$ of the converter state variable $v_o(t)$ is equal to the switching frequency:

$$f_{sampling} = f_{switching} \tag{2.3.1}$$

The digital signal $\hat{v}_s[k]$ is compared with a digital reference $\hat{v}_{ref}$. The resulting error signal $\hat{e}[k]$ is then processed by the digital compensator. In what follows we will assume a linear and time-invariant compensation system which processes the error

signal by means of a control law of the type (2.1.7) to produce the discrete time modulating signal $\hat{m}[k]$. The z-domain transfer function corresponding to (2.1.7) is given by:

$$G_c(z) \equiv \frac{M(z)}{E(z)} = \frac{\sum_{j=0}^{m} b_j z^{-j}}{1 - \sum_{i=1}^{n} a_i z^{-i}}, \tag{2.3.2}$$

The control signal $\hat{m}[k]$ represents the output of the digital system and the input of the digital pulse-width modulator, which acts as a D/A converter. Its output, $\hat{d}(t)$, is related to $\hat{m}[k]$ by the modulator transfer function $G_{PWM}(s)$. A quantization of the control signal $\hat{m}[k]$ due to the finite DPWM resolution is also involved, as shown in Fig. 2.3.1.

When employing digital pulse-width modulators the relationship between $\hat{d}$ and $\hat{m}$ exhibits characteristics which do not have an analog counterpart, and therefore have to be carefully modeled. The next Subsection has the purpose of summarizing the differences between analog and digital pulse-width modulators, as well as to precisely specify the $\hat{m}$-$\hat{d}$ small-signal relationship that holds in a digitally controlled converter.

As this Section deals with small-signal modeling, quantization effects present along the feedback loop will be temporarily ignored. The subject will be discussed in Section 2.4.

2.3.2. The Pulse-Width Modulator

Generally speaking, two main families of pulse-width modulators can be identified, namely *naturally sampled* and *uniformly sampled* modulators. The purpose of this subsection is to clarify the differences between these two classes, as well as summarizing their small-signal behavior. The main results discussed here are derived in [60-62].

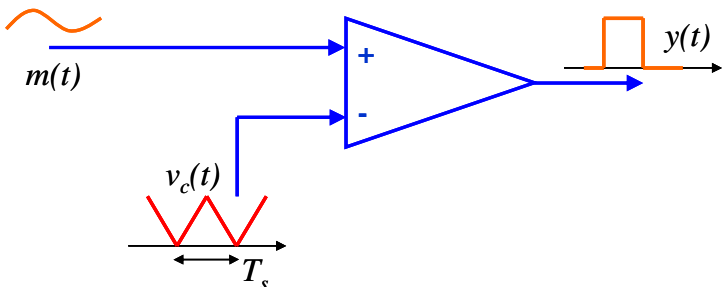

Fig. 2.3.2 – Naturally Sampled Pulse-Width Modulator

i. Naturally Sampled And Uniformly Sampled PWMs

A large signal equivalent model of a naturally sampled modulator is shown in Fig. 2.3.2; a comparator generates the PWM waveform *y(t)* by comparing the modulating signal *m(t)* with a periodic carrier $v_c(t)$. The *switching period* T_s is defined as the period of the carrier waveform. The turn-on and turn-off events are generated when the carrier equals the instantaneous value of *m(t)*; thus, the modulator *naturally samples m(t)* during each switching period. Depending on the shape of the carrier $v_c(t)$, different modulation schemes are obtained. Figure 2.3.3 summarizes the three most common modulation schemes obtained from a triangular carrier. In the *trailing-edge modulation* $v_c(t)$ is a positive slope sawtooth waveform; the turn-on instant of the modulator output, i.e. the position of the leading edge, is kept constant, while the turn-off event is modulated by *m(t)*. A perfectly symmetrical situation is the *leading-edge modulation*, obtained from a negative slope sawtooth-like carrier. Now *m(t)* modulates the leading

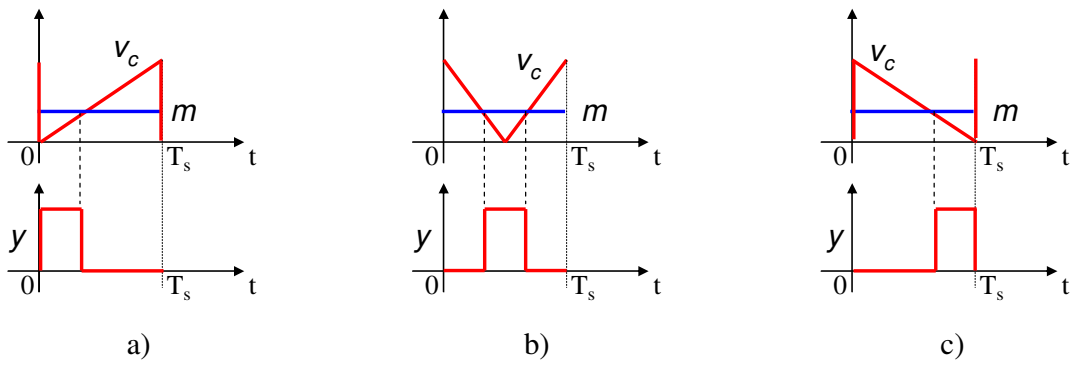

Fig. 2.3.3 – Common PWM Modulation Schemes: trailing edge modulation (a), triangular modulation (b) and leading edge modulation (c)

edge, while the turn-off event is kept constant. Finally, a *triangular modulation* is obtained when $v_c(t)$ is a triangular signal with equal rise and fall times within the switching period. Both the turn-on and turn-off events are modulated, and the PWM pulse is now centred in the middle of the switching period. Figure 2.3.4 illustrates the equivalent large signal model of a *uniformly sampled modulator*. These modulators differ from the naturally sampled ones in the way they process the input modulating signal before comparing it with the carrier. More precisely, the input modulating signal $m(t)$ now undergoes a *sample-and-hold* action before being compared with $v_c(t)$. As already mentioned, we are assuming in this Section that a single-sampling strategy is adopted by the modulator, i.e. the sampling frequency equals the switching frequency. Thus, the signal actually compared with $v_c(t)$ – denoted with $m_h(t)$ in Fig. 2.3.4 – is a staircase-like signal which assumes a constant value throughout the whole switching period, this value being equal to the sample of the input modulating signal m.

Analog pulse width modulators, i.e. modulators which process an analog modulating signal, can be either naturally sampled or uniformly sampled. On the other hand, digital pulse-width modulators employed in digital control loops like the one illustrated in Fig. 2.3.1 inherently have a uniformly-sampled nature. In this case no analog signal $m(t)$ is present, as the discrete-time sequence $m[k]$ directly comes from a discrete-time system, i.e. the digital compensator.

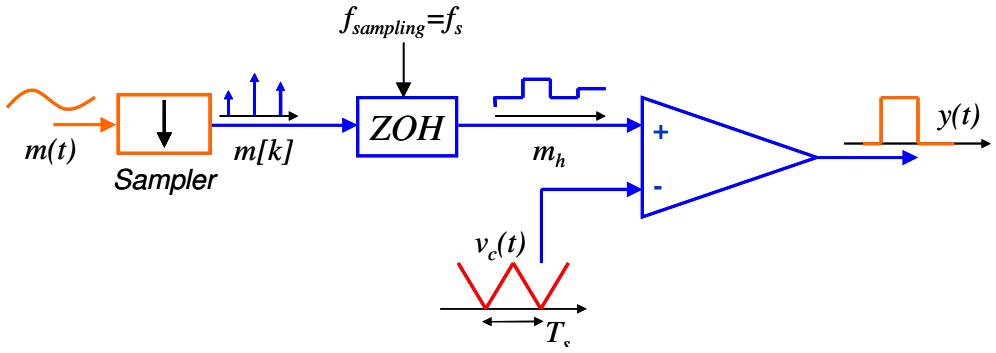

Fig. 2.3.4 – Uniformly Sampled Pulse-Width Modulator

Tab. 2.3.1 – Small-signal analysis results for uniformly-sampled modulators

Modulation Type	$A(j\omega,D)$	$t_d(D),\ \Delta t=0$	$t_d(D),\ \Delta t>0$
Trailing Edge	$1/v_{c,max}$	$D\cdot T_s$	$D\cdot T_s+(T_s-\Delta t)$
Leading Edge	$1/v_{c,max}$	$(1-D)\cdot T_s$	$(1-D)\cdot T_s+(T_s-\Delta t)$
Triangular	$\cos(\omega DT_s/2)/v_{c,max}$	$T_s/2$	$T_s/2+(T_s-\Delta t)$

ii. Small-Signal Modeling

The small-signal analysis of a pulse-width modulator consists in establishing the relationship between the modulating signal $m(t)$ and $\hat{d}(t)$ – defined in (2.1.1) – under the hypothesis of a small perturbation $\hat{m}(t)$ superimposed on $m(t)$. Moreover, a *small-ripple approximation* will be assumed here, based on the hypothesis that any switching-frequency ripple superimposed on $m(t)$ is of negligible amplitude with respect to the carrier amplitude.

The calculation is based on the Fourier analysis of the signal $y(t)$ and depends on the specific nature of the modulator considered, i.e. naturally sampled or uniformly sampled. This analysis is not presented in this Section, as a more general calculation will be proposed in Chapter III for multiple-sampled modulators. The results summarized in this section will be then obtainable as limit cases, as we will see.

As far as the naturally sampled modulators are considered, their small-signal action on $\hat{d}(t)$ is that of a simple gain:

$$G_{PWM}(s) \equiv \frac{D(s)}{M(s)} = \frac{1}{v_{c,\max}}, \tag{2.3.3}$$

where $v_{c,max}$ represents the amplitude of the carrier signal. Thus, a naturally sampled modulator does not introduce any phase shift within the feedback loop.

On the other hand, uniformly sampled modulators exhibit a radically different behavior, as their small-signal transfer function has the form:

$$G_{PWM}(s) \equiv \frac{D(s)}{M(s)} = A(s,D)\exp(-st_d(D)), \qquad (2.3.4)$$

where $A(s,D)$ is a real quantity, while t_d represents a time delay. Both A and t_d are, in general, dependent on the steady-state duty ratio D, i.e. on the converter operating point.

As far as the gain $A(s,D)$ is concerned, this is either a constant or a slow-varying function of both the frequency and D. In all cases of practical interest it can be approximated with $1/v_{c,max}$.

The equivalent delay time t_d, however, cannot in general be neglected and represents the most profound difference between uniformly sampled and naturally sampled modulators. It can be shown that t_d depends both on D and on Δt, i.e. the relative position of the sampling instant of the modulating signal with respect to the turn-on / turn-off instants of the PWM waveform $y(t)$. *Uniformly sampled pulse-width modulators, and therefore digital pulse-width modulators, introduce a small-signal phase lag which depends on the converter operating point and on the adopted sampling strategy*.

Table 2.3.1 reports the expressions of $t_d(D)$ and $A(j\omega,D)$ for the three modulation schemes illustrated in Fig. 2.3.3 for $\Delta t=0$ and $\Delta t>0$. The general considerations discussed above can be verified.

2.3.3. Discrete-Time Equivalent Of The Power Converter

We are now in the position of deriving the discrete-time equivalent model $G_p(z)$ of the power converter. $G_p(z)$ will be defined here as the z-domain relationship between the digital control signal $\hat{m}[k]$ produced by the compensator and the sequence $\hat{v}_s[k]$. The latter represents – once subtracted from $\hat{v}_{ref}$ – the input signal of the compensator itself. Thus, looking back at Fig. 2.2.1 and letting $\hat{v}_{in}=0$ and $\hat{\imath}_o=0$, we define $G_p(z)$ as:

$$G_p(z) \equiv \frac{V_s(z)}{M(z)} \tag{2.3.5}$$

Sampled data systems theory asserts that the impulse response of the discrete-time system (2.3.5) is the sampled version of the impulse response of the analog system defined by:

$$G_p(s) \equiv G_{PWM}(s) G_{vd}(s) H_{sense}(s) \exp(-s\Delta t_{digital}) \tag{2.3.6}$$

The desired discretization equation is thus obtained:

$$G_p(z) = T_s Z_{T_s}[G_p(s)], \tag{2.3.7}$$

where $Z_{Ts}[\cdot]$ denotes the Z-transform operator applied with a sampling step equal to the switching period T_s.

Equation (2.3.7) allows, in principle, the analytical derivation of $G_p(z)$. However, if certain extremely simple cases are excluded, the calculation is lengthy and often results in rather cumbersome expressions, from which poor physical insight can be drawn. Nor a closed-form expression of $G_p(z)$ is required in many practical design situations. Thus, the discretization (2.3.7) is better computed with the aid of a computer-based mathematical environment (e.g. Matlab).

From (2.3.7) and given the digital compensator transfer function (2.3.2) the system loop gain can be explicited:

$$T(z) = G_c(z)G_p(z) \tag{2.3.8}$$

2.3.4. Examples

Two simulation examples will be presented in this Section, namely a voltage-mode control and a current-mode control of a given power converter, with the main purpose of verifying the accuracy of the discrete-time models presented in Section 2.3.3.

Let us consider a 12V-to-5V, 50W synchronous buck converter with L = 2μH, C = 1mF, ESR = 1mΩ, switching frequency f_s = 200kHz. Stability margins specifications require a minimum phase margin $m_{\Phi,min}$ = 45° and a minimum gain margin GM_{min} = 10dB. A triangular, uniformly sampled modulator will be employed. A/D conversion delays as well as the compensator computational delays will be assumed to form a negligible fraction of the switching period T_s = 5μs and therefore neglected.

i. Voltage-Mode Control

Voltage mode control has been discussed in Section 2.2.3. Please refer to Fig. 2.3.1

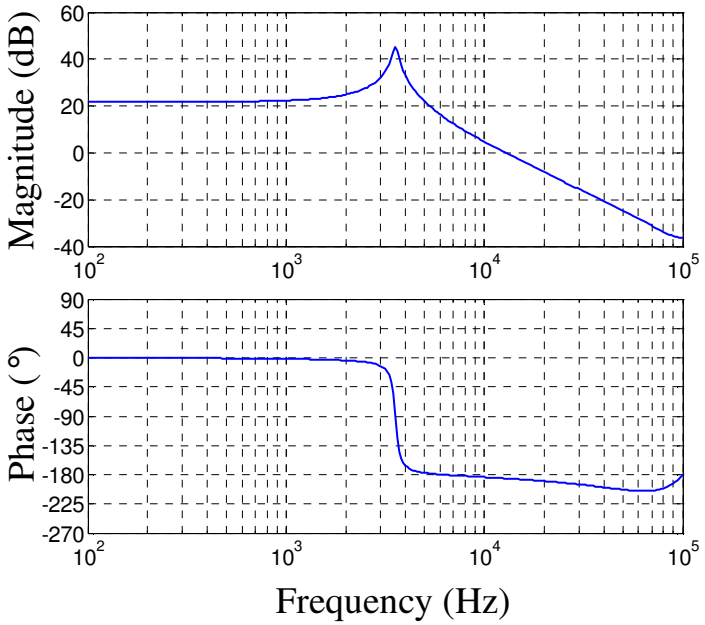

Fig. 2.3.5 – Bode diagrams of the control-to-output discrete-time transfer function $G_p(z)$

for the corresponding block diagram.

A (1,0)-sampled digital PID compensator will be designed here to achieve the desired stability margins at a closed-loop bandwidth $f_c = f_s/10 = 20$kHz. On this purpose, let us first evaluate the discrete-time equivalent of the power converter. According to (2.3.7) and letting $H_{sense}(s) = 1$:

$$G_p(z) = T_s Z_{T_s}[G_{vd}(s)\exp(-s\frac{T_s}{2})], \tag{2.3.9}$$

where the transfer function of the triangular modulator has been approximated with $G_{PWM}(s) = \exp(-sT_s/2)$, according to the discussion developed in Section 2.3.2. Bode diagrams of $G_p(z)$ are illustrated in Fig. 2.3.5, from which a phase lag greater than 180° is seen at $f = f_c = 20$kHz. A PID structure is therefore mandatory to achieve the necessary phase margin:

$$G_c(z) = K\frac{(1-z_1 z^{-1})(1-z_2 z^{-1})}{1-z^{-1}} \tag{2.3.10}$$

The design of the PID compensator was carried out by first placing one of the two PID zeros close to the resonant frequency $f_0 = 3.6$ kHz of the power converter, then placing the second zero so that a phase margin of about $m_\Phi = 50°$ is achieved at $f = f_c = 20$kHz. Finally, the PID gain K was selected to achieve a unity loop gain at f_c. A

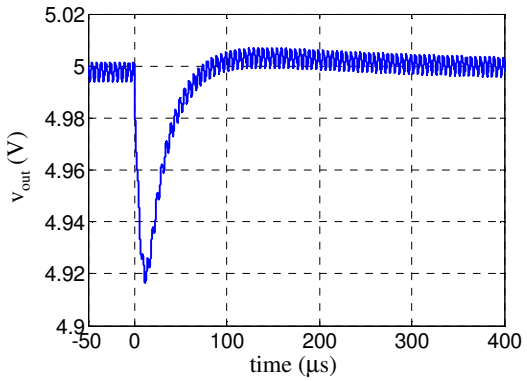

Fig. 2.3.6 – Output voltage during a 0A→10A load step up transient

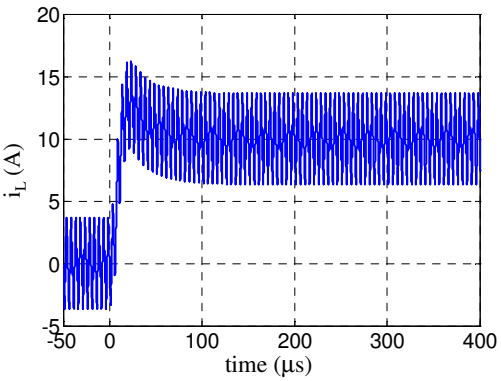

Fig. 2.3.7 – Inductor current during a 0A→10A load step up transient

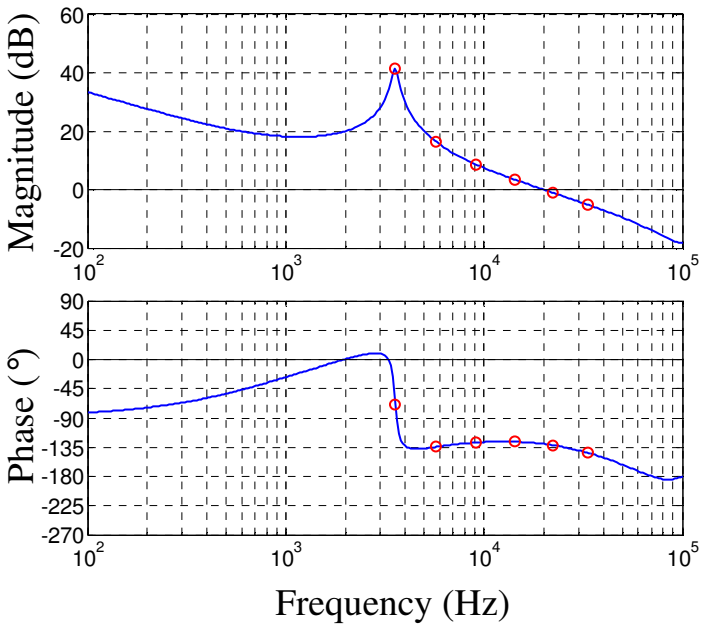

Fig. 2.3.8 – Theoretical (continuous line) and simulated (dots) Bode diagrams of the compensated loop gain T(z)

Matlab routine was written to refine calculations, yielding z_1 = 0.974, z_2 = 0.894, K = 4.38 V^{-1}. These parameters define the PID structure (2.3.10) and allow the calculation of the system loop gain $T(z)$ (2.3.8).

The designed control has been simulated in the Matlab/Simulink environment. Load step-up transients from 0A to 10A are shown in Fig. 2.3.6 and 2.3.7 for the output voltage and inductor current respectively. Damping and settling time of the load transient responses are in agreement with the designed phase margin and bandwidth.

A further verification of the modeling accuracy of (2.3.9) is given in Fig. 2.3.8. Loop gain simulations were carried out in the frequency range f_0-f_s/5 on the same Simulink model used to obtain the load transients illustrated in Fig. 2.3.7 and 2.3.8. Simulation points are superimposed to the theoretical loop gain $T(z) = G_c(z) \cdot G_p(z)$ in the Bode diagrams shown in Fig. 2.3.8, yielding an excellent matching both in magnitude and phase. Inspection of Fig. 2.3.8 reveals a gain margin GM = 14dB, well above the given specifications.

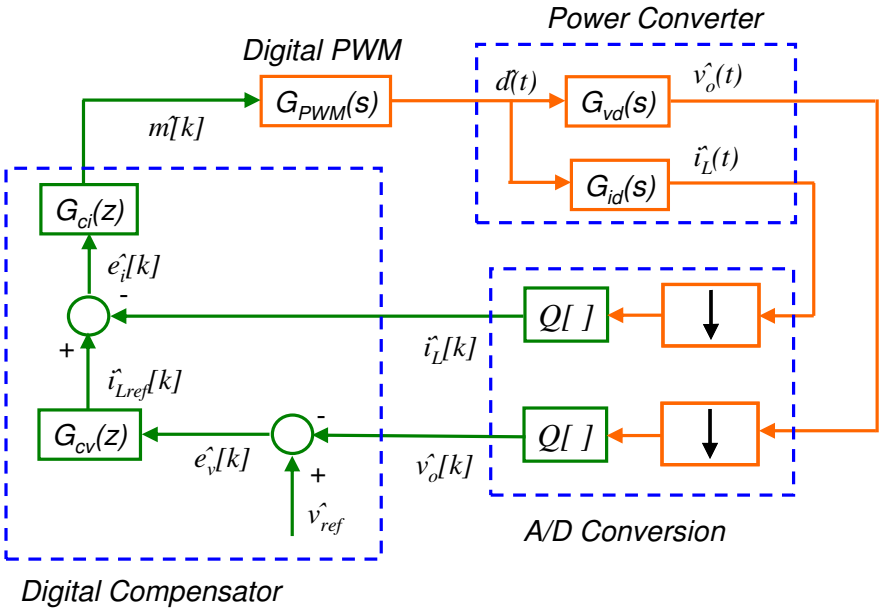

Fig. 2.3.9 – Block diagram of a digital current mode control scheme

ii. Current-Mode Control

It is interesting to develop a current mode controller for the case study considered in this Section, as this will allow to appreciate how the modeling concepts presented in Section 2.3.3 for voltage-mode loops naturally extend to more complex control schemes.

Let us consider the current-mode control block diagram illustrated in Fig. 2.3.9. The inner current loop samples the inductor current and compares it with the reference sequence $\hat{\imath}_{L,ref}$ set by the voltage loop controller $G_{cv}(z)$. The current error $\hat{e}_i[k]$ is processed by the current loop regulator $G_{ci}(z)$, which produces the modulating signal $\hat{m}[k]$. The voltage loop regulator generates the reference signal for the current loop by processing the voltage error $\hat{e}_v[k]$, obtained through sampling of the converter output voltage. For the sake of simplicity, other independent inputs of the power stage such as the load current $\hat{\imath}_o(t)$ and the input voltage $\hat{v}_{in}(t)$ are not shown in Fig. 2.3.9.

Similarly to what is usually done in analog control design, the current loop gain will be designed to achieve a rather high bandwidth, this being possible because of the good

phase behavior of the duty cycle-to-inductor current transfer function $G_{id}(s)$ of the power converter:

$$G_{id}(s) = V_{in} \frac{sC}{1 + sESR \cdot C + s^2 LC} \tag{2.3.11}$$

A note on (2.3.11). In this context we define $G_{id}(s)$ as the *open circuit* inductor current $\hat{\imath}_L(s)$ over the applied duty cycle $\hat{d}(s)$, i.e. when $\hat{\imath}_o(s) = 0$, implying that the load is being modeled by an independent current source. Whenever the load is modeled by a resistor R_o, and as long as R_o is much greater than the open-loop impedance $Z_o(s)$ of the power converter, it is easy to prove that its effect on (2.3.11) is that of moving the zero from the origin to $s_z = -1/(R_oC)$. Beside these modeling details, the following considerations can be considered of general validity. A (1,0) sampling strategy will be adopted for both the voltage and current sampling. Due to the triangular shape of the inductor current, this translates in a correct sampling of its average value, thus reducing aliasing effects discussed in Section 2.2.

The design of the current loop compensator $G_{ci}(z)$ will be carried out by first

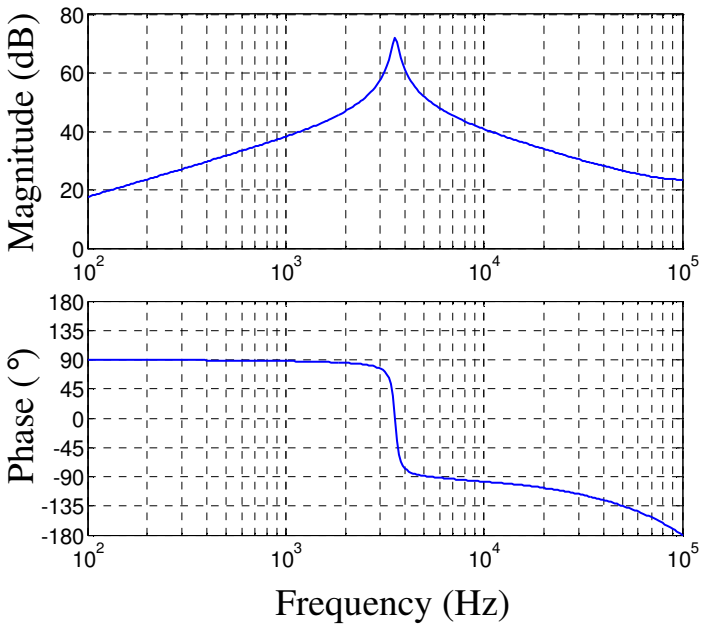

Fig. 2.3.10 – Bode diagrams of the current loop control-to-output transfer function $G_{pi}(z)$

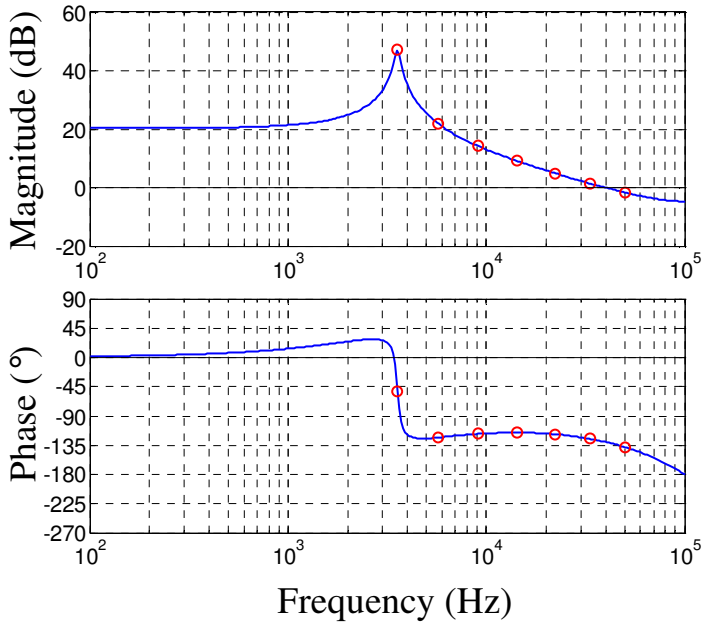

Fig. 2.3.11 – Theoretical (continuous line) and simulated (dots) Bode diagrams of the compensated current loop gain $T_i(z)$

deriving the current loop control-to-output transfer function $G_{pi}(z)$ of the power converter, i.e. the discrete-time transfer function between the modulating signal $\hat{m}$ and the sampled inductor current $\hat{\imath}_L[k]$. The derivation of $G_{pi}(z)$ can be obtained through the very same reasoning already developed in Section 2.3.3, leading to:

$$G_{pi}(z) \equiv \frac{i_L(z)}{M(z)} = T_s Z_{T_s}[G_{id}(s)\exp(-s\frac{T_s}{2})] \qquad (2.3.12)$$

Bode diagrams of $G_{pi}(z)$ are shown in Fig. 2.3.10. Similarly to what happens in the analog domain, the good phase behavior of $G_{id}(s)$ is preserved in the digital domain. Comparison with Fig. 2.3.5 reveals a drastically lower phase lag at high frequencies.

A PI compensator can be designed to achieve a current loop bandwidth $f_{ci} = f_s/5 = 40\text{kHz}$ by placing its zero close to f_0 and properly adjusting the compensator gain. The current loop regulator $G_{ci}(z)$ has therefore the following structure:

$$G_{ci}(z) = K_{pi} + \frac{K_{ii}}{1 - z^{-1}}, \qquad (2.3.13)$$

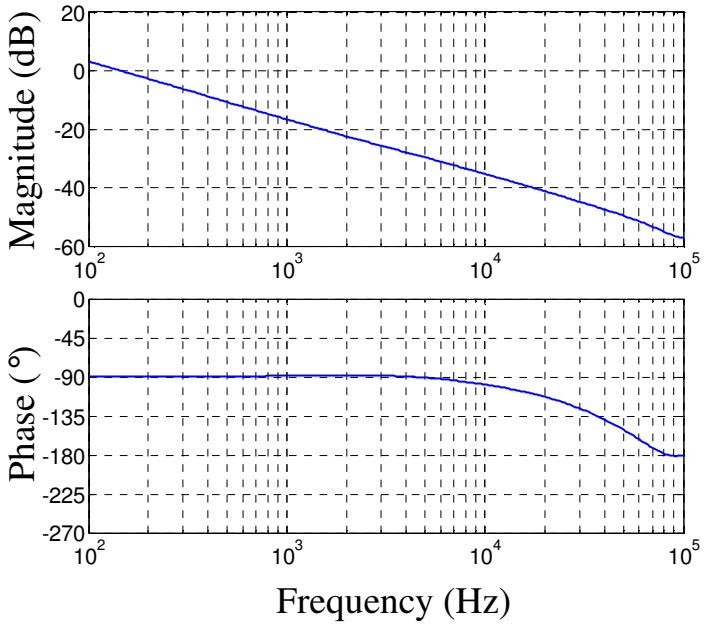

Fig. 2.3.12 – Bode diagrams of the voltage loop control-to-output transfer function $G_{pv}(z)$

with K_{pi} = 0.037 A^{-1} and K_{ii} = 4.3·10^{-3} A^{-1}. The Bode diagrams of the resulting current loop gain $T_i(z) = G_{ci}(z) \cdot G_{pi}(z)$ are shown in Fig. 2.3.11, from which a phase margin of about 50° and a gain margin of 4.7dB are visible.

Having designed the current loop regulator, the design of the voltage loop transfer function $G_{cv}(z)$ can be performed once the voltage loop control-to-output transfer function $G_{pv}(z)$ is obtained, $G_{pv}(z)$ being defined as the transfer function between the reference current signal $\hat{\imath}_{Lref}[k]$ and the sampled output voltage $\hat{v}_o[k]$. Straightforward block diagram algebra can be employed to derive $G_{pv}(z)$:

$$G_{pv}(z) \equiv \frac{v_o(z)}{i_{Lref}(z)} = \frac{G_{ci}(z)}{1+T_i(z)} \cdot T_s Z[G_{vd}(s)\exp(-s\frac{T_s}{2})] \qquad (2.3.14)$$

It is easily seen from its Bode diagrams visible in Fig. 2.3.12 that $G_{pv}(z)$ has a capacitive-like behavior up to about a frequency of 10kHz. This result is by all means expected, since as long as frequencies well below the current loop bandwidth f_{ci} are considered $\hat{\imath}_L \approx \hat{\imath}_{Lref}$ and thus $G_{pv}(z)$ approaches the capacitive impedance Z_c of the power stage.

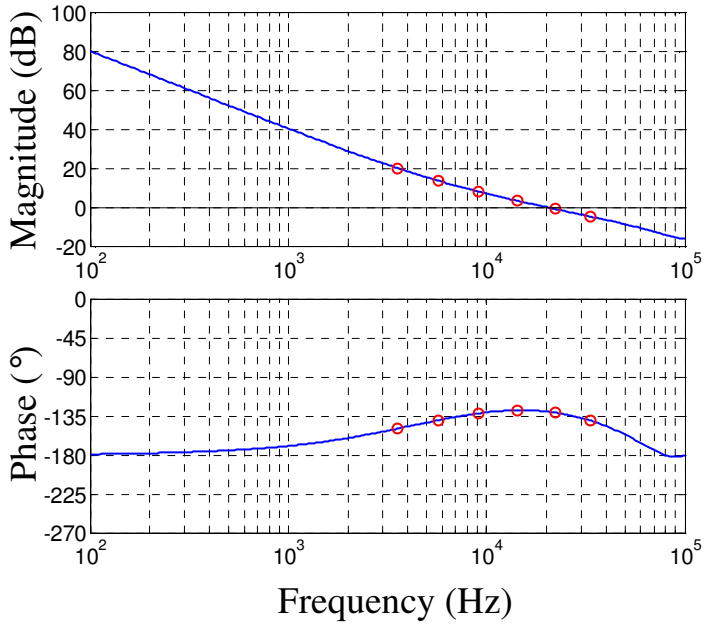

Fig. 2.3.13 – Theoretical (continuous line) and simulated (dots) Bode diagrams of the compensated voltage loop gain $T_v(z)$

Similarly to what done for the current loop, a PI structure will be chosen for the voltage loop regulator, designed for a closed loop bandwidth $f_{cv} = f_s/10 = 20$kHz and 50° phase margin:

$$G_{cv}(z) = K_{pv} + \frac{K_{iv}}{1 - z^{-1}} \tag{2.3.15}$$

with $K_{pv} = 99$ V^{-1} and $K_{iv} = 22$ V^{-1}. The Bode diagrams of the resulting voltage loop gain $T_v(z) = G_{cv}(z) \cdot G_{pv}(z)$ are shown in Fig. 2.3.13. A 14dB gain margin is found, within the minimum 10dB specification.

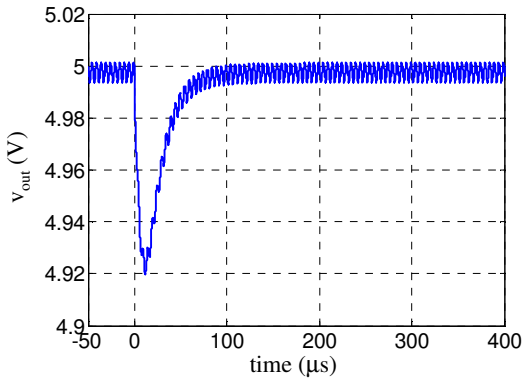

Fig. 2.3.14 – Output voltage during a 0A→10A load step up transient

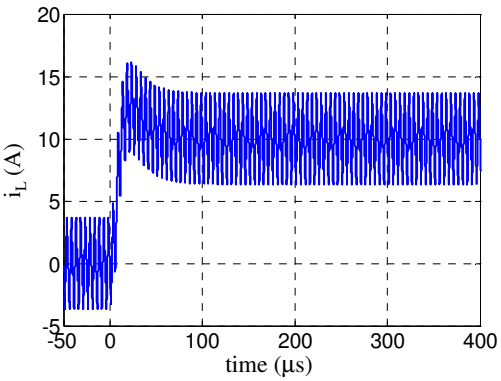

Fig. 2.3.15 – Inductor current during a 0A→10A load step up transient

Following the previous approach aimed to verify the correctness of the discrete-time models, the loop gains $T_i(z)$ and $T_v(z)$ have been simulated and the results compared to the analytically derived plots. In both Fig. 2.3.11 and 2.3.13 the simulation points exactly match the expected results.

The simulated transient response of the resulting current-mode control is shown in Fig. 2.3.14 and 2.3.15 as far as the output voltage and inductor current are concerned.

2.4. Quantization Effects And Limit Cycling

Quantization effects represent one of the aspects that are unique to digital control systems. The nonlinearities introduced by the different quantizations present in the feedback loop may degrade the system performance affecting its behavior in different ways, the effects ranging from accuracy issues to limit cycle oscillations.

2.4.1. Sources Of Quantization

This section provides some basic classification among the different sources of quantization present in a typical digital control system. In what follows, the voltage-mode control illustrated in Fig. 2.2.1 will be taken as a reference. Three points can be identified in the feedback loop where quantization effects come into play: the A/D conversion, the DPWM quantization and the digital compensator, where finite-precision arithmetic causes quantization errors to affect both the compensator coefficients and the calculations. In this Section *uniform* quantizers will be considered, i.e. characterized by a constant quantization step. Uniform quantizers are common in digital control, where the low cost and low complexity requirements of microcontrollers or hardwired logic dictate the use of fixed-point arithmetic for calculation purposes, preferred to floating point arithmetic which has significantly higher overheads in terms of both hardware requirements and speed.

i. A/D Resolution

The A/D resolution, expressed by the width n_{AD} of the A/D converter output binary word, introduces a quantization error affecting the error signal *e[k]* processed by the digital compensator. Thus, n_{AD} limits the extent to which the actual error is known to the digital compensator. Denoting with FSR the *full scale range* of the A/D converter, the *quantization step* $\Delta q_{e,AD}$ on the voltage error signal is:

$$\Delta q_{e,AD} \equiv \frac{FSR}{2^{n_{AD}}} \tag{2.4.1}$$

In most cases it is more meaningful to refer the quantization step to the converter state variable being acquired; for the voltage mode control shown in Fig. 2.2.1:

$$\Delta q_{v,AD} \equiv \frac{FSR}{2^{n_{AD}}} \frac{1}{H_{sense}(0)} \tag{2.4.2}$$

The quantization step (2.4.2) represents an upper limit to the *regulation accuracy* achievable by a given control loop. Of particular importance is the *zero error bin*, which represents the $\Delta q_{v,AD}$-wide interval of output voltage values that produce $e[k] = 0$ and therefore are not distinguished by the digital compensator. Any steady state output voltage lying within the zero-error bin does not produce any further regulating action. As a consequence, given a setpoint V_{ref}, A/D quantization causes the digital compensator to be able to regulate V_{ref} only to within $\Delta q_{v,AD}$.

ii. DPWM Resolution

The DPWM resolution n_{DA} is usually limited by either area and power consumption requirements. For this reason the DPWM digital input is usually stored in a binary word which is smaller than the word length of the modulating signal $m[k]$ produced by the control algorithm. The necessary conversion, i.e. truncation, round-off etc…, represents a quantization for the signal $m[k]$ that translates in a duty cycle quantization:

$$\Delta q_{DA} = \frac{1}{2^{n_{DA}}} \tag{2.4.3}$$

Thus, n_{DA} limits the extent to which a desired duty ratio D can be realized to drive the power stage. Even if an infinite resolution A/D is considered, (2.4.3) degrades the output regulation accuracy; referring again the quantization step to the converter output voltage, one has:

$$\Delta q_{v,DA} = \frac{1}{2^{n_{DA}}} G_{vd}(0) \tag{2.4.4}$$

iii. Finite Precision Arithmetic

Two other important sources of quantization error are represented by the quantization of the compensator coefficients and by the truncation and round-off operations occurring during the computational activity of the digital compensator. Both these phenomena can be designed as *finite precision arithmetic quantizations*.

It is well known in the theory of digital filters how coefficients quantization cause the actual – i.e. implemented – transfer function to differ from the desired one. This, of course, also holds when considering the implementation of a digital compensator. The entity of the deviation depends on the word length n_{Coeff} that defines the coefficients resolution, and on the particular realization of the compensator transfer function. The degree of complexity of a digital compensator employed in a SMPS control system is usually quite small, and general guidelines can be followed to ensure a robust implementation in most cases.

Taking, as an example, a digital PID compensator, its *series* – or interacting – implementation allows a direct control on the quantization errors affecting the gain K and the two zeros $z_{1,2}$:

$$G_c(z) = \frac{K_t}{1 - z^{-1}} \cdot (1 - z_1 z^{-1}) \cdot (1 - z_2 z^{-1}) \tag{2.4.5}$$

The PID coefficients K_t, z_1 and z_2 can be then implemented with the required resolution. Another common and quite robust implementation of a PID regulator is the non interacting, or parallel form:

$$G_c(z) = K_p + \frac{K_i}{1 - z^{-1}} + K_d (1 - z^{-1}), \tag{2.4.6}$$

with K_p, K_i and K_d representing the proportional, integral and derivative gain respectively.

Round-off and truncation operations also affect the behavior of the implemented compensator, generating what is known as *calculation noise*. A typical example is the operation of digital multipliers. Given two n-bit binary words, the minimum number of bits required to represent their product without error is $2n$. Thus, whenever the result has to be stored in a shorter binary register, a truncation or round-off operation occurs, depending on the particular multiplier implementation.

Worst-case and stochastic methods exist to estimate the calculation noise superimposed to the output signal produced by the digital compensator and therefore infer the minimum number of bits to be used to store intermediate results. Proper sizing of the intermediate registers and handling of truncations and round-offs usually makes the calculation noise effects negligible with respect to more important contributions like A/D quantizations and DPWM resolution.

2.4.2. Limit Cycle Oscillations

Limit cycle oscillations (LCO) indeed represent the most typical and undesired nonlinear effect in a feedback-based digital or mixed-signal system [65-69]. They represent persistent, amplitude-limited oscillatory modes originated by nonlinearities present in the feedback loop. Beside affecting a clean and stable regulation of the output voltage, LCOs may be undesirable also from an electromagnetic interference (EMI) point of view, as they represent additional frequencies – usually much lower than the converter switching frequency – present in an otherwise stable system.

The study of LCOs present many mathematical difficulties due to their intrinsic nonlinear nature. General criteria and guidelines have nevertheless been proposed in the

literature [65] aimed to establish *necessary* conditions aimed to avoiding LCOs. Some basic considerations will be reported here, assuming that a digital PID compensator is employed. Further details and more sophisticated approaches can be found in the literature.

From (2.4.2) and (2.4.4) a first simple consideration can be formulated: if there is no DPWM quantization level that maps in the ADC zero error bin, then the system *will* exhibit limit cycle oscillations. The reason is that under this condition no DC operating point exists that nulls the error *e[k]*. On the other hand, a constant nonzero error would be indefinitely integrated by the PID integrator, thus violating the DC hypothesis. As a result, *e[k]* will oscillate around the zero error bin maintaining a zero average value. From this discussion, the existence of a DC operating point compatible with *e[k]* = 0 is ensured if the DPWM resolution, referred to the converter output voltage, is finer than the ADC resolution:

$$\Delta q_{v,DA} < \Delta q_{v,AD} \tag{2.4.7}$$

In practice, it is recommended to realize (2.4.7) with a certain margin; an equivalent DPWM resolution two or three bits higher than the A/D resolution is usually advisable.

Even with an infinite resolution DPWM (i.e. $\Delta q_{v,DA} = 0$) the existence of a limit cycle-free DC operating point is not guaranteed because of the integral gain of the PID compensator. To show this, let us consider a steady state condition in which *e[k]* = 0 and let us assume that a transient perturbation occurs, after which the controller restores the correct DC operating point reaching the zero error bin *e[k]* = 0. The final value of the *unquantized* error $e_s[k]$ can be evaluated by application of the final value theorem:

$$\left|e_s[+\infty] - e_s[0]\right| = \left|\lim_{z\to 1}(1-z^{-1})G_c(z)G_p(z)E(z)\right|, \tag{2.4.8}$$

where $G_c(z)$ represents the PID transfer function (2.4.6) and $G_p(z)$ is the discrete-time equivalent of the power converter (see (2.3.9)). For the sake of simplicity, $H_{sense}(s) = 1$ was assumed in (2.4.8).

Evaluation of (2.4.8) yields:

$$\left|e_s[+\infty] - e_s[0]\right| = K_i G_p(1)\left|E(1)\right| \tag{2.4.9}$$

Consistence with the hypothesis $e[+\infty] = 0$ requires that the overall variation of the unquantized error is smaller than the ADC quantization step:

$$K_i G_p(1)\left|E(1)\right| < q_{v,AD} \tag{2.4.10}$$

A *necessary* condition for (2.4.10) is obtained by letting $E(1)$ be equal to the smallest possible error perturbation, i.e. $q_{v,AD}$. Hence:

$$K_i G_p(1) < 1, \tag{2.4.11}$$

which poses a necessary constraint on the compensator integral gain. The meaning of (2.4.11) is that a necessary no-limit cycling condition requires the integral gain to be sufficiently small to fine tune the error in response to small perturbations, so that the zero error bin can be reached through small corrections of the duty cycle command.

Equations (2.4.2) and (2.4.11) are formulated in [65] as two static, necessary no-limit cycling conditions. It must be underlined that the existence of a DC solution compatible with $e[k] = 0$ by no means guarantees that the converter will actually converge to this particular steady-state mode of operation. *Dynamic* no-limit cycling conditions are derived in [66] that formulate additional constraints and better investigate the causes of the onset of LCOs in a digitally controlled SMPS.

As a final note, it is worth to mention other LCO modeling approaches proposed in literature based on energetic and statistical descriptions [67-68].

Chapter III

Multiple Sampling

In Section 2.1.3 we defined the multiple sampling technique as a sampling strategy which consists of employing a sampling frequency $f_{sampling}$ strictly *higher* than the power converter switching frequency f_s, and evaluating the control signal *m[k]* on a sampling cycle basis [39]. In the following we will assume that the sampling frequency is an integer multiple of the switching frequency, so that a number *N* of sampling events occur during each switching period:

$$f_{sampling} = Nf_s \tag{3.1}$$

The present Chapter presents an in-depth analysis of the consequences of (3.1) on the converter equilibrium and closed-loop dynamics. The main result, which is the ultimate motivation for increasing the sampling frequency, is the strong reduction of the DPWM small-signal phase lag which gets decreased, roughly speaking, by a factor *1/N*. This gives rise to the possibility of achieving higher closed-loop bandwidths with respect to the single sampling approach, still maintaining robust stability margins.

On the other hand, oversampling of the converter waveforms containing switching-frequency ripple represent an additional injection of disturbances into the feedback loop; this has been already pointed out in Section 2.3 when considering the spectrum of a discrete-time sequence $x_s[k]$ obtained through a $(N,\Delta t)$ sampling of a continuous signal $x(t)$:

$$X_s(f) = \sum_{m=-\infty}^{+\infty} X(f - mNf_s) e^{j2\pi(f-mNf_s)\Delta t} \tag{3.2}$$

It will be shown how the Pulse-Width Modulator static and dynamic behavior is profoundly affected by the presence of sampled ripple in the modulating waveform, the most striking effect being the onset of *sampling-induced dead bands* in the modulator transcharacteristics. Presence of the sampling-induced dead bands negatively affect the behavior of the closed-loop control system as they easily trigger regulation failures or even oscillating behaviors.

Solutions aimed to restoring the DPWM linearity thus appear mandatory when the multiple sampling strategy is adopted. Chapter IV presents a detailed analysis of different *linearization techniques* which restore partially or completely the DPWM linearity, still retaining the main *phase-boost* property of the multiple sampling approach.

3.1. Motivations For Increasing The Sampling Frequency

The main advantage of the multiple sampling approach is the dramatical reduction of the small-signal phase lag introduced by the DPWM modulator. A rigorous analysis of the small-signal transfer function of a multi-sampled DPWM will be presented in Section 3.2; however, the argument of the phase delay reduction due to the increased

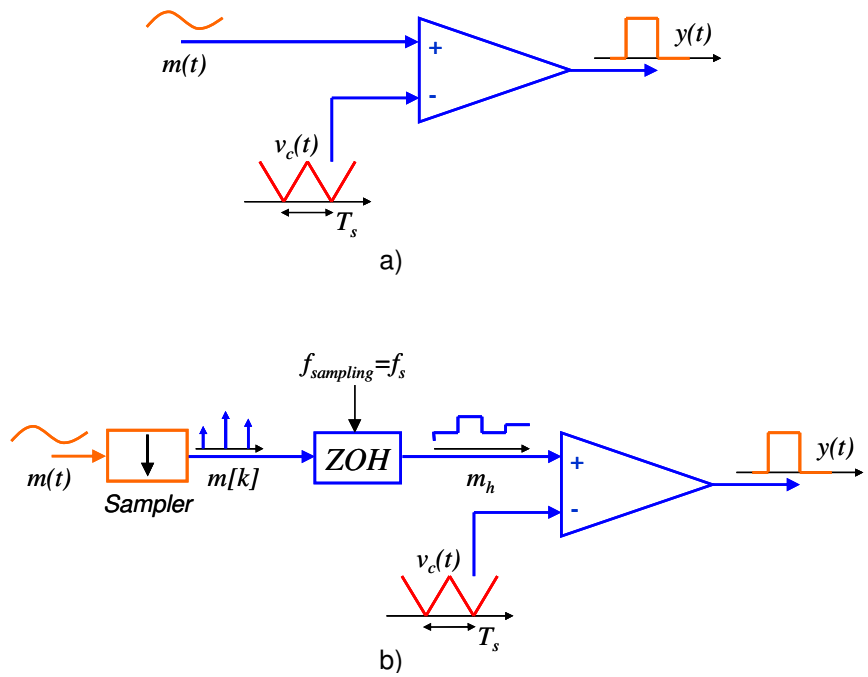

Fig. 3.1.1 – Large-signal models for naturally sampled (a) and uniformly sampled (b) modulators

sampling frequency can be nevertheless understood on an intuitive basis through the following reasoning.

Let us first consider the switching dynamics of a *naturally sampled* pulse width-modulator. Its large-signal model, discussed in Section 2.3, is shown in Fig. 3.1.1.a. The carrier $v_c(t)$ and the modulating signal $m(t)$ are shown in Fig. 3.1.2. A trailing edge

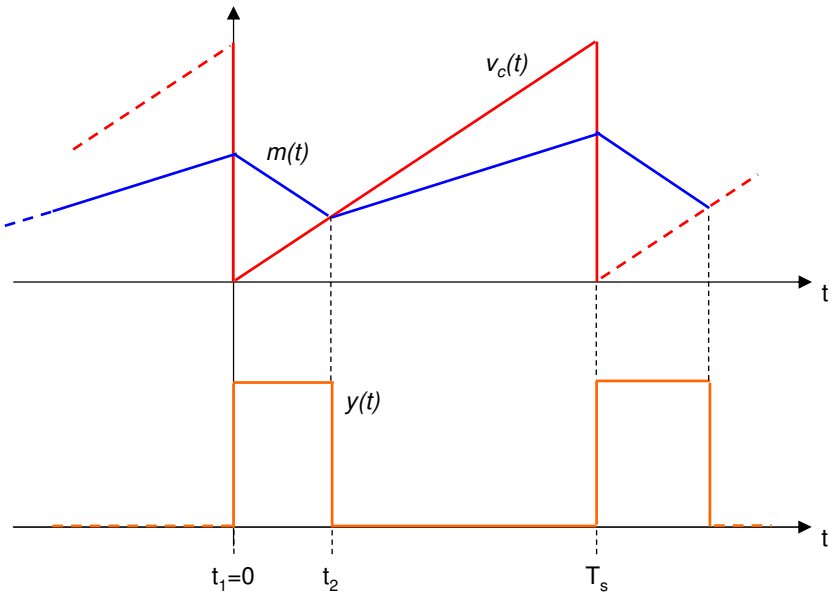

Fig. 3.1.2 – Switching dynamics of a naturally-sampled modulator

PWM modulation and a a triangular-shaped modulating signal was assumed. In a buck converter, this situation may correspond to an ESR-dominated output voltage ripple processed by a proportional or proportional-integral (PI) analog compensator; the switching ripple inherently present in the error waveform is amplified by the proportional gain of the compensator itself. This results in the modulating signal depicted in Fig. 3.1.2. It is important to point out that these hypotheses are by no means necessary and have been here assumed for the sake of definiteness.

As shown in Fig. 3.1.2, the turn-on event t_1, i.e. the leading edge of the modulator output signal, always occurs at the beginning of the switching cycle, while the turn-off instant t_2 is implicitly defined by the condition:

$$v_c(t_2) = m(t_2) \tag{3.1.1}$$

The switching event t_2 is thus determined by the value that the modulating signal assumes *at that instant*. The pulse-width modulator naturally samples the value of the modulating signal in $t=t_2$ and instantaneously updates the PWM waveform by generating the trailing edge.

Let us now consider the operation of a *uniformly sampled* pulse width modulator; its large-signal model is shown in Fig. 3.1.1.b, while Fig. 3.1.3 illustrates the modulating and carrier waveforms during a transient condition. As described in Chapter II, the input modulating signal *m(t)* is sampled once during the switching period, and its value held constant until the next sampling event. That is, the input modulating signal is processed by a *zero-order hold system* that generates the signal $m_h(t)$:

$$m_h(t) = m(t_{sampling}(k)), \qquad t_{sampling}(k) \le t < t_{sampling}(k+1) \tag{3.1.2}$$

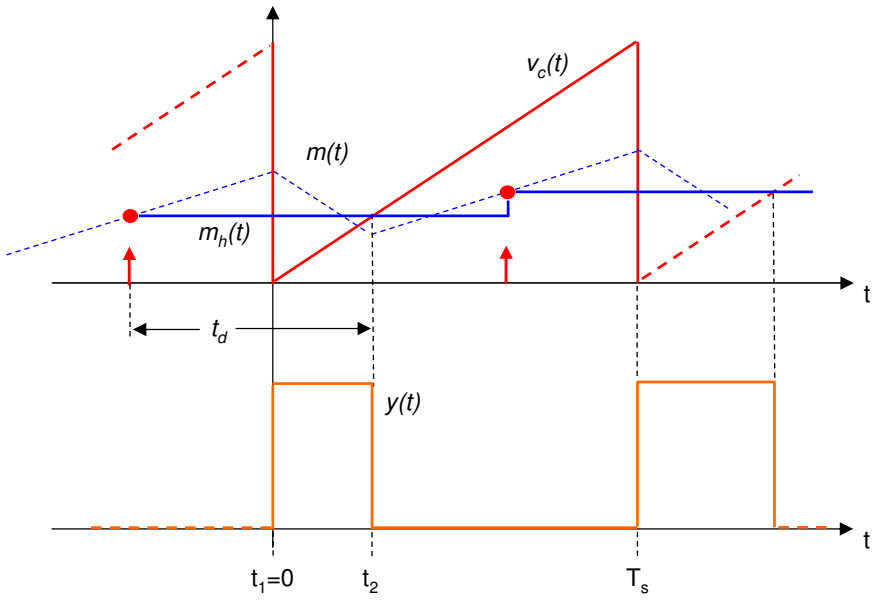

Fig. 3.1.3 – Switching dynamics of a uniformly sampled modulator

In Fig. 3.1.3 a $(1,T_s(1+D)/2)$ sampling strategy was used. As discussed in Chapter II, this allows the correct sampling of the output voltage average value in steady-state condition.

The turn-off event is now defined by the condition:

$$v_c(t_2) = m_h(t_2) \tag{3.1.3}$$

Equation (3.1.3) is deeply different from (3.1.1) in that now the turn-off event depends on the value of the modulating signal *at the sampling event*, as it is clear from the relationship existing between m and m_h and expressed by (3.1.2). The sampling action of the comparator inherently present in the PWM modulator just *re-samples* m_h and not m. The result is a *small-signal delay* t_d in the PWM action which can be quantified as the difference between the actual turn-off instant and the sampling event immediately preceding it. Small-signal wise, this delay is a function of the steady-state duty cycle D.

From a simple inspection of Fig. 3.1.3 it can be deduced that:

$$t_d = [D + \frac{1-D}{2}]T_s = \frac{1+D}{2}T_s, \tag{3.1.4}$$

a result which agrees with the one reported in Tab. 2.2.1 for the trailing edge modulation.

A phase lag can be associated to (3.1.4) as:

$$\Delta\phi(\omega) = -\omega t_d \tag{3.1.5}$$

Impact of (3.1.5) on the system phase margin can be easily evaluated. As an example, for low-voltage applications where $D<<1$ and assuming a closed-loop bandwidth of about $f_c=f_s/10$, (3.1.5) yields $\Delta\Phi \approx$-18°.

The delay (3.1.4) is intimately related to the difference between the *extrinsic* sampling event due to the adopted sampling strategy and the *intrinsic* sampling operated by the PWM comparator, which is in turn related to the converter operating point. It now appears intuitively reasonable how increasing the sampling frequency by a factor N will reduce the modulator equivalent delay by approximately the same factor. A small-signal analysis of *multi-sampled PWM modulators* will be presented in the next section that will prove this statement.

Increasing the sampling frequency brings with it a number of drawbacks that have to be carefully evaluated. *Functional* drawbacks, i.e. related to the malfunctioning of the closed-loop system due to an increased sampling frequency, have already been mentioned in the introduction and will be extesively addressed in this Chapter. Solutions aimed to their overcome will be investigated in Chapter IV. Beside these effects, one may ask if there are *technological* or *design* drawbacks that may suggest not to go oversampling the converter state variables.

Limitations of modern digital technology do not seem to represent a problem. A typical modern digital process employed for consumer applications allow for clock

frequencies that can easily reach tens of MHz. The switching frequency in pulse-width modulated power converters, on the other hand, can only be pushed up to several hundreds of kHz or few MHz, the upper limit being imposed by switching losses in the power semiconductor devices employed. A hard-wired digital compensator can thus be pushed to clock frequencies on the order of $\sim 10 f_s$ without even approaching the technological limits of a modern digital process. The same reasoning also holds for A/D converters, which can be easily designed to achieve conversion rates well above the ones dictated by a multi-sampled application.

The main objection against increasing the sampling frequency is related to the well-known design tradeoff existing in digital systems between clock frequency and power consumption. Indeed, power consumption of a digital electronic circuit based on standard CMOS technology increases about linearly with the operating clock frequency. This may pose limitations to the application of the multiple sampling strategy in low-power or micro-power applications.

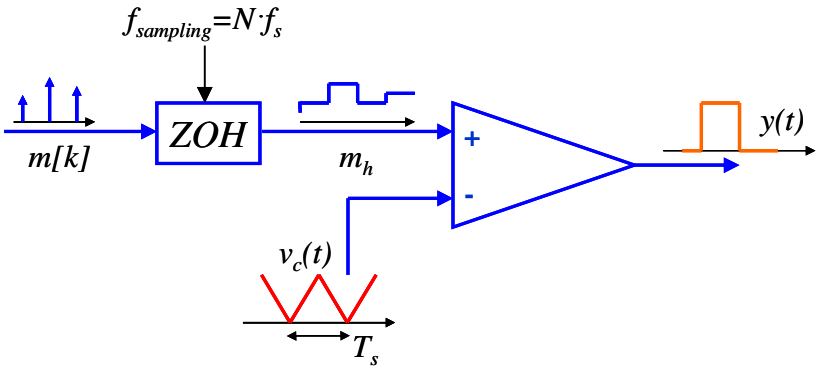

Fig. 3.2.1 – Large-signal model of a multiple sampled modulator

3.2. Multi-Sampled Pulse-Width Modulators

In a (N,Δt) multi-sampled digital control scheme the control signal *m[k]* is updated N times per switching period. A *multi-sampled modulator* (MSPWM) is thus required which latches the value of *m[k]* on a sampling-cycle basis rather than on a switching cycle basis as classical uniformly sampled modulators do.

This section presents an analysis of MSPWMs from both a small-signal and large-signal point of view. The starting point is the large-signal equivalent model illustrated in Fig. 3.2.1. This model describes the operation of the modulator independently on its

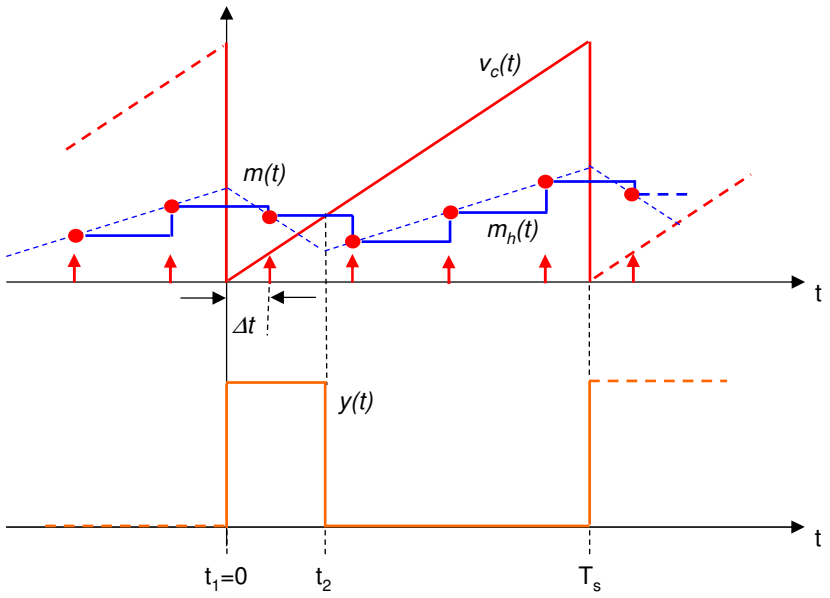

Fig. 3.2.2 – Switching dynamics of a (4,Δt) multiple-sampled pulse-width modulator

actual implementation. The modulating sequence *m[k]* is converted to the analog signal $m_h(t)$ through a zero-order hold action clocked at $f=f_{sampling}$. A comparator generates the pulse-width modulated waveform *y(t)* by comparing $m_h(t)$ with the triangular carrier signal $v_c(t)$. This operation is illustrated in Fig. 3.2.2 in the case of a trailing edge modulation.

In order to generalize the following analyses and simplify the notation, a number of hypotheses and assumptions will be made from here on:

- The time axis will be normalized to T_s. The notation t_n will be employed, defined as $t_n = t/T_s$, to denote a generic instant in time. The origin of the time axis will be aligned with the beginning of a switching period. Thus, the generic *n*-th switching period under consideration will correspond to the interval $n \le t_n \le n+1$.
- Without loss of generality, only (*N*,0) multiple sampling strategies will be considered. Extension of the results to $\Delta t>0$ is straightforward and does not present any conceptual difficulties.
- The periodic carrier signal will be written in a parameterized form; during the *n*-th switching cycle the following analytical expression will be assumed:

$$v_c(t_n;\alpha) = \begin{cases} 1-\dfrac{1}{\alpha}(t_n-n), & n < t_n < n+\alpha \\ \dfrac{1}{(1-\alpha)}(t_n-n-\alpha), & n+\alpha < t_n < n+1 \end{cases} \tag{3.2.1}$$

- The carrier amplitude is normalized to unity and parameterized so that the instants $t_{n,\alpha}=\alpha+n$ represent the points at which $v_c(t_{n,\alpha})=0$. Trailing edge, leading edge and triangular modulations are obtained from (3.2.1) by letting $\alpha=0$, $\alpha=1$ and $\alpha=0.5$ respectively.

- *Time quantization* due to the sampling process will be denoted with the following notation:

$$q_N[t_n] \equiv \frac{floor(Nt_n)}{N}, \tag{3.2.2}$$

where *floor(x)* denotes the greatest integer smaller than or equal to *x*. Operation (3.2.2) associates to each normalized instant the sampling instant immediately preceding it.

3.2.1. Small-Signal Modeling Of MSPWM. Phase Boost.

The purpose of this section is to establish the small-signal relationship existing between the modulating signal *m[k]* and the low-frequency content *d(t)* of the PWM waveform *y(t)*.

A general preliminar result, the derivation of which is straightforward, will be useful in the development of the analysis:

Theorem: Let us consider a generic modulator employing the carrier $v_c(t_n;\alpha)$ and processing the modulating signal *m[k]*. Let *y(t)* be the PWM output signal. Then *y(t)* can be written as:

$$y(t) = y_2(t) - y_1(t), \tag{3.2.3}$$

where $y_1(t)$ and $y_2(t)$ are two PWM waveforms obtained by trailing-edge modulation of *m[k]* by means of two carriers $v_{c1}(t_n;\alpha)$ and $v_{c2}(t_n;\alpha)$ respectively. The carriers $v_{c1}(t_n;\alpha)$ and $v_{c2}(t_n;\alpha)$ are defined as:

$$v_{c1}(t_n,\alpha) \equiv \begin{cases} v_c(t_n,\alpha), & n \le t_n \le n+\alpha \\ 0, & n+\alpha < t_n \le n+1 \end{cases} \tag{3.2.4.a}$$

$$v_{c2}(t_n,\alpha) \equiv \begin{cases} 0, & n \le t_n \le n+\alpha \\ v_c(t_n,\alpha), & n+\alpha < t_n \le n+1 \end{cases} \tag{3.2.4.b}$$

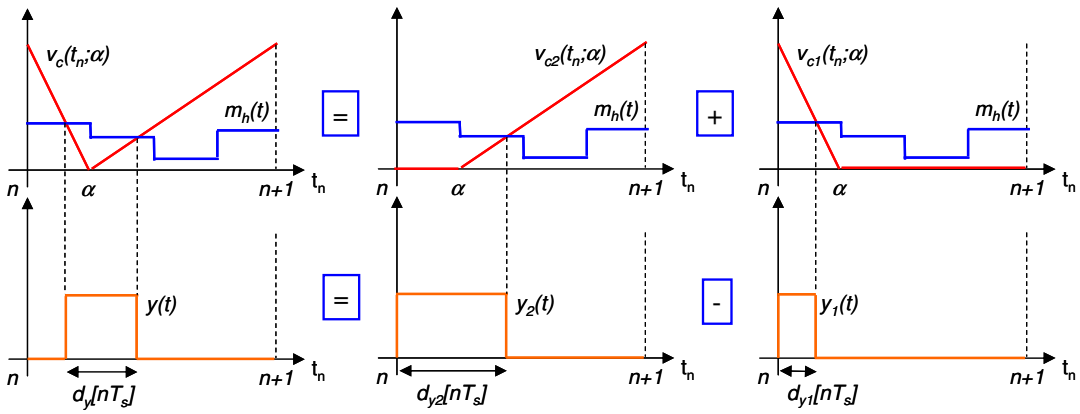

Fig. 3.2.3 – Decomposition of a generic modulation in two trailing-edge modulations

This basic result is illustrated in Fig. 3.2.3, where the generic *n*-th switching cycle is shown for a (4,0) multisampled modulator.

We shall denote with $t_{1n}[nT_s]$ and $t_{2n}[nT_s]$ the normalized turn-on and turn-off instants of $y(t)$ during the *n*-th switching cycle. These quantities are related to the duty cycles $d_{y1}[nT_s]$ and $d_{y2}[nT_s]$ of $y_1(t)$ and $y_2(t)$ during the same switching period by the following relationships:

$$t_{1n}[nT_s] = n + d_{y1}[nT_s] \tag{3.2.5.a}$$

$$t_{2n}[nT_s] = n + d_{y2}[nT_s] \tag{3.2.5.b}$$

If $d_y[nT_s]$ is the duty cycle of $y(t)$ dring the *n*-th switching cycle, the decomposition (3.2.3) implies that:

$$d_y[nT_s] = d_{y2}[nT_s] - d_{y1}[nT_s] \tag{3.2.6.a}$$

In a similar way, if $d_1(t)$, $d_2(t)$ and $d(t)$ are the low-frequency contents of $y_1(t)$, $y_2(t)$ and $y(t)$ respectively, then:

$$d(t) = d_2(t) - d_1(t) \tag{3.2.6.b}$$

i. Small-Signal Analysis

Given these preliminar results, the small-signal analysis can be carried out following these steps:

1) First, the relationships between $m[k]$ and the duty ratios $d_{y1}[nT_s]$ and $d_{y2}[nT_s]$ will be derived.
2) Second, the relationships between $d_{y1}[nT_s]$ and $d_1(t)$ and between $d_{y2}[nT_s]$ and $d_2(t)$ will be obtained.
3) Finally, the decompositions (3.2.6) will be used to derive the small-signal relationship between $m[k]$ and $d(t)$.

Let us consider the following modulating signal *m[k]*, obtained by superposition of a DC value *M* to a small-signal sinusoidal perturbation $\hat{m}[k]$:

$$m[k] = M + \hat{m}[k] = M + \Delta m \sin(\frac{\theta_0}{N} k + \varphi), \tag{3.2.7}$$

where Δm represents the perturbation amplitude, φ its initial phase and θ_0 a normalized angular frequency:

$$\theta_0 = \omega_0 T_s = 2\pi f_0 T_s \tag{3.2.8}$$

We will further assume f_0/f_s to be a rational number, thus making *m[k]* a periodic sequence. Though unnecessary to derive the main result of the following analysis, this hypothesis considerably simplifies the calculations.

In equation (3.2.7) the only time-varying term is the small-signal perturbation; thus we are implicitly making a *small-ripple approximation*, assuming no switching frequency ripple superimposed to *m[k]*. The effect of the ripple will be discussed in the next section discussing the modulator static transcharacteristics.

The analog signal $m_h(t_n)$ actually compared with the modulator carrier is obtained from (3.2.7) by means of a sample-and-hold action:

$$m_h(t_n) = M + \Delta m \sin(\theta_0 q_N[t_n] + \varphi) \tag{3.2.9}$$

The duty cycles $d_{y1}[nT_s]$ and $d_{y2}[nT_s]$ are implicitly defined by the conditions:

$$m_h(t_{1n}[nT_s]) = v_{c1}(t_{1n}[nT_s]; \alpha) \tag{3.2.10.a}$$

$$m_h(t_{2n}[nT_s]) = v_{c2}(t_{2n}[nT_s]; \alpha) \tag{3.2.10.b}$$

By substituting (3.2.9) in the left-hand side and (3.2.1) in the right-hand side of (3.2.10), and employing the relationships (3.2.5), one obtains:

$$M + \Delta m \sin(\theta_0 n + \theta_0 q_N[d_{y1}[nT_s]] + \varphi) = 1 - \frac{1}{\alpha} d_{y1}[nT_s] \qquad (3.2.11.a)$$

$$M + \Delta m \sin(\theta_0 n + \theta_0 q_N[d_{y2}[nT_s]] + \varphi) = \frac{1}{1-\alpha}(d_{y2}[nT_s] - \alpha) \qquad (3.2.11.b)$$

Further manipulation of Eqs. (3.2.11) will be carried out by making use of a small-signal approximation. More precisely, d_{y1} and d_{y2} will be written as the superposition of a DC component and a perturbation:

$$d_{y1}[nT_s] = D_1 + \Delta d_{y1}[nT_s] \qquad (3.2.12.a)$$

$$d_{y2}[nT_s] = D_2 + \Delta d_{y2}[nT_s] \qquad (3.2.12.b)$$

Then the small-signal approximation will be formulated in the following way:

$$q_N[d_{y1}[nT_s]] = q_N[D_1 + \Delta d_{y1}[nT_s]] = q_N[D_1] \qquad (3.2.13.a)$$

$$q_N[d_{y2}[nT_s]] = q_N[D_2 + \Delta d_{y2}[nT_s]] = q_N[D_2] \qquad (3.2.13.b)$$

As long as (3.2.13) are verified, (3.2.11) can be re-written in the form:

$$M + \Delta m \sin(\theta_0 n + \theta_0 q_N[D_1] + \varphi) = 1 - \frac{D_1}{\alpha} - \frac{1}{\alpha} \Delta d_{y1}[nT_s] \qquad (3.2.14.a)$$

$$M + \Delta m \sin(\theta_0 n + \theta_0 q_N[D_2] + \varphi) = \frac{D_2 - \alpha}{1-\alpha} + \frac{1}{1-\alpha} \Delta d_{y2}[nT_s] \qquad (3.2.14.b)$$

From (3.2.14) the DC terms and perturbation terms can be equated separately. As far as the DC terms are considered, a relationship is established between D_1 and D_2:

$$M = 1 - \frac{D_1}{\alpha} = \frac{D_2 - \alpha}{1-\alpha} \qquad (3.2.15)$$

On the other hand the steady state duty ratio is $D = D_2 - D_1$. Combining this condition with (3.2.15) the expected result is found:

$$D = M \qquad (3.2.16)$$

Expressions of D_1 and D_2 as a function of D are also obtained:

$$D_1 = \alpha(1-D) \tag{3.2.17.a}$$

$$D_2 = \alpha + (1-\alpha)D \tag{3.2.17.b}$$

Equations (3.2.17) state that the steady state duty cycle D determines the DC position of the turn-on and turn-off instant in a *unique* way. A generalized result, which will include the effect of the switching ripple, will be derived in Section 3.2.2.

Equating the perturbed terms in (3.2.14) and using the relations (3.2.17) yields:

$$\Delta d_{y1}[nT_s] = -\alpha\Delta m \sin(\theta_0 n + \theta_0 q_N[\alpha(1-D)] + \varphi) \tag{3.2.18.a}$$

$$\Delta d_{y2}[nT_s] = (1-\alpha)\Delta m \sin(\theta_0 n + \theta_0 q_N[\alpha + (1-\alpha)D] + \varphi) \tag{3.2.18.b}$$

Equations (3.2.18) represent the result of the first step of the calculation, as they express the perturbation of the turn-on and turn-off instant of $y(t)$ as a function of the input modulating signal amplitude and phase.

Let us denote with $M(j\omega_0)$ the Fourier component of $\hat{m}[k]$ at the perturbation frequency ω_0, and let $\Delta D_{y1}(j\omega_0)$ and $\Delta D_{y2}(j\omega_0)$ be the Fourier components of $\Delta d_{y1}[nT_s]$ and $\Delta d_{y2}[nT_s]$ at the same frequency. Equations (3.2.18) can be then summarized as follows:

$$\frac{\Delta D_{y1}(j\omega_0)}{M(j\omega_0)} = -\alpha \exp(j\omega_0 q_N[\alpha(1-D)]T_s) \tag{3.2.19.a}$$

$$\frac{\Delta D_{y2}(j\omega_0)}{M(j\omega_0)} = (1-\alpha)\exp(j\omega_0 q_N[\alpha + (1-\alpha)D]T_s) \tag{3.2.19.b}$$

The second step of the analysis consists in the derivation of the relationship between the low-frequency content of the PWM waveforms $y_1(t)$ and $y_2(t)$, i.e. the analog signals $\hat{d}_1(t)$ and $\hat{d}_2(t)$, and the discrete-time sequences $d_{y1}[nT_s]$ and $d_{y2}[nT_s]$ given by 3.2.12.

This analysis does not depend on the nature of the modulator considered – if uniformly sampled, naturally sampled or multi-sampled – but only on the particular

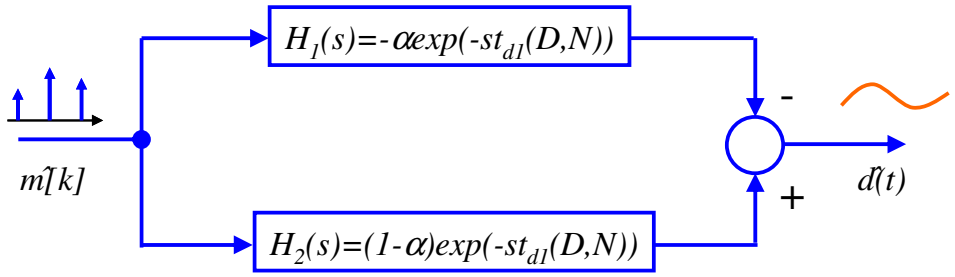

Fig. 3.2.4 – Small-signal model of a multi-sampled pulse-width modulator

modulation type. The calculation, based on a detailed Fourier analysis of the PWM waveform, has been carried out in [60] for trailing edge modulations and will not be repeated here. The main result can be summarized as follows: the Fourier components $D_1(j\omega_0)$ and $D_2(j\omega_0)$ of $\hat{d}_1(t)$ and $\hat{d}_2(t)$ at the input perturbation frequency are related to $\Delta D_{y1}(j\omega_0)$ and $\Delta D_{y2}(j\omega_0)$ by the following equations:

$$\frac{D_1(j\omega_0)}{\Delta D_{y1}(j\omega_0)} = \exp(-j\omega_0 D_1 T_s) \qquad (3.2.20.a)$$

$$\frac{D_2(j\omega_0)}{\Delta D_{y2}(j\omega_0)} = \exp(-j\omega_0 D_2 T_s)\,, \qquad (3.2.20.b)$$

with D_1 an D_2 given by (3.2.17). This result completes the second step of the small-signal analysis.

Equations (3.2.19) and (3.2.20) can be now combined to obtain the desired small-signal relationship between $\hat{m}[k]$ and $\hat{d}(t)$. The decomposition relations (3.2.6) allow us to write the transfer function $G_{PWM}(j\omega_0)$ in the form:

$$G_{PWM}(j\omega_0) \equiv \frac{D_2(j\omega_0) - D_1(j\omega_0)}{M(j\omega_0)} = H_2(j\omega_0) - H_1(j\omega_0)\,, \qquad (3.2.21)$$

with:

$$H_1(j\omega_0) = -\alpha \exp(-j\omega_0(\alpha(1-D) - q_N[\alpha(1-D)])T_s) \qquad (3.2.22.a)$$

$$H_2(j\omega_0) = (1-\alpha)\exp(-j\omega_0(\alpha+(1-\alpha)D - q_N[\alpha+(1-\alpha)D])T_s) \qquad (3.2.22.b)$$

The small-signal block diagram of a multiple sampled pulse-width modulator is shown in Fig. 3.2.4. The modulation of the turn-on and turn-off edges of the PWM signal gives rise to two distinct paths, each of them introducing a small-signal *delay time*:

$$t_{d1}(D,N) = (\alpha(1-D) - q_N[\alpha(1-D)])T_s \qquad (3.2.23.a)$$

$$t_{d2}(D,N) = (\alpha+(1-\alpha)D - q_N[\alpha+(1-\alpha)D])T_s \qquad (3.2.23.b)$$

These delay times are dependent on the converter operating point through the steady-state duty ratio D and on the multisampling factor N through the time quantization $q_N[\cdot]$.

ii. Discussion

Equations (3.2.23) formalize the intuitive reasoning developed in Section 3.1 concerning the delay time reduction operated by the increased sampling frequency. Indeed, if we let N=1 and thus consider single-sampled modulators, the terms in $q_N[\cdot]$ vanish and one obtains:

$$t_{d1}(D,N=1) = \alpha(1-D)T_s \qquad (3.2.24.a)$$

$$t_{d2}(D,N=1) = (\alpha+(1-\alpha)D)T_s \qquad (3.2.24.b)$$

It is a matter of simple mathematical manipulations to verify that plugging (3.2.24) into (3.2.22) yields, for $\alpha = 0$, 1 or 0.5, the same results summarized in Chapter II – see Table 2.1 - when uniformly sampled modulators were analyzed. These results have been extensively discussed in [60-62].

When N>1 the terms in $q_N[\cdot]$ in general do not vanish and act as to decrease the equivalent delay time of the turn-on and turn-off path. Recalling the intuitive reasoning carried out in Section 3.1, as N increases, the delay time between the *extrinsic* sampling

instant due to time quantization and the *intrinsic* sampling instant due to the downsampling action of the PWM comparator decreases. Indeed, as N approaches infinity, these two sampling instants tend to become equal and null the overall delay time. Formally:

$$\lim_{N\to+\infty} q_N[t_n] = t_n \tag{3.2.25}$$

Thus:

$$t_{d1}(D, N \to +\infty) = 0 \tag{3.2.26.a}$$

$$t_{d2}(D, N \to +\infty) = 0 \tag{3.2.26.b}$$

The multi-sampled modulator thus approaches the behavior of a naturally sampled modulator as the multisampling factor increases.

A rough estimation of the time delay reduction expressed by (3.2.23) can be derived by noting that for every t_n one has $t_n - q_N[t_n] < 1/N$. As anticipated in Section 3.1, the multiple sampling action reduces the PWM time delays by at least a factor $1/N$:

$$t_{d1,2}(D, N) \le \frac{T_s}{N} \tag{3.2.27}$$

A more insightful expression of the modulator transfer function (3.2.21) can be derived if the three basic modulation schemes are considered. For α = 0, 1 and 0.5, simple algebraic manipulation of (3.2.21) shows that:

$$G_{PWM}(s) = A(s, D, N)\exp(-st_d(D, N)), \tag{3.2.28}$$

where $A(s,D,N)$ is a real function and t_d represents the *overall delay time* of the modulator. Table 3.1 summarizes the expressions of A and t_d. As anticipated in Chapter II, A represents a constant or slowly varying function and can be always approximated with unity (please recall that a normalized carrier was considered). The overall delay time t_d of the modulator is a discontinuous function of the steady-state duty ratio D as

Tab. 3.1 - Small-signal analysis results for multiple-sampled modulators

Modulation Type	$A(j\omega,D,N)$	$t_d(D,N)$
Trailing Edge (α=0)	*1*	$(D-q_N[D])\cdot T_s$
Leading Edge (α=1)	*1*	$(1-D-q_N[1-D])\cdot T_s$
Triangular (α=0.5), *N* even	$\cos(\omega(D/2-q_N[D/2]-1/(2N))T_s)$	$T_s/(2N)$
Triangular (α=0.5), *N* odd	$\cos(\omega(D/2-q_N[D/2+1/(2N)])T_s)$	$T_s/(2N)$

long as trailing edge and leading edge modulations are considered. An exception is represented by the triangular modulation achieved for $\alpha = 0.5$, for which t_d does not depend on D and is exactly equal to $T_s/2N$. This result is not surprising, as $\alpha = 0.5$ represents a condition in which the two turn-on and turn-off edges of the PWM waveform are symmetrical with respect to $T_s/2$, and the overall dependence on D vanishes.

This observation is a first hint of a general property of the triangular modulator, i.e. that of maintaining a superior *linearity* with respect to trailing-edge or leading-edge modulators when multiple-sampling strategies are adopted. In the next Section a stronger evidence of the superior performences of multi-sampled triangular modulators will be presented.

iii. Model Validation

The small-signal model presented in this section has been validated both in simulation and experimentally. A multi-sampled modulator was simulated in the Matlab / Simulink environment and post-simulation FFT analyses were carried out on the PWM output signal *y(t)*. As an example, Fig. 3.2.5 illustrates the phase plot of a triangular modulator ($\alpha = 0.5$) operated at N=1, N=4 and N=8 times the switching frequency at a steady state operating point D=0.3. In Fig. 3.2.5 dots represent simulation results, while the continuous lines are theoretical plots derived from the analytical small-signal model previously discussed. The input perturbation frequency spanned the range $f_s/50$ to $f_s/3$. The modulator phase lag appears to be rigorously linear with respect to frequency, thus confirming the existence of the overall equivalent delay time t_d as well as its value and dependence on N. At $f = f_s/5$ the single-sampled modulator exhibits a $\Delta\varphi \approx$ -36° phase lag. Oversampling to N=4 reduces the phase lag to $\Delta\varphi \approx$ -9°, and N=8 yields $\Delta\varphi \approx$ -4.5°. It is interesting to observe how even a slight oversampling action dramatically reduces the small-signal phase lag. The phase plot for a multi-sampled trailing edge modulator operated at D=0.7 is shown in Fig. 3.2.6, from which similar

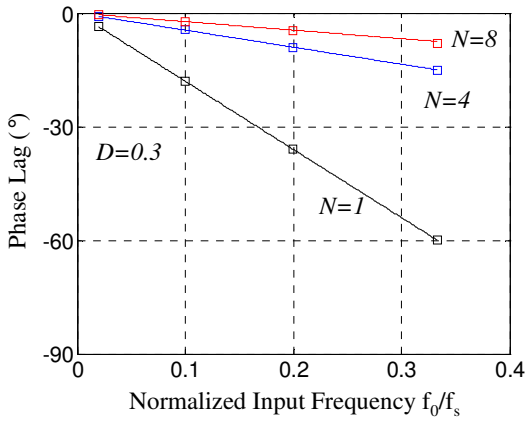

Fig. 3.2.5 – Simulated phase plot of a multi-sampled triangular modulator; D=0.3

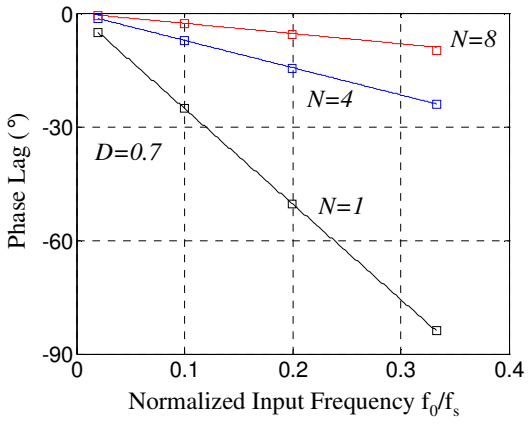

Fig. 3.2.6 – Simulated phase plot of a multi-sampled trailing edge modulator; D=0.7

considerations can be drawn.

The dependence of the equivalent delay time on the converter operating point *D* is shown in Fig. 3.2.7 for triangular and trailing edge modulators operated at *N*=4. The delay time is normalized to its maximum value T_s/N (see (3.2.27)). As anticipated, time quantization introduces discontinuities in the dependence of t_d on *D* in the trailing-edge (or leading edge) modulations. On the other hand a *constant* delay time equal to $T_s/(2N)$ is observed for the triangular modulator. Simulation results shown in Fig. 3.2.7 fully confirm the previous discussion.

In order to experimentally validate the small signal model, a digital pulse-width modulator was VHDL coded and implemented on a Xilinx Spartan3 FPGA. The implemented counter-based DPWM was clocked at 100 MHz and set for a 500 kHz switching frequency. The input signal *m[k]* was obtained by D/A conversion of the sinusoidal output of a waveform generator and superimposing an offset *M* set digitally. A free-running 25 MHz A/D converter was employed, its digital output stream downsampled to 500 kHz or 2 MHz, corresponding to a multisampling factor *N*=1 and *N*=4 respectively. A frequency analyzer was employed to obtain the amplitude/phase

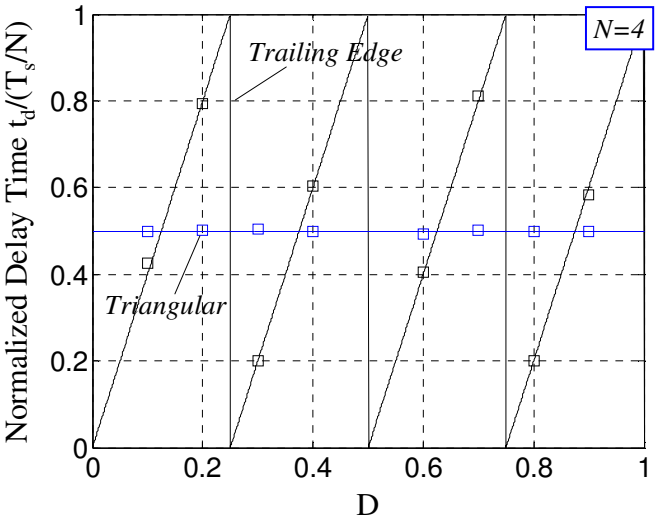

Fig. 3.2.7 – Normalized equivalent delay time vs. steady state duty ratio D.
Comparison between triangular and trailing edge modulators. N=4, f_0/f_s=1/5

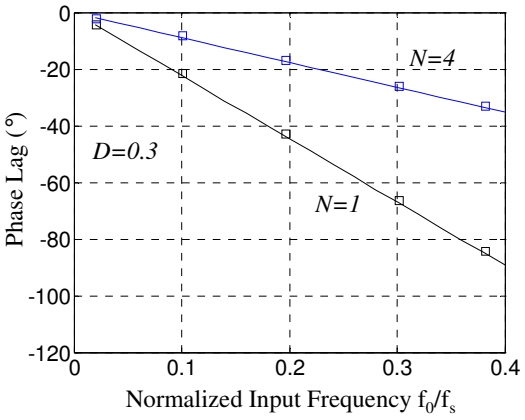

Fig. 3.2.8 – Experimental phase plot of a multi-sampled triangular modulator; D=0.3

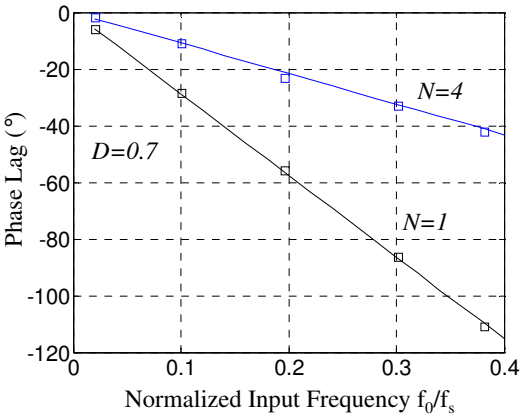

Fig. 3.2.9 – Experimental phase plot of a multi-sampled trailing edge modulator; D=0.7

relationship between the DPWM output signal and the input perturbation.

In Fig. 3.2.8 the experimental phase plot of a multi-sampled triangular modulator is shown for the two different sampling rates and for *D*=0.3. For the theoretical plot, the A/D conversion time of the employed converter was accounted by summing it to the DPWM intrinsic delay time. As shown in Fig. 3.2.8, experimental data fit the theoretical predictions. In Fig. 3.2.9 the experimental phase plot of a trailing edge modulator is shown for *D*=0.7.

Experimental results concerning the independence of the equivalent delay time on

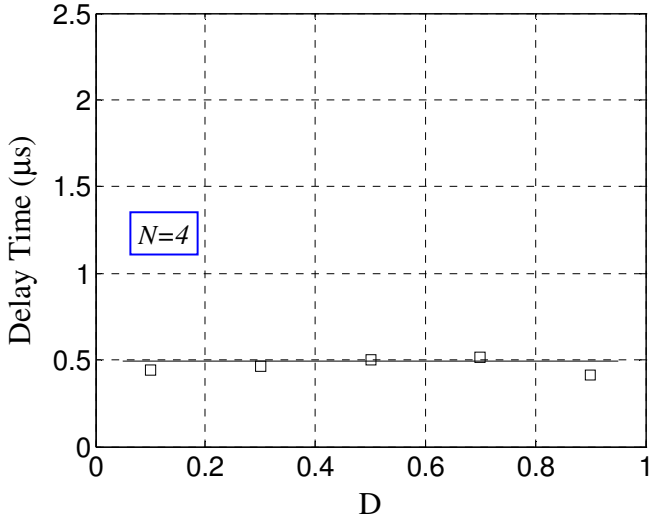

Fig. 3.2.10 – Experimental normalized equivalent delay time vs. steady state duty ratio D for a triangular modulator. N=4, f_0/f_s=1/5

the steady state duty ratio *D* for triangular modulators are shown in Fig. 3.2.10.

3.2.2. Steady-State Analysis Of MSPWM. Sampling-Induced Dead Bands

It is well known that switching frequency ripple superimposed to the modulating signal of an analog PWM modulator affects its behavior by lowering its DC and small-signal gain. In a multiple-sampled modulator this effect plays a fundamental role and deserves a detailed study. In fact, the *sampled* nature of the switching ripple can induce *zero-gain regions*. These *sampling-induced dead bands* are visible if the static modulator transcharacteristics are drawn, and define a set of operating points for which no duty cycle modulation can be achieved. Proper closed-loop operation of the system is seriously compromised if the converter is operating close to a PWM dead band, the effects spanning from poor dynamic performances to steady-state oscillating behaviors.

This section provides a systematic study of the static behavior of pulse-width modulators in presence of switching ripple superimposed to the modulating signal. An analytical approach will be first introduced in the context of naturally sampled modulators, and will be then extended to multi-sampled modulators.

i. Injection Of Switching Frequency Ripple

Switching harmonics are inherently present in the analog state variables $x_i(t)$ of the power converter under control and are therefore injected into the feedback loop as these variables are sensed and / or sampled for control purposes. Their most critical effect is to induce a periodic disturbance superimposed to the control signal *m* produced by the compensator, thus affecting the control action itself. The process by which the switching frequency ripple is injected into the feedback loop is illustrated in Fig. 3.2.11 and 3.2.12 for a naturally sampled and multiple sampled modulator respectively. These

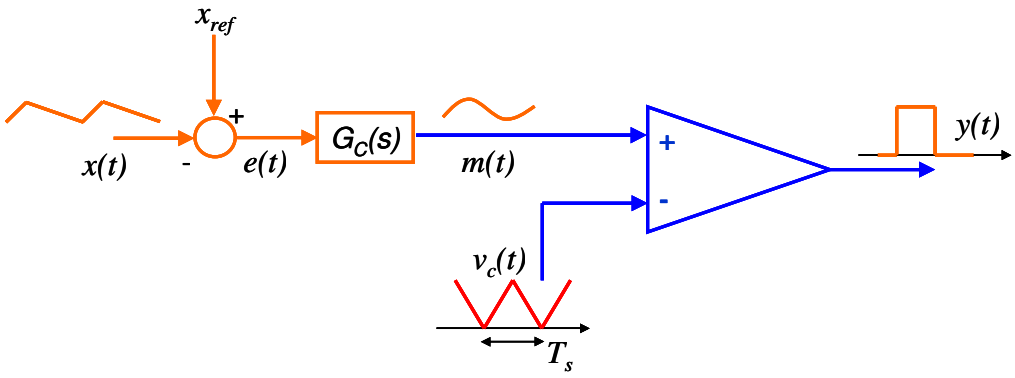

Fig. 3.2.11 – Switching frequency ripple injection process for a naturally sampled modulator

figures show the portion of the feedback loop that goes from the sensed analog state variable *x(t)* of the converter to the PWM output signal *y(t)*.

Single-sampled systems represent a special case in which the sampling process actually *removes* any switching harmonic present in the sensed variable. As the multisampling factor increases, however, frequencies multiple of f_s are sampled and processed by the digital compensator.

In this Section the *steady-state* operation of PWM modulators will be considered, meaning that the modulator is operating at a constant duty ratio *D*. Its input modulating signal is periodic over time, with period equal to T_s. Let us denote with <*m*> the DC value of the modulating signal and with m_r the ripple component containing the switching harmonics; for naturally sampled modulators we shall write:

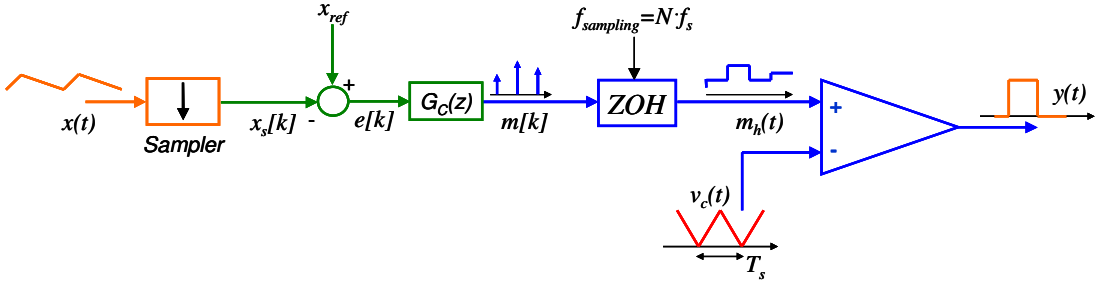

Fig. 3.2.12 – Switching frequency ripple injection process for a multiple sampled modulator

$$m(t) =< m > + m_r(t) \tag{3.2.29a}$$

while the following holds for a generic (N,Δt) multi-sampled modulator:

$$m[k] =< m > + m_r[k] \tag{3.2.29b}$$

In both cases the quantity $<m>$ is defined as the average value of m within a switching period:

$$< m >\equiv \frac{1}{T_s}\int_{t-T_s}^{t} m(\tau)d\tau \tag{3.2.30.a}$$

$$< m >\equiv \frac{1}{N}\sum_{j=k-N}^{k} m[j], \tag{3.2.30.b}$$

It is of utmost importance to realize that $<m>$ *is not equal to the steady state duty ratio D at which the modulator is operating*. For this to be rigorously true, no switching ripple has to be superimposed to m. This is coherent with the small-ripple approximation which allowed the derivation of (3.2.16).

When the modulator is operated in a closed-loop feedback control system, m_r depends on the shape of the analog ripple superimposed to the converter analog state variable(s) $x(t)$ processed by the compensator, on the adopted sampling strategy and on the frequency response of the compensator itself. All these elements are shown in Fig. 3.2.12.

Formally, a decomposition similar to (3.2.29) can be assumed for the analog sensed state variable $x(t)$:

$$x(t) =< x > + x_r(t), \tag{3.2.31}$$

Due to the periodicity of $x_r(t)$, its transform consists of a series of spectral lines:

$$X_r(f) = \sum_{m\neq 0} X_{r,m}\delta(f - mf_s), \tag{3.2.32}$$

where $X_{r,m}$ is the m-th Fourier component of $x_r(t)$.

The spectrum of the sampled state variable $x_s[k]$ is given by (3.2); taking into account (3.2.32) and retaining only the ripple spectrum $X_{s,r}(f)$ of $x_s[k]$, i.e. neglecting the DC component of $x_s[k]$, one can write:

$$X_{s,r}(f) = \sum_{m=-\infty}^{+\infty} \sum_{l=1}^{N-1} \delta(f - (l + mN) f_s) \sum_{i=-\infty}^{+\infty} X_{r,l+iN} \exp(j2\pi(l + iN) f_s \Delta t) \qquad (3.2.33)$$

$X_{s,r}(f)$ is a periodic stream of spectral lines, its period being equal to the sampling frequency Nf_s. The $N-1$ spectral lines located at $f_l = lf_s$, $1 \le l \le N-1$ are repeated all over the frequency axis to form the typical spectrum of a periodic, discrete-time signal.

Given the frequency response $G_c(f)$ of the digital compensator, the general frequency domain relationship between m_r and $x_r(t)$ is:

$$M_r(f) = \sum_{l=1}^{N-1} \delta(f - lf_s) G_c(lf_s) \sum_{i=-\infty}^{+\infty} X_{r,l+iN} \exp(j2\pi(l + iN) f_s \Delta t) \qquad (3.2.34)$$

, the expression being valid for $0 \le f \le (N-1)f_s$. A very special case is when the compensator frequency response can be considered constant at the switching frequency and its harmonics. This happens, for instance, whenever a digital PI regulator is employed. In this case $m_r[k]$ is the sampling of a scaled version of the analog ripple, and preserves its shape.

ii. Steady-State Solution Of A PWM Modulator

The problem of studying the steady-state behavior of a pulse-width modulator will be formulated as follows: given a steady state duty ratio D and having specified – in a manner that will be clearer later on - the shape of the ripple waveform m_r, the problem consists in determining the modulating signal $m(t)$ or $m[k]$ that generates D. The knowledge of m allows for the calculation of its average value $\langle m \rangle$. The couple $(D, \langle m \rangle)$ will be denoted as the steady-state operating point of the modulator under the

ripple m_r. If D is swept from 0 to 1, this process identifies the set of all possible steady-state solutions (D,<m>) of the modulator. This set represents the *modulator static transcharacteristic* under the ripple m_r.

Being a steady-state analysis, the study of all the waveforms can be limited to a single switching period. In what follows, the normalized time interval $0 \le t_n \le 1$ will be considered. Moreover we shall indicate with t_{1n} and t_{2n} the turn-on and turn-off instants of the PWM output signals. Please note that t_{1n} and t_{2n} represent *unknowns* for the problem, the only *a priori* relationship being:

$$t_{2n} = t_{1n} + D \tag{3.2.35}$$

Let us now consider a naturally sampled modulator; due to the fact that the turn-on and turn-off events are unknown, $m_r(t)$ can only be specified to within a time translation. This fact is easily understood from Fig. 3.2.11. A variation in the turn-on instant t_{1n} is equivalent to a time translation of $x(t)$. As long as the compensator is a time-invariant system, the same time translation is observed in $m(t)$. Thus, we can arbitrarily call $m_{r0}(t)$ the ripple waveform obtained when $t_{1n}=0$, and state that the ripple waveform related to a generic value of t_{1n} is:

$$m_r(t_n;t_{1n}) \equiv m_{r0}(t_n - t_{1n}) \tag{3.2.36}$$

For reasons that will become clearer in the next sections, the shape of the ripple waveform m_r will be specified through its time derivative s:

$$s(t_n;t_{1n}) \equiv \frac{\partial m_r}{\partial t_n} = s_0(t_n - t_{1n}) \tag{3.2.37}$$

The periodicity of m_r represents a constraint on $s(t_n;t_{1n})$, namely that its average value over a switching period be zero:

$$\int_0^1 s(\tau;t_{1n})d\tau = 0, \qquad 0 \le t_{1n} \le 1 \tag{3.2.38}$$

Things are somewhat different when we consider multi-sampled modulators. The main difference resides in the fact that the ripple waveshape cannot be specified to within a simple time translation. Let us examine Fig. 3.2.12. Though the analog ripple $x_r(t)$ superimposed to the sensed state variable $x(t)$ actually shifts in time as a function of t_{1n}, the corresponding sampled ripple $x_{s,r}[k]$ *modifies its shape*. This phenomenon is intimately related to the fact that a sampler is *not* a time-invariant system.

Correspondingly, the discrete-time ripple $m_r[k]$ superimposed to the modulating waveform undergoes the same phenomenon. Thus, no simple relationship similar to (3.2.36) can be assumed for discrete-time modulating waveforms. The ripple waveform will be a generic function of two variables $m_r[k;t_{1n}]$ that will depend on the particular analog ripple waveshape.

Beside this important difference, the ripple waveform at the modulator input can be nevertheless specified by its time derivative if we consider the analog signal $m_h(t)$ rather than the discrete-time signal $m[k]$. Indeed, the decomposition (3.2.29.b) translates in a similar decomposition of $m_h(t)$:

$$m_h(t_n;t_{1n}) = < m > + m_{h,r}(t_n;t_{1n}), \tag{3.2.39}$$

where $m_{h,r}(t_n;t_{1n})$ is the sampled-and-held version of $m_r[k;t_{1n}]$.

We will thus define:

$$s_h(t_n;t_{1n}) \equiv \frac{\partial m_{h,r}}{\partial t_n} \tag{3.2.40}$$

The periodic nature of $m_r[k;t_{1n}]$ again poses a constraint on its slope (3.2.40):

$$\int_0^1 s_h(\tau;t_{1n})d\tau = 0, \qquad 0 \le t_{1n} \le 1 \tag{3.2.41}$$

Summarizing, the problem of finding the possible steady-state operating points of a naturally sampled or multi-sampled PWM modulator is formulated by specifying the pair (D, $s(t_n;t_{1n})$) for naturally sampled modulator or the pair (D, $s_h(t_n;t_{1n})$) for multi-sampled modulators, and then searching for a modulating waveform $m(t_n)$ or $m_h(t_n)$ which generates D and has the specified slope.

iii. Naturally Sampled Modulators

We shall start the steady-state analysis of naturally sampled modulators with a specific, simple example, namely the case of purely triangular ripple. The analysis of this particular case will nevertheless clarify the basic concepts that will be generalized to arbitrary ripple waveforms. Moreover, the triangular ripple hypothesis is by all means justified in a number of cases of practical interest, namely every time an ESR-dominated voltage ripple, or a current ripple, are processed by a proportional-integral (PI) compensator.

Let us then specify a triangular-shaped ripple associated to a given steady-state duty ratio D:

$$s(t_n;t_{1n}) = \begin{cases} -s_{ON}, & t_{1n} \le t_n \le t_{1n} + D \\ \dfrac{D}{1-D} s_{ON}, & otherwise \end{cases}, \tag{3.2.42}$$

where $s_{ON}>0$ represents the slope (in absolute value) of the ripple during the turn-on switching phase. It can be verified that (3.2.42) satisfies the fundamental constraint (3.2.38).

The values $m(t_{1n})$ and $m(t_{2n})$ of the modulating signal at the turn-on and turn-off instants are related by:

$$m(t_{2n}) = m(t_{1n}) - s_{ON} D \tag{3.2.43}$$

On the other hand, in an analog modulator the turn-on and turn-off instants occur when the modulating signal equals the modulator carrier v_c:

$$m(t_{1n}) = v_c(t_{1n};\alpha) \tag{3.2.44.a}$$

$$m(t_{2n}) = v_c(t_{2n};\alpha) \tag{3.2.44.b}$$

Thus, taking into account (3.2.35), this fundamental steady-state condition is derived:

$$v_c(t_{1n} + D;\alpha) - v_c(t_{1n};\alpha) = -s_{ON} D \tag{3.2.45}$$

Equation (3.2.45) is easily solved employing the expression (3.2.1) of the carrier:

$$t_{1n} = \alpha[1 - D - (1-\alpha)s_{ON} D] \tag{3.2.46.a}$$

$$t_{2n} = t_{1n} + D = \alpha + (1-\alpha)(D - \alpha s_{ON} D) \tag{3.2.46.b}$$

It is useful to compare (3.2.46) with (3.2.17), obtained using a small-ripple approximation. Indeed, if s_{ON} vanishes then the previous results are obtained. On the other hand, when the switching frequency ripple cannot be neglected, corrective terms appear and modify the general steady-state solution.

From (3.2.46) the modulating signal waveform for every t_n can be easily obtained:

$$m(t_n) = v_c(t_{1n};\alpha) + \int_{t_{1n}}^{t_n} s(\tau;t_{1n})\,d\tau \tag{3.2.47}$$

The steady-state problem is now solved, as $m(t_n)$ has been determined.

Equation (3.2.45) can be interpreted in the following manner: the carrier variation over the time interval $[t_{1n}, t_{1n}+D]$ equals the variation of the modulating signal over the same interval. This basic observation can be generalized to arbitrary ripple waveforms:

$$v_c(t_{1n} + D;\alpha) - v_c(t_{1n};\alpha) = \int_{t_{1n}}^{t_{1n}+D} s(\tau;t_{1n})\,d\tau \tag{3.2.48}$$

Let us define:

$$I(t_{1n}) \equiv \int_{t_{1n}}^{t_{1n}+D} s(\tau;t_{1n})d\tau \tag{3.2.49}$$

$$f(t_{1n}) \equiv v_c(t_{1n};\alpha) - v_c(t_{1n}+D;\alpha) + I(t_{1n}) \tag{3.2.50}$$

Then, the search for solutions of (3.2.48) is equivalent to finding the zero of $f(t_{1n})$.

As far as naturally sampled modulators are considered, the problem has a straightforward solution. In fact, it can be easily shown that the integral $I(t_{1n})$ is actually independent on t_{1n}. To show this one has simply to use (3.2.37):

$$I(t_{1n}) = \int_{t_{1n}}^{t_{1n}+D} s_0(\tau - t_{1n})d\tau = \int_0^D s_0(\tau)d\tau \equiv I \tag{3.2.51}$$

Being $I(t_{1n})$ a constant, the function defined in (3.2.50) can be easily verified to have a continuous, monotonically decreasing behavior. A unique solution exists to the equation $f(t_{1n}) = 0$, expressed by:

$$t_{1n} = \alpha(1-D) + \alpha(1-\alpha)I \tag{3.2.52.a}$$

$$t_{2n} = t_{1n} + D = \alpha + (1-\alpha)D + \alpha(1-\alpha)I \tag{3.2.52.b}$$

Again, the modulating signal is found by applying (3.2.47).

Equations (3.2.52) represent the generic solution to the steady-state problem of a naturally sampled pulse-width modulator and can be employed to generate the modulator transcharacteristics under any switching ripple.

Before coming to the subject of the steady-state analysis of multi-sampled modulators, a number of examples based on (3.2.52) will be made to better appreciate their meaning. A simplifying assumption will be made considering a constant frequency response of the analog compensator at the switching frequency and its harmonics:

$$G_c(lf_s) \cong K_p, \qquad l \in \mathbf{Z}^+ \tag{3.2.53}$$

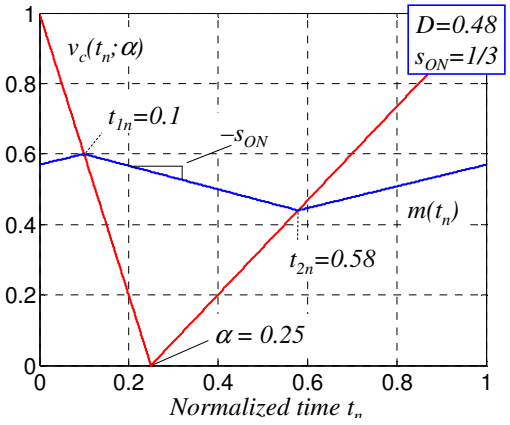

Fig. 3.2.13 – Modulation diagram of a naturally sampled modulator under triangular ripple

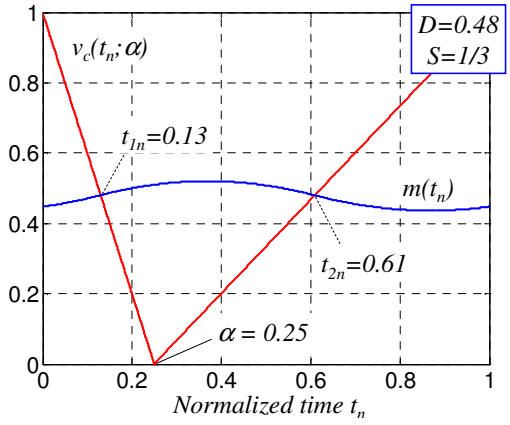

Fig. 3.2.14 – Modulation diagram of a naturally sampled modulator under parabolic ripple

As already discussed, this condition implies that the modulating ripple m_r is proportional to the sensed ripple x_r. Moreover, for the sake of definiteness we shall focus on a DC-DC buck converter application.

Two ripple waveshape will be considered, namely triangular and parabolic ripple.

Triangular ripple (3.2.42) has already been analyzed and the corresponding solution is given in (3.2.46). This kind of waveshape is typically encountered when the output capacitors of the converter present a non-negligible equivalent series resistance (ESR). The output voltage ripple waveform is thus practically proportional to the inductor current ripple, the constant of proportionality being given by the ESR. In this context the slope of the ripple at the modulation point is:

$$s_{ON} = K_p \frac{V_{in} - V_o}{f_s L} ESR \tag{3.2.54}$$

An example is shown in Fig. 3.2.13 for α = 0.25, D = 0.48 and s_{ON} = 1/3. The solution given in (3.2.46) yields t_{1n}=0.1 and t_{2n}=0.58, producing the illustrated modulating waveform $m(t_n)$.

Next, a parabolic ripple case is shown in Fig. 3.2.14. Parabolic ripple is typically originated from the integration of a triangular waveshape, a common example being the output voltage ripple of a buck converter when ceramic output capacitors are employed.

The following expression can be given for *s*:

$$s(t_n;t_{1n})=\begin{cases} S+\dfrac{2S}{1-D}(t_n-t_{1n}), & 0\le t_n\le t_{1n} \\ S-\dfrac{2S}{D}(t_n-t_{1n}), & t_{1n}\le t_n\le t_{1n}+D \\ -S+\dfrac{2S}{1-D}(t_n-t_{1n}-D), & t_{1n}+D\le t_n\le 1 \end{cases} \tag{3.2.55}$$

The parameter *S* defines the maximum and minimum slope of the ripple and is related to the peak-to-peak ripple Δm itself, being $\Delta m = S/4$. If a buck converter with output ceramic capacitance is considered, the following expression for S can be easily derived:

$$S=K_p\frac{V_{in}-V_o}{2f_s^2LC}D \tag{3.2.56}$$

It is straightforward to verify from (3.2.55) that $I = 0$, thus the turn-on and turn-off instants coincide with the no-ripple solution.

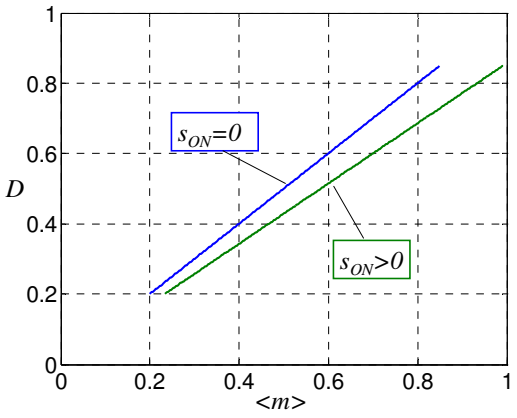

Fig. 3.2.15 – Static transcharacteristic of a trailing edge naturally sampled modulator under triangular ripple

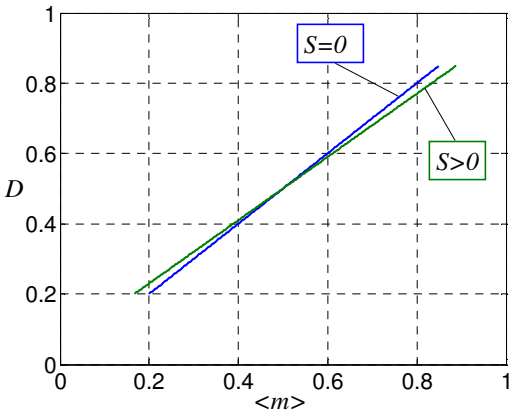

Fig. 3.2.16 – Static transcharacteristic of a trailing edge naturally sampled modulator under parabolic ripple

The static transcharacteristics of a trailing edge modulator under triangular and parabolic ripple are shown in Fig. 3.2.15 and 3.2.16. In each case the solution obtained in presence of the ripple is compared with the no-ripple transcharacteristic (3.2.16). The well known reduction of the modulator gain in presence of switching frequency ripple is clearly visible.

Figures 3.2.15 and 3.2.16 have been plotted using a constant value for the parameters s_{ON} and S. However, (3.2.54) and (3.2.56) point out a general dependence of these parameters on the steady state duty ratio. This *ripple modulation* effect could be easily accounted for by introducing in the slope $s(t_n;t_{1n})$ the proper dependence on D. This approach will be followed in Section 3.3, when discussing the closed-loop behavior of multiple-sampled modulators.

iv. Multiple-Sampled Modulators

The approach for deriving the steady-state transcharacteristics of a multi-sampled modulator will follow the general method presented in the previous Subsection for naturally sampled PWMs. There are, however, important differences that must be clearly discussed.

Let us write the equation that relates the variation of the modulating signal $m_h(t)$ from the turn-on instant t_{1n} to the turn-off instant t_{2n}:

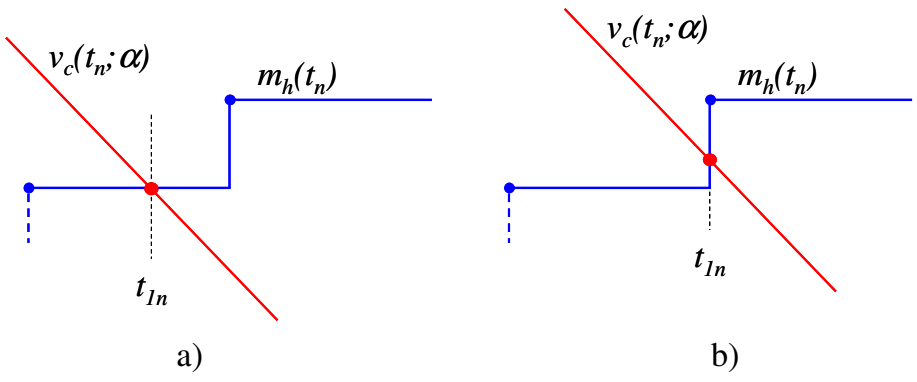

Fig. 3.2.17 – Turn-on crossing configurations in a multiple sampled modulator; horizontal crossing (a) and vertical crossing (b)

$$m_h(t_{1n}+D) = m_h(t_{1n}) + \int_{t_{1n}}^{t_{1n}+D} s_h(\tau;t_{1n})d\tau \tag{3.2.57}$$

This equation always holds provided that the derivative s_h of the staircase-like signal m_h is intended in a generalized sense. This means that s_h consists of a stream of Dirac pulses centered at the sampling instants, i.e. where m_h is discontinuous.

When discussing naturally sampled modulators, equation (3.2.57) was the starting point of the analysis, the second step being using relationships (3.2.44) to obtain the steady-state equation (3.2.48). No such substitution can be performed if multiple sampled modulators are considered. The reason is that the modulating signal and the carrier signal have, in general, different values in t_{1n} and t_{2n}. Examples are shown in Fig. 3.2.17 concerning the turn-on instant: whenever m_h crosses v_c horizontally, then $m_h(t_{1n})=v_c(t_{1n})$. On the other hand, when a vertical crossing occurs we have $m_h(t_{1n})>v_c(t_{1n})$. A similar reasoning can be applied to the turn-off instant $t_{2n}=t_{1n}+D$. The condition $m_h(t_{2n})=v_c(t_{2n})$ is fulfilled if and only if a horizontal crossing occurs in t_{2n}; a vertical crossing yields $m_h(t_{2n})<v_c(t_{2n})$.

Having made these observations, let us define:

$$f_h(t_{1n}) \equiv v_c(t_{1n}) - v_c(t_{1n}+D) + I_h(t_{1n}) \tag{3.2.58.a}$$

$$I_h(t_{1n}) \equiv \int_{t_{1n}}^{t_{1n}+D} s_h(\tau;t_{1n})d\tau \tag{3.2.58.b}$$

Equation (3.2.58.a) defines f_h in a similar way to what already did for naturally sampled modulator, i.e. as the difference between the carrier variation during the interval $[t_{1n},t_{1n}+D]$ and the corresponding variation of m_h, expressed by the quantity I_h. The potential presence of vertical crossings in the modulation diagram means that for a given duty ratio D, the searched solution t_{1n} does not necessarily null f_h. However, f_h can be nevertheless employed to solve the problem as t_{1n} represents the point at which f_h

changes its sign. Thus *the search for the zero crossing of f_h yields the steady-state position of the turn-on instant t_{1n}*.

Let us summarize the main properties of f_h and I_h, leaving the formal proofs in Appendix B:

- The integral $I_h(t_{1n})$ is a function of t_{1n}. The reason is that $s_h(t_n;t_{1n})$ does not depend on t_{1n} by means of a simple time translation, as observed in Subsection ii. I_h has a regular (continuous) behavior everywhere except when $t_{1n}=q_N[t_{1n}]$ or $t_{1n}+D=q_N[t_{1n}+D]$, i.e. when t_{1n} or $t_{1n}+D$ coincide with sampling instants; these points represent negative-slope discontinuities for I_h.
- The function $f_h(t_{1n})$ is monotonically decreasing with a regular behavior except where I_h is discontinuous. f_h inherits the negative discontinuities of I_h.
- If there exist a t_{1n}^* such that $f_h(t_{1n}^*) = 0$, then t_{1n}^* and t_{1n}^*+D are the turn-on and turn-off instants of the searched solution. Both the intersection are horizontal.
- If f_h changes its sign with a discontinuity, i.e. if $f_h(t_{1n}^*-\delta) > 0$ and $f_h(t_{1n}^*+\delta) < 0$, then t_{1n}^* and t_{1n}^*+D are the turn-on and turn-off instants of the searched solution. At least one vertical crossing will be found in the modulation diagram.

The problem formulated by (3.2.58) cannot in general be solved analytically, mostly due to the discontinuities present in the functions involved. It is nevertheless possible to find the solution by means of numerical integration. Whatever method is used to solve (3.2.58) for a given value of D, it will give a unique solution (t_{1n}, $t_{1n}+D$) for the turn-on and turn-off instants. The modulating signal $m_h(t_n)$ is then constructed once its value at t_{1n} or at $t_{1n}+D$ is known. For instance, if t_{1n} does not coincide with a sampling instant, then $m_h(t_{1n})=v_c(t_{1n})$ and:

$$m_h(t_n) = v_c(t_{1n};\alpha) + \int_{t_{1n}}^{t_n} s_h(\tau;t_{1n})d\tau \tag{3.2.59.a}$$

Similarly, if $t_{1n}+D \neq q_N[t_{1n}+D]$:

$$m_h(t_n) = v_c(t_{1n}+D;\alpha) + \int_{t_{1n}+D}^{t_n} s_h(\tau;t_{1n})d\tau \tag{3.2.59.b}$$

However, if *both* t_{1n} and $t_{1n}+D$ coincide with sampling instants, the modulating signal is defined to within an additive constant δm, yielding multiple solutions to the problem:

$$m_h(t_n) = v_c(t_{1n};\alpha) + \int_{t_{1n}}^{t_n} s_h(\tau;t_{1n})d\tau + \delta m\,, \tag{3.2.59.c}$$

the only constraint on δm being that the given duty ratio D is preserved by the vertical translation.

These solutions (3.2.59.c) share the same duty ratio D and correspond to different values of $<m>$. They form a *dead band* in the modulator transcharacteristic, i.e. a region in which the MSPWM loses its modulating capabilities. The dead band extension is defined by the upper and lower bounds of δm in (3.2.59.c).

Similarly to what done concerning the naturally sampled modulators, few examples will be given now of modulation diagrams and static transcharacteristics of a multiple sampled PWM. Hypothesis (3.2.53) will be assumed to remain valid for the high-frequency response of the digital compensator:

$$G_c(lf_s) \cong K_p\,, \qquad 1 \le l \le N-1 \tag{3.2.60}$$

This assumption implies that the shape of the discrete time ripple sequence $m_r[k]$ is essentially proportional to the ripple $x_r(t_n)$ superimposed to the sensed analog state variable. Having defined an "analog" modulating waveform in this manner:

$$m_a(t_n) =< m_a > + m_{a,r}(t_n) \equiv < m_a > - K_p x_r(t_n)\,, \tag{3.2.61}$$

the following relationship holds:

$$m_h(t_n) \equiv m_a(q_N[t_n]) =< m_a > + m_{a,r}(q_N[t_n]) \tag{3.2.62}$$

Under these assumptions it is particularly easy to derive the ripple derivative s_h of m_h (see 3.2.40) from the corresponding derivative s of $m_{a,r}$:

$$s_h(t_n;t_{1n}) = \delta(t_n - q_N[t_n]) \int_{t_n - 1/N}^{t_n} s(\tau;t_{1n}) d\tau\,, \tag{3.2.63}$$

and the important quantity $I_h(t_{1n})$ finds this alternative useful expression:

$$I_h(t_{1n}) = \int_{q_N[t_{1n}]}^{q_N[t_{1n}+D]} s(\tau;t_{1n}) d\tau \tag{3.2.64}$$

As an example, let us apply (3.2.64) to derive the expression of $I_h(t_{1n})$ when the "analog" ripple $m_{a,r}(t)$ is supposed to have a triangular shape. Integration of (3.2.42) as expressed by (3.2.64) yields:

$$I_h(t_{1n}) = \frac{D}{1-D} s_{ON}(t_{1n} - q_N[t_{1n}]) - s_{ON}(q_N[t_{1n}+D] - t_{1n}) \tag{3.2.65}$$

As anticipated in the general discussion, $I_h(t_{1n})$ is a function of t_{1n} and presents negative discontinuities when t_{1n} or $t_{1n}+D$ coincide with sampling instants. The presence of the discontinuities is deduced from the time quantization $q_N[\cdot]$.

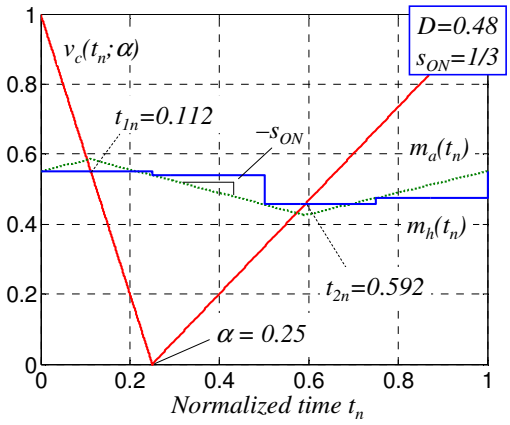

Fig. 3.2.18 – Modulation diagram of a 4-sampled modulator under triangular ripple

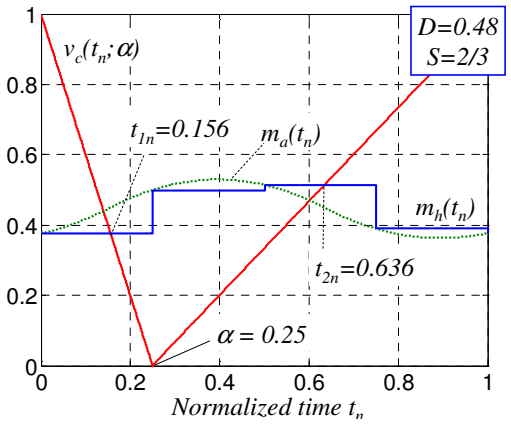

Fig. 3.2.19 – Modulation diagram of a 4-sampled modulator under parabolic ripple

In Fig. 3.2.18 an example of modulation diagram of a multiple sampled modulator (N=4, α=0.25) is shown in the case of triangular ripple. The numerical solution of (3.2.58.a) was carried out using (3.2.65) as expression for I_h and employing the Matlab environment. The "analog" signal $m_a(t)$ is also shown in Fig. 3.2.18 to better visualize the triangular-shaped ripple. Figure 3.2.19 illustrates an example where parabolic ripple was assumed. Relationship (3.2.64) was employed to derive an expression for I_h – not reported here – from (3.2.55).

Let us now consider the static transcharacteristic of a 4-sampled trailing edge modulator shown in Fig. 3.2.20. The ideal transcharacteristic, obtained assuming no switching ripple superimposed to m, is compared with the curve obtained assuming a triangular ripple waveshape (s_{ON} = 1/3). Three large dead bands are visible in the latter curve at D = 0.25, 0.5 and 0.75. The sampled switching ripple superimposed to $m[k]$ causes the modulator transcharacteristic to largely depart from the ideal one. Each of the three dead bands visible in Fig. 3.2.20 correspond to a vertical crossing between the carrier and the modulating signal. In the trailing edge modulator, where α = 0 and therefore the turn-on event t_{1n} is always unmodulated, the vertical crossing occurs at the turn-off instant.

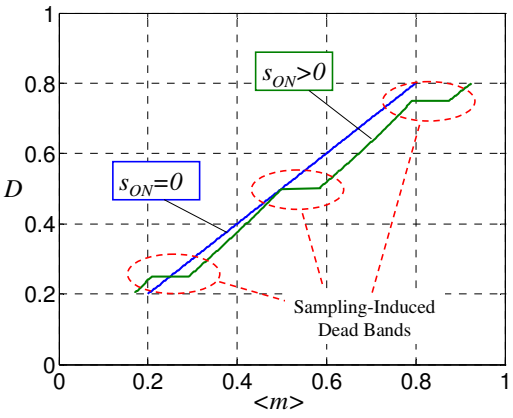

Fig. 3.2.20 – Static transcharacteristic of a 4-sampled trailing edge modulator under triangular ripple

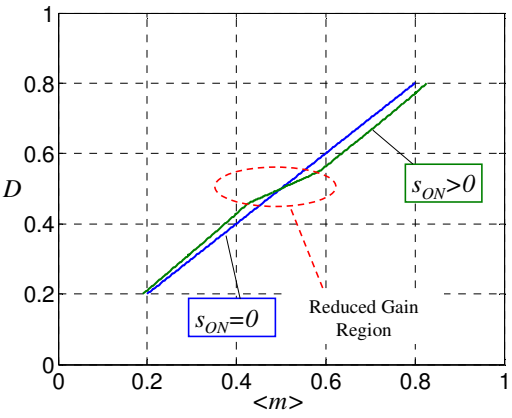

Fig. 3.2.21 – Static transcharacteristic of a 4-sampled triangular modulator under triangular ripple

It is interesting to compare the transcharacteristic shown in Fig. 3.2.20 to the one illustrated in Fig. 3.2.21, where a triangular modulator was employed while keeping fixed the other boundary conditions (N=4, s_{ON}=1/3). No dead bands are found in the plot, meaning that no steady-state operating points are found where *both* the rising and falling edges are originated from vertical intersections. Instead, a *reduced gain region* is observed around D = 0.5. Reduced gain regions are common in the static transcharacteristics of multiple sampled modulators, and correspond to situations where *only one* vertical crossing occurs, hence the reduction in the modulator gain.

The absence of dead bands is not a general property of triangular modulators; however, triangular modulators exhibit an overall superiority with respect to leading edge and trailing edge modulators in terms of linearity. On this purpose, let us denote with $D_N(<m>)$ the static transcharacteristic of a N-sampled modulator under the ripple $m_{a,r}(t)$ and with $D_\infty(<m>)$ the static transcharacteristic of a naturally sampled modulator under the same ripple. The nonlinearity NL of D_N with respect to D_∞ can be defined in this way:

$$NL \equiv \left\| D_N - D_\infty \right\|_2 = \left(\int_0^1 \left| D_N(<m>) - D_\infty(<m>) \right|^2 d<m> \right)^{1/2} \qquad (3.2.66)$$

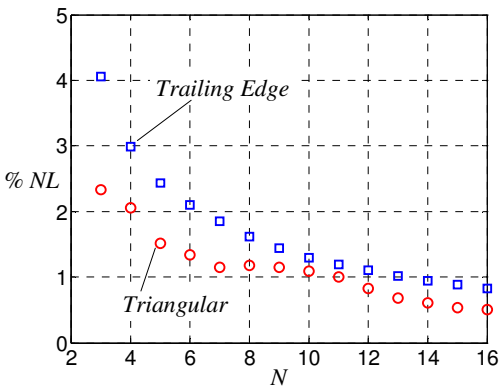

Fig. 3.2.22 – Nonlinearities of a trailing edge and a triangular modulator under triangular ripple

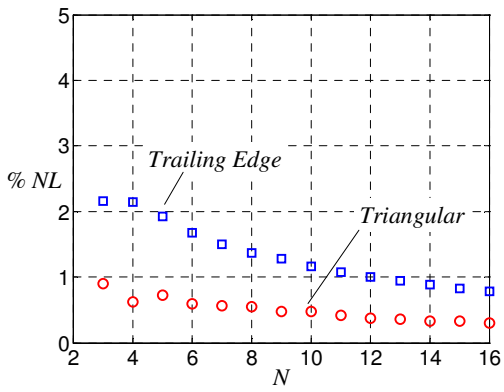

Fig. 3.2.23 – Nonlinearities of a trailing edge and a triangular modulator under parabolic ripple

Definitions differerent from (3.2.66) can be adopted, yielding slightly different results without altering the following general conclusions. In Fig. 3.2.22 the nonlinearity functions of a trailing edge and a triangular modulators under triangular ripple are compared for increasing values of the multiple sampling factor *N*. The triangular modulator is seen to exhibit a drastically lower nonlinearity even at small values of *N*. A comparison carried out using parabolic ripple is shown in Fig. 3.2.23, from which similar conclusions can be drawn concerning the superior linearity of the triangular modulation. Further evidence will be given in the next Section, where the closed-loop operation of multiple sampled modulators will be addressed.

3.3. Closed-Loop Operation Of Multi-Sampled Modulators

In the previous Sections the small-signal and steady-state analysis of multi-sampled modulators mainly addressed their open loop operation. The sensing and sampling processes of the converter state variables were mentioned to explain the ripple injection mechanism and therefore justify the presence of switching frequency harmonics in the spectrum of modulating signal. We wish now to make a step further and consider the operation of a multi-sampled modulator within the feedback control loop.

3.3.1. Multi-Sampled Voltage Mode Control

A case study is presented in this Section to show how the multiple sampling technique can lead to significantly improved performances in the closed-loop dynamics. Let us consider a 12V-to-2V step down buck converter intended for high current applications. Let f_s = 500 kHz be the switching frequency, C = 1.5mF be the output filter capacitance, ESR = 1.2mΩ its equivalent series resistance and L = 400nH the phase inductance. Stability margin specifications require a minimum phase margin $m_{\Phi,min} = 45°$ and a minimum gain margin $GM >$ 10dB. A single-sampled control will be

compared with a 4-sampled solution in terms of achievable closed-loop bandwidth f_c. In order to simplify the discussion, no quantization phenomena will be considered in this Section.

A triangular modulation will be employed for both the solutions. To achieve correct sampling of the output voltage average value, a (1,0) sampling strategy will be employed (see Section 2.1.3) for the single-sampled solution.

The small-signal model of the power converter is given by its control-to-output transfer function $G_{vd}(s)$:

$$G_{vd}(s) = V_{in} \frac{1 + sESR \cdot C}{1 + sESR \cdot C + s^2 LC}, \tag{3.3.1}$$

while the small-signal model of the pulse-width modulator will be approximated as:

$$G_{PWM}(s) \cong \exp(-st_d) \tag{3.3.2}$$

This approximation is by all means justified, as the amplitude variation of G_{PWM} with frequency has been shown to be negligible. The time delay t_d is equal to $T_s/2$ = 1µs

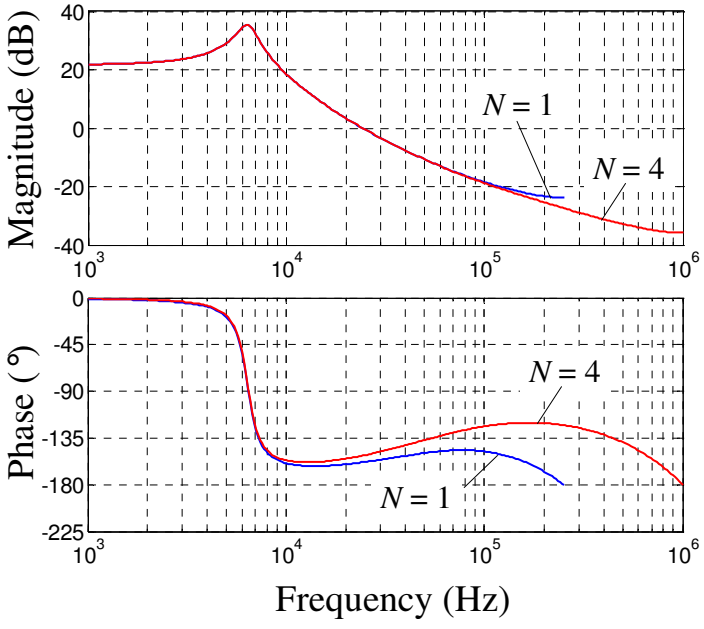

Fig. 3.3.1 – Uncompensated loop gain Bode diagrams of the single-sampled and multi-sampled converter

for the single-sampled system and to $T_s/8$ = 250ns in the multiple sampled system. With these information, the small-signal z-domain equivalent model of the power converter can be obtained for the single and multiple sampled loops:

$$G_{p,SS}(z) = T_s Z_{T_s}[G_{vd}(s)\exp(-s\frac{T_s}{2})] \tag{3.3.3.a}$$

$$G_{p,MS}(z) = \frac{T_s}{N} Z_{\frac{T_s}{N}}[G_{vd}(s)\exp(-s\frac{T_s}{2N})] \tag{3.3.3.b}$$

These transfer functions are to be considered as *uncompensated loop gains*. Their Bode diagrams are compared in Fig. 3.3.1, where the phase boost effect due to the multi-sampling approach is clearly seen.

In particular, the phase lag of the 4-sampled power converter is seen to be above -135° at $f_s/5$ = 100kHz. This suggests that a simple Proportional-Integral compensator can be designed to achieve $f_c=f_s/5$, the proportional term setting the desired bandwidth and the PI zero boosting the loop gain magnitude at low frequency, its upper limit being set by the phase margin and gain margin constraints. Given these considerations, a PI

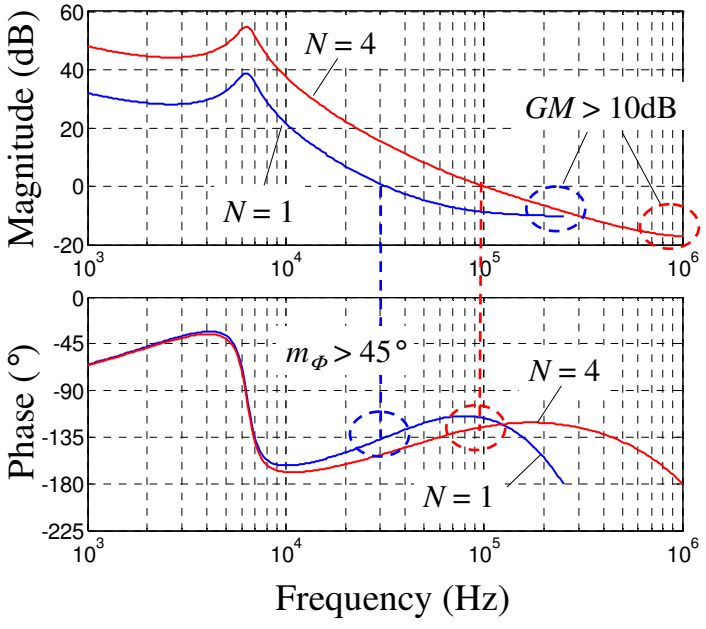

Fig. 3.3.2 – Compensated loop gain Bode diagrams for the single-sampled and multi-sampled solution

regulator was designed to achieve $f_c = f_s/5$, $m_\Phi = 55°$, $GM = 17$dB.

On the other hand, no PI compensator can be designed for the single-sampled system. The phase lag compensation requires a derivative action, leading to a PID structure. Closed-loop bandwidth can now be pushed as long as the high-frequency gain boost of the derivative action does not cause the gain margin to fall out of specification. The designed PID achieves $f_c = f_s/16$, $m_\Phi = 45°$, $GM = 10$dB.

The Bode diagrams of the compensated loop gains T_{SS} and T_{MS} are shown in Fig. 3.3.2. From these designs, the multi-sampled system will exhibit a faster and more damped transient response with respect to its single-sampled counterpart.

Systeml-level simulations were carried out using the Simulink/Matlab environment to investigate the dynamic performances of the two designs. The output voltage $v_{out}(t)$ and inductor current $i_L(t)$ during a 0A-20A load step are shown in Fig. 3.3.3 and 3.3.4 respectively. Each figure compares the single sampling solution to the multiple sampled one, confirming the previous discussion.

As previously mentioned, quantization effects will practically limit the achievable bandwidth mainly because of the onset of limit cycle oscillations. Though simplified, this example nevertheless shows how a slight increase in the sampling frequency could bring significant improvement in the dynamic performances of the closed loop system.

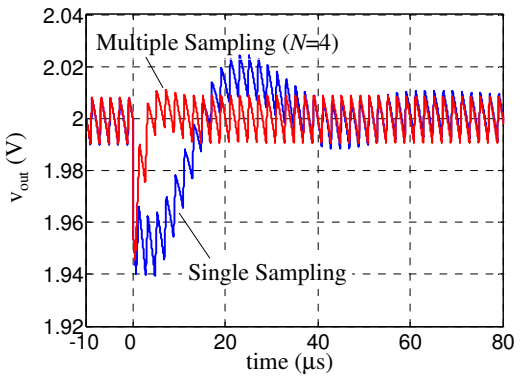

Fig. 3.3.3 – Output voltage transient during a 0A→20A load step up transient

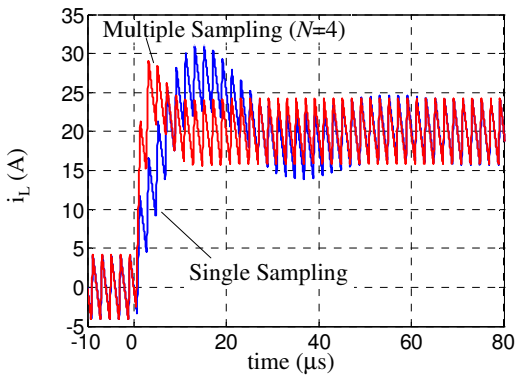

Fig. 3.3.4 – Output voltage transient during a 0A→20A load step up transient

Interestingly, the structure of the multi-sampled compensator could be greatly simplified because of the intrinsic phase boost of the multi-sampled process.

3.3.2. Sampling Induced Dead Bands

Presence of the sampling induced dead bands in the modulator trascharacteristics was discussed in Section 3.2.2. From a steady-state point of view, a dead band identifies a precise value of the duty ratio D that cannot be maintained with stability over time by a closed-loop configuration, as its loop gain would be *exactly* zero over a finite range of modulating signals. Dynamically, zero gain regions affect the control action, giving rise to poor transient performances or even oscillatory behaviors. This Section is devoted to analyze the dead bands phenomenon in the context of the closed-loop operation of the converter by means of simulation and experimental investigations.

i. Closed Loop Transcharacteristics

The static transcaracteristic of a multi-sampled modulator operating in a closed-loop configuration can be obtained using the model presented in Section 3.2.2. However, the switching frequency ripple is now a function of the steady-state duty ratio D and this dependence has to be taken into account. The *ripple modulation effect* is a typical closed-loop phenomenon and affects the shape of the transcharacteristic and the extension of its dead bands.

Let us consider a buck converter operating with high-ESR output capacitors. As anticipated by (3.2.51), the slope of the output voltage ripple is given by:

$$s_{ON} = K_p \frac{V_{in} - V_o}{f_s L} ESR \tag{3.3.4}$$

Since $V_o = DV_{in}$, the dependence of s_{ON} on D can be explicited:

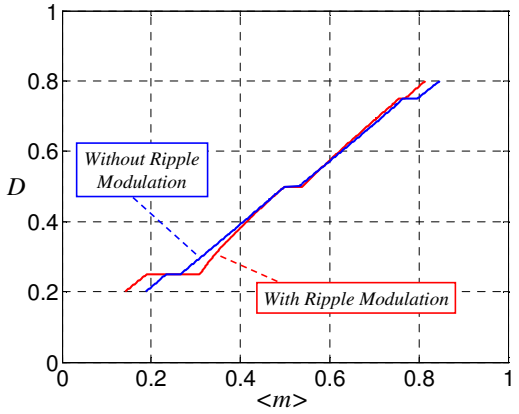

Fig. 3.3.5 – Ripple modulation effect on the static transcharacteristic of a 4-sampled trailing edge modulator under triangular ripple

$$s_{ON}(D) = K_p V_o \frac{ESR}{f_s L} \frac{1-D}{D} \tag{3.3.5}$$

Adding equation (3.3.5) to the model presented in Section 3.2.2 allows the closed-loop static transcharacteristic to be plotted. Figure 3.3.5 exemplifies the effect of the ripple modulation (3.3.5) over a 4-sampled modulator. A "*(1-D)/D*" modulated characteristic is compared with a constant-s_{ON} characteristic. The constant s_{ON} value was chosen to be equal to the variable s_{ON} at a specific duty ratio D_0=*0.56*. The effect of the ripple modulation is particularly evident in the lowest dead band, which appears to be greatly enlarged by the *(1-D)/D* dependence. Indeed, when *D* is low the ripple slope

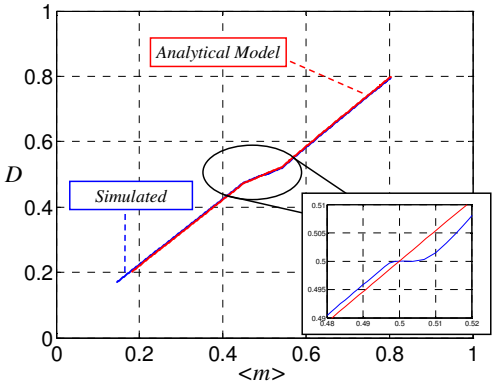

Fig. 3.3.6 – Simulated and analytical PWM transcharacteristic of a 4-sampled triangular modulator

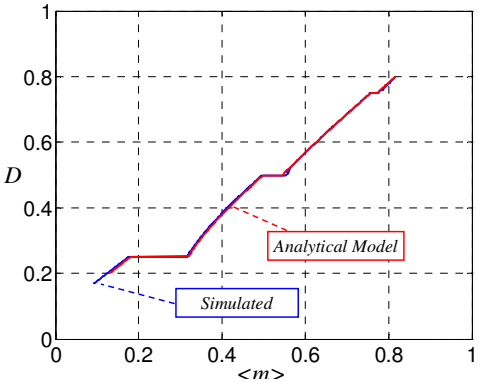

Fig. 3.3.7 – Simulated and analytical PWM transcharacteristic of a 4-sampled trailing edge modulator

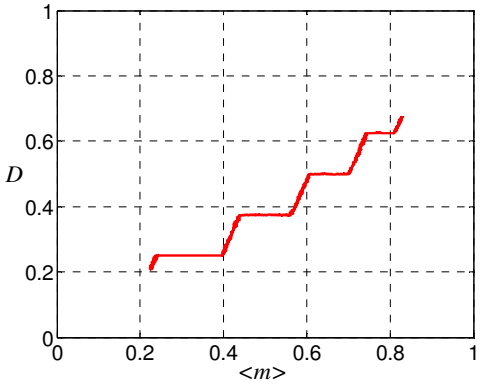

Fig. 3.3.8 – Experimental PWM transcharacteristic of a 8-sampled trailing edge modulator

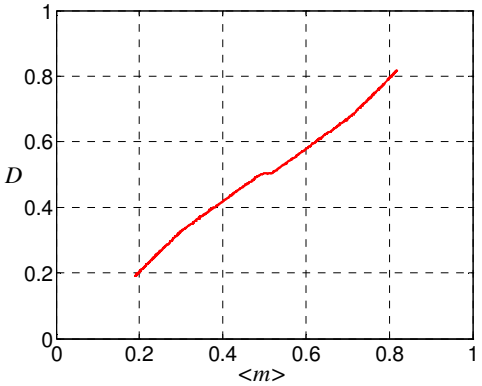

Fig. 3.3.9 – Experimental PWM transcharacteristic of a 8-sampled triangular modulator

(3.3.5) tends to be large, thus leading to higher peak-to-peak ripple. This in turn corresponds to a larger interval of $<m>$ for which the double vertical crossing occurs.

ii. Simulation and Experimental Tests

System-level simulations have been carried out using the Simulink/Matlab environment to compare the analytically-derived closed-loop transcharacteristics to the simulated ones. On this purpose, the 4-sampled system discussed in Section 3.3.1 was operated in a quasi-steady state condition, where the power converter input voltage V_{in} was slowly swept from 12V to 2.5V, thus forcing the duty cycle to sweep between 17% and 80%. In the meanwhile, the cycle-by-cycle duty ratio applied to the converter was evaluated together with the running average $<m>$ of the modulating signal produced by the modulator, calculated as in (3.2.27.b). These two waveforms were then used to construct the simulated PWM transcharacteristic.

The analytical transcharacteristic was generated assuming a purely triangular ripple and employing (3.3.5). The triangular ripple assumption appears to be justified because of the PI nature of the compensator and because of the relatively high ESR of the output filter capacitors of the converter.

The analytical and simulated transcharacteristic are compared in Fig. 3.3.6, where perfect matching can be observed. A similar analysis was carried out changing the

modulator to a trailing edge PWM, leaving unaltered the other parameters. The comparison is shown in Fig. 3.3.7, again confirming the accuracy of the steady-state model presented in Section 3.2.2.

It is worth to notice the presence of a dead band at $D = 0.5$ in the simulated transcharacteristic shown in Fig. 3.3.6, visible in the inset. The dead band is not present in the analytically derived curve. The reason is that the analytic curve has been generated assuming a perfectly triangular shape of the output voltage ripple, while in the simulation a capacitive component is always present. This slight difference in the ripple waveform gives rise to a dead band of small amplitude, surrounded by low gain regions.

Experimental evidence of the sampling induced dead bands was obtained employing a method by all means similar to the one previously described and employed to simulate the modulator transcharacteristics. A 5V-to-2.5V buck converter switched at 200 kHz in closed-loop configuration was tested, measuring the duty ratio and modulating signals while sweeping the control reference voltage. Power stage parameters were $L = 400\text{nH}$, $C = 1.5\text{mF}$, $ESR = 2\text{m}\Omega$. A digital PI regulator was employed, sampled at $N = 8$ times the switching frequency. Tests were carried out for a trailing edge and a triangular modulator, yielding the transcharacteristics shown in Fig. 3.3.8 and 3.3.9. Dead bands appear in the trailing edge modulator characteristic, while the triangular modulator exhibits a large reduced gain zone. The main conclusions previously drawn concerning the superior linearity of the triangular modulation are confirmed. In Fig. 3.3.9 the presence of a small dead band at $D = 0.5$ is found, similarly to what observed in the simulated curve of Fig. 3.3.6 and explainable through the same arguments.

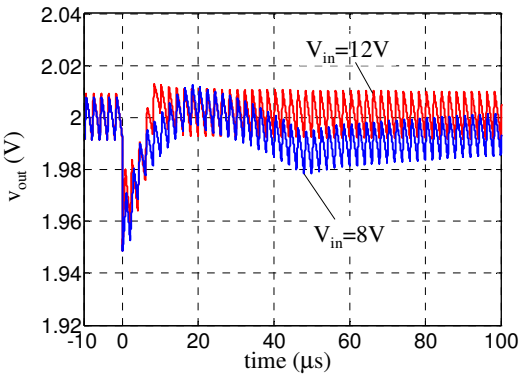

Fig. 3.3.10 – Output voltage transient during a 0A→20A load step up transient, V_{in} = 8V and 12V

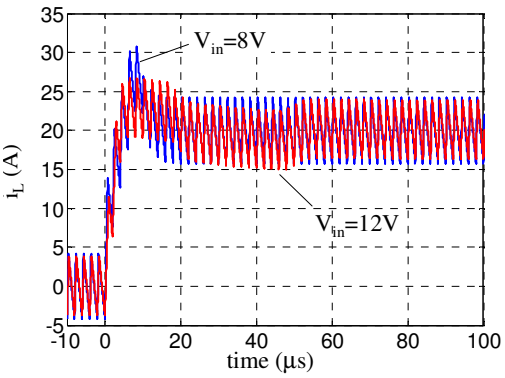

Fig. 3.3.11 – Inductor current transient during a 0A→20A load step up transient, V_{in} = 8V and 12V

iii. Effects On The Converter Closed-Loop Operation

Converter steady state equilibrium is compromised whenever its operating point falls into or sufficiently close to a dead band. Let us consider the 12V-to-2V step-down converter discussed in Subsection *i* when a trailing edge modulator is used instead of a triangular modulator. Nominally, the converter operating point lies at $D = 2/12 \approx 0.17$; from Fig. 3.3.7, critical operating points for the converter are $D = 0.5$ and $D = 0.25$, while a smaller dead band appears at $D = 0.75$. Thus, if the input voltage decreases down to, for instance, 8V, the closed-loop system will operate in the vicinity of a critical point. Simulations were carried out to compare the converter transient responses to a 0A-20A load step up when the input voltage is V_{in} = 12V or V_{in} = 8V. In the latter case the converter was kept operating slightly below $D = 0.25$, then the load step was applied. This forces the control to reach a new steady-state operating point D situated slightly *above* $D = 0.25$, in order to compensate for the increased conduction losses. Looking at Fig. 3.3.7, this means that the contoller will have to *cross* the dead band located at $D = 0.25$ by properly offsetting the average value of the modulating signal. During the dead band crossing the converter will operate in open loop configuration, resulting in a degraded transient response.

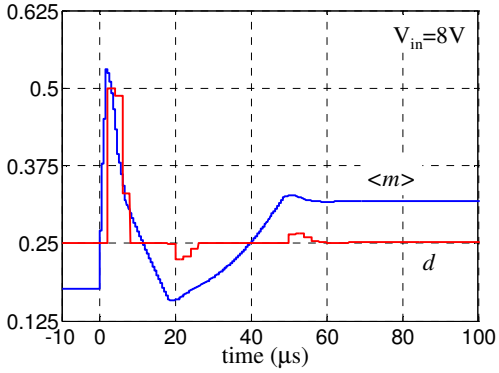

Fig. 3.3.12 – Duty cycle and modulating signal during a 0A→20A load step up transient, V_{in} = 8V

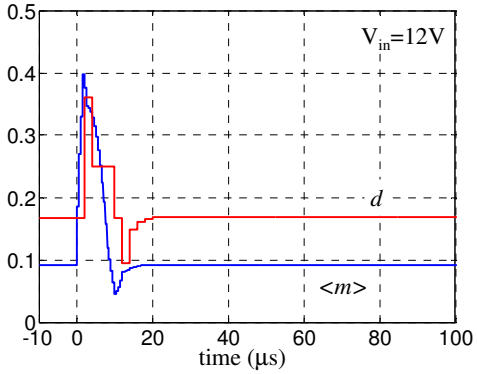

Fig. 3.3.13 – Duty cycle and modulating signal during a 0A→20A load step up transient, V_{in} = 12V

Figures 3.3.10 and 3.3.11 show the comparison. The difference in the dynamic behavior is particularly evident in the output voltage response, in which a temporary open-loop operation is visible for V_{in} = 8V immediately after the load step. It is important to realize that the degraded response is not due to the lower bandwidth that results from the input voltage reduction. It is a strictly non-linear phenomenon generated by the sampling induced dead bands.

The dead band crossings during the transient can be clearly seen from Fig. 3.3.12, in which the average modulating signal $\langle m \rangle$ and the cycle-by-cycle duty ratio d are shown during the transient response for V_{in} = 8V. Careful examination of this plot leads to the observation that the dead band at D = 0.25 is crossed two times during the transient. During the dead band crossing the modulating signal experiences large variations due to the action of the controller. As expected, the final steady state value of $\langle m \rangle$ is offset with respect to the initial value, meaning that a dead band has been crossed. In Fig. 3.3.13 the same plot is shown for the V_{in} = 12V transient. A strikingly faster transient is achieved.

Chapter IV

PWM Linearization Techniques

The previous Chapter illustrated the fundamentals of the multiple sampling technique, presenting modeling approaches for both the small-signal and steady-state behavior of multi-sampled modulators. The modulator phase lag reduction due to an increased sampling frequency can be successfully employed to design compensators that easily achieve large control bandwidths compared to classical single-sampling control loops. However, increasing the sampling frequency with the purpose of reducing the PWM equivalent delay time comes at the price of injecting switching frequency harmonics into the feedback loop. This deeply affects the operation of a multi-sampled system both statically and dynamically, the most relevant effect being the appearing of dead bands in the modulator transcharacteristics. Examples were made in the previous Chapter showing how the presence of a dead band in the vicinity of the converter operating point leads to severe degradation of the control action.

In this Chapter a number of *linearization techniques* will be considered that share the common purpose of eliminating, totally or partially, the sampling induced dead

bands phenomenon, thus restoring the linear behavior of the digital modulator [40,42,44]. A second, but not less important objective of the proposed techniques is that of preserving the phase boost property of the multi-sampling approach.

Two categories of linearization techniques will be examined in this Chapter, namely *ripple removal techniques* and *PLL-based techniques*. The former obtain the PWM linearization by means of proper small-signal processing of the sampled error signal aimed to remove the switching frequency ripple. In PLL-based techniques, on the other hand, no ripple removal is performed and the linearization of the modulator transcharacteristic is achieved by properly phase-shifting the modulating signal with respect to the carrier waveform.

Both these two approaches will be discussed in terms of linearization effectiveness, phase boost preservation and complexity.

4.1. Ripple Removal Techniques

Ripple removal techniques work on the basic concept illustrated in Fig. 4.1.1 for a voltage mode control. Before being processed by the control algorithm $G_c(z)$, the sampled error signal $e[k]$ undergoes some signal processing operation $RR(z)$ aimed to remove its switching frequency components. Being the resulting sequence $e_f[k]$ ripple-free, no or negligible switching harmonic content is found superimposed to the modulating signal $m[k]$, yielding a linear modulator operation.

Two ripple removal solutions differ in the structure of $RR(z)$. More precisely, $RR(z)$ determines both the technique's ripple rejection capability and its degree of phase boost preservation. Indeed, if $T_0(z)$ represents the system's loop gain with no ripple removal provision employed, the actual loop gain is:

$$T(z) = RR(z)T_0(z) \tag{4.1.1}$$

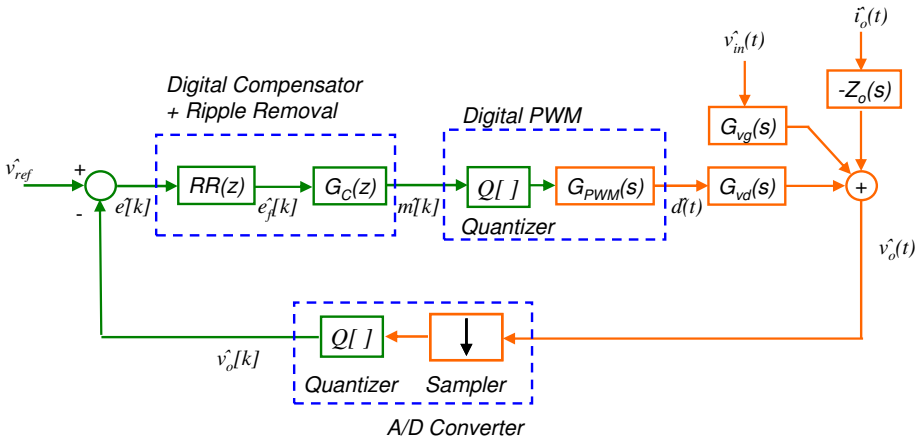

Fig. 4.1.1 – Multisampled voltage mode control employing a ripple removal technique

A ripple removal technique able to *completely* remove the switching frequency ripple is characterized by a transfer function *RR(z)* that has *N-1* zeros placed on the unit circle, where *N* is the multisampling ratio:

$$RR(z_l = \exp(j2\pi f_l \frac{T_s}{N})) = 0, \qquad f_l = lf_s, \quad 1 \le l \le N-1 \tag{4.1.2}$$

On the other hand, to maintain the phase boost property of the multisampling technique, one should have:

$$\arg(RR(z = \exp(2\pi f_c \frac{T_s}{N}))) = 0, \tag{4.1.3}$$

i.e. no phase lag should be introduced by *RR* at the designed crossover frequency f_c.

Requirements (4.1.2) and (4.1.3) cannot be simultaneously satisfied, and a certain degree of tradeoff exist between the phase boost preservation requirement and the switching frequency ripple attenuation.

Two ripple removal techniques will be described in the following Subsections based on different structures for *RR(z)*.

4.1.1. Moving Average Filtering

The most straightforward solution to the ripple removal problem is to calculate $e_f[k]$ as a running average of the N most recent samples of $e[k]$:

$$e_f[k] = \frac{1}{N}\sum_{i=0}^{N-1} e[k-i] \tag{4.1.4}$$

In the theory of digital filters (4.1.4) is recognized as the time-domain equation of a *moving average* filter. Its z-domain transfer function is easily calculated as:

$$RR_{MA}(z) \equiv \frac{E_f(z)}{E(z)} = \frac{1}{N}\sum_{i=0}^{N-1} z^{-i} = \frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}} \tag{4.1.5}$$

This Finite-Impulse-Response (FIR) filter has N-1 zeros located exactly as described by (4.1.2), and therefore is able to perform a *complete* ripple removal. Moreover, its FIR nature allows the ripple cancellation to be performed in N sampling steps, i.e. one switching period.

In spite of these desirable properties, a ripple removal technique based on (4.1.5) lacks any phase boost preservation capability and is therefore not recommended for multisampling applications. It is nevertheless useful to dedicate this section to the study of the moving average filtering, as it will clarify the role and effect of $RR(z)$ in the closed-loop configuration and will naturally lead to the development of other, more effective ripple removal techniques.

Let us consider the case study presented in Chapter III, Section 3.3.1, namely a 12V-to-2V buck converter intended for high-current applications. In Section 3.3.1 a 4-sampled digital PI regulator was designed so as to achieve a closed loop bandwidth $f_c = f_s/5$, a phase margin $m_\Phi = 55°$ and a gain margin GM = 17dB. The simulated dynamic performances revealed a fast and damped response as far as a triangular modulation was employed. However, when a trailing edge modulator was used,

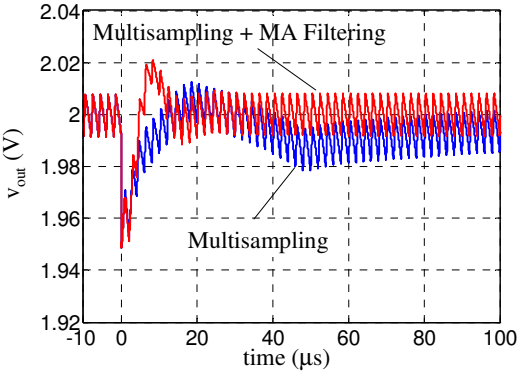

Fig. 4.1.2 – Output voltage transient during a 0A→20A load step up transient, V_{in} = 8V, with and without MA ripple filtering

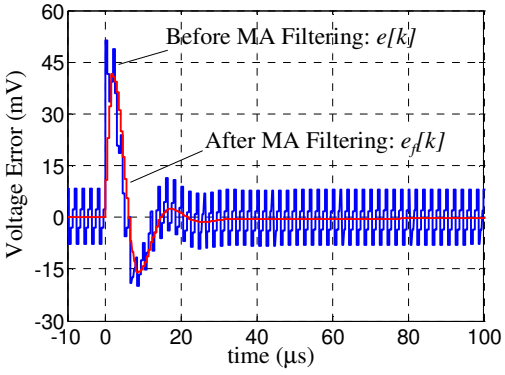

Fig. 4.1.3 – Voltage error transient during a 0A→20A load step up transient, V_{in}=8V, before and after moving average filtering

presence of large sampling induced dead bands in the modulator transcharacteristics revealed severe dynamical limitations, clearly visible if the converter operates around certain critical operating points. We wish now to show first how the moving average filtering (4.1.5) effectively linearizes the modulator by removing the static dead bands. Secondly, we will prove that the same moving average action severely deteriorates the system's phase margin.

Let us consider the critical operation at V_{in} = 8V used in Section 3.3.2 to highlight the negative impact of the modulator dead bands on the converter dynamics. In Fig. 4.1.2 simulation results are reported which compare the converter response to a 0A-20A load step up with and without the filter $RR_{MA}(z)$ inserted in the regulation loop. When no ripple removal provision is employed, the output voltage transient (already seen in Fig. 3.3.10) exhibits a temporary open-loop evolution immediately after the load step, due to the modulating signal m crossing the dead band located at D = 0.25. On the other hand, when the moving average filtering is applied to $e[k]$, a clearly faster transient is achieved. The action of $RR_{MA}(z)$ can be appreciated from Fig. 4.1.3, where its input and output waveforms $e[k]$ and $e_f[k]$ are illustrated during the same load step.

The faster transient response shown in Fig. 4.1.2 is due to the suppression, operated by $RR_{MA}(z)$, of the modulator dead band located at D = 0.25. To see this, let us examine

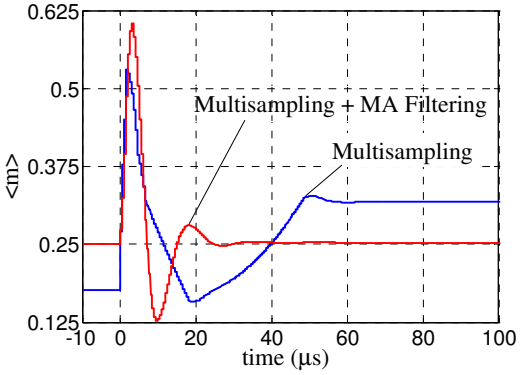

Fig. 4.1.4 – Modulating signal during a 0A→20A load step up transient, V_{in} = 8V, with and without MA ripple filtering

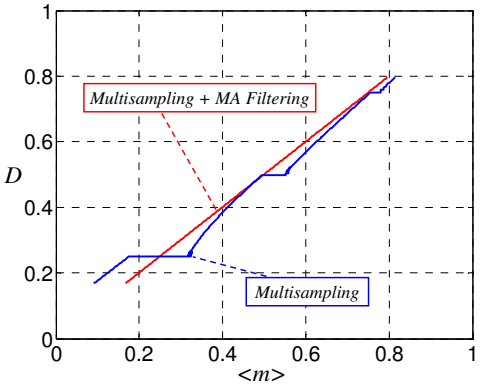

Fig. 4.1.5 – Simulated PWM transcharacteristic, with and without MA ripple filtering

in detail Figure 4.1.4, where average value <*m*> of the modulating signal is shown during the load transient for both the linearized and unlinearized system. In Section 3.3.2 we observed how the presence of the dead band forces the final steady state value of <*m*> to be largely offset with respect to its initial value due to the crossing of the dead at D = 0.25. No such offset appears in Fig. 4.1.4 when the ripple removal algorithm is operating. Moreover, the transient behavior of <*m*> in the linearized system does not experiment the large variations visible in the unlinearized case, meaning that a partial removal of *dynamic dead bands* is also achieved by $RR_{MA}(z)$.

The final and strongest proof of the dead bands elimination operated by the filtering action is shown in Fig. 4.1.5, which illustrates the simulated static transcharacteristics

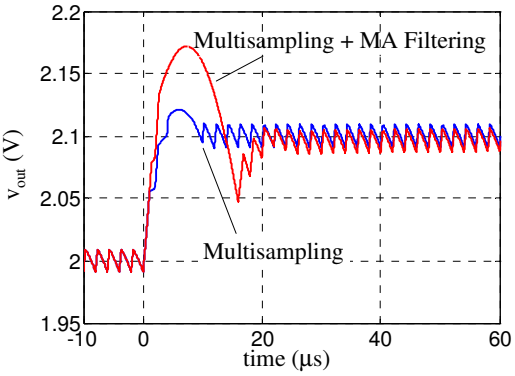

Fig. 4.1.6 - Output voltage during a 2V→2.1V reference step up transient, Vin=12V, with and without MA ripple filtering

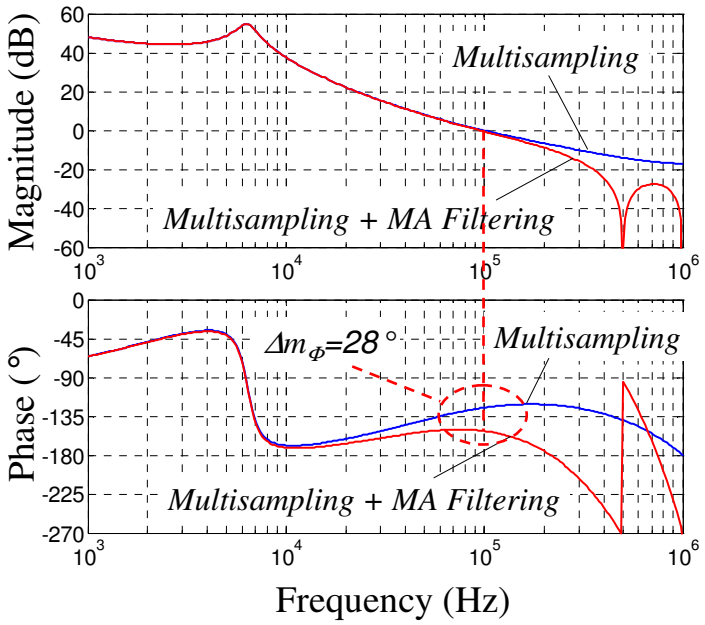

Fig. 4.1.7 – Loop gain Bode diagrams with and without moving average filtering of the ripple

obtained with and without the ripple removal. *Zero* static nonlinearity is achieved (see eq. 3.2.66).

The excellent ripple rejection capabilities of moving average filters are entirely overcome by their intrinsic inability to preserve the phase boost property deriving from the multiple sampling. Indeed, though the load step response shown in Fig. 4.1.2 is greatly improved by the presence of the ripple filtering, the resulting system exhibits an unacceptably low phase margin. The poor stability margins of the system can be appreciated in Fig. 4.1.6, where a 2V→2.1V reference step is applied to the closed loop configuration at V_{in} = 12V. In the case of multisampling with moving average filtering, a significant overshoot originated by temporary duty cycle saturation is observed. This nonlinear behavior is nevertheless originated by the poor damping of the closed-loop system; on the other hand, the transient response of the pure multisampled system exhibits a less deep duty cycle saturation and therefore a significantly smaller overshoot.

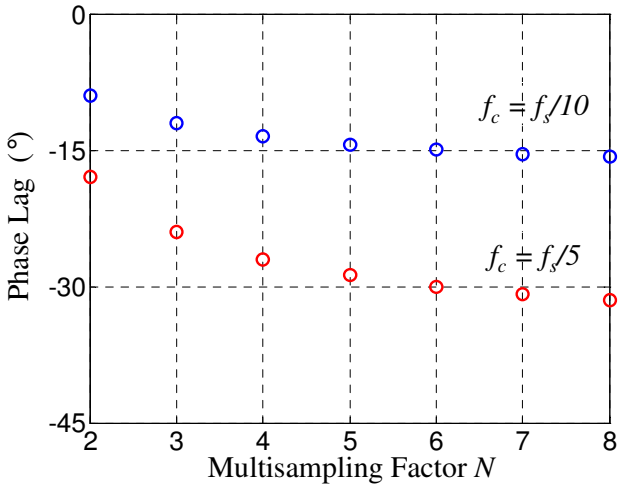

Fig. 4.1.8 – Phase lag introduced by the moving average filtering action

The transient response of the control loop designed in Section 3.3.1 to have a phase margin of 55° is compared with the one achieved after the insertion of $RR_{MA}(z)$. Bode diagrams of T and T_0 are shown in Fig. 4.1.7, from which the phase margin reduction can be estimated as $\Delta m_\Phi = 28°$. Thus, after the insertion of $RR_{MA}(z)$ the system phase margin is 27°. Though the PI compensator could be re-designed to partially compensate for the phase margin loss in presence of the moving-average filter, no small-signal performances comparable to the pure multisampling approach could be achieved.

Though derived in the context of a specific case study, the inadequacy of the moving average filtering as a ripple removal technique can be stated generally. Figure 4.1.8 shows the phase lag introduced by a moving average filter as a function of the multisampling factor N and evaluated at $f_c = f_s/10$ and $f_c = f_s/5$. An analytical expression for the phase lag is easily derived from (4.1.5) by letting $z = exp(j2\pi fT_s/N)$ and performing simple algebraic manipulations:

$$\arg(RR_{MA}(f)) = -2\pi \frac{fT_s}{2} \frac{N-1}{N}, \tag{4.1.6}$$

which represents an additional time delay for the control loop. Equation (4.1.6) rapidly approaches $-2\pi fT_s/2$, destroying the modulator phase boost achieved through

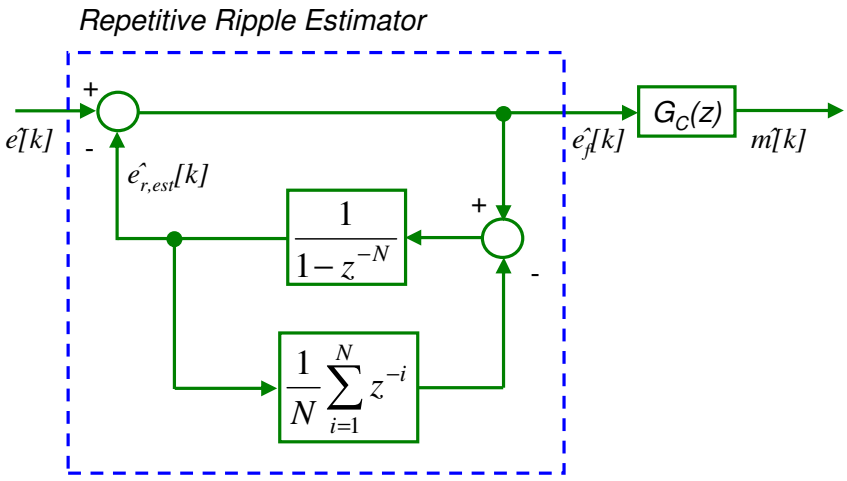

Fig. 4.1.9 – Ripple removal technique by means of repetitive estimation

multiple sampling. From (4.1.6) it can be stated that, as far as the phase boost and hence the achievable closed-loop bandwidth are concerned, the moving average filtering is by all means comparable to the classical single sampling approach.

Filter families indeed exist that ensure a strong ripple rejection *and* maintain adequate phase boost preservation. The next Subsection is devoted to their study, in the context of the repetitive ripple estimation algorithms.

4.1.2. Repetitive Ripple Estimation

Let us consider the ripple removal filter illustrated in Fig. 4.1.9. It exploits the periodic nature of the ripple $e_r[k]$ superimposed to $e[k]$ to generate a periodic sequence $e_{r,est}[k]$ which, in steady state operation, is *equal* to $e_r[k]$, hence the name *repetitive ripple estimation* (RRE) under which this technique is known. The error and the estimated ripple are subtracted to form the sequence $e_f[k]$, yelding a total ripple rejection.

The filter operates as a feedback system which uses the signal $e_f[k]$ as a reference and sees the switching ripple superimposed to $e[k]$ as a disturbance. The $1/(1-z^{-N})$ block in the feedeback path represents a digital oscillator that infinitely amplifies the

switching harmonics $f_l = lf_s$, $1 \le l \le N-1$, so that the steady-state signal $e_{r,est}[k]$ is an exact copy of the error ripple $e_r[k]$. The moving average block that processes $e_{r,est}[k]$ is fundamental to ensure that the DC component of $e[k]$ is not canceled by the ripple estimation process. In fact, as the $1/(1-z^{-N})$ block contains an integrating action due to its pole at $z = 1$, whatever DC component present at its input would be compensated, thus nulling the DC component of $e_f[k]$. The moving average block provides the necessary DC compensation at the digital oscillator input.

Straightforward block diagram algebra can be employed to determine the transfer function $RR_{RE}(z)$ of the repetitive estimator:

$$RR_{RE}(z) = \frac{1}{1+T_{RE}(z)} = \frac{1 - z^{-N} + \frac{1}{N}\sum_{i=1}^{N} z^{-i}}{1 - z^{-N} + \frac{1}{N}\sum_{i=1}^{N} z^{-i} + K_{RE}}, \qquad (4.1.7)$$

having defined the repetitive estimator loop gain $T_{RE}(z)$:

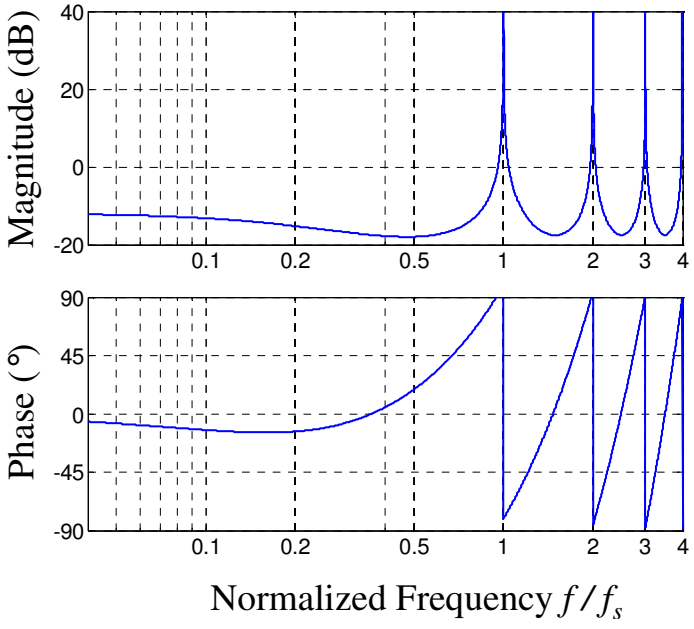

Fig. 4.1.10 – Bode diagrams of the Repetitive Ripple Estimator loop gain; N=8, K_{RE}=0.25

$$T_{RE}(z) = \frac{K_{RE}}{(1 - z^{-N} + \frac{1}{N}\sum_{i=1}^{N} z^{-i})} \tag{4.1.8}$$

Equation (4.1.8) can be written in a far more insightful form using the equality:

$$\frac{1}{N}\sum_{i=1}^{N} z^{-i} = \frac{1}{N}\frac{z^{-1}(1 - z^{-N})}{1 - z^{-1}} \tag{4.1.9}$$

Plugging (4.1.9) into (4.1.8) yields:

$$T_{RE}(z) = \frac{K_{RE}}{\frac{1 - z^{-N}}{1 - z^{-1}}(1 - \frac{N-1}{N} z^{-1})} \tag{4.1.10}$$

Bode plots of $T_{RE}(z)$ are shown in Fig. 4.1.10 in the case $N = 8$ and $K_{RE} = 0.25$. As anticipated, the magnitude of $T_{RE}(z)$ is infinite at the switching harmonics because of the poles of the digital oscillator, while the low-frequency magnitude is limited by the pole located at $z = (N-1)/N$. Correspondingly, the Bode diagrams of $RR_{RE}(z)$ shown in Fig. 4.1.11 exhibit total ripple rejection and a low-phase lag behavior at low frequencies.

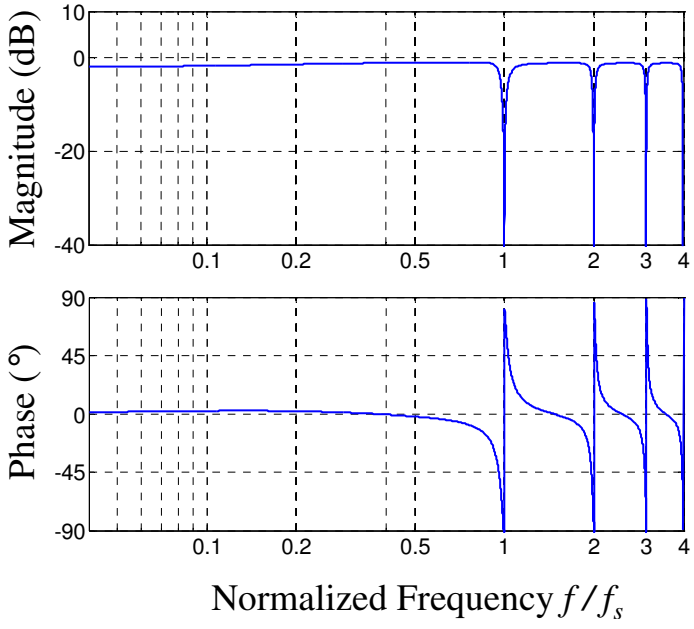

Fig. 4.1.11 – Bode diagrams of the Repetitive Ripple Estimator transfer function; N=8, K_{RE}=0.25

This latter observation, i.e. the good phase behavior of $RR_{RE}(z)$ in the low frequency range, is what makes this technique interesting and suitable for multisampling applications. Moreover, the repetitive estimator is essentially a feedback system. Therefore its ability to reconstruct and cancel the switching ripple does not depend on the particular converter topology, operating condition or ripple waveshape, but relies only in the periodic nature of the ripple itself.

The only design parameter of the repetitive estimator (4.1.7) is the gain K_{RE}, which is primarily related to the number n_c of sampling cycles required for the ripple reconstruction to be performed. Rigorously speaking, (4.1.7) is a IIR system and therefore its transients extend to infinity; however, a representative number n_c can nevertheless be defined as the number of sampling cycles required by the estimator to reduce the estimation error to negligible levels and therefore obtain the ripple cancellation. The higher K_{RE}, the fastest is the ripple reconstruction due to the increased estimator loop gain T_{RE}.

Increasing K_{RE}, however, reduces the low-frequency magnitude of $RR_{RE}(z)$, and therefore of the whole control loop gain. More precisely, the repetitive estimator introduces a low-frequency attenuation which is more pronounced as K_{RE} increases. At DC, evaluation of (4.1.7) yields:

$$RR_{RE}(1) = \frac{1}{1 + K_{RE}} \tag{4.1.11}$$

The attenuation introduced by K_{RE} estimator is not constant over frequency and cannot be compensated, in general, by a mere adjustment of the compensator gain. Thus, a tradeoff exists between a fast ripple reconstruction and elimination, and an overall loop gain reduction due to a low-frequency attenuation operated by the estimator. As pointed out in [40] suitable values of K_{RE} lie between 0.125 and 0.25, for

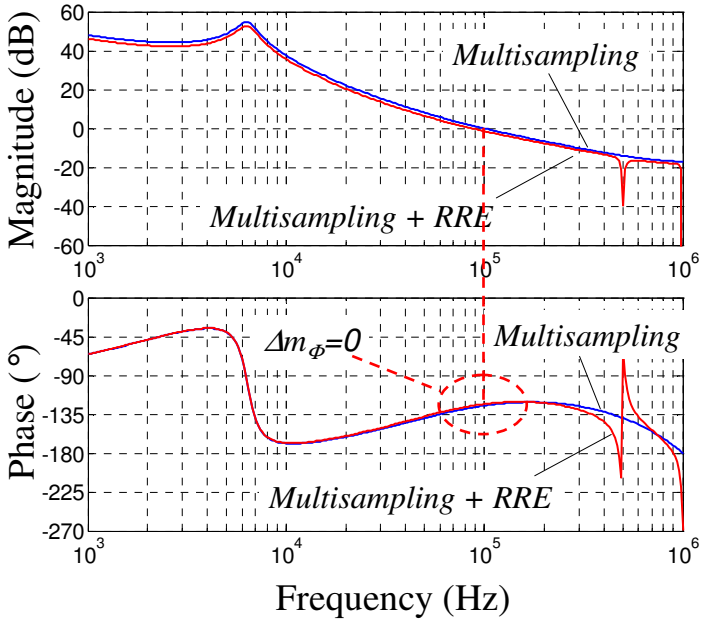

Fig. 4.1.12 – Loop gain Bode diagrams with and without repetitive ripple estimation

which the ripple compensation is achieved in few tens of sampling steps with negligible loop gain attenuation.

Similarly to what done in the previous Section concerning the moving average filtering, we will exemplify the operation of a repetitive ripple estimator on the case study introduced in Section 3.3.1. Basing on the previous observations, we will choose $K_{RE} = 0.25$ and consider a 4-sampled repetitive estimator.

Bode diagrams of the system loop gain with and without the repetitive estimator are

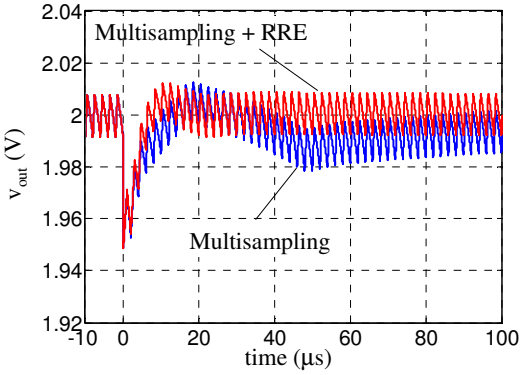

Fig. 4.1.13 – Output voltage during a 0A→20A load step up transient, V_{in} = 8V, with and without RRE

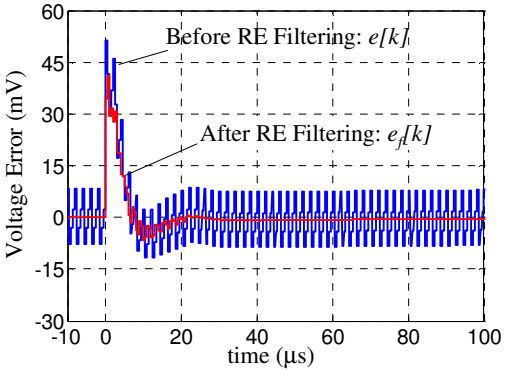

Fig. 4.1.14 – Voltage error during a 0A→20A load step up transient, V_{in}=8V, before and after RRE filtering

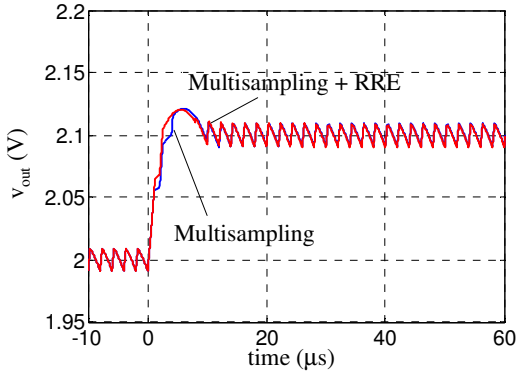

Fig. 4.1.15 – Output voltage during a 2V→2.1V reference step up transient, V_{in}=12V, with and without RRE filtering

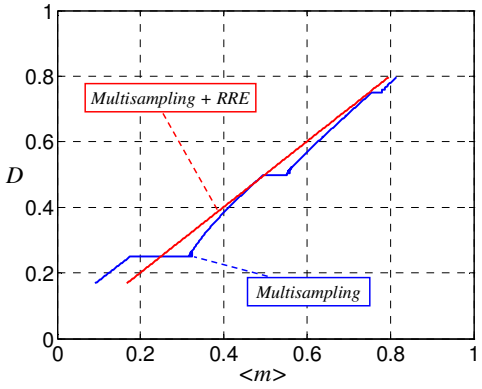

Fig. 4.1.16 – Simulated PWM transcharacteristic, with and without RRE ripple filtering

shown in Fig. 4.1.12. No appreciable phase deviation occurs up to the designed closed-loop bandwidth $f_c = f_s/5$ = 100kHz. The system phase margin is thus entirely preserved. The load step-up transient shown in Fig. 4.1.13 for V_{in} = 8V is now fast and well damped compared with the response obtained without ripple removal. The voltage error during the transient response is shown in Fig. 4.1.14 before and after the repetitive estimation. From this plot the dynamics of the ripple reconstruction after a transient event can also be appreciated.

A 2V→2.1V reference step transient is shown in Fig. 4.1.15 compared to the pure multisampling solution. The two responses show an essentially equal dynamics, this being a further evidence of the phase boost preservation property of the repetitive estimator.

Finally, in Fig. 4.1.16 the modulator static transcharacteristic with and without repetitive ripple removal is shown. As observed when discussing the moving average filtering, *perfect* linearization is performed in steady state condition.

A single-phase Voltage Regulation Module (VRM) prototype board was employed to experimentally investigate the ripple cancellation technique. A 4-sampled Adaptive Voltage Positioning (AVP) control was implemented to design a resistive output impedance, this being a common requirement in VRM applications; with AVP control

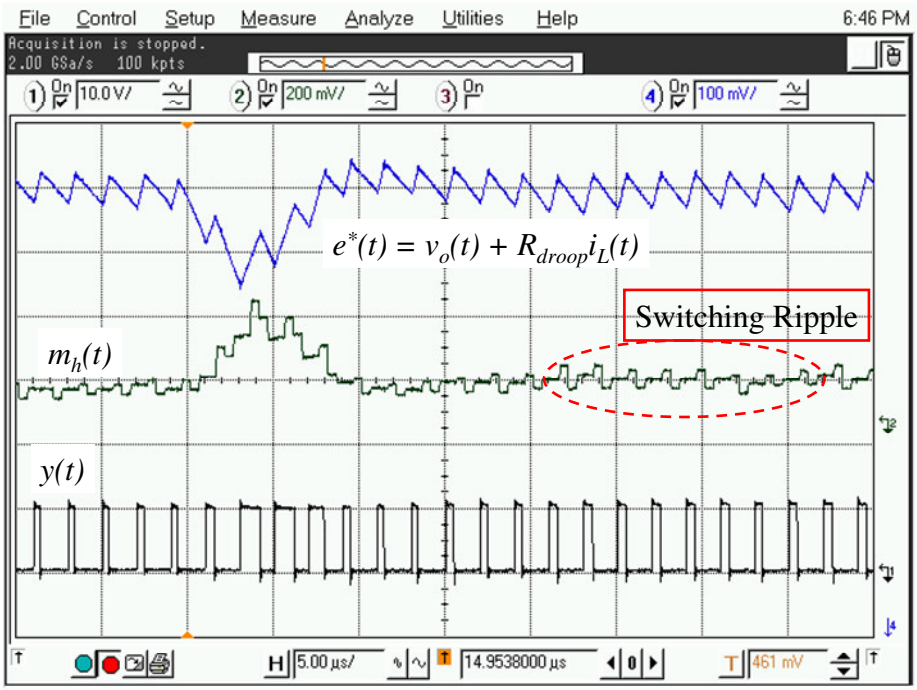

Fig. 4.1.17 – Experimental 0→15A load step without RRE filtering; e*(t) 100mV/div, m_h(t) 200mV/div, y(t) 10V/div, time scale 5µs/div

[101-105] the analog error signal representing the error *e(t)* to be sampled and processed by the digital compensator is a linear combination of inductor current and output voltage:

$$e(t) = V_{ref} - v_o(t) - R_{droop} i_L(t) \tag{4.1.12}$$

where R_{droop} is the droop resistance. The parameters of the VRM synchronous buck converter employed for the experimental tests were V_{in} = 5V input, V_o = 1V output, L = 400 nH, C = 1.54 mF (tantalum), ESR=2 mΩ, R_{droop} = 2 mΩ. The digital control has been implemented using a Spartan3 Field Programmable Gate Array (FPGA) by Xilinx. A typical 0 to 15A load transient response achieved without RRE filtering is depicted in Fig. 4.1.17. Please note that the waveform $e^*(t) = v_o(t)+R_{droop} \cdot iL(t)$ is shown as the error signal in Fig. 4.1.17, along with the ripple-affected modulating signal $m_h(t)$ and the PWM output waveform $y(t)$. When the RRE algorithm is active, the load transient illustrated in Fig. 4.1.18 is obtained. The switching frequency ripple is now effectively

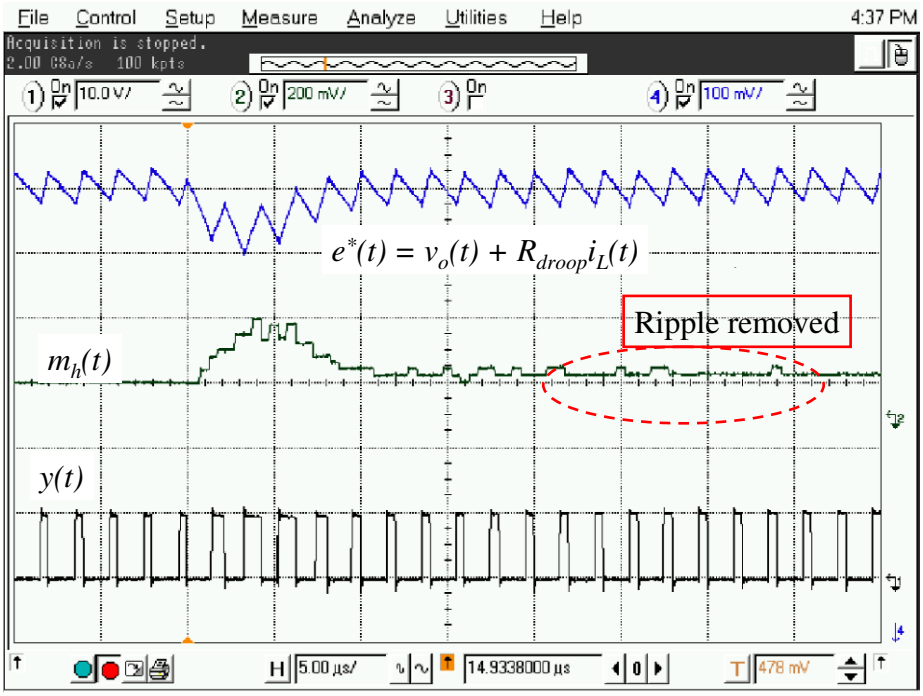

Fig. 4.1.18 – Experimental 0→15A load step with RRE filtering; e*(t) 100mV/div, $m_h(t)$ 200mV/div, y(t) 10V/div, time scale 5µs/div

removed from $m_h(t)$, confirming the expected operation of the repetitive estimation. As a side effect of the ripple removal, the transient dynamics shown in Fig. 4.1.18 is slightly faster compared with Fig. 4.1.17.

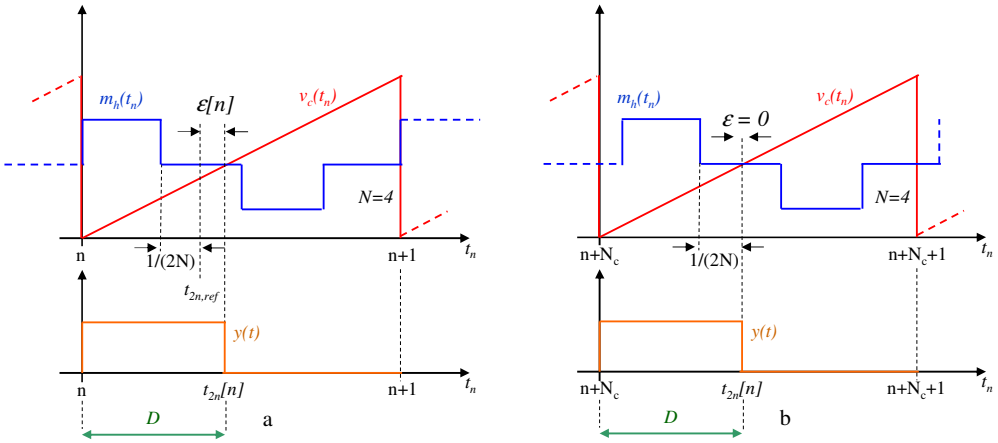

Fig. 4.2.1 – Modulation diagrams before (a) and after (b) PLL locking

4.2. PLL-Based Technique

The linearization approaches discussed in Section 4.1 achieve the elimination of the sampling-induced dead bands by complete steady-state removal of the switching ripple from the sampled error waveform processed by the comparator.

An alternative way to remove the PWM dead bands is that of eliminating the possibility of vertical crossings between the modulating signal m_h and the carrier v_c [44]. This approach, which does not involve the removal of the switching harmonics, relies on a dynamic adjustment of the relative phase shift between m and v_c that ensures horizontal crossings for every steady-state operating point. Thus, in steady state condition m and v_c are properly *phase-locked*, hence the name of this kind of approach.

Let us consider Fig. 4.2.1.a, in which the generic n-th switching cycle is shown for a (N,0)-sampled trailing-edge modulator operating in steady-state. Please note that the time axis is normalized with respect to the switching period T_s, as done in Chapter III. We shall denote with $\varepsilon[n]$ the error between the actual turn-off instant $t_{2n}[n]$ and a *reference* turn-off instant $t_{2n,ref}[n]$ located in the midpoint of the sampling cycle:

$$t_{2n,ref}[n] \equiv q_N[t_{2n}[n]] + \frac{1}{2N} \tag{4.2.1}$$

$$\varepsilon[n] \equiv t_{2n}[n] - t_{2n,ref}[n] \tag{4.2.2}$$

The PLL correction algorithm will force $\varepsilon[n]$ to zero by properly *phase-shifting m* with respect to v_c. After a number N_c of switching cycles that depends on the dynamics of the correction algorithm, the error ε will become negligible and the steady-state modulation diagram will approach the one depicted in Fig. 4.2.1.b. It is clear that as long as the error converges to zero, no steady-state operating point will exhibit vertical crossings between m_h and v_c, meaning a complete elimination of the static sampling-induced dead bands.

The required phase-shifting is achieved by temporarily modulating the sampling period. Let us denote with $T_c[n]$ the sampling period decided by the correction algorithm after the measurement of the error $\varepsilon[n]$:

$$T_c[n] = \frac{1}{N} + \Delta T_c[n] \tag{4.2.3}$$

In the $n+1$-th switching cycle the measured error $\varepsilon[n+1]$ is related to $\varepsilon[n]$ by the following relationship:

$$\varepsilon[n+1] = \varepsilon[n] - N\Delta T_c[n] \tag{4.2.4}$$

Indeed, if the sampling period is corrected by $\Delta T_c[n]$, the overall error reduction after N sampling steps, i.e. after one switching period, is $N \cdot \Delta T_c[n]$. It is important to point out that (4.2.4) is an approximated relationship, in that it is assumed that a time shift of the sampling instants brings a corresponding time shift of the modulating signal. As discussed in Chapter III, Section 3.2.2, the sampler is not a time-invariant system and a shift in the sampling events causes the modulating signal to modify its shape. However, as long as a small corrections in the sampling pattern are considered, this effect can be neglected.

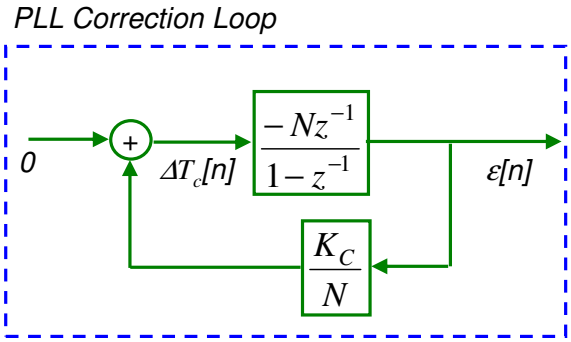

Fig. 4.2.2 – Block diagram of the PLL correction

Equation (4.2.4) can be thought as the difference equation describing the system to be controlled by the PLL correction algorithm, the feedback signal being $\varepsilon[n]$ and the control signal being $\Delta T_c[n]$. Please note that (4.2.4) contains an inherent integrating action, and therefore allows the error signal to be nulled by means of a purely proportional control law:

$$\Delta T_c[n] = \frac{K_C}{N}\varepsilon[n], \tag{4.2.5}$$

where K_C plays the role of proportional gain and represents the design parameter for the correction algorithm. These concepts are illustrated in Fig. 4.2.2. Please note that when the correction is achieved, $\varepsilon = 0$, $\Delta T_c = 0$ and thus $T_c = 1/N$: the steady state sampling frequency is always equal to Nf_s. This property is of extreme importance, as it means that no provisions have to be taken to ensure stabilization of the sampling frequency.

Solving (4.2.4) and (4.2.5) for the *correction loop gain* $T_{Corr}(z)$ yields:

$$T_{Corr}(z) = K_C \frac{z^{-1}}{1 - z^{-1}} \tag{4.2.6}$$

The dynamics of the correction algorithm is then determined by solving the characteristic equation $1 + T_{Corr}(z) = 0$. The single pole which governs the closed-loop response of the correction law is:

$$p_C = 1 - K_C \tag{4.2.7}$$

Stable correction is achieved for $0 < K_C < 2$. However, oscillatory modes are found for $1 < K_C < 2$ and should be avoided. Thus the range of interest of K_C is $0 < K_C \leq 1$. The higher the proportional gain K_C, the faster will result the correction action. Interestingly $K_C = 1$ yields a dead-beat corrector, which achieves the required correction in one switching step. Though the possibility of emplying a dead beat corrector is indeed appealing, care must be taken when designing very fast correction algorithms. In fact, a fast correction law may affect the duty cycle modulation operated by the control law of the digital compensator, resulting in possible malfunctioning. On the other hand, if the control loop and the correction loop have different dynamics – i.e. one is faster than the other – more robust performances are achieved.

Considering, as usual, the 12V-to-2V step down converter taken as a case study, Fig. 4.2.3 illustrates the static PWM transcharacteristic linearization operated by the PLL approach. For the PLL design, $K_C = 0.8$ was chosen. Please note that perfect

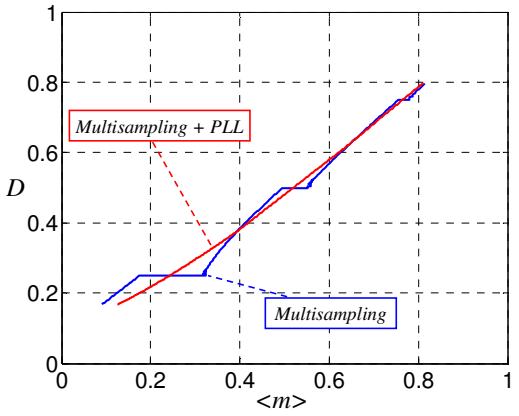

Fig. 4.2.3 – Simulated PWM transcharacteristic, with and without PLL correction

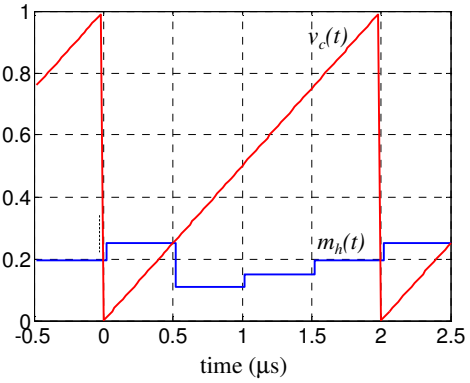

Fig. 4.2.4 – Modulation diagram at D = 0.25 without PLL correction

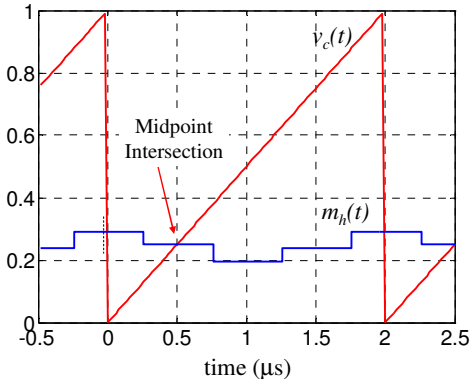

Fig. 4.2.5 – Modulation diagram at D = 0.25 with PLL correction

linearization can *not* be achieved through this technique, as no switching ripple removal occurs. The resulting characteristic is nevertheless very close to the ideal one and dead bands are completely eliminated.

Figures 4.2.4 shows the modulating signal $m_h(t)$ and the carrier $v_c(t)$ for a steady state operation at V_{in} = 8V when no PLL correction is active. As expected, the system operates in the vicinity of a vertical crossing, i.e. next to a dead band. On the other hand, when the PLL is operating the modulation diagram of Fig. 4.2.5 is obtained, clearly showing the correct phase-locking at the desired midpoint intersection.

Figure 4.2.6 illustrates the 0A→20A load transient with and without the PLL correction and for V_{in} = 8V. The closed-loop response clearly benefits from the m-v_c

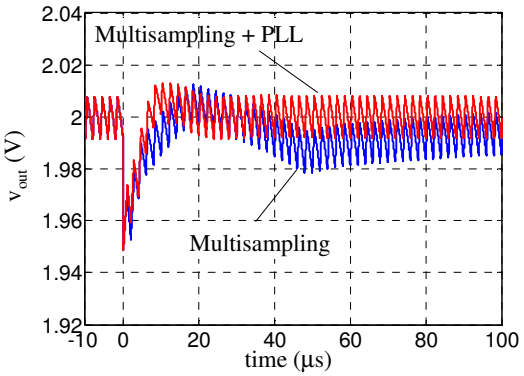

Fig. 4.2.6 – Output voltage during a 0A→20A load step up transient, V_{in} = 8V, with and without PLL correction

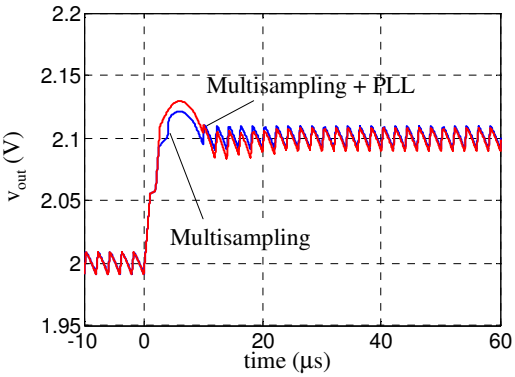

Fig. 4.2.7 – Output voltage during a 2V→2.1V reference step up transient, V_{in}=12V, with and without PLL correction

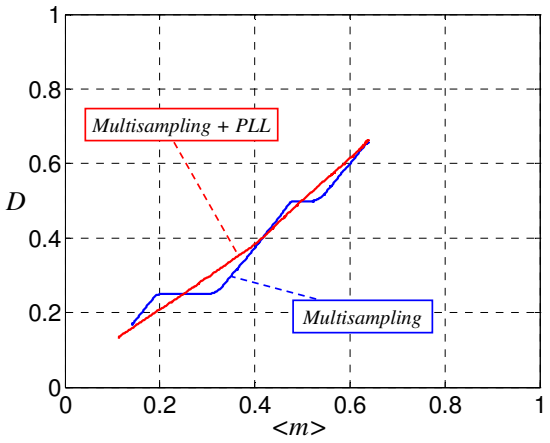

Fig. 4.2.8 – Experimental PWM transcharacteristic, with and without PLL correction

phase locking. Moreover, this technique does not interfere with the system's phase margin. In Fig. 4.2.7 the 2V→2.1V reference step response with PLL operation is compared to the operation with no PLL, showing no dynamical differences.

Experimental tests were carried out in order to verify the effectiveness of the PLL-based dead bands removal technique. On this purpose, the proposed correction algorithm was VHDL-coded on an Altera EP200KE FPGA development board and tested on a step-down prototype converter; the parameters of the power stage were

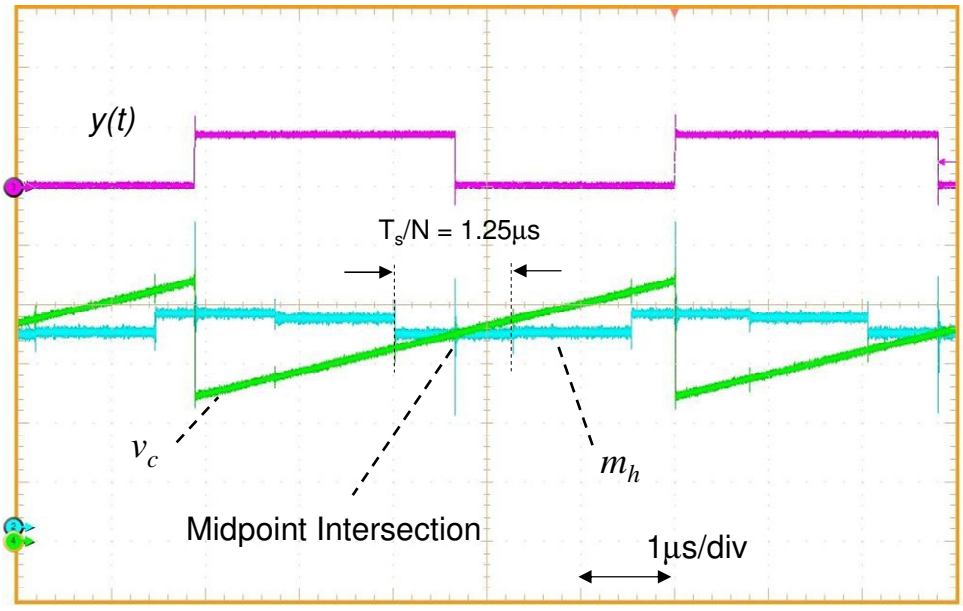

Fig. 4.2.9 – PWM Waveforms with the PLL Locked. Time scale 1µs/div

f_s = 200kHz switching frequency, V_{in} = 5V input voltage, V_o = 2.5V output voltage, L = 400 nH, C = 1.5 mF, ESR = 2 mΩ. A digital PI regulator sampling at N = 4 times the switching frequency was employed, tuned in order to obtain a closed-loop bandwidth of about f_c = 18 kHz, i.e. about one tenth of the switching frequency. The correction law (4.2.5) was implemented with K_C = 1; a simple counter was used to measure the error $\varepsilon[n]$, this being the only additional hardware requirement for the correction algorithm implementation. Comparative results are illustrated in Fig. 4.2.8, where the experimental static PWM transcharacteristic are shown with and without the PLL algorithm active. Finally, Fig. 4.2.9 shows the modulator waveforms with the PLL locked.

As a final note, it is worth to underline that the choice of the sampling period midpoint as the reference for the m-v_c phase locking is not the only possibility. In principle, any point within the sampling period could be used as reference point. However, from a small-signal perturbation point of view, the midpoint choice keeps the modulator operating point equally distant from the two neighboring sampling instants and thus to the respective dead bands. For this reason this approach has been used to present the PLL-based technique.

Chapter V

Autotuning Of Digitally Controlled SMPS: Digital Relay Feedback Approach

Autotuning [45-56] is a feature that enables a control system to automatically calculate the compensator parameters in order to achieve some specified closed-loop performances, usually expressed in terms of stability margins and dynamic capabilities. The self-calibration of a compensator enhances the versatility of a control system especially in those situations where the control design boundary conditions are only known to a limited extent. These include a precise knowledge of the plant transfer function, its parametric variations due to components tolerances, aging, temperature drifts as well as *failures* that may affect the behavior of the process being controlled.

Autotuning features may also be strictly connected with *availability* requirements when system non-catastrophic failures are temporarily handled by re-tuning of the compensator parameters to ensure stable operation and thus a higher degree of fault tolerance.

The autotuning process can be conceptually thought as composed of two phases, namely *identification* and *tuning*. The identification activity relies on a number of measurements aimed to determine some key parameters concerning the process to be controlled. In the field of SMPS, examples include the resonant frequency of the power stage, its input or output voltages, its control-to-output transfer function at a specified frequency or over an entire frequency range. These parameters may or may not be directly measurable. Thus, the identification process usually involves a certain degree of computational complexity. The *tuning phase* consists of elaborating the information gained from the identification activity in order to calculate the compensator parameters that allow the fulfillment of the specifications. This phase is usually handled by a *tuning algorithm*, the complexity of which depends on the specific technique. Both the identification and tuning phases inherently involve a high degree of *programmability* of the compensator parameters.

From this discussion it is clear how autotuning features strongly point to *digital* implementations. The intrinsic programmability of a digital compensator allows for a complete control of both its parameters and the applied control law. Tuning algorithms are easily implemented using microcontrollers or hardwired digital logic based on finite state machines (FSM). Identification-related computations can be realized by means of standard arithmetic blocks, the implementation of which is straightforward in the digital world. Thus, feasibility of a self-calibrating controller dictates a degree of freedom that has no analog counterpart, making the autotuning a potential feature *unique* to digital control systems.

In this Chapter some general considerations on self-tuning digital compensators will be made before presenting a specific tuning approach, based on the *digital relay feedback*. After a detailed description of the technique and the provisions aimed to

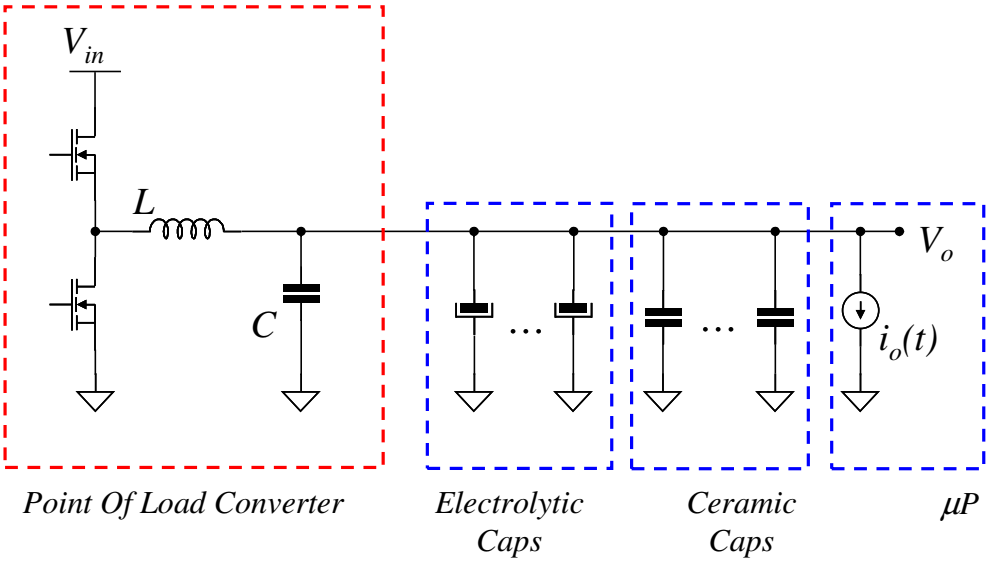

Fig. 5.1.1 – Point Of Load Converter

enhance its robustness, simulation and experimental results will be provided to give proof of its effectiveness and relatively modest hardware requirements.

5.1. Introduction to Self-Tuning Digital Compensators

Before presenting the digital relay feedback technique in its details, some general boundary conditions will be discussed to identify a possible application context as well as to give the necessary definitions that will be used later on.

5.1.1. A Motivating Example: Point Of Load Applications

Point-Of-Load (POL) converters represent an excellent case study for a tuning technique. In a distributed power architecture, these are the converters supplying the different loads present in the system. As an example, in server applications the electronic equipment to be powered consists of microprocessors, hard disk drives, peripherals and fans with different power supply specifications and voltage regulation requirements.

A simplified schematic diagram of a POL step-down converter is exemplified in Fig. 5.1.1. A synchronous buck topology is here employed to supply a low-voltage, high-

current load – such as a microprocessor –, modeled in Fig. 5.1.1 as a current source. The converter module has its own phase inductance *L* and its own output bulk capacitance *C*; in addition, a number of decoupling capacitors are usually placed in close proximity to the load. This capacitor bank is normally composed by both electrolytic caps for low-frequency decoupling and ceramic caps for high-frequency bypass purposes. The overall capacitive impedance seen by the POL converter determines, together with the phase inductance *L*, the open-loop dynamic behavior of the power stage. Parasitic resistances and inductances due to the POL-load interconnections, not shown in Fig. 5.1.1, usually also come into play when high *di/dt* load transients are considered.

In these applications the control designer has limited knowledge of the number and type of the decoupling capacitors, because they strictly depend on the load and on its voltage regulation requirements. Temperature drifts as well as component aging, the latter phenomenon especially affecting electroytic caps, also contribute to parametric variations in the converter behavior.

In these conditions a worst-case analysis of the system is always possible, leading to control design guidelines that aim to achieve some minimum stability margins, usually at the price of very poor dynamic performances. On the other hand, a self-calibrating compensator would ensure optimized performances regardless of the specific boundary conditions in which the POL converter is employed.

5.1.2. Overview of Proposed Techniques for Digital Autotuning

As digital techniques gained increasing attention from the scientific community during the last years, a number of techniques for precise and hardware-effective identification and autotuning have been proposed. Of particular interest are identification techniques based on cross-correlation methods [45-47], in which the whole frequency response of the power converter is identified through white noise

injection and consequent post-processing of the power stage response. A tuning approach based on these identification techniques was proposed in [48]. Another family of identification and tuning techniques relies on inducing amplitude-limited limit cycle oscillations in the system [49-51]. The relay-feedback approach described in section 5.2 belongs to this family. More recently, techniques partially or totally based on frequency injection methods have been developed [53-55]. An example will be given in section 5.3, where a frequency injection technique will be employed to perform the PID gain tuning. Self-calibrating controllers have also been proposed based on linear prediction methods [56].

Tuning techniques for POL converters with wide range of capacitive loads have been proposed in [52], showing feasibility and hardware-effectiveness of tuning compensators capable of handling parametric variations of the power stage capacitance covering several orders of magnitude. This work was carried out at the Colorado Power Electronics Center (CoPEC), University of Colorado at Boulder, during part of this PhD activity, under the supervision of Prof. Dragan Maksimović and Prof. Regan Zane and in collaboration with CoPEC student Mariko Shirazi.

5.1.3. Tuning Strategies

An important aspect related to the self-calibration of a digital compensator is *when*, or more precisely *how often* the autotuning should be performed. Two distinct situations can be identified, namely *start-up*, i.e. the power-on event for the converter under control, and the *normal operation* of the converter itself.

The start-up sequence of a power converter often involves a *soft-start phase*, in which the output voltage is linearly increased from 0V to the regulation level V_{ref}, then the digital compensator is enabled to provide regulation. A *start-up tuning* is performed on this purpose, which carries out initial measurements on the converter and calculates

the proper compensator parameters before entering the regulation state. Start-up is perhaps the most critical situation for a tuning technique, as it corresponds to a condition in which the knowledge of the power plant is minimum. Moreover, load specifications usually require the output voltage to stay confined within some tolerance band centered around the regulation level, meaning that proper regulation has to be maintained even *during* the tuning process.

Tuning may be necessary also during the system normal operation. Parametric variations in the plant behavior can be caused by thermal drifts, component aging or failures. An *online tuning* strategy can be planned to periodically re-calculate the compensator parameters to ensure stability and proper dynamic performances. Again, the tuning has to be carried out without significantly perturb the output voltage.

The technique presented in this work has been mainly developed as a start-up tuning process. It can be nevertheless extended and modified to include online tuning features.

5.1.4. Formulation of the Tuning Targets

The tuning technique that will be presented in the next section will consider the single-sampled voltage-mode control scheme illustrated in Fig. 5.1.2 and employing a programmable digital PID compensator of the form:

$$G_{PID}(z) = \frac{K_i}{1-z^{-1}}(1+K_{z1}-K_{z1}z^{-1})(1+K_{z2}-K_{z2}z^{-1}) \qquad (5.1.1)$$

The compensator (5.1.1) is uniquely identified once the triplet (K_i, K_{z1}, K_{z2}) is specified. In particular, the two zeros z_1 and z_2 of (5.1.1) are determined by K_{z1} and K_{z2} respectively:

$$z_{1,2} = \frac{K_{z1,2}}{1+K_{z1,2}} \qquad (5.1.2)$$

The cascade implementation of form (5.1.1) will result to be particularly useful for a number of reasons. First of all, the two PID zeros can be tuned by varying K_{z1} and K_{z2}. Please note that relationship (5.1.2) is bijective, i.e. to a given K_z corresponds only one real positive zero and viceversa. Moreover, each factor ($1+K_z - K_z z^{-1}$) maintains a unity value at DC independently on K_z. Thus, a variation in $K_{z1,2}$ moves the corresponding zero without affecting the low-frequency portion of the PID response.

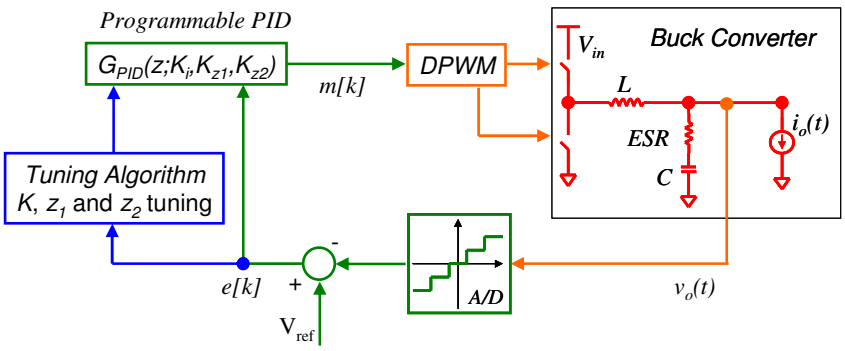

Fig. 5.1.2 – Voltage-mode digital control employing a self-tuning PID compensator

It is also worth to notice that the overall PID gain K_i in (5.1.1) is equal to the *integral gain* of the compensator in its non-interacting – or parallel – implementation (see Appendix A). Thus, the integral gain is directly available in form (5.1.1) and allows for simple no-limit cycling checks, according to the discussion carried out in Chapter II.

Similarly to what is done in the analog domain, it is useful to associate two frequencies f_{z1} and f_{z2} to the zeros z_1 and z_2. By applying the inverse Euler transformation to (5.1.1) one obtains an analog PID compensator with zeros located at:

$$f_{z1,2} \equiv \frac{f_s}{2\pi K_{z1,2}} \tag{5.1.3}$$

Equation (5.1.3) will be taken as *definition* of the frequencies associated to the digital PID zeros. It must be kept in mind, however, that $f_{z1,2}$ are not related to the magnitude and phase response of the compensator by the same relationships that hold for an analog system, the approximation being valid only for $f_z << f_s$. Please also note that $K_{z1,2}$ defines, to within a constant factor, the ratio between the switching frequency f_s and $f_{z1,2}$.

As shown in Fig. 5.1.2, during the autotuning process the tuning algorithm elaborates the digitized error signal *e[k]* and calculates (K_i, K_{z1}, K_{z2}) so that the resulting compensator will meet proper *stability* and *dynamic* constraints. Leaving the detailed description of the tuning process to the next section, the tuning targets will be now defined.

In particular, a *target phase margin* m_Φ^* will be assumed as a stability objective, while a target closed-loop bandwidth f_c^* will represent the dynamic objective.

As far as this latter tuning target is concerned, a first approach consists in choosing a fixed value for f_c^*, which thus becomes a tuning constant. This choice is suitable to guarantee the same dynamics regardless of the specific power stage characteristics.

As a second approach [52], rather than expressing f_c^* as an absolute value, it may be specified as a function of the resonant frequency f_0 of the power converter:

$$f_c^* \equiv \alpha f_0 , \tag{5.1.4}$$

with $\alpha > 1$. Equation (5.1.4) represents a possible criterion for dynamically selecting the target closed-loop bandwidth once f_0 is known. It therefore assumes that f_0 has been previously measured during the identification process. Details related to the identification of f_0 by means of the relay-feedback technique will be given in the next section.

The reasoning behind the empirical criterion expressed by (5.1.4) is based on a number of observations.When f_0 ranges over a wide interval, as may happen for the POL converters discussed in section 5.1.1, a constant f_c^* specification may lead to poor bandwidth optimization for high-f_0 power converters, while the design of high-bandwidth compensators for very low-f_0 power stages could be impractical and result in tuning failures. Moreover, a high-f_c, low-f_0 control design would probabily lead to limit cycle oscillations whenever a large integral gain is required by the digital compensator. Thus, in these conditions a possible approach is to relate f_c and f_0 through (5.1.4). Simulations and experimental tests point at $2 < \alpha < 4$ as a suitable range.

Care must be taken in applying (5.1.4) with extremely high-f_0 values, as the resulting target bandwidth could be a significant fraction of the switching frequency f_s. If $f_s/10$ is taken as an upper limit for the closed-loop bandwidth in a voltage-mode control, criterion (5.1.4) can be easily corrected to account for the switching frequency limit:

$$f_c^* \equiv \min(\alpha f_0, \frac{f_s}{10}) \tag{5.1.5}$$

Having formulated the tuning objectives, the proposed tuning algorithm can now be specified. Its flowchart is illustrated in Fig. 5.1.3. Three tuning phases are identified,

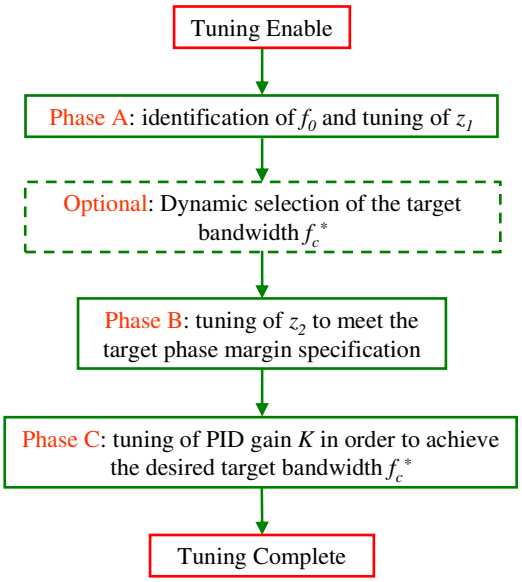

Fig. 5.1.3 – Flowchart of the proposed tuning algorithm

each of them associated to the tuning of one of the three PID parameters. The relay-feedback technique will be efficiently exploited for the tuning of the two PID zeros z_1 and z_2, with the purpose of achieving the target phase margin m_Φ^*. Details of phases A and B will be given in section 5.2.

As far as the PID gain K_i is concerned, a different tuning approach will be employed, based on a frequency injection method. Explained in section 5.3, this approach allows for accurate tuning of K_i in order to achieve the target closed-loop bandwidth f_c^*.

Please note that the flowchart illustrated in Fig. 5.1.3 can be extended to include no-limit cycling conditions as well as outer loops that allow for a finer selection of the closed-loop bandwidth. In this context, criterion (5.1.5) can be thought as a starting point for more sophisticated tuning approaches.

5.2. *Digital Relay-Feedback Autotuning*

Tuning techniques based on the relay-feedback concept are widely used in industrial controllers. The technique consists in inducing *amplitude-limited* oscillations in the feedback loop by introducing a strong nonlinearity in the loop itself. The nonlinear block used is a relay, i.e. a nonlinear system which outputs a constant positive or constant negative signal depending on the sign of its input. The frequency and the amplitude of the oscillation can be used to gain information on the plant under control and consequently choose the regulator parameters.

The use of the relay-feedback technique has been proposed as a viable approach for the self-tuning of digitally controlled SMPS in [51] and further investigated in [52-53]. This technique, defined as *digital relay-feedback autotuning*, will be now presented.

5.2.1. *Digital Relay Feedback Fundamentals*

Let us consider the voltage-mode scheme illustrated in Fig. 5.2.1. The closed-loop configuration during the tuning process of z_1 and z_2 is shown. The structure of the digital compensator consists of a non-linear part, which implements the relay function:

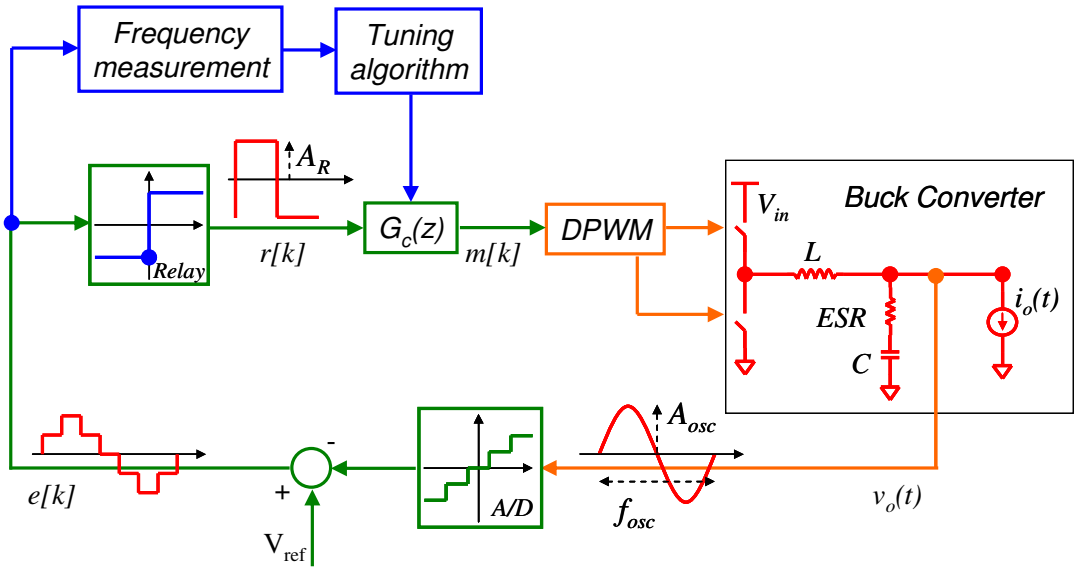

Fig. 5.2.1 – Block diagram of digital relay-feedback autotuning

$$r[k] = \begin{cases} +A_R, & e[k] > 0 \\ -A_R, & e[k] \le 0 \end{cases}, \tag{5.2.1}$$

where $A_R > 0$ is the amplitude of the relay output, and a linear part described by an ordinary linear difference equation:

$$m[k] = -\sum_{i=1}^{n} a_i m[k-i] + \sum_{j=0}^{m} b_j r[k-j], \qquad m \le n \tag{5.2.2a}$$

$$G_c(z) \equiv \frac{M(z)}{R(z)} = \frac{\sum_{j=0}^{m} b_j z^{-j}}{1 - \sum_{i=1}^{n} a_i z^{-i}} \tag{5.2.2.b}$$

The precise structure of (5.2.2) – i.e. its coefficients – depends on the particular tuning phase and will be explicited later on. For now, let us simply assume that (5.2.2) contains an integrating action, i.e. a pole at $z = 1$.

Under this assumption it is easy to realize that a limit cycle oscillation will arise in the system shown in Fig. 5.2.1. In fact, the action of the integrator is that of nulling whatever DC component is present in its input signal. However, from (5.2.1) it is seen that the relay output *cannot* be zero. Thus, *r[k]* must be oscillating between $+A_R$ and $-A_R$ with zero average value. We will further postulate that the oscillation at the output of the power converter is essentially sinusoidal, i.e. the filtering action of the power converter is strong enough to let only the fundamental frequency of *r[k]* pass, attenuating higher frequency harmonics. Under these assumptions, we shall denote with f_{osc} and A_{osc} the oscillating frequency and amplitude measured at the output of the power converter, as indicated in Fig. 5.2.1.

Formally, the above hypotheses allow us to analyse the system employing the *describing function* method. Let us denote with *T(z)* the *linear part* of the system's loop gain:

$$T(z) \equiv G_c(z)G_p(z), \tag{5.2.3}$$

where $G_p(z)$ is the equivalent z-domain control-to-output transfer function of the power converter, as defined in (2.3.7). For a persistent oscillation of amplitude A_{osc} and frequency f_{osc} to be sustained in the loop, the following fundamental equation has to be verified:

$$\frac{4A_R}{\pi A_{osc}} T(z)\Big|_{z=\exp(j2\pi f_{osc}^{*} T_s)} = -1 \tag{5.2.4}$$

The left-hand term represents the *non-linear loop gain*, defined as the product of (5.2.3) and the amplitude-dependent relay describing function $4A_R/(\pi A_{osc})$. Similarly to what happens when considering linear oscillators, (5.2.4) states that the system loop gain evaluated at the oscillating frequency has to present a unity magnitude and a 180° phase lag. Equation (5.2.4) is fundamental for understanding the relay-feedback concept. The key point to realize is that, for a given structure of the linear compensator (5.2.2), the oscillating frequency and amplitude implicitly defined by (5.2.4) *will depend on the power stage*. Thus, the oscillation frequency carries information on the power stage and its measurement can be used for identification and tuning purposes. The operation of the relay-feedback autotuner is that of measuring the oscillating frequency and consequently adjusting the compensator parameters until the tuning targets are met. The frequency measurement operation and the action of the tuning algorithm are also shown in Fig. 5.2.1. The *measure-and-tune* strategy employed by the relay-feedback autotuner interleaves the identification and tuning phases to achieve a continuous adjustment the the PID parameters. It differs from other tuning techniques in which identification and tuning phases are well-separated in time. From an implementation point of view, the frequency measurement block can be easily

implemented by means of counters and proper surrounding control logic. Please refer to section 5.4 for further details.

Before going through the details and showing how (5.2.4) is actually employed by the relay-based autotuner, it is important to point out some facts and approximations related to this important equation.

First, the nonlinear part of (5.2.4) apparently only accounts for the relay, while no contribution comes from the A/D quantizer. Actually, it is easy to realize that the cascade of a *n*-bit quantizer and a relay is, in turn, a relay. Thus, it is formally correct to neglect the A/D contribution. Seen from another point of view, one may think of having lumped the A/D quantizer and the relay block in an equivalent relay function. This intermediate step was not explicited in the present discussion.

An approximation has nevertheless been made in writing (5.2.4), and more precisely in writing the describing function of the relay block. Actually, $4A_R/(\pi A_{osc})$ is the describing function of an *analog* relay. The details and consequences of this modeling issue are not further investigated in this work.

Finally, in a practical implementation a small hysteresis band is going to be implemented in the relay function in order to eliminate noise-induced chatter. This introduces an amplitude-dependent phase lag in the relay describing function, not predicted by (5.2.4). The effects of the hysteresis-induced phase lag will be addressed later on.

5.2.2. *Phase A: Identification of the Resonant Frequency and Tuning of z_1*

Letting $G_c(z)$ be the transfer function of a pure digital integrator represents a straightforward way to identify the power converter resonant frequency. Let us then assume:

$$G_c(z) = \frac{1}{1 - z^{-1}} \tag{5.2.5}$$

By plugging (5.2.5) in (5.2.4) and taking the argument one obtains:

$$\arg[\frac{G_p(\exp(j2\pi f_{osc}T_s))}{1 - \exp(j2\pi f_{osc}T_s)}] = -180° \tag{5.2.6}$$

As long as the oscillating frequency is much lower than the converter switching frequency the product $f_{osc}T_s$ is very close to zero; by Taylor expansion of the denominator $1-\exp(j2\pi f_{osc}T_s)$ the following approximation can be made:

$$\arg[\frac{G_p(\exp(j2\pi f_{osc}T_s))}{1 - \exp(j2\pi f_{osc}T_s)}] \cong \arg[\frac{G_p(\exp(j2\pi f_{osc}T_s))}{j2\pi f_{osc}T_s}] = -180° \tag{5.2.7}$$

Thus:

$$\arg[G_p(\exp(j2\pi f_{osc}T_s))] \cong -90° \tag{5.2.8}$$

Equation (5.2.8) implies that the oscillating frequency is very close to f_0. For most practical cases one may assume:

$$f_{osc} \cong f_0 \tag{5.2.9}$$

Thus, when structure (5.2.5) is employed, the system oscillation will be at the power stage resonant frequency. Measurement of f_{osc} directly allows for the identification of f_0.

More generally, when the damping of the power coverter is significant, f_{osc} may result *higher* than the actual resonant frequency. Equation (5.2.8) nevertheless implies that the oscillation occurs where the process transfer function lags -90°:

$$f_{osc} = f_{-90°} \tag{5.2.10}$$

Independently on these details, the proposed tuning strategy for phase A is to place the first PID zero so that f_{z1} equals the identified frequency $f_{-90°}$:

$$f_{z1} = f_{-90°} \tag{5.2.11}$$

This tuning criterion (5.2.11) is simetimes employed in manual design. The zero z_1 introduces a phase boost where the power stage phase response starts dropping – i.e. at $f \approx f_0$ and beyond – without unnecessarily lowering the low-frequency magnitude of the loop gain. The remaining phase boost necessary to achieve the target phase margin will be provided by the second zero, z_2.

According to (5.1.3), the tuning of z_1 consists in selecting:

$$K_{z1} \leftarrow \frac{f_s}{2\pi f_{-90}} \tag{5.2.12}$$

It is important to point out that (5.2.12) only apparently involves a division. A counter-based frequency measurement directly outputs the ratio f_s/f_0, thus reducing assignment (5.2.12) to a multiplication by a constant. Further details will be given in section 5.4 when some aspects of the VHDL implementation of the autotuner will be discussed.

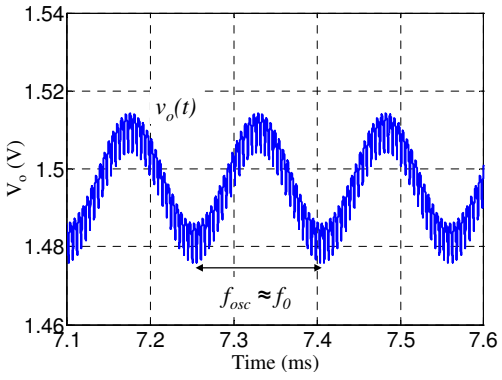

Fig. 5.2.2 – Output voltage perturbation during phase A

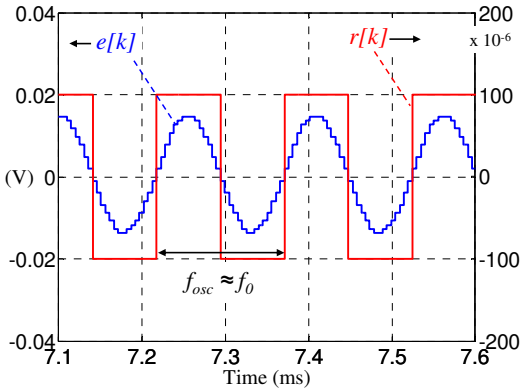

Fig. 5.2.3 – Error signal and relay output during phase A

The relay-feedback configuration shown in Fig. 5.2.1 has been modeled in the Matlab/Simulink environment and simulated on a 12V-to-1.5V buck coverter switched at f_s = 200 kHz and with L = 1μH, C = 600μF, ESR = 1mΩ. Simulation results for phase A are shown in Fig. 5.2.2, in which the output voltage oscillation is illustrated, and Fig. 5.2.3, in which the digitized error signal *e[k]* is superimposed to the relay output *r[k]*. The observed oscillating frequency is f_{osc} = 6.5 kHz, which correctly approaches the power stage resonant frequency.

As a last point, the identification of f_0 – or, more rigorously, of $f_{-90°}$ – allows the calculation of the target closed-loop bandwidth f_c^* whenever the dynamic bandwidth selection (5.1.5) is adopted.

5.2.3. *Phase B: Tuning of z_2 for the Target Phase Margin*

As previously mentioned, z_2 is tuned so that the target phase margin is obtained at the desired crossover frequency. This condition is expressed as follows:

$$\arg[T_{PID}(z)\big|_{z=\exp(j2\pi f_c^* T_s)}] = \theta_{PID}(f_c^*) + \theta_G(f_c^*) = -180° + m_\varphi^*, \tag{5.2.13}$$

where $T_{PID}(z)$ represents the system loop gain in its normal regulation state:

$$T_{PID}(z) \equiv G_{PID}(z) G_p(z) \tag{5.2.14}$$

and having defined $\theta_{PID}(f)$ and $\theta_G(f)$ as the phase responses of $G_{PID}(z)$ and $G_p(z)$ respectively.

It is important to realize the difference between (5.2.14), i.e. the loop gain *after* the tuning process has completed, and (5.2.3), i.e. the linear part of the loop gain *during* the relay-feedback operation.

The system configuration during phase B is the same used for phase A and depicted in Fig. 5.2.1, but with $G_c(z)$ defined as follows:

$$G_c(z) = G_{PID}(z) F(z), \tag{5.2.15}$$

with $G_{PID}(z)$ expressed by:

$$G_{PID}(z) = \frac{(1 + K_{z1} - K_{z1} z^{-1})(1 + K_{z2} - K_{z2} z^{-1})}{1 - z^{-1}} \tag{5.2.16}$$

and $F(z)$ defined as a digital low-pass filter, the role of which will be clear soon.

In (5.2.16) the parameter K_{z1} is given by (5.2.12), while K_{z2} is the parameter being tuned during this phase. A suitable *initial value* for K_{z2} is zero, which corresponds to a PI structure for $G_{PID}(z)$. Please note that the gain K_i is set to unity and it will be determined later on in the tuning process.

To understand how condition (5.2.13) can be realized by means of the relay-feedback configuration illustrated in Fig. 5.2.1, let us derive a phase equation from the fundamental relationship (5.2.4):

$$\arg[T(z)\big|_{z=\exp(j2\pi f_{osc}T_s)}] = \theta_{PID}(f_{osc}) + \theta_F(f_{osc}) + \theta_G(f_{osc}) = -180°, \qquad (5.2.17)$$

where θ_F denotes the phase response of *F(z)*. Equation (5.2.17) can be re-arranged in the following form:

$$\theta_{PID}(f_{osc}) + \theta_G(f_{osc}) = -180° + \left|\theta_F(f_{osc})\right| \qquad (5.2.18)$$

The left-hand term represents the phase response of T_{PID} evaluated at the oscillation frequency. This key point is rigorously true as long as the relay describing function is real. Comparison between (5.2.18) and (5.2.13) reveals the trick: if the system is forced to oscillate at $f_{osc} = f_c^*$ and as long as the lowpass filter *F(z)* is designed to introduce a phase lag $|\theta_F(f_c^*)| = m_\Phi^*$, then (5.2.18) *implies* (5.2.13). In other words, *the tuning of* z_2 *for a desired phase margin is equivalent to tune* z_2 *in order to force* $f_{osc} = f_c^*$.

Beside the constraint $|\theta_F(f_c^*)| = m_\Phi^*$, the structure of *F(z)* can be arbitrary. A single-pole or double pole structure is the common choice. Please note that whenever a dynamic bandwidth selection is employed, the filter *F(z)* has to be online-tuned, as f_c^* is not known a priori.

As long as the loop gain phase response is monotonic within the frequency range under consideration, the system oscillation can be driven to any desired value by a measure-and-tune strategy which detects the current oscillating frequency, compares it with the target value f_c^* and consequently adjusts K_{z2}. More precisely, whenever $f_{osc} > f_c^*$, f_{osc} can be decreased by lowering f_{z2}, i.e. increasing K_{z2}. Conversely, condition $f_{osc} < f_c^*$ can be handled by lowering K_{z2}. Thus, the tuning of z_2 only relies on frequency measurements followed by slight adjustments of a PID parameter.

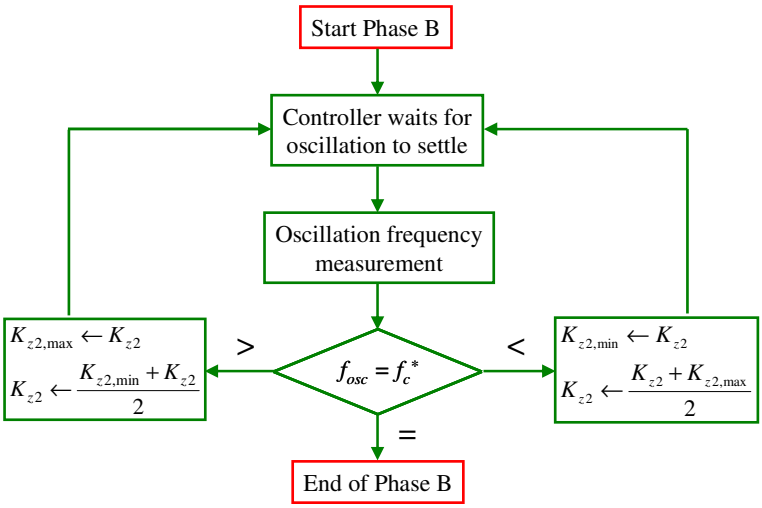

Fig. 5.2.4 – Bisection algorithm for the tuning of the second PID zero (phase B)

Different methods exist that correctly implement the positioning of z_2. A possibility is to evaluate the frequency error and let it be processed by a digital integrator that acts on K_{z2}. Another approach is the *bisection method*, illustrated in Fig. 5.2.4 in a flowchart form. This method can be thought as a binary search algorithm that converges to the target oscillation frequency by iteratively splitting in two the allowed range for K_{z2}.

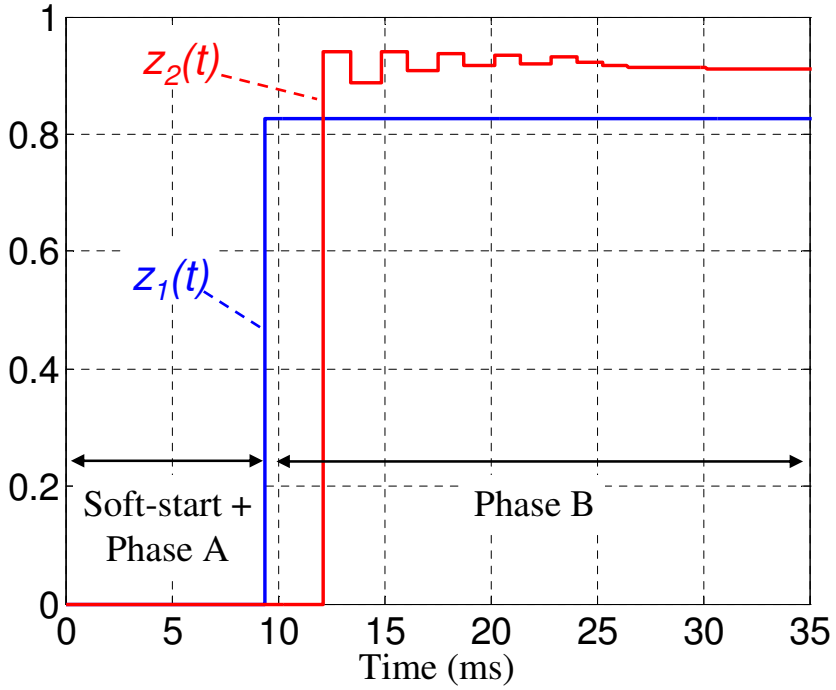

Fig. 5.2.5 – Tuning of the two PID zeros (phases A and B)

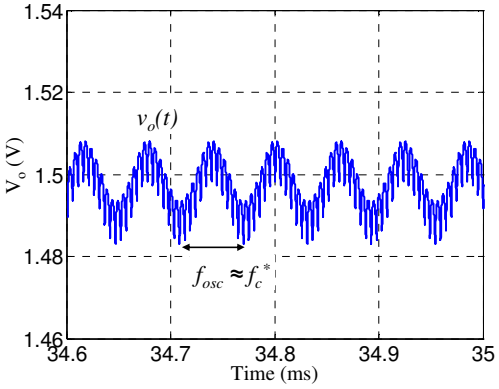

Fig. 5.2.6 – Output voltage perturbation at the end of phase B

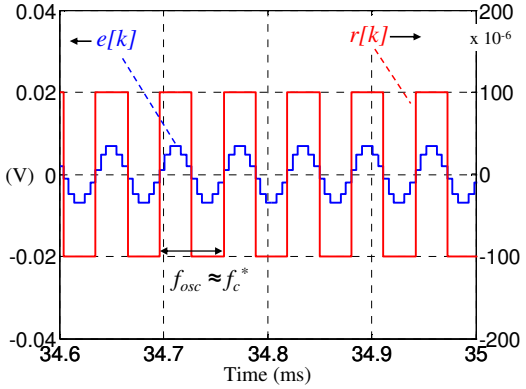

Fig. 5.2.7 – Error signal and relay output at the end of phase B

Again, this method relies on the measurement of the oscillation frequency and consequent comparison with the target value f_c^*. The algorithm terminates when the upper and lower bounds of K_{z2} are sufficiently close one to another. The implementation of the bisection method is particularly hardware-efficient and thus well-suited for hardwired logic realizations.

Simulation results of the tuning of z_1 and z_2 are shown in Fig. 5.2.5 for the same converter considered in the previous section. For this simulation the tuning targets were set to $f_c^* = 16.3$ kHz and $m_\Phi^* = 50°$.

After the soft-start phase, in which the output voltage ramps up to the regulation band, the system enables the tuning process with phase A, which terminates with the positioning of z_1 according to (5.2.12). Phase B is then initiated with the compensator in a PI configuration – i.e. $z_2 = 0$, or $K_{z2} = 0$ – and the lowpass filter inserted in the feedback loop. The iterative adjustment of z_2 by hand of the bisection algorithm can be appreciated in Fig. 5.2.5. Phase B lasts until the measured oscillation frequency equals the target closed-loop bandwidth, according to the discussion carried out in this section.

The output voltage oscillation *at the end* of phase B is illustrated in Fig. 5.2.6, from which the oscillation frequency is correctly observed at $f_{osc} = 16.3$ kHz. The error signal *e[k]* and the relay output *r[k]* during the same time interval are shown in Fig. 5.2.7.

Please note how the output voltage oscillation maintains a rather good sinusoidal shape even at $f_{osc} = f_c^*$, this being a fundamental hypothesis on which (5.2.4) relies.

As far as the output voltage amplitude is concerned, simulation results shown in Fig. 5.2.2 and 5.2.6 point out how A_{osc} tends to decrease as the tuning proceeds, the intuitive reason being that the higher is the oscillation frequency, the stronger is the filtering action of the power converter. The value of A_{osc} is essentially determined by the power stage parameters and by the relay output amplitude A_R. An interesting property of the proposed tuning is that it does rely solely on *frequency* measurements. Thus, A_{osc} can be kept as low as desired as long as the oscillating frequency is measured correctly. For the same reason quantization of the output voltage does not significantly impact the tuning results. Simulations shown in Fig. 5.2.2 – 5.2.7 were carried out with a quantization step set to $\Delta q_v \approx 1\text{mV}$. The important subject of limiting A_{osc} is discussed in the next section.

5.2.4. Limitation of the Output Voltage Perturbation

When supplying loads requiring tight voltage regulation, perturbations that exceed the specified regulation band are not allowed. A tuning perturbation not respecting this condition may induce operation failures if not permanent damage in the load.

As far as the relay-feedback tuning presented in the previous sections is concerned, an effective way to limit the oscillation amplitude A_{osc} is to properly select the relay output amplitude A_R. Worst-case calculations will be now presented that allow for the determination of the maximum allowed A_R that keeps A_{osc} below some predefined value $A_{osc,max}$.

It is easy to realize that the worst-case condition occurs during phase A, i.e. when the power stage is oscillating close to its resonant frequency f_0. This is physically intuitive, as the power stage tends to enhance any frequency close to its resonance. Formally, $f_{osc} \approx f_0$ places the oscillation close to the resonance peak in the magnitude response of the linear loop gain T. From (5.2.4), this condition maximizes A_{osc}. Let us write (5.2.4) taking the magnitude of the left-hand and right-hand terms:

$$\frac{4A_R}{\pi A_{osc}} \frac{1}{\omega_0 T_s} QV_{in} = 1, \tag{5.2.19}$$

where expression (5.2.5) was used for $G_c(z)$, along with the low-frequency approximation $f_{osc}T_s << 1$. This same low-frequency approximation was used to approximate the z-domain control-to-output transfer function $G_p(z)$ at $f \approx f_0$ as the product of the power stage quality factor Q and the input voltage V_{in}.

From (5.2.19) an letting $A_{osc} < A_{osc,max}$ one obtains:

$$A_R < \frac{\pi}{4} A_{osc,\max} \frac{\omega_0}{Q} \frac{1}{f_s V_{in}} \tag{5.2.20}$$

From (5.2.20) a worst-case design for A_R can be derived as long as the minimum value assumed by the ratio ω_0/Q can be estimated. An example will be proposed here, assuming that Q is limited solely by the inductor and capacitor equivalent series resistances r_L and ESR. In this case the following approximation holds:

$$\frac{\omega_0}{Q} \cong \frac{\frac{1}{\sqrt{LC}}}{\frac{1}{r_L + ESR}\sqrt{\frac{L}{C}}} = \frac{r_L + ESR}{L} \tag{5.2.21}$$

Thus, from (5.2.20), the following worst-case design criterion for A_R is obtained:

$$A_{R,\max} = \frac{\pi}{4} A_{osc,\max} \frac{r_{L,\min} + ESR_{\min}}{L_{\max}} \frac{1}{f_s V_{in,\max}} \tag{5.2.22}$$

Please note that (5.2.21) is an extremely conservative estimation, which makes (5.2.22) a somewhat restrictive upper bound for A_R. Additional damping sources like the load, on-resistances of the power switches and gate driving dead times would probably allow for larger values of A_R.

As a numerical example, the 12V-to-1.5V synchronous buck converter simulated in the previous sections had $Q \approx 1.9$. If a maximum ±3% output voltage perturbation is allowed, then from (6.2.20) one obtains $A_{R,max} = 300 \cdot 10^{-6}$. Simulations shown in Fig. 5.2.2 – 5.2.7 were carried out with $A_R = 100 \cdot 10^{-6}$. The oscillation amplitude is effectively limited well within the tolerance band specification, as visible from Fig. 5.2.2 and Fig. 5.2.6.

5.3. *Phase C: PID Gain Tuning via Frequency Injection*

The relay-feedback technique presented in section 5.2 has been employed to tune the two zeros of the PID compensator. Tuning of z_1 and z_2 according to the proposed strategies only involved frequency measurements and thus found straightforward implementation with the relay-based method.

As far as the tuning of the PID gain K_i is concerned, its value has to be determined in order to bring the crossover frequency f_c of the system to its target value f_c^*. This process involves the measurement – directly or indirectly – of the loop gain magnitude at $f = f_c^*$ and, in turn, of the oscillation amplitude at some point along the feedback path.

In [52], K_i was found by approximate calculations based on assumptions about the shape of the loop-gain magnitude response. An alternative, more robust approach presented in [53] is introduced in this section.

5.3.1. *Frequency Injection Method*

The closed-loop configuration during phase C is shown in Fig. 5.3.1. The relay block and the lowpass filter used during phase B have been removed from the loop. The PID compensator has its zeros now placed, and its gain K_i represents the remaining

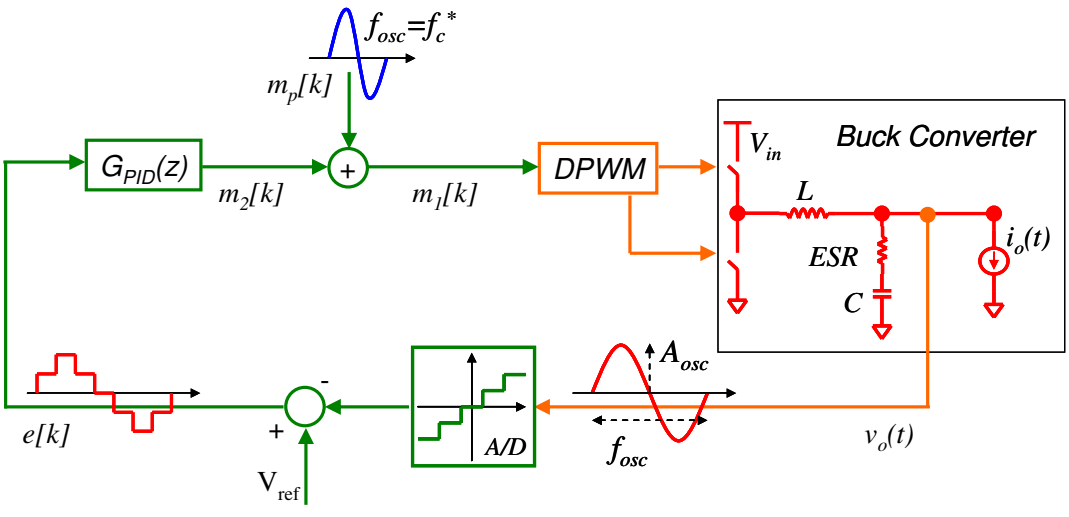

Fig. 5.3.1 – Frequency injection method

untuned parameter. At the beginning of Phase C K_i is brought to an initial value K_{i0} low enough to ensure a stable, low-bandwidth condition.

In this configuration, a sinusoidal perturbation signal $m_p[k]$ oscillating at $f = f_c^*$ and with amplitude Δm_p is superimposed to the PID output sequence $m_2[k]$ to form the actual modulating signal, which we shall indicate with $m_1[k]$:

$$m_1[k] = m_2[k] + m_p[k] = m_2[k] + \Delta m_p \sin(2\pi f_c^* T_s \cdot k) \qquad (5.3.1)$$

As long as quantization effects occurring in the A/D conversion and in the DPWM modulation can be neglected, the linearity of the system implies that m_1 and m_2 are also sinusoidal signals. Moreover, as a single frequency is being injected in the system, a phasor representation will be used to develop the analysis. Denoted with $\hat{m}_1[k]$ and $\hat{m}_2[k]$ the ac sinusoidal components of $m_1[k]$ and $m_2[k]$ respectively, let M_1 and M_2 be the corresponding phasors. Straightforward block diagram analysis can be used to derive the phasor relationship between M_1 and M_2:

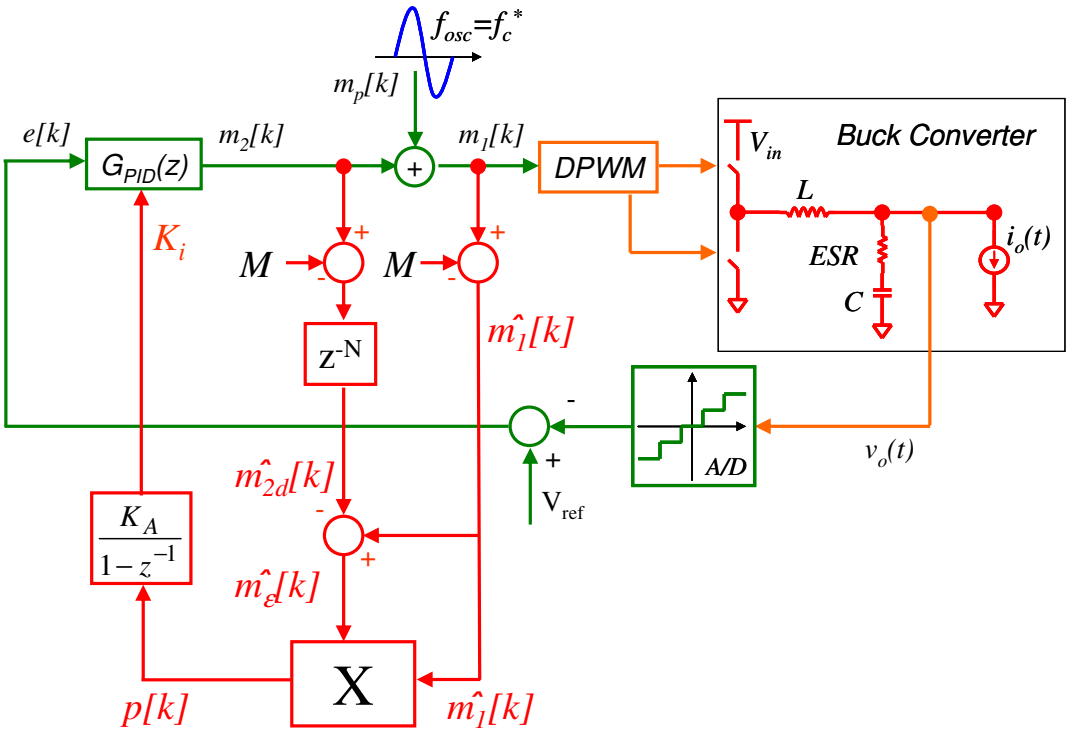

Fig. 5.3.2 – PID gain tuning via frequency injection (phase C)

$$\frac{M_2}{M_1} = -T_{PID}(z)\Big|_{z=\exp(j2\pi f_c^* T_s)} = A_T \exp(jm_\varphi^*), \tag{5.3.2}$$

where A_T denotes the magnitude of the loop gain at $f = f_c^*$. The phase relationship between M_1 and M_2 is the result of tuning phases A and B, after which the PID zeros are positioned to yield the target phase margin m_Φ^* at the desired crossover frequency. As far as the loop gain magnitude A_T is concerned, its initial value is less than one; the objective of phase C is to achieve $A_T = 1$ through proper adjustment of K_i.

The tuning process, illustrated in Fig. 5.3.2, works as follows: ac signals $\hat{m}_1[k]$ and $\hat{m}_2[k]$ are sensed by measuring $m_1[k]$ and $m_2[k]$ and successivley subtracting their common DC component M. Signal $\hat{m}_2[k]$ is then delayed by m_Φ^* degrees. The delayed signal $\hat{m}_{2,d}[k]$ is thus in phase with respect to $\hat{m}_1[k]$, as implied by (5.3.2). An error signal $m_\varepsilon[k]$ is then calculated as $\hat{m}_\varepsilon[k] = \hat{m}_1[k] - \hat{m}_{2,d}[k]$. In phasor representation:

$$M_\varepsilon \equiv M_1 - M_2 \exp(-jm_\varphi^*) \tag{5.3.3}$$

Combining (5.3.2) with (5.3.3) yields:

$$M_\varepsilon \equiv M_1(1 - A_T) \tag{5.3.4}$$

Equation (5.3.4) states that M_ε is a measure of the tuning error, i.e. how far is A_T from unity. The phasor diagram in Fig. 5.3.3 gives a graphical description of (5.3.2) through (5.3.4).

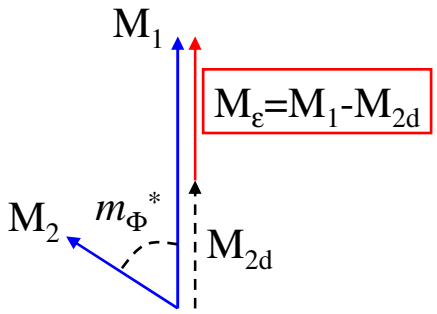

Fig. 5.3.3 – Phasor diagram for signals $\hat{m}_1$, $\hat{m}_2$, $\hat{m}_{2d}$ and $\hat{m}_\varepsilon$

A time-domain multiplication between $\hat{m}_1[k]$ and $\hat{m}_\varepsilon[k]$ is then performed:

$$p[k] \equiv \hat{m}_1[k] \cdot \hat{m}_\varepsilon[k] = (1 - A_T)\hat{m}_1^2[k] \tag{5.3.5}$$

The product defined by $p[k]$ contains a DC component proportional to the tuning error ($1-A_T$). To see this it is sufficient to average both sides of (5.3.5):

$$< p >= (1 - A_T)\left\|M_1\right\|^2 \tag{5.3.6}$$

A digital integrator, shown in Fig. 5.3.2, performs the tuning by processing $p[k]$ and forcing $<p>$ to zero by properly adjusting K_i. The tuning is completed when a steady state condition is reached in which $\|M_1\| = \|M_2\|$, and thus $A_T = 1$. The tuning speed is determined by the gain K_A of the tuning integrator. As usual when adjusting a compensator parameter, the action of K_A should be slow enough not to interfere with the compensator regulating function.

Results for phase C on the simulation case study examined in the previous sections are shown in Fig. 5.3.4, where the signals $\hat{m}_1[k]$ and $\hat{m}_2[k]$ are illustrated. Please note how the amplitude of $\hat{m}_2[k]$, initially small because $A_T < 1$, gradually increases as the tuning proceeds. The phase shift between the two signals shows how $\hat{m}_2$ actually *leads* $\hat{m}_1$ by $m_\Phi^* = 50°$, according to (5.3.2). The time-domain waveform of the PID gain $K_i(t)$

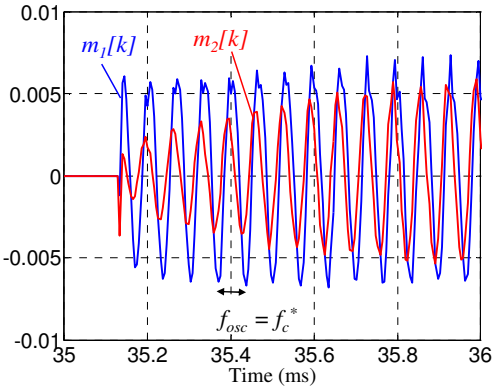

Fig. 5.3.4 – Time domain waveforms for $\hat{m}_1$ and $\hat{m}_2$ during phase C

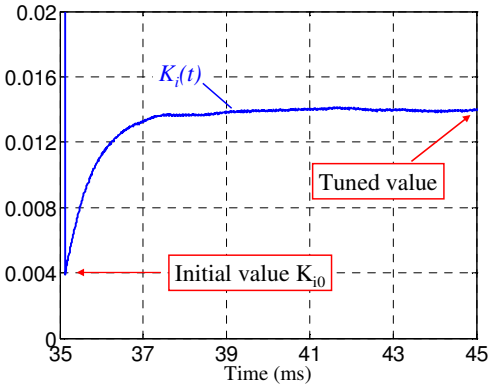

Fig. 5.3.5 – Time-domain waveform for the PID gain during phase C

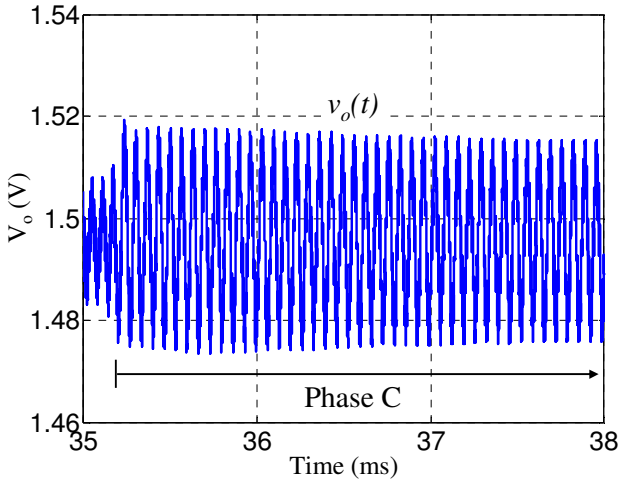

Fig. 5.3.6 – Output voltage perturbation during phase C

is illustrated in Fig. 5.3.5. When phase C starts K_i is brought to a safe level K_{i0}; the tuning integrator is then enabled. The output voltage waveform is shown in Fig. 5.3.6 during the first couple of milliseconds after phase C has begun. The oscillation amplitude is now limited by the amplitude Δm_p of the perturbation signal m_p. Worst-case considerations similar to those discussed in the previous section are necessary to ensure safe limitation of A_{osc} during the tuning process. For the simulation results shown in Fig. 5.3.4 through 5.3.6, $\Delta m_p = 5 \cdot 10^{-3}$ was used.

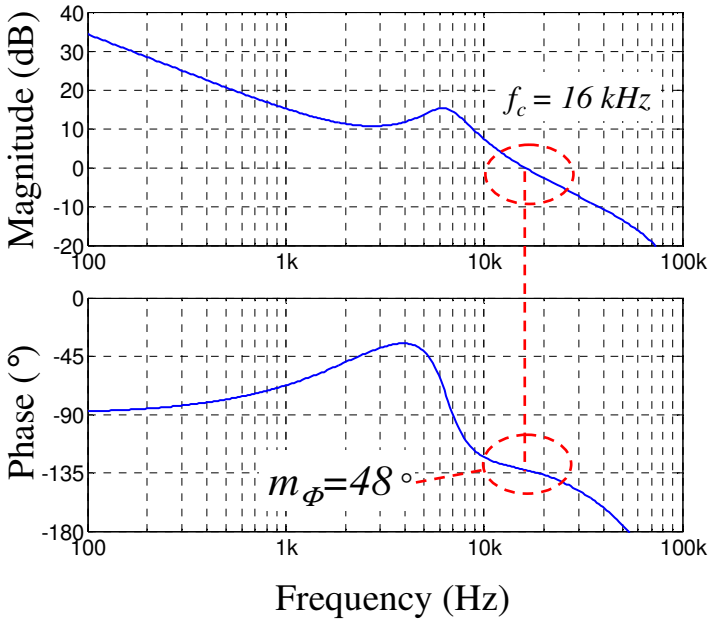

Fig. 5.3.7 – Post-tuning loop gain

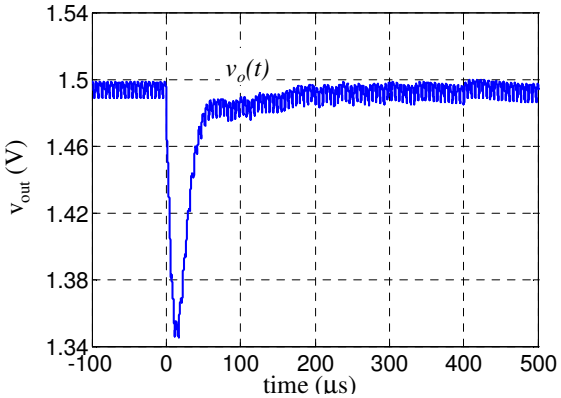

Fig. 5.3.8 - Post-tuning 0→10A load transient

The post-tuning loop gain of the system is shown in Fig. 5.3.7. Both the phase margin and the closed-loop bandwidth specifications are met with high accuracy; the simulated post-tuning 0→10A load transient shown in Fig. 5.3.8 exhibits dynamics and damping in agreement with the specified tuning targets.

5.3.2. Accuracy and Implementation Issues

A couple of points need to be briefly analysed concerning the accuracy of the tuning process in achieving a target closed-loop bandwidth as well as slight modifications of the basic scheme of Fig. 5.3.2 aimed to more hardware-efficient implementations.

i. Delay Error on $\hat{m}_2[k]$

The multiplication between $\hat{m}_\varepsilon[k]$ and $\hat{m}_1[k]$ can be viewed as a projection of the first signal onto the direction defined by the latter. Indeed, the DC component of the product $p[k]$ given by (5.3.5) can be written as:

$$< p >= \|M_1\| \cdot \|M_\varepsilon\| \cos(\Delta\varphi_\varepsilon)\,, \tag{5.3.7}$$

where $\Delta\varphi_\varepsilon$ represents whatever phase difference exists between $\hat{m}_\varepsilon$ and $\hat{m}_1$. Quantity (5.3.7) is the scalar product between phasors M_1 and M_ε. For this reason, whatever phase error exists between $\hat{m}_\varepsilon$ and $\hat{m}_1$, a *tuning error* on f_c will result.

In the previous description of the tuning algorithm employed during phase C it was implicitly assumed that the signals $\hat{m}_{2d}[k]$ and $\hat{m}_1[k]$ were exactly in phase. However, as digital sequences can be delayed by only integer multiples of the sampling period, a *delay error* will always occur, causing $\hat{m}_{2d}[k]$ to be out of phase with respect to $\hat{m}_1[k]$. In turn, the error phasor M_ε will present a non-zero component along the direction orthogonal to M_1. Formally, if $\Delta\varphi$ represents the delay error between $\hat{m}_{2d}[k]$ and $\hat{m}_1[k]$, then (5.3.4) becomes:

$$M_\varepsilon = M_1(1 - A_T \exp(-j\Delta\varphi)) \tag{5.3.8}$$

Substituting (5.3.8) in (5.3.7) yields:

$$< p >= \sqrt{2}\left\|M_1\right\|^2 \cos(\Delta\varphi_\varepsilon)\sqrt{1 - A_T \cos(\Delta\varphi)} \tag{5.3.9}$$

Thus, the tuning integrator will force (5.3.9) to zero by adjusting K_i until:

$$A_T = \frac{1}{\cos(\Delta\varphi)} \tag{5.3.10}$$

Equation (5.3.10) represents the tuning error in terms of the loop gain magnitude at $f = f_c^*$; as a worst case estimation, a delay error corresponding to $\pm 0.5 \cdot T_s$ at $f_c^* = f_s/10$ yields $\Delta\varphi \approx 18°$. The corresponding tuning error $\Delta f_c/f_c$ on the closed-loop bandwidth can be roughly estimated by assuming a -20dB/decade slope of the loop gain magnitude around $f = f_c$, which yields $\Delta f_c/f_c \approx 5\%$. This result points to a surprisingly accurate tuning even in presence of large delay errors. Though the present calculation only accounts for time quantization, neglecting amplitude quantization effects coming into play, the results can be considered representative of the good accuracy of the proposed approach.

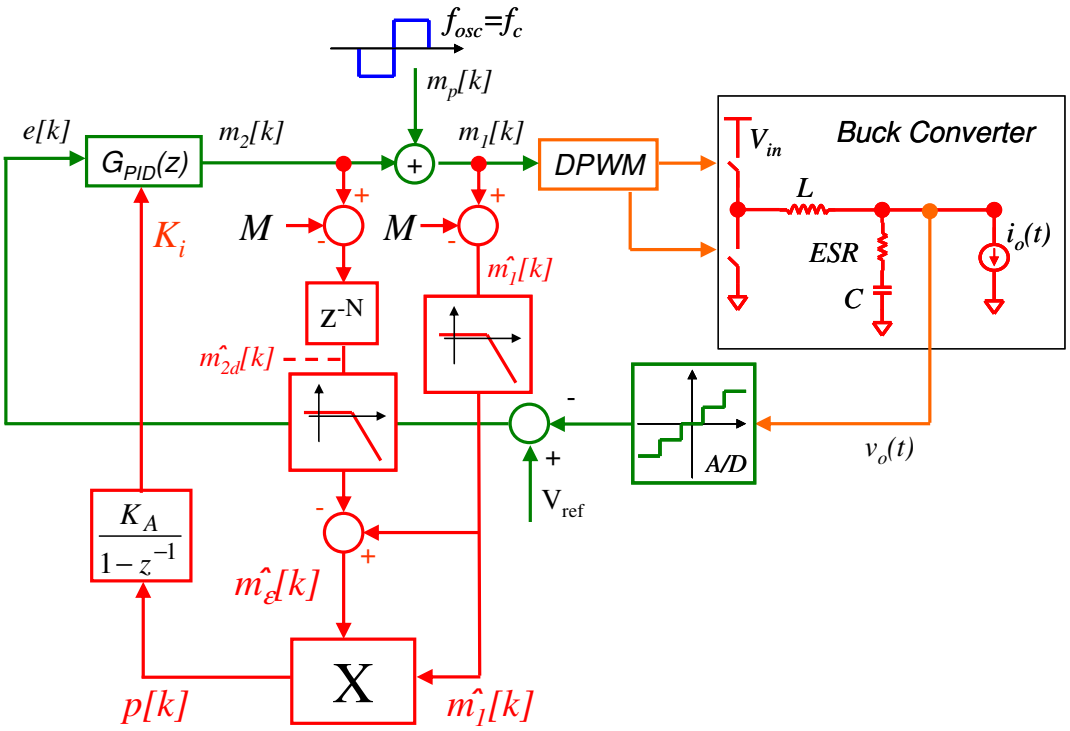

Fig. 5.3.9 – Square-wave injection scheme

ii. Square-Wave Perturbation

The single-frequency injection scheme of Fig. 5.3.1 has been used to present the concept of the proposed tuning method. However, its implementation requires the generation of the sinusoidal signal $\hat{m}_p[k]$ and may thus involve the use of look-up tables. Moreover, whenever the target bandwidth f_c^* is dynamically selected, proper digital circuitry has to be provided to synthesize the correct perturbation frequency. More hardware-effective implementations can be achieved with other perturbation waveforms. Square waves or triangular waves are easily generated and can be

C	f_c^*	m_Φ^*	f_c	m_Φ	$\Delta f_c/f_c$	$\Delta m_\Phi/m_\Phi$
	(kHz)		(kHz)			
600µF	16.3	50°	16.3	47.2°	0%	-5.6%
1mF	12.9	50°	12.5	49.7°	-3.1%	-0.6%
3mF	7.4	50°	7.5	49.1°	1.4%	-1.8%
10mF	4.4	50°	4.6	51.9°	4.5%	-3.8%

Tab. 5.1 – Tuning simulations with square-wave injection (ESR=1mΩ)

conveniently used. A square-wave injection scheme is provided in Fig. 5.3.9. The tuning process is by all means similar to the one already described. The difference lies in that we are now dealing with a multiple-frequency injection, as the square-wave harmonics contribute in perturbing the system. The phasor analysis presented previously no longer holds – or it can be applied to the fundamental frequency only – and the harmonic distortion of $\hat{m}_p[k]$ contributes to an additional tuning error. Indeed, when $\hat{m}_1[k]$ and $\hat{m}_\varepsilon[k]$ are multiplied, the average value of $p[k]$ is affected by the entire spectrum of the two factors and not only by their fundamental frequency. A possible provision is to reduce the harmonic content of $\hat{m}_1[k]$ and $\hat{m}_{2d}[k]$ through two identical digital filters, as shown in Fig. 5.3.9.

Simulations were carried out with this modified version of the autotuner. The 12V-to-1.5V buck converter previously examined was considered, and simulations were performed for different values of the output capacitance C. Tuning targets were set to $m_\Phi^* = 50°$ and $f_c^* = 2.5 \cdot f_0$. A square-wave perturbation was used during phase C, with amplitude $\Delta m_p = 5 \cdot 10^{-3}$. First-order digital lowpass filters tuned at 10kHz were employed along the tuning feedback path. Table 5.1 reports the tuning results, showing an overall good accuracy over more than one order of magnitude in the variation of the output capacitance.

5.4. Implementation Details and Experimental Results

The tuning algorithm described through sections 5.2 and 5.3 has been experimentally tested on a 12V-to-1.5V, 10A synchronous buck converter prototype. The converter was operated at $f_s \approx 195$ kHz ($T_s = 5.12$ µs); the phase inductance was $L = 1$ µH, while the filter capacitance was $C = 600$ µF, composed by both ceramic and tantalum electrolytic caps. Power stage board included signal conditioning circuitry as well as 12-bit, 4V full scale range A/D converters, for a voltage quantization step $\Delta q_{v,AD} \approx 1$mV.

The control and tuning hardware were entirely VHDL-coded and implemented on a Xilinx FPGA development board based on a Virtex-4 device. A 12-bit trailing edge modulator was employed, with a time resolution $\Delta q_t = 1.25$ ns. The programmable digital PID was realized in the cascade form (5.1.1) with 16-bit internal registers. Tuning phases A, B and C were sequenced by a main finite-state-machine (FSM), while local FSMs were employed for the algorithmics of each phase. The control and tuning VHDL code was synthesized and implemented using Xilinx ISE environment, for an

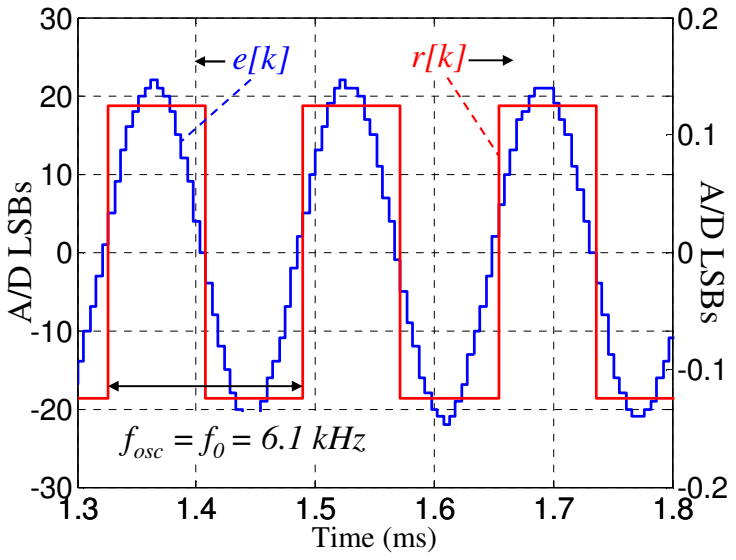

Fig. 5.3.10 – Experimental error signal and relay output during phase A

about 18,000 equivalent gates design.

For the experimental tests the tuning targets were set to $f_c^* = 16.3$ kHz and $m_\Phi^* = 50°$; in Fig. 5.3.10 the experimental error sequence *e[k]* is illustrated along with the relay output *r[k]* during phase A of the tuning process. These waveforms, as well as the one that will be illustrated later on, have been acquired using the Xilinx Chipscope debugging tool, which allowed for an on-line acquisition of digital signals from the FPGA during the tuning process.

Both the waveforms shown in Fig. 5.3.10 are expressed in terms of A/D LSB units. The relay amplitude has been set to $A_R \approx 122 \cdot 10^{-6}$, i.e. 1/8 of the A/D LSB. With this choice the output voltage oscillation amplitude is found to be $A_{osc} \approx 20$ mV, i.e. 1.3% of the regulation value. The oscillation frequency is measured by a counter clocked at the switching frequency which is enabled by the tuning algorithm and frozen after a fixed number N_{osc} of system oscillation cycles, detected by the zero crossings of the relay waveform *r[k]*. The measurement of the oscillating frequency f_{osc} is represented by the number N_s of counted switching clock cycles. With this technique extremely hardware-effective implementations are achieved that ensure accurate frequency measurements. In the autotuner implementation $N_{osc} = 16$ was used, which yields a worst-case resolution of about 120 Hz at $f_{osc} = f_s/10 = 19.5$ kHz, more than enough for the tuning purposes. With a 12-bit counter, frequencies down to 760 Hz can be measured.

The oscillation frequency measured during phase A is 6.1 kHz, as illustrated in Fig. 5.3.10. From the discussion carried out in section 5.2, this also represents the converter resonant frequency f_0. The measured value slightly differs from the theoretical one – about 6.5 kHz – calculated using nominal *L* and *C* mainly because of component tolerances. Off-board measurements on the buck phase inductor pointed at *L* close to 1.2 μH, which would yield $f_0 = 5.9$ kHz. Taking into account the slight difference

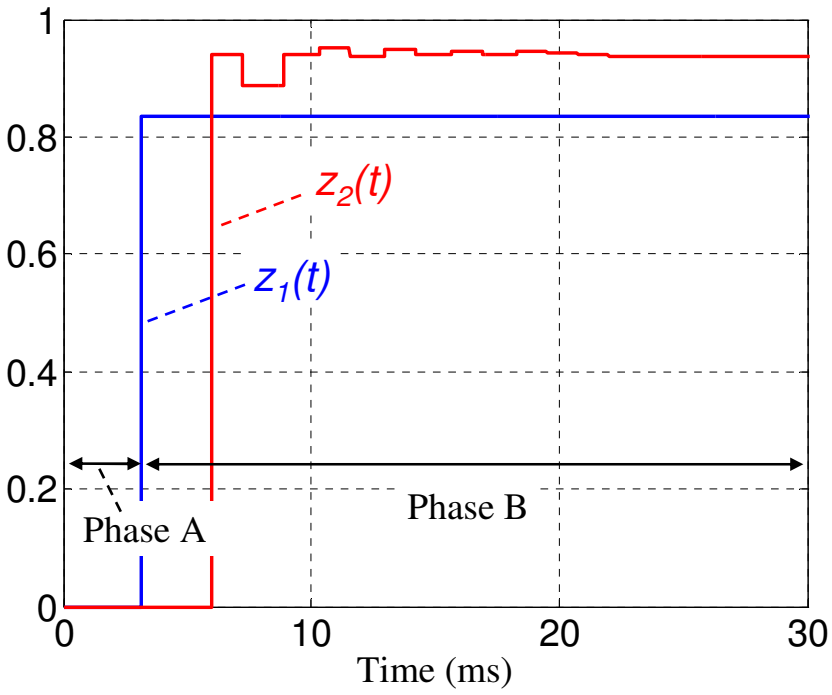

Fig. 5.3.11 – Experimental tuning of the two PID zeros (phases A and B)

between f_{-90} and f_0 discussed in section 5.2, the measured value of 6.1 kHz appears by all means reasonable. A further evidence will be provided later on when showing the experimental post-tuning loop gains.

Experimental waveforms of the PID zeros during phases A and B are shown in Fig. 5.3.11. The first zero is positioned according to (5.2.12) as soon as f_0 is measured. Then,

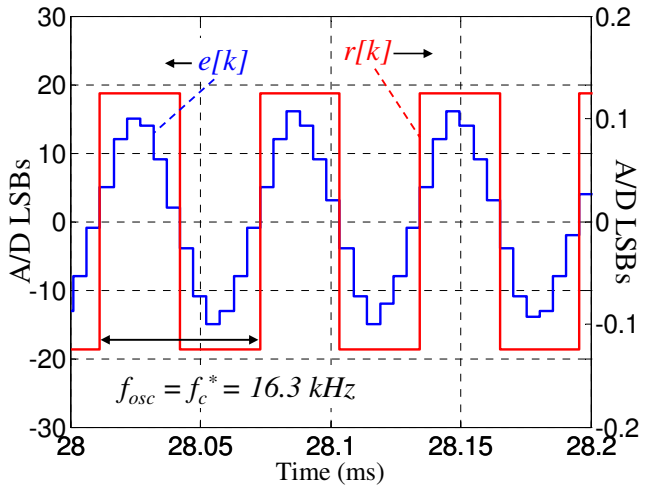

Fig. 5.3.12 – Experimental error signal and relay output at the end of phase B

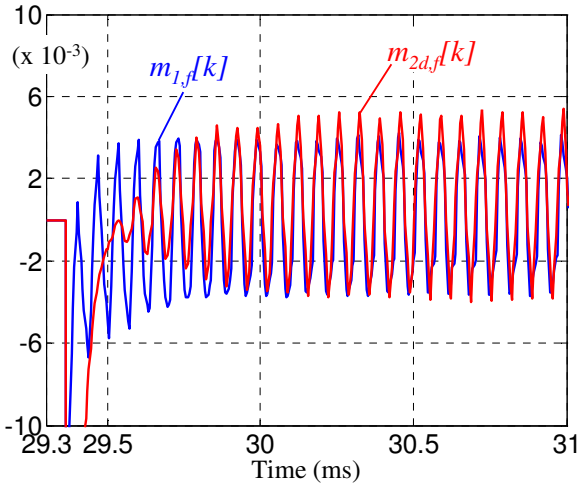

Fig. 5.3.13 – Experimental waveforms for $m_{1,f}$ and $m_{2d,f}$ during phase C

during phase B the bisection algorithm iteratively adjusts z_2 until the system oscillation frequency is equal to f_c^*. This latter point is illustrated in Fig. 5.3.12, which shows the error and relay waveforms at the end of phase B. The oscillating frequency, measured through the same counter-based technique described previously, is equal to f_c^* = 16.3 kHz, as expected.

After the tuning of z_1 and z_2, phase C is started. In the VHDL implementation the square-wave injection method illustrated in Fig. 5.3.9 was implemented, with the amplitude of the perturbation set to $10 \cdot 10^{-3}$. Reduction of the harmonic content of

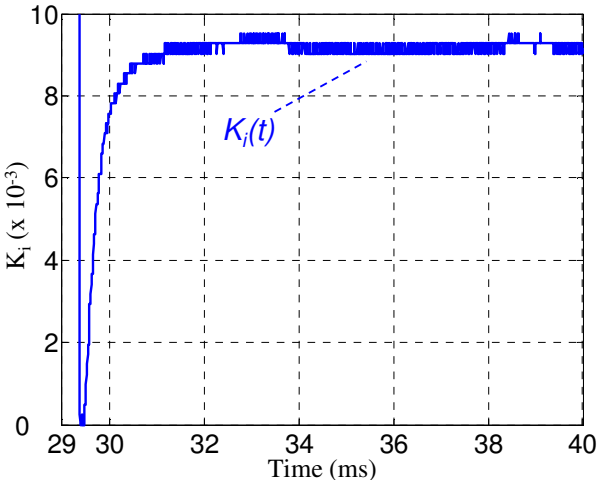

Fig. 5.3.14 – Experimental waveform for the PID gain K_i during phase C

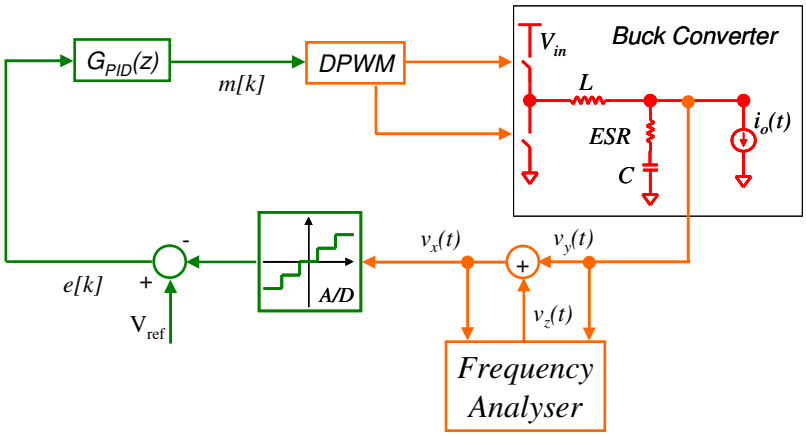

Fig. 5.3.15 – Voltage injection method for loop gain measurements

signals $\hat{m}_1[k]$ and $\hat{m}_{2d}[k]$ was accomplished through two identical first-order filters tuned at 5 kHz. Experimental waveforms of the filtered signals $m_{1,f}[k]$ and $m_{2d,f}[k]$ during phase C are shown in Fig. 5.3.13. The amplitudes of the two signals rapidly converge to the same value through the action of the tuning integrator. In the HDL implementation, K_A = 15 was used. The experimental waveform for the PID gain K_i is finally illustrated in Fig. 5.3.14, from which a settling time of few milliseconds can be appreciated.

Post-tuning performances of the system were investigated through loop gain and transient response measurements. As far as the loop gain measurement is concerned, the voltage injection method illustrated in Fig. 5.3.15 was employed [115], which allows for the loop gain to be measured in closed-loop configuration. A frequency analyser was used to perturb the system through injection of an AC voltage signal v_z; the amplitude and phase relationship between signals v_y and v_x located before and after the injection point were then measured. The experimental loop gain is then defined as:

$$T_{\exp}(f) \equiv -\frac{v_y(f)}{v_x(f)} \tag{5.3.11}$$

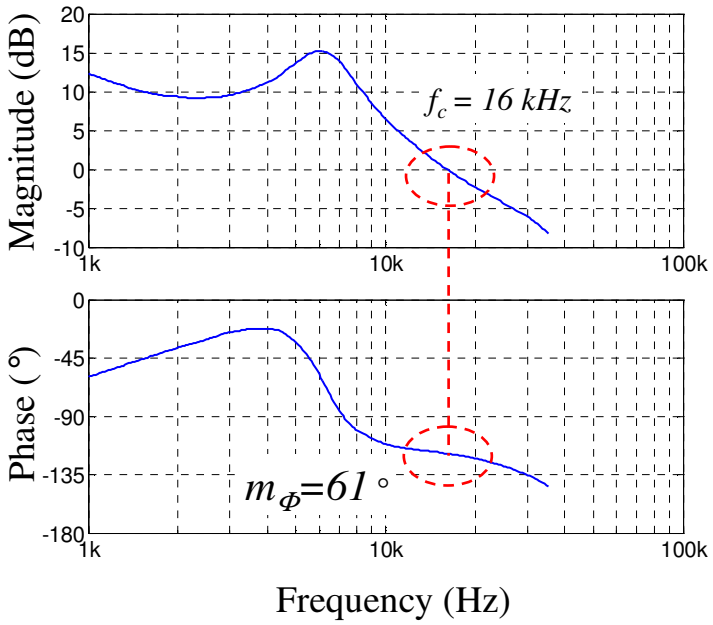

Fig. 5.3.16 – Experimental post-tuning loop gain

The perturbation frequency f was swept from 1 kHz to about 30kHz. Bode diagrams of the experimental loop gain (5.3.11) are shown in Fig. 5.3.16. The system exhibits a closed-loop crossover frequency f_c = 16 kHz, with a phase margin m_Φ = 61°. The excess of phase margin with respect to the target value of 50° is explainable by the relay hysteresis. Indeed, in the HDL implementation of the relay a small hysterisis band equal

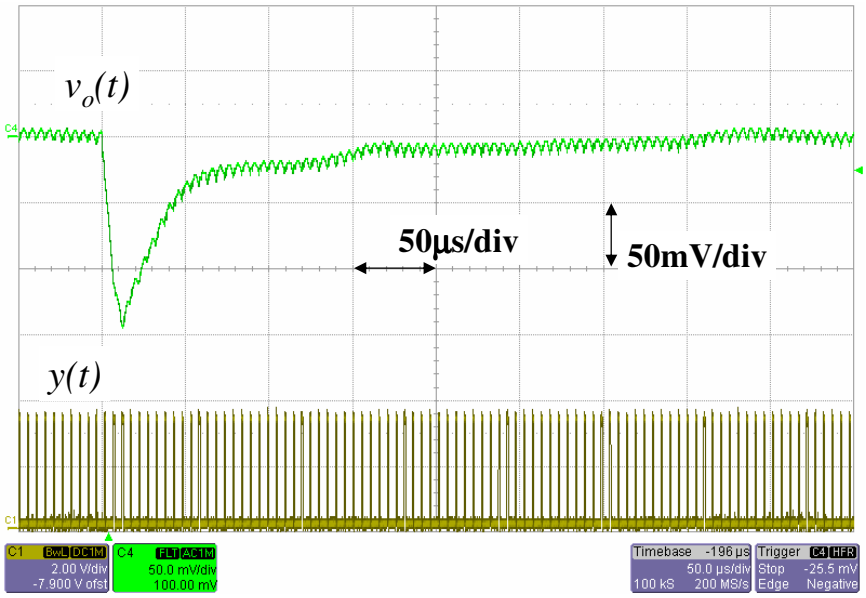

Fig. 5.3.17 – Experimental post-tuning 0→9A load step response; v_o 50mV/div, y 2V/div, time 50µs/div

to ±2LSBs was used to reduce noise-induced chatter and obtain a clean oscillating waveform. The presence of the hysteresis band introduces a phase lag in the relay describing function. Thus, the tuning of the PID zero z_2 operated by the bisection method compensates for an additional phase lag not present during normal system operation. This additional term in (5.2.17) results in the observed excess of phase margin. Please note that this phenomenon does not compromise stability, since the phase margin deviation is always positive. Whenever a precise phase margin has to be obtained, the hysteresis effect can be quantified and compensated by targeting for a somewhat smaller m_Φ^*.

The experimental transient response of the converter to a 0→9A load step change is illustrated in Fig. 5.3.17. The damping and recovery time of the transient agree with the designed bandwidth and phase margin.

The tuning was then performed with the input voltage decreased by 20% with respect to its nominal value. Experimental loop gain and transient response for V_{in} = 9.6V are shown in Fig. 5.3.18 and 5.3.19 respectively. Comparison with Fig. 5.3.16 and

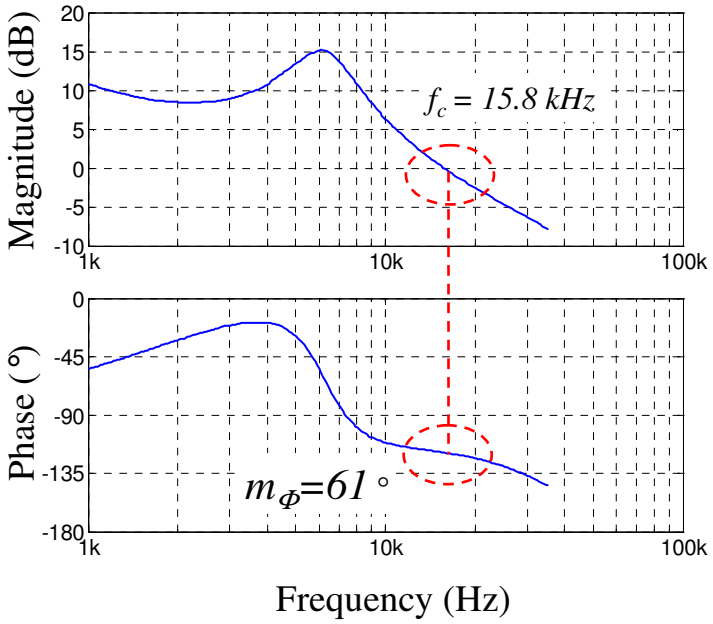

Fig. 5.3.18 – Experimental post-tuning loop gain, V_{in} = 9.6V

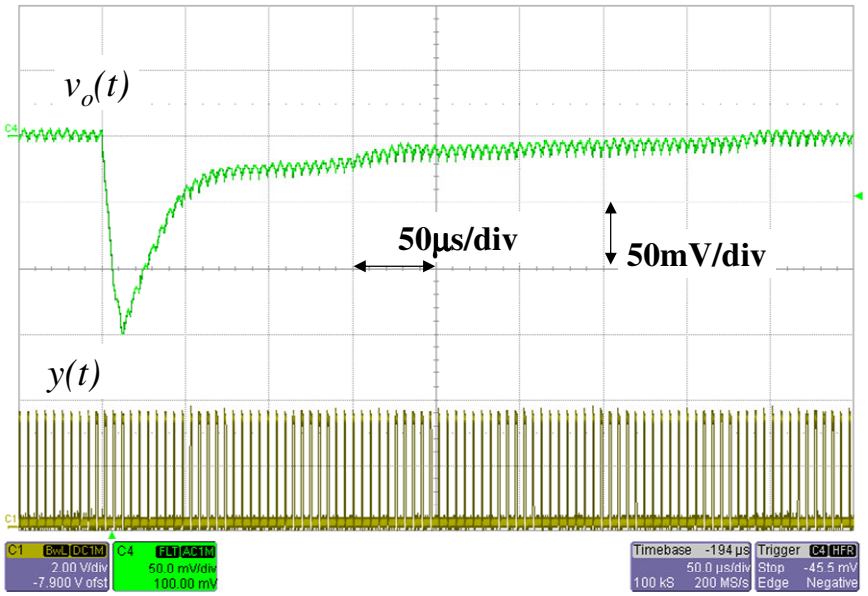

Fig. 5.3.19 – Experimental post-tuning 0→9A load step response, V_{in} = 9.6V; v_o 50mV/div, y 2V/div, time 50µs/div

5.3.17 reveals the same stability margins and dynamic characteristics, proving that the tuning approach correctly handled the decreased input voltage by converging to a higher compensator gain, keeping the same locations for the PID zeros.

Chapter VI

Conclusions and Future Work

This work investigated two main topics related to the digital control of switched mode power supplies. Dynamic performances of digital control loops for SMPS have been shown to gain great ehancements in terms of achievable bandwidth from an increased sampling frequency. Such multi-sampled systems approach performances of analog solutions, still retaining the robustness and versatility of digital controllers. An in-depth modeling discussion has been presented which addressed the small-signal and steady-state large signal behavior of multi-sampled converters. The main drawback of the increased sampling frequency was identified as the injection of switching harmonics into the feedback loop, which causes nonlinear effects to arise in the DPWM behavior. Solutions aimed to restore the PWM linearity have been presented and validated through computer simulations and experimental tests, proving their effectiveness.

As a second topic, a specific autotuning technique based on the digital relay feedback approach was discussed and presented in its analytical and implementation details. The approach was successfully validated through experimental tests on a FPGA-

controlled prototype Point-of-Load converter and via HDL coding of the control and tuning hardware. Accurate and repeatable tuning results were achieved with limited hardware requirements.

Future research lines which would naturally follow the studies proposed in this work may address modeling aspects of quantization effects in multi-sampled systems. The subject appears to be particularly interesting in that it is not clear whether or not the increased sampling frequency may help in reducing limit cycle oscillations and quantization-related phenomena.

Further research in the field of self-tuning of digital compensators may lead to the formulation of more sophisticated tuning algorithms which may account for no-limit cycle conditions, “smart” dynamic selection of the control bandwidth as well as strategies for complete periodic online self-calibration of the controller. These aspects, not necessarily related to a specific tuning technique, are of extreme importance from an industrial point of view, as would allow the definition of robust, intelligent controllers able to safely operate the system in a broad range of environmental conditions.

Appendix A

Digital PID Compensators

A.1 Analog PID Compensators

Proportional-Integral-Derivative (PID) compensators are well known and widespread in the world of analog control design for their versatilty, easy-to-implement and easy-to-tune features. Analog PIDs are briefly recalled in this section before treating digital PID compensators.

An analog PID compensator processes a continuous-time *error signal e(t)* and produces a continuous-time *control signal m(t)*, which is the superposition of three terms:

$$m(t) = m_p(t) + m_i(t) + m_d(t), \tag{A.1.1}$$

where:

$$
\begin{aligned}
m_p(t) &= K_p^{'} e(t) \\
m_i(t) &= m_i(0) + K_i^{'} \int_0^t e(\tau) d\tau \\
m_d(t) &= K_d^{'} \frac{de}{dt}
\end{aligned}
\tag{A.1.2}
$$

That is, the control signal *m(t)* contains a term *proportional* to the error signal, a term proportional to the *integral* of *e(t)*, and a term proportional to the *derivative* of *e(t)*. The three constants K_p', K_i' and K_d' are defined as the proportional, integral and derivative gains respectively.

Taking the Laplace transform of (A.1.1) allows the derivation of the additive form of the PID transfer function, which explicitly highlights the three contributions to the control signal:

$$
G_c(s) \equiv \frac{M(s)}{E(s)} = K_p^{'} + \frac{K_i^{'}}{s} + K_d^{'} s\,, \tag{A.1.3}
$$

The triplet ($K_p^{'}$, $K_i^{'}$, $K_d^{'}$) uniquely defines the shape of the PID frequency response and is determined by the design constraints dictated by the specific application.

Equation (A.1.3) is also known as the *non-interacting* form of the PID transfer function, as it suggests a *parallel* implementation of the compensator where the three gains can be adjusted independently. The *interacting* form, which can be associated to a *series* implementation of the compensator, has the following expression:

$$
G_c(s) = K^{'} \frac{(1 + \frac{s}{\omega_{z1}})(1 + \frac{s}{\omega_{z2}})}{s}\,, \tag{A.1.4}
$$

in which the *Bode gain* $K^{'}$ and the frequencies ω_{z1} and ω_{z2} associated to the compensator zeros are explicited. As (3) and (4) indeed describe the same system, the following relationships hold between the two triplets (K_p', K_i', K_d') and (K', ω_{z1}, ω_{z2}):

$$
\begin{aligned}
K^{'} &= K_i^{'} \\
\omega_{z1} &= \frac{K_p^{'}}{2K_d^{'}}\left(1-\sqrt{1-\frac{4K_i^{'}K_d^{'}}{K_p^{'\,2}}}\right), \\
\omega_{z2} &= \frac{K_p^{'}}{2K_d^{'}}\left(1+\sqrt{1-\frac{4K_i^{'}K_d^{'}}{K_p^{'\,2}}}\right)
\end{aligned}
\tag{A.1.5a}
$$

$$
\begin{aligned}
K_p^{'} &= K^{'}\left(\frac{1}{\omega_{z1}}+\frac{1}{\omega_{z2}}\right) \\
K_i^{'} &= K^{'} \\
K_d^{'} &= \frac{K^{'}}{\omega_{z1}\omega_{z2}}
\end{aligned}
\tag{A.1.5b}
$$

where two real zeros were assumed, with $\omega_{z1}<\omega_{z2}$. Whenever $4K_i^{'}K_d^{'}/K_p^{'2}>1$, two complex conjugate zeros are obtained. The *interacting* nature of the form (A.1.4) is expressed by Eq. (A.1.5b), from which it is clear how the PID zeros affect *both* the proportional and derivative actions. Interestingly, the overall PID gain $K^{'}$ in the series form is equal to the integral gain $K_i^{'}$ in the parallel representation.

Simplified relationships between (K_p', K_i', K_d') and ($K^{'}$, ω_{z1}, ω_{z2}) can be found assuming two real and well-separated zeros, i.e. $\omega_{z1}<<\omega_{z2}$. Under this assumption, the following approximated relationships are obtained:

$$
\begin{aligned}
K^{'} &= K_i^{'} \\
\omega_{z1} &\cong \frac{K_i^{'}}{K_p^{'}} \\
\omega_{z2} &\cong \frac{K_p^{'}}{K_d^{'}}
\end{aligned}
\tag{A.1.6}
$$

Thus, for a given proportional gain, the low-frequency zero depends on the integral gain, while the derivative gain defines the position of the high-frequency zero. On the other hand, increasing the proportional gain tends to further separate the two zeros, moving ω_{z1} to lower frequencies and pushing ω_{z2} at higher frequencies.

Analog PID compensators are typically implemented employing one or more *operational amplifiers* with passive feedback R-C networks. In integrated analog controllers an *on-chip* error amplifier is usually found, and the compensator transfer function is often shaped by the control designer through external resistors and capacitors. Finally, in every analog application additional poles are present that limit the high-frequency gain of the compensator and ensure a proper filtering action at frequencies beyond the designed crossover frequency.

A.2 Discrete-Time PID Compensators

A *discrete-time* PID compesator processes a discrete time error sequence *e[kT]* and produces a discrete time control signal *m[kT]*, where *T* is the sampling period.

Discrete-time PID compensators can be formally derived by discretization of their analog counterparts. Let us apply, for instance, the *backward Euler* discretization method $s = (1-z^{-1})/T$ and derive the non-interacting (parallel) form of a discrete-time PID from (3):

$$G_c(z) \equiv \frac{M(z)}{E(z)} = K_p + \frac{K_i}{1-z^{-1}} + K_d(1-z^{-1}), \qquad \text{(A.2.1)}$$

where K_p, K_i and K_d are the discrete-time counterparts of the three analog PID gains K_p', K_i' and K_d':

$$\begin{aligned} K_p &= K_p' \\ K_i &= K_i' T \\ K_d &= \frac{K_d'}{T} \end{aligned} \qquad \text{(A.2.2)}$$

In the time domain, the control signal *m[kT]* is again decomposed in three terms:

$$m[kT] = m_p[kT] + m_i[kT] + m_d[kT], \qquad \text{(A.2.3)}$$

with:

$$\begin{aligned} m_p[kT] &= K_p e[kT] \\ m_i[kT] &= m_i[(k-1)T] + K_i e[kT] \\ m_d[kT] &= K_d\,(e[kT] - e[(k-1)T]) \end{aligned} \tag{A.2.4}$$

From (A.2.2) it can be observed that the integral and derivative gains both depend on the sampling period T: for a given desired *analog* integral action, the discrete-time integral gain K_i will scale with the sampling period; similarly, the discrete-time derivative gain K_d will scale inversely with the sampling period for a given desired *analog* derivative action.

The interacting (series) form of a discrete-time PID transfer function can be obtained from (A.1.4) and still applying the backward Euler discretization rule:

$$G_c(z) = \frac{K}{1-z^{-1}} \frac{(1-z_1 z^{-1})(1-z_2 z^{-1})}{(1-z_1)(1-z_2)}, \tag{A.2.5}$$

where:

$$\begin{aligned} K &= K' T \\ z_{1,2} &= \frac{1}{1+\omega_{z1,2} T} \end{aligned} \tag{A.2.6}$$

As in the case of analog PID compensators, each of the two forms (A.2.1) and (A.2.5) is uniquely defined by three parameters; the following relationships exist between (K_p, K_i, K_d) and (K, z_1, z_2) that allow to switch from the parallel form to the series form and viceversa:

$$\begin{aligned} K &= K_i \\ z_1 &= \frac{K_p + 2K_d}{2(K_p + K_i + K_d)} \left(1 + \sqrt{1 - \frac{4K_d(K_p + K_i + K_d)}{(K_p + 2K_d)^2}}\right) \\ z_2 &= \frac{K_p + 2K_d}{2(K_p + K_i + K_d)} \left(1 - \sqrt{1 - \frac{4K_d(K_p + K_i + K_d)}{(K_p + 2K_d)^2}}\right) \end{aligned} \tag{A.2.7a}$$

$$K_p = K\frac{z_1 + z_2 - 2z_1 z_2}{(1-z_1)(1-z_2)}$$
$$K_i = K \qquad \text{(A.2.7b)}$$
$$K_d = K\frac{z_1 z_2}{(1-z_1)(1-z_2)}$$

The discrete-time PID transfer functions (A.2.1) and (A.2.5) have been here derived by discretization from their analog counterparts; this approach provides an intuitive link to the analog domain that helps in gaining better insight on the behavior of discrete-time PIDs. However, this should not lead to the conclusion that the *design* of a discrete-time PID compensator should start from an analog PID and then derive the discrete-time regulator by discretization. A more rigorous approach is to design discrete-time PIDs *directly in the digital domain*, provided a discrete-time equivalent of the plant is available.

Appendix B

Steady-State Analysis of Multisampled PWMs Mathematical Details

A.1 The function $I_h(t_{1n})$

The behavior of the function $I_h(t_{1n})$ defined in (4.2.58.b) and here reported:

$$I_h(t_{1n}) \equiv \int_{t_{1n}}^{t_{1n}+D} s_h(\tau;t_{1n})d\tau = m_h(t_{1n}+D) - m_h(t_{1n}) \qquad \text{(A.1.1)}$$

is continuous except for $t_{1n} = q_N[t_{1n}]$ or $t_{1n}+D = q_N[t_{1n}+D]$, i.e. when the turn-on or turn-off instants (or both) coincide with a sampling event. With the exception of these critical points, the continuity of (A.1.1) is ensured by the regularity of the function $s_h(\cdot,t_{1n})$ and will not be questioned any further in this work.

As long as the critical points of (A.1.1) are concerned, it will be now shown that these represent negative discontinuities for $I_h(t_{1n})$ if proper hypotheses, verified in all cases of practical interests, are assumed.

Let us consider the behavior of the modulating signal $m_h(t_n)$ in the neighbourhood of the turn-on instant t_{1n}, shown in Fig. A.1.1.a. The figure represents a critical condition,

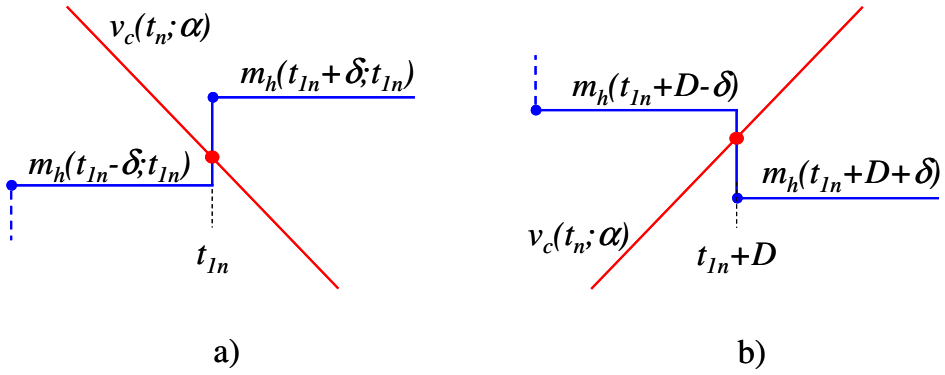

Fig. A.1.1 – Critical turn-on (a) and turn-off (b) events

i.e. $t_{1n} = q_N[t_{1n}]$. In all cases of practical interest, the condition $m_h(t_{1n}+\delta) \geq m_h(t_{1n}-\delta)$ is satisfied – with $0 < \delta < 1/N$ – while it is clear that the opposite situation, i.e. $m_h(t_{1n}+\delta) < m_h(t_{1n}-\delta)$, would not be compatible with a turn-on event generated by a negative-slope carrier. For similar reasons, a critical turn-off event $t_{1n}+D = q_N[t_{1n}+D]$ is characterized by the condition $m_h(t_{1n}+D+\delta) \leq m_h(t_{1n}+D-\delta)$, as illustrated in Fig. A.1.1.b. These conditions will be taken as general properties of the modulating signal $m_h(t_n;t_{1n})$:

$$\begin{cases} m_h(t_{1n}+\delta;t_{1n}) \geq m_h(t_{1n}-\delta;t_{1n}) \\ m_h(t_{1n}+D+\delta;t_{1n}) \leq m_h(t_{1n}+D-\delta;t_{1n}) \end{cases} \tag{A.1.2}$$

If we focus on a critical turn-on event $t_{1n} = q_N[t_{1n}]$, the variation ΔI_{h1} of (A.1.1) from $t_{1n}-\delta$ to $t_{1n}+\delta$ is:

$$\begin{aligned} \Delta I_{h1} &\equiv I_h(t_{1n}+\delta) - I_h(t_{1n}-\delta) = \\ &= m_h(t_{1n}-\delta) - m_h(t_{1n}+\delta) \leq 0 \end{aligned} \tag{A.1.3.a}$$

Thus, ΔI_{h1} is a negative discontinuity for I_h. The same holds for discontinuities associated with critical turn-off events $t_{1n}+D = q_N[t_{1n}+D]$:

$$\begin{aligned} \Delta I_{h2} &\equiv I_h(t_{1n}+\delta) - I_h(t_{1n}-\delta) = \\ &= m_h(t_{1n}+D+\delta) - m_h(t_{1n}+D-\delta) \leq 0 \end{aligned} \tag{A.1.3.b}$$

Equations (A.1.3) prove that (A.1.1) exhibits negative discontinuities for both critical turn-on and turn-off events.

A.2 The function $f_h(t_{1n})$

The function $f_h(t_{1n})$ was defined in (4.2.58.a) as:

$$f_h(t_{1n}) \equiv v_c(t_{1n}) - v_c(t_{1n} + D) + I_h(t_{1n}) \tag{A.2.1}$$

Lke (A.1.1), f_h exhibits a regular behavior with the exception of some critical points, which f_h inherits from I_h.

It is possible to show that f_h is a monotonically decreasing function of t_{1n}. In fact, as long as regular points are cosidered:

$$\frac{df_h}{dt_{1n}} = -\frac{1}{\alpha(1-\alpha)} + \frac{dI_h}{dt_{1n}} \tag{A.2.2}$$

The α-dependent term in the right-hand side of (A.2.2) is associated with the carrier waveshape, and more precisely to its slopes. The term dI_h/dt_{1n} is instead originated from the shape variation of $m_h(t_n;t_{1n})$ as the turn-on instant t_{1n} is varied, or, equivalently, as the sampling instants are shifted in time. An alternative expression can be given for (A.2.2) if I_h is written in terms of the *average* slope of m_h during the turn-on time D:

$$I_h(t_{1n}) = D \cdot < s_h > (t_{1n}) \tag{A.2.3}$$

From (A.2.3), derivative (A.2.2) is written in this form:

$$\frac{df_h}{dt_{1n}} = -\frac{1}{\alpha(1-\alpha)} + D\frac{d < s_h >}{dt_{1n}} \tag{A.2.4}$$

In all cases of practical interest the average slope during the turn-on time is a slowly varying function of t_{1n}, and the main contributor to the variation of f_h comes from the carrier waveshape. thus, (A.2.2) is negative and f_h is monotonically decreasing.

When critical points are considered, f_h inherits the negative discontinuities of I_h and preserves its negative monotonicity.

Let us now suppose that t_{1n}^* represents the steady-state turn-on event of a pulse-width modulator operating at a duty cycle D, and let us analyse the behavior of f_h in the neighbourhood of t_{1n}^*. Four possible situations can arise, depending on how the modulating signal intersects the carrier:

a) Neither t_{1n}^* nor t_{1n}^*+D coincide with a sampling instant

b) $t_{1n}^*+D= q_N[t_{1n}^*+D]$ but $t_{1n}^* \neq q_N[t_{1n}^*]$

c) $t_{1n}^* = q_N[t_{1n}^*]$, but $t_{1n}^*+D \neq q_N[t_{1n}^*+D]$

d) Both t_{1n}^* and t_{1n}^*+D coincide with sampling instants, i.e. $t_{1n}^* = q_N[t_{1n}^*]$ and $t_{1n}^*+D = q_N[t_{1n}^*+D]$

In case a) the modulating signal and the carrier exhibit horizontal crossings for both the turn-on and the turn-off event: $m_h(t_{1n}^*) = v_c(t_{1n}^*)$ and $m_h(t_{1n}^*+D) = v_c(t_{1n}^*+D)$. Hence:

$$f_h(t_{1n}^*) = 0 \qquad \text{(A.2.5)}$$

Thus, when no vertical crossing occurs, the steady-state solution of the modulator corresponds to the zero of the function f_h.

Case b) corresponds to a horizontal turn-on crossing and a vertical turn-off crossing. This means that $m_h(t_{1n}^*) = v_c(t_{1n}^*)$, but $m_h(t_{1n}^*+D+\delta) \leq v_c(t_{1n}^*+D)$. The latter inequality is graphically represented in Fig. A.1.1.b, where it is evident how the carrier must lie above the modulating signal if a critical turn-off event is considered. Evaluation of f_h then yields:

$$f_h(t_{1n}^*) = v_c(t_{1n}^*) - v_c(t_{1n}^* + D) + m_h(t_{1n}^* + D) - m_h(t_{1n}^*) \geq 0\,, \qquad \text{(A.2.6.a)}$$

On the other hand, evaluation of f_h at $t_{1n} = t_{1n}^* + \delta$ yields a negative result:

$$f_h(t_{1n}^* + \delta) = f_h(t_{1n}^*) + \Delta I_{h2} = \\ = -\frac{\delta}{\alpha(1-\alpha)} + m_h(t_{1n}^* + D + \delta) - v_c(t_{1n}^* + D) \le 0 \qquad \text{(A.2.6.b)}$$

Thus, t_{1n}^* corresponds to the *zero-crossing* of f_h. A similar reasoning can be carried out for case c), i.e. when $m_h(t_{1n}^*+D) = v_c(t_{1n}^*+D)$ but $m_h(t_{1n}^* - \delta) \le v_c(t_{1n}^*)$. In this case:

$$f_h(t_{1n}^*) = v_c(t_{1n}^*) - v_c(t_{1n}^* + D) + m_h(t_{1n}^* + D) - m_h(t_{1n}^*) \le 0\,, \qquad \text{(A.2.7.a)}$$

while a positive value is found in $t_{1n} = t_{1n}^* - \delta$:

$$f_h(t_{1n}^* - \delta) = f_h(t_{1n}^*) - \Delta I_{h1} = \\ + \frac{\delta}{\alpha(1-\alpha)} + v_c(t_{1n}^*) - m_h(t_{1n}^* - \delta) \ge 0 \qquad \text{(A.2.7.b)}$$

Again, the steady-state solution is found at the zero-crossing of the function f_h. Case d) can be treated in a similar way as cases b) and c), yielding the same conclusion.

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