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Analysis and design of CMOS and bipolar SiGe:C integrated circuits for low power RF receivers and radar applications

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Abstract

This dissertation proposes the analysis and the design of two radio-frequency integrated circuits.

In the first part a low-power wireless receiver front-end for Wireless Sensor Networks is developed. The circuit comprises a Low-Noise Amplifier, Voltage Controlled Oscillators and Mixers, building a complete single-stage quadrature receiver front-end for low-power applications. The compact architecture based on a current reuse topology is described and motivated; an in-depth time-variant analysis is performed to optimize the circuit; a test 2.4 GHz receiver is finally designed and realized in a cheap 90 nm CMOS technology with a 3 μm thick top metal for high-quality integrated inductors. Measurement results confirm the correctness of our analysis and the validity of the proposed circuit architecture.

In the second part of this dissertation a X-band upconverter for a Frequency-Modulated Continuous-Wave radar system is developed. The goal of the project is that of developing a wideband upconverter with a clean output spectrum and low phase noise. The proposed architecture is constituted by two mixers, baseband interfaces, a pre-power amplifier and the on-chip circuitry to generate quadrature local oscillator signals from an external reference local oscillator. Several mechanisms which lead to spurious tones at the output are discussed, with emphasis on the design issues related to the image-rejection, the mismatches and the nonlinearities in the large-signal baseband interface. Two versions of the modulator are designed and compared: a) a CMOS version built in a 65 nm digital technology based on a zero DC current passive mixer for minimum flicker noise and b) a bipolar version built in a 0.35 μm SiGe:C technology based on an active Gilbert mixer.

Sommario

Questa tesi di dottorato propone l'analisi e la progettazione di due circuiti integrati a radio-frequenza.

Nella prima parte del lavoro viene sviluppato il front-end di un ricevitore wireless a basso consumo di potenza per Wireless Sensor Networks. Il circuito, che comprende un amplificatore a basso rumore, oscillatori locali e mixer, costituisce un sistema di ricezione completo implementato in un singolo stadio per ridurre il consumo di potenza. L'architettura proposta, basata sulla tecnica del riutilizzo della corrente di polarizzazione, viene motivata e descritta in dettaglio; segue un'accurata analisi tempo-variante dell'architettura per l'ottimizzazione del circuito proposto; il ricevitore a 2.4 GHz è stato infine realizzato con una tecnologia CMOS digitale a 90 nm con top metal ottimizzato per la realizzazione di induttori integrati con alto fattore di qualità. Le misure effettute sui campioni confermano la correttezza della nostra analisi e la validità dell'architettura proposta.

Nella seconda parte di questa tesi di dottorato viene sviluppato un upconverter per un Frequency-Modulated Continuous-Wave radar in banda X. L'obiettivo del progetto è quello di realizzare un upconverter a banda larga, con uno spettro in uscita libero da toni spuri e con minimo phase noise. L'architettura proposta comprende due mixer con relative interfacce in banda base, un amplificatore a radiofrequenza e tutta la circuiteria per la generazione dei segnali in quadratura per pilotare i mixer a partire da un oscillatore locale esterno di riferimento. Vengono analizzati vari meccanismi di generazione di toni spuri all'uscita, con particolare enfasi sui problemi legati alla reiezione dell'immagine, ai mismatches ed alle nonlinearità generate nell'interfaccia in banda base. Due versioni del modulatore sono state progettate e confrontate: a) una versione realizzata in una tecnologia CMOS a 65 nm digitale basata su un mixer passivo a corrente di polarizzazione nulla per minimizzare la generazione di rumore flicker e b) una versione realizzata in una tecnologia bipolare SiGe:C a 0.35 μm basata su un mixer di Gilbert attivo.

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Introduction

Motivations

Radio-frequency integrated circuits find application in a multitude of different fields, both civil and military. Examples of applications where highly integrated RF circuits are required are:

- telecommunication systems, for the implementation of wireless transceivers for the exchange of both voice (in mobile phones) and data information (Bluetooth, WLANs, WPANs or specific Line-Of-Sight communication systems);
- environmental monitoring, for the transmission of data among sensors as in Wireless Sensor Networks;
- positioning systems, for an accurate determination of the position of mobile objects, as in Global/Local Positioning Systems;
- target detection (phased array radars, imagers, or radar altimeters);
- identification and security applications (RF signal generation/reception in RFIDs and transponders, security scanners).

The market of wireless systems is growing rapidly, followed by a constant improvement of the performances of the wireless integrated circuits, as is evident in the case of telecommunication systems and in the consumer electronics in general. From a technical perspective, most of the improvements are due to the digitalization of the wireless systems: in the telecom field, for example, improved modulation schemes and larger use of digital signal processing allow a transceiver to reach higher performances even in noisy environments. The current tendency is that of reducing the analog signal processing and doing most of the computation in the digital domain, keeping in analog form only the few RF blocks closest to the antenna.

The whole performances of wireless systems are essentially limited by the analog RF circuitry; the basic motivations are listed in the following.

- For cost reasons, RF circuits are often designed in digital CMOS technologies. Every time transistor sizes shrink, the digital circuitry can be easily converted to the new technological node with little effort, while analog radio-frequency circuitry typically has to be redesigned from scratch. Moreover, the performances of radio-frequency circuits are more sensitive to process spreads, mismatches, supply and temperature

variations; since the circuit target specifications have to be met in every condition, more effort in the design phase is needed.

- RF circuits typically contain passive devices, whose sizes do not scale as that of the active devices. Therefore, if the transistor sizes are halved, the area required by the digital circuits is halved too (neglecting the wiring) but the RF circuitry follows a lighter scaling. The whole transceiver chip area therefore does not fully benefit from the technology scaling and the overall chip cost *increases*.

- With the even faster proliferation of new wireless standards older standards becomes obsolete, meaning that the average chip lifetime tends to decrease. More effort is needed to develop a chip but less time is available to recover from the development costs: the chip price further *increases*.

To counteract these inefficiencies, two solutions are possible:

- research for new RF integrated circuit architectures which lead to smaller layouts to keep the scaling effective, or

- separate the RF and digital circuitry into two different dies, which allow to use the most suitable technology for each chip (latest CMOS for digital circuits, non-CMOS technologies for RF front-ends). In this case the RF technology is chosen such that product specifications are met easier, in order to reduce the development time.

The decision of which is the best approach strongly depends on the target product market, the required performances and the expected chip lifetime. In this thesis, we explore both solutions.

Organization of the work

In the first part of this dissertation (chapter 1) a low-power wireless receiver front-end for Wireless Sensor Networks (WSNs) or other similar low-power short-range low-data-rate wireless communication networks is developed. WSNs are decentralized networks composed by a large number of nodes for environmental monitoring, communicating each other through a wireless channel (section 1.1). In WSNs the large number of nodes requires an extremely highly integrated hardware for cost reduction; each wireless module needs to work for several years relying only on a limited amount of energy available, requiring an extremely low-power hardware; the short-range low-data-rate communication allows for relaxed transceiver specifications (section 1.2).

An ISM-band wireless receiver front-end based on a current-reuse topology is proposed (section 1.3). The circuit comprises a low-noise amplifier, cross-coupled voltage controlled oscillators and mixers, building a full quadrature receiver tailored for low-power applications (subsection 1.3.1).

The classical small-signal linear time invariant analysis is proved to be inaccurate for the prediction of the frequency conversion gain of the receiver. The cause of this inaccuracy is identified and an in-depth linear time-variant analysis is performed (subsection 1.3.2); the validity of the proposed analysis is verified through transistor-level SpectreRF simulations. The derived expression for the conversion gain is therefore used to optimize the circuit performances.

A test 2.4 GHz receiver is finally designed and realized in a cheap 90 nm digital CMOS technology with a 3 μm thick top metal for high-quality factor integrated inductors. The

measured frequency response of the circuit agrees with the predicted theoretical result; the performances of the receiver are competitive when compared to recently published state-of-the-art low-power receivers (section 1.4).

In the second part of the dissertation (chapter 2) a wideband X-band upconverter for Frequency-Modulated Continuous-Wave (FMCW) radar systems is developed. In a continuous wave radar system, the presence of a target is identified by transmitting a high power signal and analyzing the echoed signal. The determination of the position, radial velocity, and distance of the target requires a modulation of the frequency of the transmitted signal according to a given law. The resolution by which the distance and the radial velocity of the target can be determined strongly depends on the accuracy of the frequency modulation.

A short introduction to continuous wave radar systems is provided and the main radar architectures are shown (section 2.1). The work then focuses on the description of the circuitry for the local oscillator frequency modulation; the design of the analog part of this modulator, i.e. the X-band upconverter, is the target of this project. FMCW radar systems impose challenging specifications in term of the required high linearity and low phase noise in the upconverter, properties which have to be assured on a wide bandwidth (section 2.2).

The proposed upconverter architecture is constituted by two mixers, baseband interfaces, a pre-power amplifier and the on-chip circuitry needed for the generation of quadrature local oscillator signals derived from an (external) reference LO. Several mechanisms which lead to spurious tones at the output are discussed, with emphasis on the image-rejection, the effect of mismatches between I/Q paths and nonlinearities in the large-signal baseband interface. The circuit is designed to accommodate a DC to 1 GHz baseband input signal and a $9-11$ GHz LO signal; the target output power is 0 dBm in the $9-11$ GHz bandwidth.

Two versions of the upconverter are designed and compared: a) a CMOS version built in a 65 nm digital technology based on a passive mixer (section 2.3), and b) a bipolar version built in a 0.35 μm SiGe:C technology based on an active mixer (section 2.4). A comparison between the two upconverters and the conclusions of this project are drawn in section 2.5.

Appendix A introduces a novel kind of tunable phase-shifter based on a modified polyphase filter; the fundamental equations of the attainable phase shifting and of the amplitude mismatch are derived. Appendix B presents a brief introduction to an integrated bipolar diode mixer which was investigated for the FMCW radar project but not implemented due to high sensitivity to process variations. Finally, appendix C gives an overview of the ESD design issues in RF CMOS integrated circuits.

Introduzione

Motivazioni

I circuiti integrati a radio-frequenza trovano applicazione in molti diversi settori, sia civili che militari. Esempi di applicazioni nelle quali sono utilizzati circuiti integrati RF sono:

- sistemi di telecomunicazioni, per l'implementazione di ricevitori/trasmettitori wireless per lo scambio di voce (telefoni mobili) e dati (Bluetooth, WLANs, WPANs, o sistemi di comunicazione ad-hoc Line-Of-Sight);
- monitoraggio ambientale, per la trasmissione di dati tra sensori in sistemi come le Wireless Sensor Networks;
- sistemi di posizionamento, per una determinazione accurata della posizione nello spazio di oggetti mobili, come nei sistemi Global/Local Positioning Systems;
- identificazione di ostacoli (phased array radars, imagers, altimetri);
- sistemi di identificazione e sicurezza (generazione/ricezione di segnali RF in sistemi RFIDs e transponders, security scanners).

Il mercato dei sistemi wireless è in rapida espansione, seguito da un costante miglioramento delle performances dei circuiti integrati wireless che li compongono, come può essere facilmente osservato nel caso dei sistemi di telecomunicazione e nel mercato di elettronica consumer in generale. Dal punto di vista tecnico, la maggior parte dei miglioramenti è dovuta alla crescente digitalizzazione dei sistemi wireless: nel settore telecom, per esempio, schemi di modulazione sempre più evoluti uniti ad una maggiore elaborazione del segnale in forma digitale permettono ad un ricetrasmettitore di ottenere prestazioni più elevate anche in ambienti disturbati. Il trend corrente è dunque quello di ridurre sempre più l'elaborazione analogica dei segnali a vantaggio di quella digitale, mantenendo analogici solo i (pochi) blocci circuitali più vicini all'antenna.

Le prestazioni globali di un sistema wireless sono sostanzialmente limitate dalle performance della sottosezione analogica a RF; le motivazioniprincipali sono elencate in seguito.

- Per motivi di costo, i circuiti integrati RF sono spesso progettati in tecnologie CMOS digitali. Ad ogni step tecnologico la dimensione dei transistor diminuiscono e la sezione digitale del sistema può essere facilmente convertita al nuovo processo con poco sforzo progettuale, mentre la sezione analogica a radio-frequenza tipicamente

deve essere riprogettata da capo. Inoltre, le prestazioni dei circuiti integrati a radiofrequenza risultano molto sensibili agli spread di processo, ai mismatches, ai disturbi sulla tensione di alimentazione ed alle variazioni di temperatura di esercizio; dal momento che le specifiche di progetto devono essere soddisfatte in ogni condizione, è richiesta una maggior attenzione nella fase di design.

- I circuiti integrati RF tipicamente contengono una larga parte di elementi passivi, le cui dimensioni non scalano allo stesso modo dei dispositiivi attivi. Pertanto, se la dimensione di un transistor viene dimezzata, l'area richiesta dalla circuiteria digitale in prima appossimazione risulta anch'essa dimezzata (trascurando le interconnessioni), ma l'area richiesta dalla sezione RF segue uno scaling più lento. L'area totale del chip dunque non beneficia interamente dello scaling tecnologico ed il costo globale del chip *aumenta*.

- Con la sempre maggior proliferazione di nuovi standard tecnologici, i vecchi standard diventano presto obsoleti ed il tempo di vita medio di un sistema sul mercato cala. Maggiore sforzo viene richesto per lo sviluppo di un chip, minore tempo è disponbile per ripianare gli investimenti progettuali: il costo finale del chip *aumenta* ulteriormente.

Per contrastare queste inefficienze sono possibili due soluzioni:

- indirizzare lo sviluppo verso nuove architetture circuitali che consentano layout più compatti per mantenere lo scaling effettivo, oppure

- separare sezione RF e sezione digitale in due chip separati, consentendo di utilizzare la teconologia più adatta per l'implementazione di ciascuna parte (CMOS più scalata per la parte digitale, tecnologie non CMOS per i front-end RF). In questo caso la tecnologia RF può essere scelta in modo da raggiungere le specifiche di progetto in modo più semplice, riducendo il tempo di sviluppo.

Quale sia il miglior approccio dipende fortemente dal tipo di mercato del prodotto finale, dalle prestazioni richieste dal sistema e dal ciclo di vita previsto per il prodotto. In questa tesi, esploreremo entrambe le possibilità.

Organizzazione del lavoro

Nella prima parte di questa tesi di dottorato (capitolo 1) viene sviluppato il front-end di un ricevitore wireless a basso consumo di potenza per applicazioni nelle Wireless Sensor Networks (WSNs) o in altri simili tipi di reti di comunicazioni wireless a corto raggio, basso data-rate e basso consumo di potenza. WSNs sono reti decentralizzate composte da un largo numero di nodi sviluppate per il controllo ambientale, comunicanti tra di loro tramite un canale wireless (sezione 1.1). Nelle WSNs il numero elevato di nodi impiegti implica la necessità di utilizzare un hardware estremamente integrato per ridurre i costi della rete; ciascun modulo wireless deve poter operare per molteplici anni facendo affidamento solo in una limitata quantità di energia a disposizione - il consumo di potenza dell'hardware diventa critico; il basso data-rate della rete e la relativa vicinanza tra i nodi permette di rilassare le specifiche di progetto della sezione RF (sezione 1.2).

Il front-end di un ricevitore wireless a 2.4 GHz basato su una architettura a riutilizzo della corrente di polarizzazione viene presentato nella sezione 1.3. Il circuito, costituito

da un amplificatore a basso rumore, oscillatori in quadratura e mixer, forma un sistema completo di ricezione in quadratura adatto ad applicazioni low-power (sottosezione 1.3.1).

Nella sottosezione 1.3.2 viene mostrato come la classica analisi lineare tempo invariante a piccolo segnale sia inaccurata e porti ad una errata valutazione del guadagno di conversione del ricevitore. La causa di questo errore viene identificata e viene quindi proposta una approfondita analsisi lineare tempo-variante, la cui validità è stata verificata con simulazioni a livello di transitor con SpectreRF. L'espressione ricavata per il guadagno di conversione viene usata come guida per l'ottimizzazione del ricevitore.

Per verificare la concretezza dell'architettura circuitale proposta il ricevitore a 2.4 GHz è stato progettato ed implementato con una tecnologia CMOS digitale a 90 nm con un top metal ad alto spessore (3 μm) per la realizzazione di induttori integrati ad alto fattore di qualità. La riposta in frequenza misurata dai test chip risulta in accordo con l'analisi teorica; le performance del ricevitore sono competitive se confrontate con lo stato dell'arte dei ricevitori wireless low-power (sezione 1.4).

Nella seconda parte della tesi (capitolo 2) viene sviluppato un upconverter per un Frequency-Modulated Continuous-Wave (FMCW) radar in banda X. In un sistema radar continuous wave la presenza di un target viene determinata irradiando nello spazio un segnale ad alta potenza ed analizzando il segnale di ritorno. La deterinazione della posizione, della distanza e della velocità del target richiede una forma di modulazione della frequenza del segnale irradiato secondo una legge nota. La risoluzione con la quale queste grandezze possono essere determinate dipende fortemente dalle caratteristiche del segnale modulato.

Nella sezione 2.1 viene riportata una breve introduzione ai sistemi radar FMCW; il lavoro poi si focalizza sulla circuiteria utilizzata per la modulazione della frequenza del segnale irradiato; l'obiettivo del progetto è la progettazione della parte analogica in banda X di questo modulatore. I sistemi radar FMCW impongono stringenti vincoli in termini di linearità e phase noise dell'upconverter, proprietà che devono essere assicurate in un ampio intervallo di frequenze (sezione 2.2).

L'architettura proposta dell'upconverter è formata da due mixer, interfacce in banda base, un amplificatore RF e tutta la circuiteria necessaria per la generazione dei segnali di LO in quadratura derivati da un segnale di riferimento esterno. Vengono discussi molteplici meccanismi di generazione di toni spuri in uscita, con particolare enfasi sulla reiezione di immagine, sugli effetti di mismatch tra i percorsi I/Q e sulle nonlinearità che vengono generate nell'interfaccia in banda base. Il circuito è progettato per ricevere in ingresso segnali in banda base da 0 a 1 GHz ed un segnale di LO nell'intervallo $9 - 11$ GHz; la potenza di uscita per il quale i circuito è dimensionato è di 0 dBm nella banda $9-11$ GHz.

Sono state realizzate e confrontate due differenti versioni dell'upconverter: a) una versione sviluppata con una tecnologia CMOS a 65 nm basata su mixer passivi (sezione 2.3), e b) una versione bipolare realizzata con una tecnologia SiGe:C a 0.35 μm basata su mixer attivi di Gilbert (sezione 2.4).

Infine, un confronto tra le due versioni e le conclusioni del progetto sono riportate nella sezione 2.5.

Nell'appendice A viene introdotto un nuovo tipo di phase-shifter accordabile basato su un filtro polifase opportunamente modificato; vengono derivate le equazioni fondamentali circa il phase-shifting che è possibile ottenere e del mismatch in ampiezza. L'appendice B presenta una breve introduzione su un mixer integrato bipolare a diodi che è stato investigato durante lo sviluppo del radar FMCW ma poi accantonato a causa dell'eccessiva

sensibilità alle variazioni di processo. Infine, l'appendice C approfondisce la tematica dei problemi legati ai fenomeni ESD nei circuiti integrati CMOS a radiofrequenza.

Chapter 1

Low-power ISM band receiver front-end

In this chapter we will develop a compact low-power wireless receiver front-end operating at 2.4 GHz for low data-rate applications like Wireless Sensor Networks (WSNs) or other similar low data-rate multi-hop networks.

1.1 Overview of Wireless Sensor Networks

1.1.1 Introduction

WSNs are networks constituted by a large number of nodes for environmental monitoring [Cook 06]; each node comprises one or more sensors, an RF transceiver to communicate with the other nodes and a CPU for the unit management. Each unit spends most of its time in an idle state and sporadically wakes up to collect data from its sensors and/or transmitting data to other nodes; the node must operate without maintenance for a long period, typically years, only relying on the power provided by a battery or other mechanisms of energy harvesting [Rabaey 06]. In this application:

- the low data-rate and relatively short distance among the sensors allow for relaxed RF specifications in term of gain, bandwidth and noise figure;
- the large number of sensor requires highly integrated wireless units to minimize the cost of each unit. The direct-conversion or low-IF architectures are almost ubiquitous for wireless transceiver due to their simpler structure and the absence of expensive external filters;
- the limited energy available to each node implies that an extremely low-power front-end is needed. Current-reuse is, for example, an attractive approach to achieve a reduction in power dissipation; several different implementations have been shown in these years, featuring structures like stacked LNAs and mixers, merged mixers and VCOs, or merged power amplifiers and mixers, just to name a few [Ghanevati 01], [Paek 09].

1.1.2 Node architecture

The typical architecture of a wireless sensor node is sketched in Figure 1.1. The fundamental building blocks are:

CPU. Microcontroller for digital signal processing / power management of the unit

Power supply. Typically a battery, with an optional circuitry for energy harvesting (solar, thermal, vibration...) to increase unit lifetime

Sensor(s). One ore more sensors/transducers including ADCs/DACs and signal conditioning circuits to interface the sensor to the central microcontroller. Sensors commonly inserted into a node include: mechanical sensors, thermal sensors, magnetic / electromagnetic sensors, acoustic sensors, optical/chemical/biological transducers

RF transceiver. Communication with other nodes

Flash memory. Data storage / unit firmware

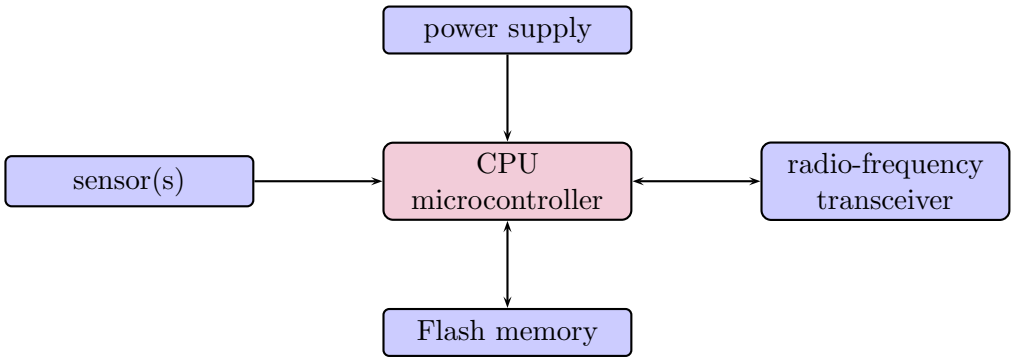


Figure 1.1: Wireless sensor node block diagram

1.1.3 Network architecture

There are three basic networks topologies that applies to Wireless Sensor Networks: the star network, the mesh network and the hybrid star-mesh network; each one is described below.

Star network

A star network is composed by a single base-station and several remote nodes (Figure 1.2). The base-station can send/receive data from/to the other nodes; the remote nodes can only communicate with the base-station.
Pros:

- The remote nodes are designed to communicate only with the base-station: simpler node architecture, reduced power consumption.
- Low latency communication.

Cons:

- The base-station is responsible of the overall network performance; a failure in the base-station compromises the whole system.
- The base-station must reside in the radio transmission range of all the remote nodes.

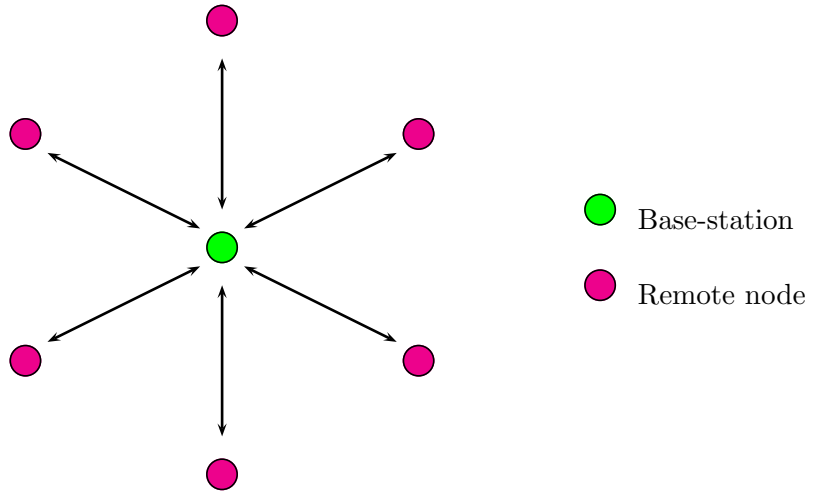


Figure 1.2: Star network topology

Mesh network

A mesh network is only composed by remote nodes; each node receives/transmits data from/to the nodes which reside within its own radio transmission range. If a node is not reachable because is out-of-range, intermediate nodes forward the messages (Figure 1.3).

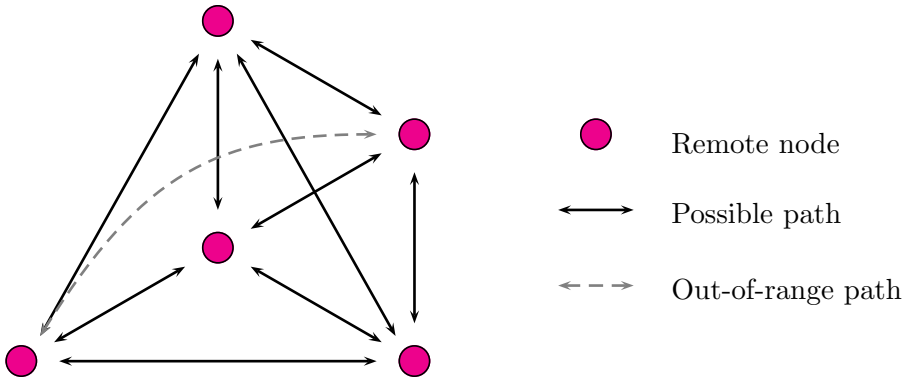


Figure 1.3: Mesh network topology

Pros:

- Redundancy: if a node ceases to work the other nodes can still communicate each other and the network remains functional.
- Scalability: other nodes can easily be added to the network for extension of the covered area.

Cons:

- Each node must be able to forward messages to other nodes: more complex architecture, more power consumption for each unit.

- The multi-hop communication between out-of-range nodes increases the communication latency.

Hybrid star-mesh network

The hybrid star-mesh network is a combination of the previous two network topologies; it comprises both remote nodes with no possibility to forward messages (therefore with minimum power consumption) and more complex nodes with forwarding capabilities (Figure 1.4).

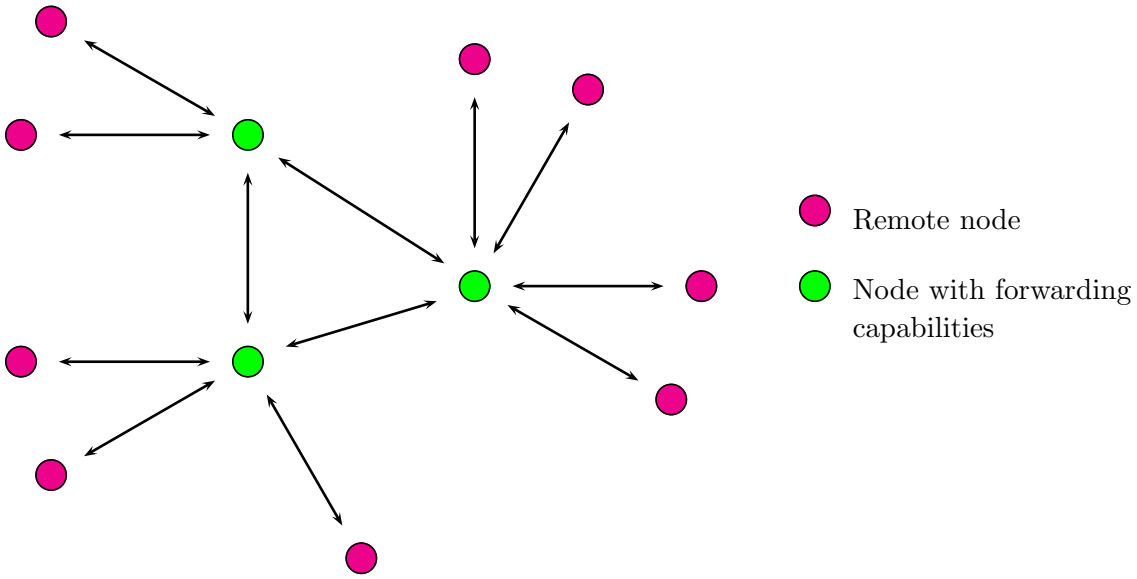


Figure 1.4: Hybrid star-mesh network topology

Pros:

- Large number of remote nodes and small number of nodes with forward capabilities allow for power consumption optimization.

- Multi-hop communication with good degree of redundancy and scalability.

Cons:

- Complex topology.

- Increased latency with respect to the star network.

The hybrid star-mesh topology is typically the preferred topology for Wireless Sensor Networks due to its flexibility.

1.1.4 Physical radio layers

The physical radio layer defines the frequency in which the link between transceivers operate, the modulation scheme and the supported network topologies. Physical radio layer divides into proprietary radio options (developed by companies such as Atmel, MicroChip, ChipCon, Micrel) and standard-based radio options; if a standard-based physical layer is adopted, a better interoperability among different devices of different companies can be achieved. The most common physical radio layers which adhere to a standard (not necessarily addressed to WSNs applications) are described below.

IEEE 802.11x (WiFi)

IEEE 802.11x is a set of standards developed for exchanging data in Local Area Networks (LANs) [IEEE 802.11-2007]. First introduced in 1997, the standard underwent several improvements (a/b/g/n) which improved the maximum data-rate, the range and the performance in presence of interferers.

The theoretical maximum transfer rate reaches 54 Mbps with a channel of 20 MHz in the 2.4 GHz Industrial, Scientific and Medical (ISM) band (IEEE 802.11g) or 600 Mbps with 4 channels of 40 MHz in the 2.4 / 5 GHz band (IEEE 802.11n). Orthogonal Frequency-Division Multiplexing (OFDM) and/or Direct-Sequence Spread-Spectrum modulation schemes are employed.

The performances of the IEEE802.11x standard are more than adequate for Wireless Sensor Networks, but power requirements are generally too high.

IEEE 802.15.x (Bluetooth)

IEEE 802.15.x is a set of standards developed for data transmission among fixed and mobile devices in Personal Area Networks (PANs) [www.bluetooth.com]. Bluetooth technology operates in the unlicensed ISM band at 2.4 to 2.485 GHz, using a frequency-hopping spread-spectrum (FHSS) modulation.

Similarly to IEEE 802.11.x, Bluetooth standard too evolved with time. The first version of the Bluetooth standard implemented a maximum transfer rate of 1 Mbps with an adaptive FHSS modulation to reduce the impact of signal interference (v1.2). The version 2 of the protocol introduced an (optional) Enhanced Data Rate (EDR) which increased the theoretical data-rate to 3 Mbps.
The main limitations of the Bluetooth standard are the following:

- the power consumption, although considerably lower than IEEE 802.11x, is still to high for WSNs applications;
- a maximum number of 7 active nodes per piconet are supported, limiting the onverall node number in the network;
- nodes take a long time to synchronize when waking-up from sleep mode, which increases the average system power.

Bluetooth v3.0, introduced in 2009, increases the theoretical maximum data-rate speed at 24 Mbps using the Bluetooth link for negotiation and establishment of the communication and a 802.11 link for data transfer. Clearly, this improvement is not helpful for WSNs.

On April 2010 the fourth version of the standard was introduced; Bluetooth v4.0 introduced a low power transmission mode with reduced latency and an increased (but still not defined) number of active nodes in the network. For further details of this standard, which could be suitable for WSNs in the near future, we refer to the official online resource at [Bluetooth v4.0 Low Energy].

IEEE 802.15.4-2006

IEEE 802.15.4-2006 is a standard specifically designed for Low-Rate Wireless Personal Area Networks (LR-WPANs), as Wireless Sensor Networks [IEEE 802.15.4-2006]. Multiple data rates, multiple transmission frequencies and several modulation schemes are supported, making the standard highly flexible. The power requirements are low, the radio can be put to sleep mode to minimize the power consumption when no data are exchanged; fast synchronization among nodes is achieved on wake-up.
Some of the characteristics of an LR-WPAN are as follows:

- data rates of 250 kb/s, 100kb/s, 40 kb/s, and 20 kb/s;
- star or peer-to-peer operation;
- carrier sense multiple access with collision avoidance (CSMA-CA) channel access;
- low power consumption;
- energy detection (ED);
- link quality indication (LQI).

Three bands of transmission are supported:

- PHY 868, 1 channel in the 868.0-868.6 MHz band;
- PHY 915, 10 channels in the 902-928 MHz band;
- PHY 2450, 16 channels in the 2400-2483.5 MHz band.

The channel center frequencies F_c in each band are given by:

- $F_c = 868.3$ MHz, for $k = 0$
- $F_c = 906 + 2(k-1)$ MHz, for $k = 1, 2, \ldots, 10$
- $F_c = 2405 + 5(k-11)$ MHz, for $k = 11, 12, \ldots, 26$

where k is the channel number. The supported modulation schemes and the corresponding transmission data rate are listed in table 1.1.

Being this standard specifically developed for Low-Rate Wireless Personal Area Networks, it will be taken as the reference standard for the proposed low-power receiver front-end.

PHY (MHz)	Band (MHz)	Chirp rate (kchirp/s)	Spread Spectrum	Modulation	Bit rate (kbps)	RX sensitivity (dBm)
868/915	868–868.6	300	Direct Sequence	BPSK	20	-92
	902–928	600	Direct Sequence	BPSK	40	
868/915	868–868.6	400	Parallel Sequence	ASK	250	-85
(optional)	902–928	1600	Parallel Sequence	ASK	250	
868/915	868–868.6	400	Direct Sequence	O-QPSK	100	-85
(optional)	902–928	1000	Direct Sequence	O-QPSK	250	
2450	2400–2483.5	2000	Direct Sequence	O-QPSK	250	-85

Table 1.1: 802.15.4-2006 frequency bands, modulations and data rates

1.1.5 The ZigBee standard

ZigBee is a open high-level communication protocol based on the IEEE 802.15.4 standard for the realization of small, ultra low-power radios; it addresses the need of low-cost wireless RF transceivers with low data-rate and long battery life [www.zigbee.org].
ZigBee protocol features include:

- support for multiple network topologies such as point-to-point, star and mesh networks,
- low duty-cycle for long battery life,
- low latency,
- Direct Sequence Spread Spectrum (DSSS) modulation,
- up to 65,000 nodes per network,
- 128-bit AES encryption for secure data connections, and
- collision avoidance, retries and acknowledgments.

Depending on the task of a device in the network, ZigBee devices can be classified as:

ZigBee coordinator (ZC). It is the core of the network, which can control the other devices and, if needed, forward the traffic to/from other networks. It corresponds to the base-station node in the star network of Figure 1.2.

ZigBee router (ZR). A router is a node that can forward the data to other devices. It corresponds to the nodes with forwarding capabilities in hybrid star-mesh network of Figure 1.4.

ZigBee end device (ZED). It's the simpler kind of device, which has only the capability to communicate to its parent node (i.e. the coordinator or a router); it cannot forward data from other devices. Due to its limited functionality, the ZED has the simplest hardware and can operate in deep duty-cycling to minimize the power consumption. It corresponds to the remote nodes of Figure 1.4.

1.1.6 WSNs applications

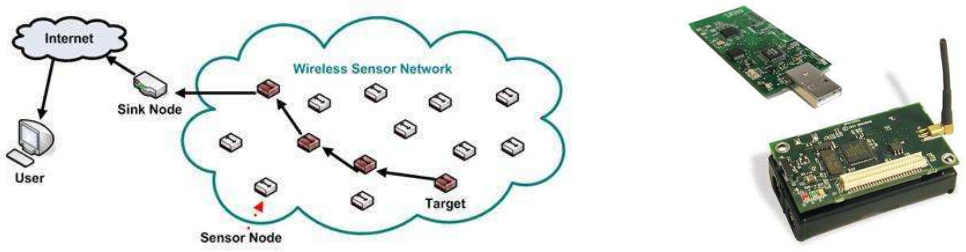
Typical applications of WSNs include the following:

Environmental monitoring. Habitat monitoring, fire detection, traffic control, home automation.

Health monitoring. Patient physiological data monitoring in hospitals.

Industrial automation. Application in structural health monitoring (automatic monitoring of machines and structures allows condition-based maintenance).

Military applications. Battlefield monitoring, targeting, monitoring of friendly / opposing forces.



(a) Network topology

(b) Commercial implementation

Figure 1.5: Applications of WSNs

1.2 Low power wireless receiver front-end for WSNs

1.2.1 Target specifications

A ZigBee compliant receiver wireless front-end is here developed. The 2.4 GHz ISM band is chosen since it is worldwide available; a quadrature receiver is required due to the Offset-Quadrature Phase Shift Keying (O-QPSK) modulation. Target specifications of the summarized in table 1.2.

Specification	Value	Comment
Gain	25–30 dB	
Bandwidth	$>$ 5 MHz	channel bandwidth
NF	$<$ 16 dB	target SNR $>$ 6 dB
Architecture	quadrature RX	O-QPSK modulation
LO tuning	greater than [2400–2483.5] MHz	
Power consumption	absolutely minimum	
Area	$<$ 1 mm^2	pads included

Table 1.2: ZigBee compliant wireless receiver front-end target specifications

1.2.2 Proposed circuit

A very low-power receiver front-end based on a current reuse topology evolution from the "LMV cell" [Liscidini 06] is proposed. In this architecture:

- a self-oscillating mixer is stacked on top of a low-noise amplifier, making the down-conversion of the incoming RF signal possible in a single stage circuit, with minimum current consumption;
- two stage are cross coupled in parallel to build a quadrature receiver with I/Q baseband output;
- additional baseband transimpedance gain is provided by a modified LC tank merged in the oscillator, consuming no additional power;
- the number of stacked transistor is kept to the absolute minimum of three, making the circuit scalable and able to operate at low voltage supply (1.0 V in our design);
- the front-end only requires three inductors, resulting in a compact design (chip area is $700\mu m \times 700\mu m$ pads included).

An analysis of this architecture by means of the classical small-signal linear time-invariant analysis is shown to overestimate the conversion-gain of the receiver chain. This interesting phenomenon is basically due to a periodical charge-sharing among the parasitic capacitances at the oscillator output nodes and the load capacitance; being the output baseband load merged into the oscillator, the charge-sharing modifies the frequency response of the output transimpedance stage, ultimately affecting both the gain and the bandwidth of the receiver chain.

An accurate periodic time-variant analysis is therefore illustrated. The key points are the following [Zadeh 50], [Signell 77]:

- the input-output relation in a linear time-variant system is defined by means of a system function $Z(f,t)$ dependent on both the frequency and the time, constituting the generalization of the LTI transfer function; the system function can be calculated as
$$Z(f,t) = \left.\frac{out(t)}{in(t)}\right|_{in(t)=e^{j2\pi ft}},$$
i.e. as the ratio between the output of the system $out(t)$ and its input $in(t)$ when $in(t) = e^{j2\pi ft}$;
- if the system is periodically linear time variant (with frequency f_0), an input tone at frequency f gives rise to a set of tones at frequencies $nf_0 + f$ at the output;
- the system function can therefore be expressed as a Fourier expansion with frequency dependent coefficients
$$Z(f,t) = \sum_n H_n(f) e^{j2\pi n f_0 t},$$
from which it is possible to derive a set of functions $H_n(f)$, each one representing the conversion gain of the system from f to $nf_0 + f$.

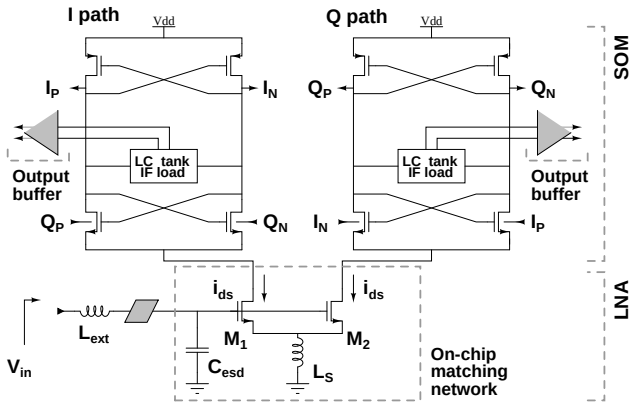


Figure 1.6: Receiver schematic.

The determination of the system function of the receiver is not straightforward. In our approach we start the analysis with a description of the system in the time domain to give a better insight into the physical phenomenon, then move to the frequency domain and calculate the Fourier expansion of the system function; since we are seeking the downconversion gain from an input tone at $f_0 + f$ to an output tone at f, $H_{-1}(f)$ is the transfer function of interest.

The theoretical result derived is verified through SpectreRF simulations. The accurate expression for the conversion-gain clearly indicates what the design trade-offs are and how to optimize the circuit for best performances.

1.3 90nm CMOS receiver design

1.3.1 Front-end design

The schematic of the proposed receiver is shown in Fig. 1.6. The circuit, based on the architecture initially proposed in [Liscidini 06], is composed by two cross-coupled stages for the I and Q path respectively. Each receiver stage is composed by an inductively degenerated nMOS transistor acting as the Low-Noise Amplifier (LNA) stacked by a Self-Oscillating Mixer (SOM), forming what was defined as a LNA-Mixer-VCO (LMV) cell; the single-ended RF input gets downconverted and is available in a differential form for digital processing. The number of stacked transistor is kept to a minimum of three, making the circuit scalable; the tunable LC tank is modified to provide IF transimpedance gain. Output buffers complete the design, interfacing the receiver to the measurement setup; all pads are ESD protected.

Input matching network and LNA

The input matching to the $50\,\Omega$ source is obtained by an input reactive T-network formed by the two single-ended LNAs, an on-chip source degeneration inductor L_s, the ESD protection devices and an external inductor L_ext (figure 1.7).

The degeneration inductor L_s creates the real part of the input impedance, namely $R_\mathrm{eq} = g_\mathrm{m} L_\mathrm{s}/C_\mathrm{gs}$ where g_m and C_gs are the nMOS transconductance and gate capacitance, respectively. The resistance R_eq is then transformed by the capacitive divider formed by

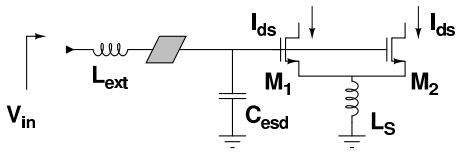


Figure 1.7: LNA stage and reactive input network

the gate capacitance $C_{\rm gs}$ and the ESD parasitic capacitance $C_{\rm esd}$ to obtain the desired 50 Ω input resistance. The external inductor $L_{\rm ext}$ sets the resonance of the reactive network at the desired angular frequency ω_0.

The proposed input network has several advantages. The source degeneration technique is an efficient way to obtain the input matching in terms of both power consumption and noise figure with respect to the resistive feedback and the common-gate approach. The induced-gate noise of the LNA nMOS is suppressed by the parasitic overlap capacitances of the device itself, so that no extra capacitance is needed in parallel to the nMOS [Rossi 05]. The capacitance introduced by the input pad can be absorbed into the parasitic capacitance of the ESD diodes $C_{\rm esd}$ and it is resonated out at the desired frequency, while the bondwire inductance can be taken into account as a part of $L_{\rm ext}$.

For the calculation of the input resistance and the input equivalent transconductance, we refer to the equivalent (half) circuit of figure 1.8(a), in which only a single LNA is considered.

The common source stage with inductive degeneration of Figure 1.8(a) can be modeled as a RLC series where the equivalent resistance is

$$R_{eq} = \frac{g_m 2Ls}{C_{gs}}. \tag{1.1}$$

In the following, we discard the inductance $2L_s$ since the tank is substantially capacitive at $f_0 = 2.4\ GHz$ and simplify the circuit as in Figure 1.8(b). The quality factor Q_2 of the right C_{gs}, R_{eq} branch of the input network is given by

$$Q_2 = \frac{1}{\omega_0 R_{eq} C_{gs}} = \frac{1}{\omega_0 g_m 2L_s}, \tag{1.2}$$

not much greater than one in our design. Series to parallel impedance conversion leads to an equivalent capacitance C_x

$$C_x = C_{gs}\frac{Q_2^2}{Q_2^2 + 1} \tag{1.3}$$

and an equivalent resistance R_x

$$R_x = R_{eq}(Q_2^2 + 1); \tag{1.4}$$

the circuit becomes that of Figure 1.8(c). Calling $C_{tot} = C_{esd} + C_x$ the total capacitance, a new quality factor for the parallel branch C_{tot}, R_{eq} can be defined:

$$Q_1 = \omega_0 R_x C_{tot} = \frac{C_{tot}}{C_{gs}}\frac{1 + Q_2^2}{Q_2} > \frac{C_{tot}}{C_{gs}} Q_2 > Q_2. \tag{1.5}$$

The input resistance R_{in} and the total input capacitance C_{in} in Figure 1.8(d) can be therefore computed as

$$\begin{aligned} R_{in} \approx \frac{R_x}{Q_1^2} &= \frac{1}{\omega_0^2 C_{tot}^2 R_x} = \\ &= \frac{1}{\omega_0^2 C_{tot}^2 R_{eq}(1+Q_2^2)} = \\ &= \frac{1}{C_{tot}^2} \frac{g_m 2L_s C_{gs}}{1+\omega_0^2 g_m^2 4L_s^2} = \\ &= \frac{C_{gs}^2}{C_{tot}^2} \frac{R_{eq}}{1+\omega_0^2 g_m^2 4L_s^2}. \end{aligned} \tag{1.6}$$

and

$$C_{in} \approx C_{tot}, \tag{1.7}$$

respectively. The resonant angular frequency is obviously

$$\omega_0 = \frac{1}{\sqrt{L_{ext} C_{in}}}, \tag{1.8}$$

and overall network quality factor Q_{in} results in

$$Q_{in} = \frac{\Delta\omega_{in}}{\omega_0} \frac{\sqrt{L_{ext}/C_{in}}}{R_{in}} = \frac{1}{\omega_0 R_{in} C_{in}} = \frac{C_{tot}}{C_{in}} Q_1 \approx Q_1 > Q_2. \tag{1.9}$$

If perfect input matching to a $R_S = 50\Omega$ source is to be assured, then we have to set $R_{in} = 2R_S$; combining (1.8) and (1.9) we get

$$\Delta\omega_{in} = \frac{1}{2R_S} \frac{1}{C_{tot}} \tag{1.10}$$

i.e. the higher the ESD protection diodes (which form the main part of the capacitance C_{tot}), the narrower the input matching bandwidth $\Delta\omega_{in}$. Assuming a loseless network, power conservation holds

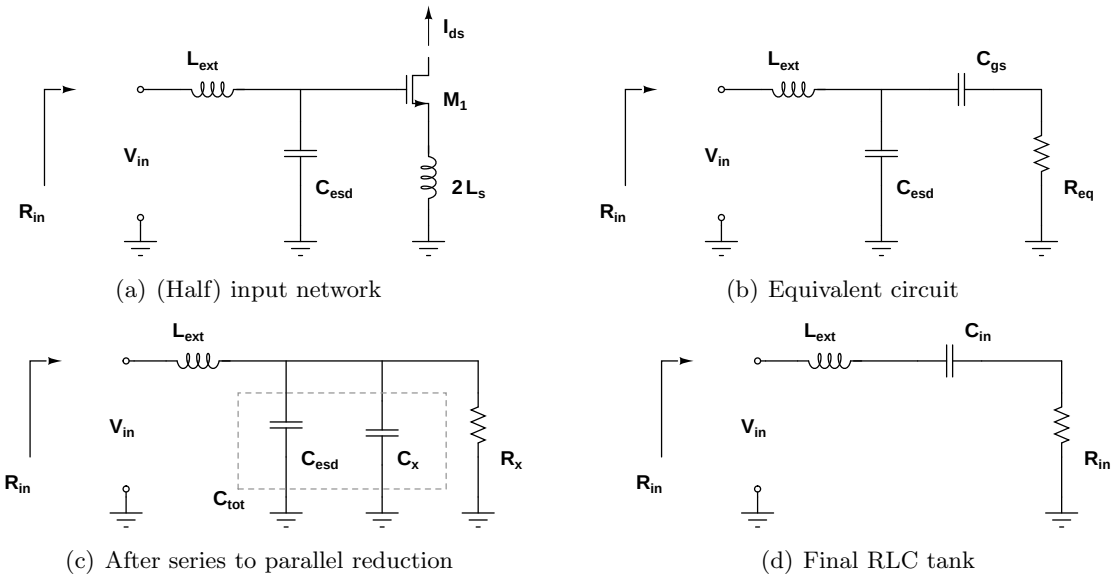
$$\frac{v_{in}^2}{R_{in}} = R_{eq} i_{gs}^2 \tag{1.11}$$

where i_{gs} is the current flowing into R_{eq}, i.e. the input current for the transistor; the output drain current i_{ds} can be therefore written as

$$i_{ds} = \beta i_{gs} = \frac{v_{in}}{\sqrt{R_{in} R_{eq}}} \frac{1}{sC_{gs}} g_m, \tag{1.12}$$

from which the equivalent conductance $G_m(\omega)$ of the input matching can be easily computed as

$$\begin{aligned} G_m(\omega) \triangleq \frac{i_{ds}}{v_{in}} &= \frac{1}{\sqrt{R_{in} R_{eq}}} \frac{g_m}{\omega C_{gs}} = \\ &= \frac{1}{R_{in}} \sqrt{\frac{1+Q_2^2}{1+Q_1^2}} \frac{\omega_T}{\omega} = \\ &= \frac{1}{R_{in}} \sqrt{\chi} \frac{\omega_T}{\omega} \end{aligned} \tag{1.13}$$



(a) (Half) input network

(b) Equivalent circuit

(c) After series to parallel reduction

(d) Final RLC tank

Figure 1.8: Input matching equivalent networks

where we defined the term

$$\chi \triangleq \frac{1+Q_2^2}{1+Q_1^2}. \tag{1.14}$$

If $\omega_0 \ll 1/(g_m L_s)$ than $Q_1 \gg Q_2 \gg 1$ and

$$\sqrt{\chi} \approx \frac{Q_2}{Q_1} = \frac{C_{gs}}{C_{tot}} = \frac{1}{1+C_{esd}/C_{gs}}. \tag{1.15}$$

If perfect matching is assumed, than $R_{in} = 2R_S$ and the equivalent input transconductance (1.13) reduces to

$$G_{\mathrm{m}}(\omega) = \frac{i_{\mathrm{ds}}}{v_{\mathrm{in}}} = \frac{1}{2R_{\mathrm{s}}} \frac{1}{1+C_{\mathrm{esd}}/C_{\mathrm{gs}}} \frac{\omega_{\mathrm{T}}}{\omega}, \tag{1.16}$$

where i_{ds} is the small signal drain-source currents of the LNA, v_{in} is the input voltage, R_{s} is the source output resistance and ω_{T} is the transistor unity current gain frequency.

While in the design we have several degree of freedom in choosing the values of the reactive components to set the resonant angular frequency, we can observe that, since the LNA is the first amplification stage in the receiver chain, the transconductance (1.16) must be maximized in order to keep the NF low; a first design tradeoff emerges between the achievable ESD protection level (which can be assumed proportional to the ratio $C_{\mathrm{esd}}/C_{\mathrm{gs}}$) and the overall gain and NF of the receiver.

Self-Oscillating Mixer and LC tank

The core of the SOM, depicted in more detail in Fig. 1.9, is formed by the classical differential CMOS *LC* oscillator. Having both pMOS and nMOS cross-coupled pairs does not significantly increase the noise of the oscillator while assuring a higher small signal negative resistance for a given bias current, making the startup of the oscillator more reliable, and achieving a doubled oscillation amplitude (which turns, ideally, into a 6 dB lower phase noise), compared to oscillators with a single switch pair using the same bias

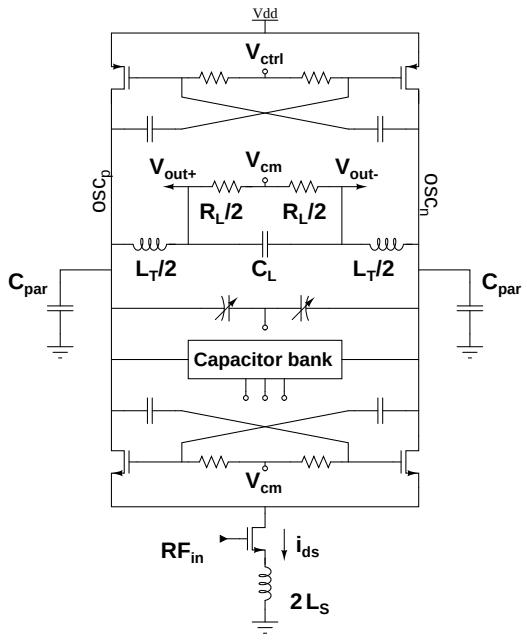
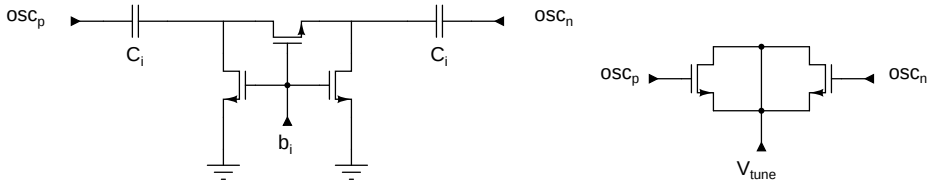


Figure 1.9: Self-Oscillating Mixer with LNA for current injection.



(a) Digitally controlled capacitor unit cell. (b) Varactor cell.

Figure 1.10: Tunable capacitor.

current [Andreani 06]. Thus, this choice results in a more efficient current-reusing LMV cell, compared to the solutions in [Liscidini 06], [Liscidini 08], [Liscidini 08b], [Allstot 09].

The sizing of the cross-coupled pair is an optimal tradeoff between flicker noise, startup conditions and parasitic capacitances at the oscillator nodes, which will be shown to have a sharp impact on the overall performance of the receiver.

A tunable capacitor is required to set the LO frequency; a large range of capacitance variation is required to get a wide tuning range of the receiver. A solution exclusively based on varactors is not optimal in terms of phase noise due to the nonlinear nature of the capacitance of these devices; in our approach, a combination of a digitally controlled bank of binary weighted capacitors for coarse tuning and varactors for the fine tuning of the oscillation frequency is adopted (Fig. 1.10).

The RF current i_{ds} injected by the LNA is chopped by the switching transistors of the SOM and thus downconverted to IF, flowing into the differential load. With a classical LC tank as a load, the low inductor impedance at low frequency would prevent any voltage gain; to overcome this limitation a modified tank is adopted, which presents a high impedance at low frequency to achieve voltage gain, while reducing to the classical LC tank at the LO frequency for proper circuit oscillation, keeping the quality factor unaffected. This

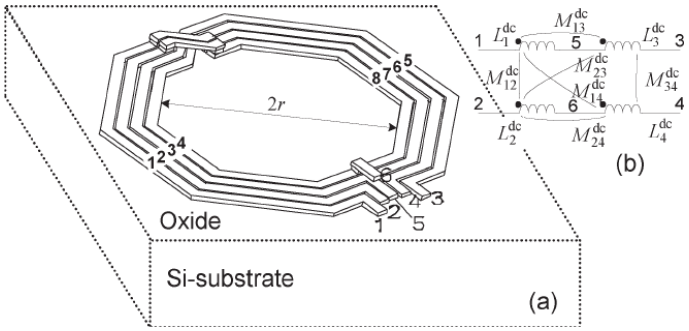


Figure 1.11: Interleaved inductors

double goal was accomplished by splitting the inductor into two equal parts $L_{\mathrm{T}}/2$ and by inserting a parallel RC network in the branch: at the LO frequency, the capacitor C_{L} acts as a short circuit across the resistor R_{L} and a high-Q inductor is obtained, while at low frequency, where the inductor impedance is negligible, R_{L} provides transimpedance gain while the capacitor C_{L} sets the -3 dB bandwidth of the receiver. To keep the layout compact, the two inductors $L_{\mathrm{T}}/2$ of each cell are realized as a single interleaved symmetrical transformer, without any area penalty, and exploiting the inductance boost given by the mutual coupling between the coils [Gao 06] (Fig. 1.11).

The IF voltage across R_{L} is immediately available for the base-band circuitry. Being the oscillation angular frequency ω_0, assuming that the input RF signal is a tone at $\omega_0+\omega_{\mathrm{m}}$ with $\omega_{\mathrm{m}} \ll \omega_0$ the overall conversion gain calculated with a classical approach is

$$\begin{aligned} A_{\mathrm{v}}(\omega_{\mathrm{m}}) = \frac{v_{\mathrm{out}}}{v_{\mathrm{in}}} &= \frac{2}{\pi} G_{\mathrm{m}}(\omega_0+\omega_{\mathrm{m}}) Z_{\mathrm{L}}(\omega_{\mathrm{m}}) \\ &\approx \frac{2}{\pi} G_{\mathrm{m}}(\omega_0) \frac{R_{\mathrm{L}}}{1+j\omega_{\mathrm{m}} R_{\mathrm{L}} C_{\mathrm{L}}}, \end{aligned} \tag{1.17}$$

where R_{L} and C_{L} are the load resistance and the load capacitance respectively and the $2/\pi$ factor accounts for the current-commutating mixing; only the low-frequency response of the load $Z(\omega_{\mathrm{m}})$ is taken into account. As it will be shown in the next section, the output parasitic capacitances C_{par} get cyclically charged and discharged at each oscillation period and behave like a switched-capacitor resistor in parallel to the tank, significantly reducing the gain of the cell. As such, wide transistors in the SOM must be avoided, and a careful layout of the cross-coupling paths is required.

Biasing and measurement circuits

At low frequency, the loop that assures positive feedback in the oscillator is open to avoid instabilities: this is accomplished by the decoupling capacitors in the cross-coupled pairs shown in Figure 1.9. Moreover, at DC, the tank is used to sense the output common-mode voltage V_{cm} and an OTA-based common-mode feedback circuit (not shown in Figure 1.9) sets the common-mode output voltage operating on V_{ctrl}.

DC-coupled output pseudo-differential buffers, based on source followers, are added for measurement purposes only; they are designed to drive the subsequent capacitive load of an off-chip differential to single-ended unity gain stage.

The I and Q oscillators are cross-connected by means of the nMOS bulk terminal, which

force them to oscillate in quadrature without requiring any additional power consumption [Kim 04].

All pads are ESD protected by means of a pair of diodes connected from the output terminal to V_{DD} and GND; these diodes are able to withstand a 2 kV HBM stress. The ESD protection is completed with a diode power clamp between the supplies.

1.3.2 Time-variant analysis of the conversion gain

In this section we investigate the impact of the parasitic capacitance C_{par} on the gain and bandwidth of the downconverted signal; we will show that the transimpedance conversion gain in the SOM is significantly affected and that a LTV analysis is required.

Consider the receiver front-end sketched in Fig. 1.9. Let f_0 be the SOM oscillating frequency and assume that the LNA is injecting a current tone at frequency $f = f_0 + f_m$ with $f_m \ll f_0$. We want to estimate how this tone is downconverted by the SOM in the presence of the parasitic output capacitances.

To make the analysis manageable, we assume that the oscillator is in hard switching regime so that we can model the SOM transistors as ideal switches (i.e. zero on resistance, infinite off resistance and instantaneous switching between the two states) driven by non-overlapping signals ϕ and $\overline{\phi}$, where $\phi(t)$ is a square wave toggling between 0 and 1 with period $T = 1/f_0$ and duty-cycle $\delta = 50\%$ (Fig. 1.12(a)-1.12(d)). This assumption, which greatly simplifies the calculations, is motivated by the large voltage swing at the oscillation nodes. As a starting point we will also assume that the cell is driving a purely capacitive load instead of the RLC network described previously; we will soon prove that this simplification makes the analysis easier to handle without invalidating the results. The circuit schematic can thus be simplified as in Fig. 1.12(e). We will later address the effect of R_L. According to the equivalent circuit in Figure 1.12(f), four phases of operation can be identified:

(a) when $\phi(t)=1$ the parasitic capacitance C_{par} connected to v^- is shorted to ac ground while the tail current charges the parallel combination of the load capacitor and the parasitic capacitance connected to v^+ (Fig. 1.12(a));

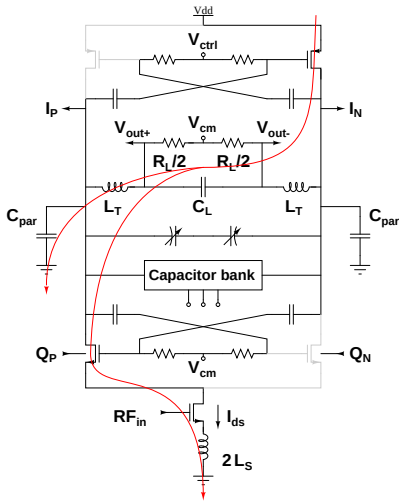
(b) at the switching instant the parasitic capacitor connected to v^+ is discharged to ac ground and charge sharing occurs between the load and the capacitor connected to v^- (Fig. 1.12(b));

(c) after the charge redistribution, $\overline{\phi}(t) = 1$ and the tail current charges the resulting overall capacitor (Fig. 1.12(c));

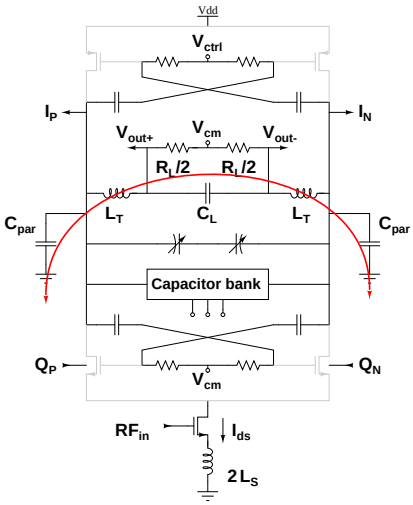
(d) a new charge sharing between the load and the capacitor connected to v^+ occurs at the next switching instant (Fig. 1.12(d)).

The process proceeds cyclically, as depicted in Fig. 1.12(f).

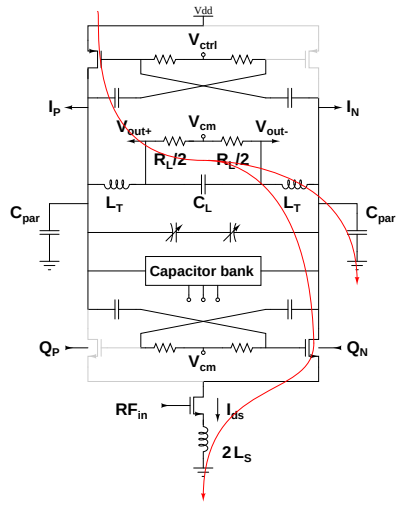
Analytically, the voltages at the output nodes v^+ and v^- at the switching instants can



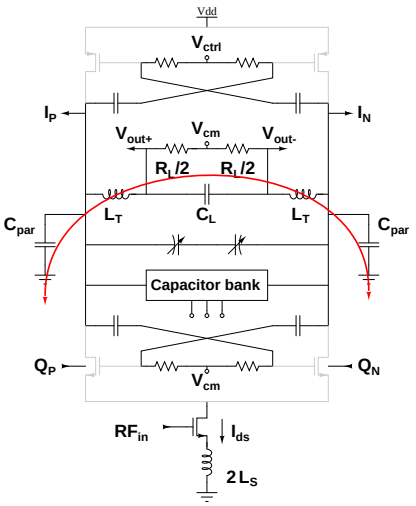
(a) First semiperiod



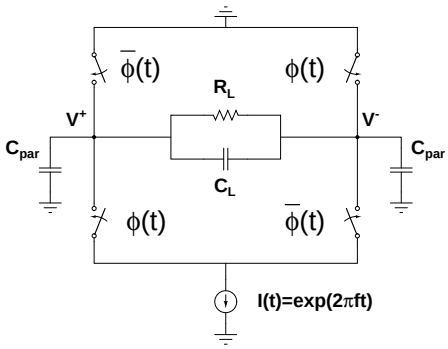
(b) Switching instant



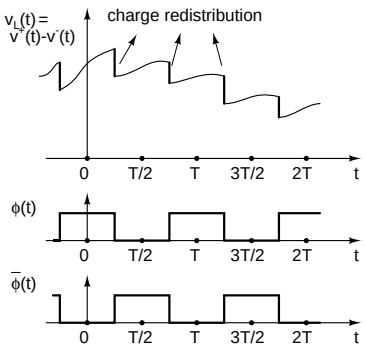
(c) Second semiperiod



(d) Second switching instant



(e) Simplified oscillator model



(f) Voltage waveform across C_{L} and driving phases.

Figure 1.12: Time-domain SOM analysis and simplified oscillator model

be expressed in the discrete time domain as

$$v^+\left(kT+\frac{T}{4}\right) = -\alpha v^-\left(kT-\frac{T}{4}\right) + \frac{q(kT+T/4)}{C_\mathrm{t}} \tag{1.18a}$$

$$v^-\left(kT+\frac{T}{4}\right) = 0 \tag{1.18b}$$

$$v^+\left(kT-\frac{T}{4}\right) = 0 \tag{1.18c}$$

$$v^-\left(kT-\frac{T}{4}\right) = -\alpha v^+\left((k-1)T+\frac{T}{4}\right) + \frac{q(kT-T/4)}{C_\mathrm{t}} \tag{1.18d}$$

where k is an integer index, T is the switching period,

$$\alpha = \frac{C_\mathrm{L}}{C_\mathrm{L}+C_\mathrm{par}} = \frac{C_\mathrm{L}}{C_\mathrm{t}} \tag{1.19}$$

is the charge sharing factor and

$$q(t) = \int_{t-T/2}^{t} i(\tau)d\tau \tag{1.20}$$

is the charge injected by the current source. In (1.18a) and (1.18d) the node voltages at a generic switching instant are expressed as a function of the same voltages in the previous instant and a term which accounts for the voltage variation in the semiperiod due to the current injected by the LNA[1]. Combining (1.18a)-(1.18d) we can calculate the differential voltage at the load $v_\mathrm{L} = v^+ - v^-$ getting

$$v_\mathrm{L}\left(kT+\frac{T}{4}\right) = v^+\left(kT+\frac{T}{4}\right) \tag{1.21a}$$

$$v_\mathrm{L}\left(kT-\frac{T}{4}\right) = -v^-\left(kT-\frac{T}{4}\right) \tag{1.21b}$$

i.e.

$$v_\mathrm{L}\left(kT+\frac{T}{4}\right) = \alpha v_\mathrm{L}\left(kT-\frac{T}{4}\right) + \frac{q(kT+T/4)}{C_\mathrm{t}} \tag{1.22a}$$

$$v_\mathrm{L}\left(kT-\frac{T}{4}\right) = \alpha v_\mathrm{L}\left((k-1)T+\frac{T}{4}\right) - \frac{q(kT-T/4)}{C_\mathrm{t}} \tag{1.22b}$$

which can be recast as:

$$v_\mathrm{L}\left(k\frac{T}{2}+\frac{T}{4}\right) = \alpha v_\mathrm{L}\left((k-1)\frac{T}{2}+\frac{T}{4}\right) + v_\mathrm{q}\left(k\frac{T}{2}+\frac{T}{4}\right) \tag{1.23}$$

where

$$v_\mathrm{q}\left(k\frac{T}{2}+\frac{T}{4}\right) = (-1)^\mathrm{k}\frac{q(kT/2+T/4)}{C_\mathrm{t}}. \tag{1.24}$$

[1]If the full RLC load were taken into account, the $v^-(s)/v^+(s)$ transfer function should be considered instead of α and the complete time-domain I-V relationship across the load network should be calculated. Since we are interested into the low frequency output voltage, we can neglect the inductor impedance and simplify the tank as in Figure 1.12(e); moreover, assuming a large C_L and a small C_par, it can be proved that $v^-(s)/v^+(s) \to \alpha$. Equations (1.18a)-(1.18d) remains therefore valid even in the case of the full RLC load.

Assuming without loss of generality that the input current is a tone with unitary amplitude at angular frequency $\omega = 2\pi(f_0 + f_\mathrm{m})$,

$$i(t) = e^{j\omega t} = e^{j2\pi f_0 t} e^{j2\pi f_\mathrm{m} t}, \tag{1.25}$$

the charge injected by the source is

$$q(t) = \int_{t-T/2}^{t} e^{j\omega\tau} d\tau = \frac{e^{j\omega t}}{j\omega}\left(1 - e^{-j\omega T/2}\right) \tag{1.26}$$

and (1.24) becomes

$$v_\mathrm{q}\left(k\frac{T}{2} + \frac{T}{4}\right) = e^{j\omega T/4} e^{j2\pi k\frac{T}{2}(f-f_0)} \frac{1 - e^{-j\omega T/2}}{j\omega C_\mathrm{t}}, \tag{1.27}$$

which simplifies in

$$\begin{aligned} v_\mathrm{q}\left(k\frac{T}{2}+\frac{T}{4}\right) &= 2\frac{e^{j2\pi f_\mathrm{m} kT/2}}{\omega C_\mathrm{t}} \cos\left(2\pi f_\mathrm{m}\frac{T}{4}\right) \\ &\approx 2\frac{e^{j2\pi f_\mathrm{m} kT/2}}{\omega C_\mathrm{t}} \end{aligned} \tag{1.28}$$

assuming that $2\pi f_\mathrm{m} T/4 \ll 1$. The discrete-time recursive equation expressing the evolution of the output voltage for a sinusoidal input current thus becomes

$$v_\mathrm{L}\left(k\frac{T}{2}+\frac{T}{4}\right) = \alpha v_\mathrm{L}\left((k-1)\frac{T}{2}+\frac{T}{4}\right) + 2\frac{e^{j2\pi f_\mathrm{m} kT/2}}{\omega C_\mathrm{t}}. \tag{1.29}$$

In the frequency domain, the voltage $V_\mathrm{L}^k(f_\mathrm{m})$ can be written as

$$\begin{aligned} V_\mathrm{L}^k(f_\mathrm{m}) &= \alpha V_\mathrm{L}^{k-1}(f_\mathrm{m}) + V_\mathrm{q}^k(f_\mathrm{m}) \\ &= \alpha e^{-j2\pi f_\mathrm{m} T/2} V_\mathrm{L}^k(f_\mathrm{m}) + V_\mathrm{q}^k(f_\mathrm{m}) \end{aligned} \tag{1.30}$$

which yields

$$V_\mathrm{L}^k(f_\mathrm{m}) = \frac{1}{1 - \alpha e^{-j2\pi f_\mathrm{m} T/2}} V_\mathrm{q}^k(f_\mathrm{m}). \tag{1.31}$$

Combining (1.31) and the Fourier transform of (1.28) we obtain the transfer function $H_\mathrm{D}(f_\mathrm{m})$ from the injected current to the output voltage

$$H_\mathrm{D}(f_\mathrm{m}) = \frac{1}{2\pi\ (f_0 + f_\mathrm{m}) C_\mathrm{t}} \cdot \frac{2\alpha}{e^{j2\pi f_\mathrm{m} T/2} - \alpha}. \tag{1.32}$$

The analysis carried out so far is only valid at discrete-time. Extending (1.23) to continuous-time we find

$$v_\mathrm{L}(t) = v_\mathrm{L,sum}(t) + v_\mathrm{L,int}(t) \tag{1.33}$$

where

$$v_\mathrm{L,sum}(t) = \sum_{k=-\infty}^{\ell} \left[\alpha v_L\left((k-1)\frac{T}{2}+\frac{T}{4}\right) + v_\mathrm{q}\left(k\frac{T}{2}+\frac{T}{4}\right)\right] \cdot \mathrm{rect}\left(\frac{t - kT/2}{T/2}\right) \tag{1.34}$$

and

$$v_{\mathrm{L,int}}(t) = \frac{(-1)^{\ell}}{C_{\mathrm{t}}} \int_{(\ell-1)T/2+T/4}^{t} i(\tau)d\tau. \tag{1.35}$$

$\ell = \left\lfloor \frac{t-T/4}{T/2} \right\rfloor$ is the index of the last switching event before t. Equation (1.33) expresses the evolution of the output voltage in the presence of the parasitic capacitances in the continuous-time domain; the summation term $v_{\mathrm{L,sum}}(t)$ is a train of rectangular functions taking into account the change in the load voltage due to the charge sharing phenomenon that occurs at every switching event; the integral term $v_{\mathrm{L,int}}(t)$ accounts for the contribution of the current source during the time elapsed from the latest switching event until the instant t.

We can now evaluate the Fourier transform of (1.33). Since the system is linear, superposition is used and the Fourier transforms of $v_{\mathrm{L,sum}}(t)$ and $v_{\mathrm{L,int}}(t)$ are evaluated separately. The summation term $v_{\mathrm{L,sum}}(t)$ is the zero-order-hold interpolation of (1.23) and expresses the behavior of the system due to charge-sharing, giving rise to the conversion gain derived in (1.32). For the integral term $v_{\mathrm{L,int}}(t)$, the frequency domain relationship between the injected current $i(t)$ and the load voltage $v_{\mathrm{L,int}}(t)$ can be calculated according to the theory of linear time-varying (LTV) networks [Zadeh 50], [Signell 77]. Specifically, the input current $i(t)$ and the output voltage $v_{\mathrm{L,int}}(t)$ are related by means of a system function $Z(f;t)$ (dependant on both frequency and time), which is a generalization of the transfer function in a LTI systems. Among many possible definitions of the system function, the most useful is [Zadeh 50]

$$Z(f;t) = \left. \frac{v_{\mathrm{L,int}}(t)}{i(t)} \right|_{i(t)=e^{j2\pi ft}} \tag{1.36}$$

i.e. the ratio between the output of the system $v_{\mathrm{L,int}}(t)$ and its input $i(t)$ when the system is driven by a tone $i(t) = e^{j2\pi ft}$. since the system is periodically time-variant with period $T = 1/f_0$, (1.36) can be expressed as

$$Z(f;t) = \sum_n H_{\mathrm{n}}(f) e^{j2\pi n f_0 t}, \tag{1.37}$$

i.e. with a Fourier expansion with frequency-dependent coefficients, indicating that the tone injected at f gives rise to a set of tones at frequencies $nf_0 + f$ at the output, and making explicitly available all the conversion gains $H_{\mathrm{n}}(f)$ (figure 1.13). The conversion gain we are seeking is the one which translates the frequency from $f = f_0 + f_{\mathrm{m}}$ to f_{m}, so we are only interested in computing the term $H_{\text{-}1}(f_0 + f_{\mathrm{m}})$.

To ease the computation of $H_{\text{-}1}(f_0 + f_{\mathrm{m}})$, it is more convenient to write the integral term $v_{\mathrm{L,int}}(t)$ as a difference of convolutions

$$v_{\mathrm{L,int}}(t) = \phi(t) \cdot [\phi \cdot i * w(t)] - \overline{\phi}(t) \cdot [\overline{\phi} \cdot i * w(t)] \tag{1.38}$$

where $\phi(t)$ and $\overline{\phi}(t)$ are the periodic waveforms driving the system of Fig. 1.12(f), $i(t)$ is the injected current and

$$w(t) = \frac{1}{C_{\mathrm{t}}} \mathrm{rect}\left(\frac{t - T/4}{T/2} \right) \tag{1.39}$$

is the impulse response of the load windowed by the semiperiod $[0, T/2]$, due to the periodic behavior of the circuit.

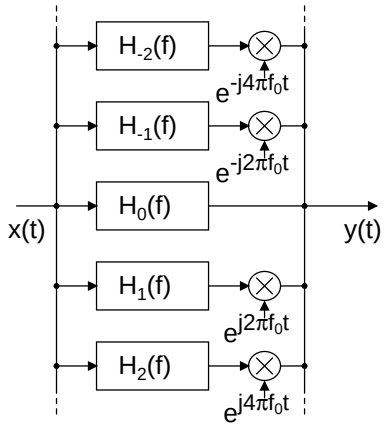


Figure 1.13: LTV decomposition

In Eqn. (1.38) the output voltage $v_{\mathrm{L,int}}(t)$ is expressed as the difference of the voltages at the oscillating nodes, $v^{+}(t)$ and $v^{-}(t)$ respectively. With reference to Figure 1.12(e), when $\phi(t) = 1$ the voltage $v^{+}(t)$ is given by the convolution between the injected LNA current and the impulse response of the load; when $\phi(t) = 0$, $v^{+}(t)$ is an AC ground:

$$v^{+}(t) = \begin{cases} i \cdot \phi * w(t) & \text{for } \phi(t) = 1 \\ 0 & \text{elsewhere;} \end{cases} \tag{1.40}$$

$v^{-}(t)$ is given by the same convolution when $\overline{\phi}(t) = 1$, while is an AC ground when $\overline{\phi}(t) = 0$:

$$v^{-}(t) = \begin{cases} i \cdot \overline{\phi} * w(t) & \text{for } \overline{\phi}(t) = 1 \\ 0 & \text{elsewhere;} \end{cases} \tag{1.41}$$

the difference of the terms results in Eqn. (1.38). The frequency dependent Fourier coefficients $H_{\mathrm{n}}(f)$ in (1.37) can now be computed from (1.38) and are given by

$$H_{\mathrm{n}}(f) = \sum_{k} \Phi_{n-k}\Phi_{\mathrm{k}} W(f + kf_0) - \sum_{k} \overline{\Phi}_{\mathrm{n\text{-}k}}\overline{\Phi}_{\mathrm{k}} W(f + kf_0), \tag{1.42}$$

Φ_{k} and $\overline{\Phi}_{\mathrm{k}}$ being the Fourier coefficients of the series expansion of $\phi(t)$ and $\overline{\phi}(t)$ respectively, and $W(f)$ the Fourier transform of $w(t)$. Since $\overline{\phi}(t) = \phi(t - T/2)$, than $\overline{\Phi}_{\mathrm{k}} = \Phi_{\mathrm{k}} e^{-j\pi k}$ and (1.42) becomes

$$\begin{aligned} H_{\mathrm{n}}(f) &= \sum_{k} \Phi_{\mathrm{n\text{-}k}}\Phi_{\mathrm{k}}(1 - e^{-jn\pi}) W(f + kf_0) \\ &= \begin{cases} \sum_k 2\Phi_{\mathrm{n\text{-}k}}\Phi_{\mathrm{k}} W(f + kf_0) & \text{for odd n,} \\ 0 & \text{otherwise,} \end{cases} \end{aligned} \tag{1.43}$$

with

$$\Phi_k = \begin{cases} 1/2 & \text{k=0,} \\ (-1)^{\frac{|k|-1}{2}}/(|k|\pi) & \text{k odd,} \\ 0 & \text{otherwise.} \end{cases} \tag{1.44}$$

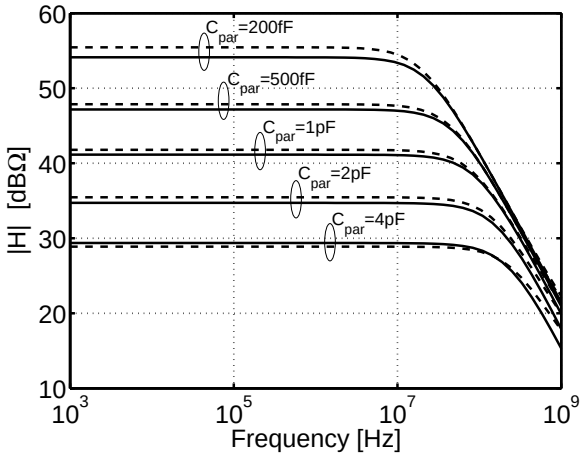


Figure 1.14: Frequency response comparison between simulation (solid line) and theory (dashed line).

For $n = -1$ the only non-null terms in (1.43) are those for $k = 0$ and $k = -1$. Consequently:

$$\begin{aligned} H_{\text{-1}}(f_0 + f_\text{m}) =& 2\Phi_{\text{-1}}\Phi_0 W(f_0 + f_\text{m}) + 2\Phi_0\Phi_{\text{-1}} W(f_\text{m}) \\ =& \frac{1}{2\pi C_\text{t} f_0}\left[\text{sinc}\left(\frac{f_0 + f_\text{m}}{2f_0}\right) e^{-j\pi(f_0+f_\text{m})/(2f_0)} + \text{sinc}\left(\frac{f_\text{m}}{2f_0}\right) e^{-j\pi f_\text{m}/(2f_0)}\right] \\ \approx& \frac{1}{2\pi C_\text{t} f_0}\left(1 - j\frac{2}{\pi}\right) \end{aligned} \tag{1.45}$$

where the approximation holds for $f_\text{m} \ll f_0$.

Using linearity, we take into account both the contribution coming from the summation term and the integral term in (1.33) by combining (1.32) and (1.45) to get

$$H(f_\text{m}) = \frac{1}{2\pi(f_0+f_\text{m})C_\text{t}}\left[\frac{2\alpha}{e^{j2\pi f_\text{m} T/2} - \alpha} + 1 - j\frac{2}{\pi}\right]. \tag{1.46}$$

Finally, the impact of R_L in parallel to C_L is very well captured by taking into account the discharge of C_L on R_L across the semiperiod, and substituting

$$\alpha_\text{R} = \alpha \cdot e^{-\frac{T/2}{R_\text{L} C_\text{L}}} \tag{1.47}$$

for α in (1.46). The $T/2$ term in (1.47) is the discharge time.

The validity of (1.46) combined with (1.47) was verified by means of transistor-level simulations. The values of the circuit components are the same as used in the implemented design, i.e. $f_0 = 2.4\,\text{GHz}$, $R_\text{L} = 10.3\ \text{k}\Omega$, $C_\text{L} = 8.3\,\text{pH}$, with C_par ranging from 200 fF to 4 pF. Good agreement between theory and simulations is obtained for both the gain and the bandwidth as shown in Figure 1.14. For comparison, note that the conversion gain without including C_par is $2R_\text{L}/\pi = 76.0\ \text{dB}\Omega$, a misleading result.

To get further insight in (1.46), we study its behavior for small offsets from the carrier; for $f_\text{m} \ll f_0$ the transfer function can be approximated as

$$H(f_\text{m}) \approx \frac{1}{2\pi f_0 C_\text{t}}\left[\frac{2\alpha_\text{R}}{1 - \alpha_\text{R} + j\pi f_\text{m}/f_0} + 1 - j\frac{2}{\pi}\right]. \tag{1.48}$$

Typically, the parasitic capacitance C_{par} is small with respect to the load C_{L} and the first term inside the brackets of (1.48) is dominant. The transfer function then shows an in-band gain

$$|H_0| = \frac{1}{\pi f_0 C_{\text{t}}} \frac{\alpha_{\text{R}}}{1-\alpha_{\text{R}}} \tag{1.49}$$

while the $-3\,\text{dB}$ bandwidth is

$$f_{\text{-3dB}} = \frac{f_0}{\pi}(1-\alpha_{\text{R}}). \tag{1.50}$$

Interestingly, assuming that $R_{\text{L}} \gg T/(2C_{\text{L}})$, $\alpha_{\text{R}} \approx \alpha$ and (1.49) becomes

$$|H_0| = \frac{1}{\pi f_0 C_{\text{t}}} \frac{C_{\text{L}}}{C_{\text{par}}} \approx \frac{2}{\pi} \frac{T/2}{C_{\text{par}}}, \tag{1.51}$$

showing that the cyclically charged capacitance C_{par} behaves as an equivalent switched-capacitor resistance $T/2C_{\text{par}}$, limiting the attainable low-frequency transimpedance gain. The $-3\,\text{dB}$ bandwidth (1.50) results in

$$f_{\text{-3dB}} = \frac{f_0}{\pi(1+C_{\text{L}}/C_{\text{par}})} \tag{1.52}$$

motivating the increase in bandwidth for larger C_{par} shown in Figure 1.14.

Finally, if $C_{\text{par}} = 0$ then $\alpha_{\text{R}} \approx 1 - T/(2R_{\text{L}}C_{\text{L}})$ and (1.49) becomes

$$|H_0| = \frac{2}{\pi} R_{\text{L}}, \tag{1.53}$$

which agrees with (1.17), while (1.50) reduces to

$$f_{\text{-3dB}} = \frac{1}{2\pi\, C_{\text{L}} R_{\text{L}}} \tag{1.54}$$

so that the low-frequency gain predicted by the standard but incomplete LTI analysis is recovered.

1.4 Experimental results and discussion

A circuit prototype was fabricated in a 1P9M 90 nm CMOS process with a $3\,\mu m$ thick top metal available for high-Q inductors. Fig. 1.15 shows the chip photograph. The two cross-coupled SOM are clearly recognizable; only three integrated inductors are used, resulting in a compact layout; the chip size is $700\,\mu m \times 700\,\mu m$ including the pads.

An evaluation PCB for interfacing the chip to the measurement setup was developed. The board, built on a FR4 substrate, includes a $50\,\Omega$ microstrip for the single-ended input RF signal on which an external high-Q thin-film SMD inductor is placed to complete the matching network. Two high-speed low-distortion differential to single-ended conversion stages from Maxim Semiconductor (MAX4444) are used at the output to pick up the differential I and Q output signals and drive the input of the Agilent E4407B ESA-E spectrum analyzer.

Due to the available values of the external inductor, input matching was obtained at 2.2 GHz. The input reflection coefficient was measured with an Agilent E8361A network analyzer and is depicted in Figure 1.16(b), showing a return loss below -10 dB in the 2.18

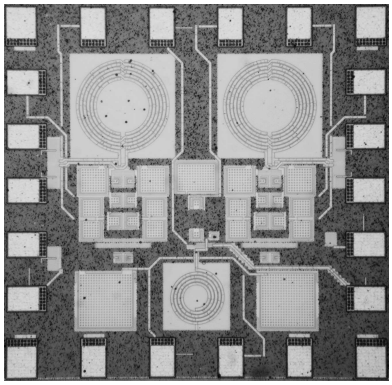
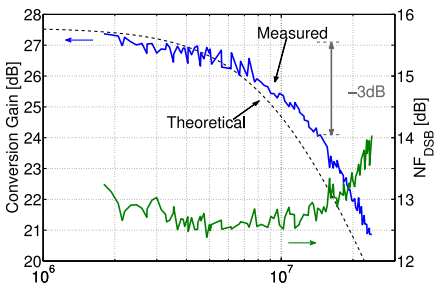
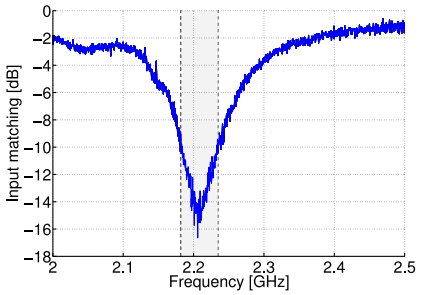


Figure 1.15: Microphotograph of the front-end (chip size is $700\,\mu m \times 700\,\mu m$).



(a) Theoretical (dashed line) vs. measured (solid line) conversion gain; NF



(b) Measured input matching. The shaded area represents the frequency range in which S_{11} < -10 dB.

Figure 1.16: Frequency response of the receiver

to 2.23 GHz range. The conversion gain of the front-end is plotted in Fig. 1.16(a) (blue solid line), showing a low-frequency gain of 27.1 dB with a -3 dB bandwidth of 14 MHz. This measured performance is compared to that predicted by our LTV analysis (dashed line); the equivalent transconductance (1.16) used for the comparison was estimated in 20.4 mS, while the parasitic capacitance C_{par} loading the oscillator nodes, which includes the intrinsic transistor capacitance, the load parasitics and the contribution introduced by the cross-coupled wires, was derived from a parasitic extraction from the layout and was set to 100 fF. The error in the prediction is below 1.5 dB and is mainly imputed to spreads in the process. The double sideband NF is also reported in Figure 1.16(a) (green solid line); it ranges from 12.4 to 13.2 dB with a flicker corner frequency of about 200 kHz. The input referred 1 dB compression point is -23.7 dBm evaluated at the output IF frequency of 1 MHz. The LO can be tuned to span the entire band from 1.96 GHz to 2.58 GHz, corresponding to a 27% tuning range. The LO leakage measured at the input port is below -52 dBm. The entire front-end draws 1.3 mA from a 1 V supply.

The performance of the receiver is summarized in Table 1.3 and a comparison with recently published receivers working in the L- or S-bands is shown. Our solution proves to be particularly competitive in terms of power dissipation and area consumption.

Table 1.3: Performance Comparison with Recently Published Low Power Receivers

	[Liscidini 06]	[Liscidini 08], [Liscidini 08b]	[Allstot 09]	[Järvinen 05]	[Song 07]	[Stanić 08]	This
Tech. [nm]	130	90	130	130	180	90	90
Freq. [GHz]	1.57	2.4	1.58	2.0	2.4	2.4	2.2
V_{DD} [V]	1.2	1.2	1	1.2	1.0	0.5	1.0
P_{DC} [mW]	5.4	3.6	7.2(1)	3.4	1.1(2)	8.5	1.3
Gain [dB]	36	75(3)	42.5	47(3)	30.5	30(3)	27
BW [MHz]	10	2	n/a	n/a	> 50	3.1	14
NF [dB]	4.8	12	6.5	28	10.1	18	13
iP_{1dBcp} [dBm]	-31	n/a(4a)	n/a	n/a(4b)	-31	-31	-23.7
Area [mm^2]	1.5(5)	0.35(5)	3.1(5)	1.0(5)	2.3	3.4	0.49

(1) Includes RF front-end, PLL, IF amplifiers and quadrature $\Sigma\Delta$ ADC.
(2) Single downconversion path. Power consumption is 0.5 mW for the RF signal and 0.6 mW for the generation of the LO.
(3) Baseband variable-gain amplifier included.
(4a) Input referred IP_3 of -13 dBm. (4b) Input referred IP_3 of -21 dBm.
(5) Active area only.

1.5 Conclusions

A 2.2 GHz low-power low-voltage CMOS receiver front-end suitable for both direct-conversion and low-IF architectures is presented. The efficient current-reuse topology, the digital CMOS implementation and the compact layout make this downconverter attractive for highly integrated low-cost devices. A detailed linear time-variant analysis on the impact of the parasitic capacitances loading the self-oscillating mixer is discussed, leading to an accurate analytical expression for the conversion gain of the receiver which validity is verified by means of transistor-level simulations and prototype measurements.

Chapter 2

Linear low-noise X-band upconverter

In this chapter we will develop a frequency upconverter for an X-band Frequency-Modulated Continuous-Wave tracking radar system. A tracking radar is capable of determining the direction, the distance and the relative velocity of a target by transmitting an EM wave and measuring the echoed signal.

2.1 Overview of radar systems

Tracking radars find application in:

Traffic surveillance. Air or maritime traffic control.

Military applications. Air, ground and sea targets location; missile defense/guidance.

Automotive. Driver assistance and safety applications: Adaptive Cruise Control (ACC), blind spot detection, collision mitigation, side impact / rear impact warning, lane change assistance.

The determination of the distance/velocity of the target(s) requires that the frequency of the transmitted EM wave is changed with time; in Frequency-Modulated Continuous-Wave (FMCW) radars, a LO reference carrier is frequency modulated by a baseband signal typically generated in the digital domain. As will be seen analytically in this chapter, the possibility to detect objects at high distance requires

- a high transmitter output power;
- a low receiver noise figure;

while a high spatial/velocity resolution of the targets can be achieved by means of

- an extremely low phase noise the modulated carrier;
- a high signal-to-spur ratio of the transmitted signal.

In the following, a brief overview of radar systems is given, motivating the need for accurate frequency modulation of the transmitted signal. The system architecture is than introduced; the issues in the design of the core of the FMCW radar front-end, i.e. the upconverter, are outlined.

(a) Drive assistance/collision avoidance

(b) Long-range military surveillance

(c) Air traffic monitoring

Figure 2.1: Radar applications

2.1.1 Classification of radar systems

Architecture. From a system-level point of view, radar systems are classified as:

- *monostatic radar.* The transmitter and the receiver share a common antenna; a T/R switch with low losses and high isolation is required;
- *bistatic radar.* The transmitter and the receiver are separated by a distance that is comparable to the expected target distance;
- *pseudo-monostatic radar.* The transmitter and the receiver use two different antennas but their spatial separation is small compared to the expected target distance; the the bistatic angle, i.e. the angle subtended between transmitter, target and receiver is close to zero.

Transmitted signal. Depending on the type of transmitted signal, the following distinction is possible:

- *Pulse Radar.* Pulses of RF energy are irradiated in the space.
- *Continuous-Wave (CW) radar.* A continuous sine wave is irradiated.

In the following we will focus our attention to CW radars, which provides greater flexibility than pulse radar; in particular, we will motivate the need for a frequency modulation of the transmitted sine wave to determine the target distance, leading to the implementation of a Frequency-Modulated Continuous-Wave radar system.

2.1.2 The radar range equation

In this section we will review the basic principles of (monostatic) radar systems. We will determine the expression of the power which is reflected back to the radar when a target is illuminated by the transmitted radiation and the radar range equation which links the target distance to the transmitted power and the signal-to-noise ratio of the received signal. Various types of losses are identified, leading to the definition of the *maximum detection range* and of the *minimum resolvable radar cross-section.*

Received power. Assume that the radar is transmitting a signal with power P_t. At a distance R, the transmitted power density Q_t is

$$Q_\mathrm{t} = \frac{P_\mathrm{t} G_\mathrm{t}}{4\pi R^2} \tag{2.1}$$

where G_t is the *transmit antenna gain* of the anisotropic transmitter. If a target at distance R is illuminated by the incident transmitted signal, it becomes itself an isotropic source of radio waves, part of which are propagated back to the radar; the reflected power P_refl is proportional to the incident power density Q_t according to a constant σ called *radar cross-section (RCS)*, which depends on

- the physical size of the target,
- the shape of the target, and
- the materials of the surface of the target.

The reflected power thus becomes

$$P_\mathrm{refl} = \sigma Q_\mathrm{t} = \frac{P_\mathrm{t} G_\mathrm{t} \sigma}{4\pi R^2}. \tag{2.2}$$

The received power density Q_r at the radar (assuming a monostatic radar) is

$$Q_\mathrm{r} = \frac{P_\mathrm{refl}}{4\pi R^2} = \frac{P_\mathrm{t} G_\mathrm{t} \sigma}{(4\pi)^2 R^4}, \tag{2.3}$$

giving rise to a received power P_r

$$P_\mathrm{r} = A_\mathrm{e} Q_\mathrm{r} = \frac{P_\mathrm{t} G_\mathrm{t} A_\mathrm{e} \sigma}{(4\pi)^2 R^4} \tag{2.4}$$

where A_e is the *effective antenna area.* The effective antenna area is usually expressed in term of the *receive antenna gain* G_r

$$G_\mathrm{r} = \frac{4\pi A_\mathrm{e}}{\lambda^2} \tag{2.5}$$

with λ the carrier wavelength. The received power P_r (2.4) becomes

$$P_\mathrm{r} = \frac{P_\mathrm{t} G_\mathrm{t} G_\mathrm{r} \lambda^2 \sigma}{(4\pi)^3 R^4}, \tag{2.6}$$

which is the basic form of the radar range equation.

Receiver thermal noise. The (weak) received signal is corrupted by additional noise. The sources of noise are

- cosmic noise, originating in the outer space, which is a significant contributor for frequencies below 1 GHz,
- solar noise, generated by the sun, which is a significant contributor due to its proximity but is usually reduced by the directional gain of the antenna (assuming that the antenna is not pointed directly towards the sun), and
- thermal noise generated in the radar receiver, which is typically the main contributor.

Assuming that the receiver thermal noise is the main contributor, the power of the noise P_{n} is given by

$$P_{\mathrm{n}} = kT_{\mathrm{n}}B = kT_0(F-1)B_{\mathrm{r}} \tag{2.7}$$

with k the Boltzmann's constant, T_{n} the noise temperature, T_0 the reference temperature $290K$, B_{r} the receiver bandwidth and F the receiver noise factor. Being the signal-to-noise ratio (SNR) the ratio between the signal power P_{r} and the noise power P_{n}, the radar range equation (2.6) can be recast as

$$SNR = \frac{P_{\mathrm{t}}G_{\mathrm{t}}G_{\mathrm{r}}\lambda^2\sigma}{(4\pi)^3R^4kT_0(F-1)B_{\mathrm{r}}}. \tag{2.8}$$

Losses. In real radar systems, the received signal power is typically lower than that predicted by (2.6) and (2.8) due to various sources of signal loss:

- the transmitter loss L_{t}, due to some loss of transmitted power from the transmitter to the antenna, the T/R switch,
- the receiver loss L_{r}, due to similar phenomena occurring in the receiver,
- the atmospheric loss L_{atm}, i.e. the attenuation of the signal through the atmosphere due to the interaction between the EM wave and oxygen molecules/water vapor, and to propagation effects like diffraction/refraction/multipath propagation, and
- the signal processing loss L_{sp}.

The total system loss Ls is defined as the product of the above losses:

$$L_{\mathrm{s}} = L_{\mathrm{t}}L_{\mathrm{r}}L_{\mathrm{atm}}L_{\mathrm{sp}}; \tag{2.9}$$

the resulting radar range equation accounting for signal losses is

$$SNR = \frac{P_{\mathrm{t}}G_{\mathrm{t}}G_{\mathrm{r}}\lambda^2\sigma}{(4\pi)^3R^4kT_0(F-1)B_{\mathrm{r}}L_{\mathrm{s}}}. \tag{2.10}$$

Detection range. The maximum detection range for a given SNR is easily determined solving (2.10) for R, leading to

$$R_{det} = \left[\frac{P_{\mathrm{t}}G_{\mathrm{t}}G_{\mathrm{r}}\lambda^2\sigma}{(4\pi)^3SNRkT_0(F-1)B_{\mathrm{r}}L_{\mathrm{s}}}\right]^{\frac{1}{4}}. \tag{2.11}$$

The above equation must be used with care, since the atmospheric loss L_{atm} in L_{s} is range-dependent.

Minimum detectable RCS. The minimum detectable radar cross-section $\sigma_{\min}$ is found when the minimum signal-to-noise ratio $SNR_{\min}$ which still guarantees a reliable detection is used. Solving (2.10) for σ yelds to

$$\sigma_{\min} = SNR_{\min} \frac{(4\pi)^3 R^4 k T_0 (F-1) B_{\mathrm{r}} L_{\mathrm{s}}}{P_{\mathrm{t}} G_{\mathrm{t}} G_{\mathrm{r}} \lambda^2}. \tag{2.12}$$

2.1.3 Determination the target velocity: the CW Doppler radar

The simplest form of continuous-wave radar is the Continuous Wave Doppler radar, in which a sinusoidal RF tone at a constant frequency is transmitted and the echoed signal is evaluated [Lübbert 05]. By Doppler effect, from the measurement of the difference between the transmitted and the received signal frequencies it is possible to evaluate the target radial velocity v_{r} (see Figure 2.2).

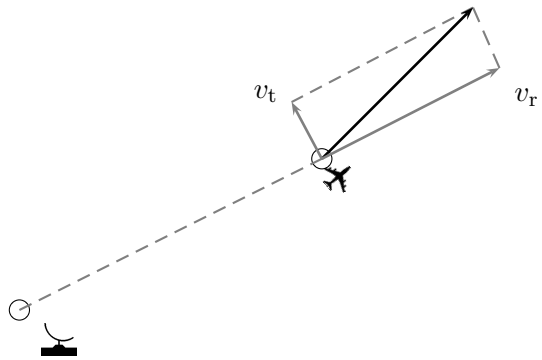


Figure 2.2: Target velocity decomposition

The architecture of a CW Doppler radar is depicted in Figure 2.3.

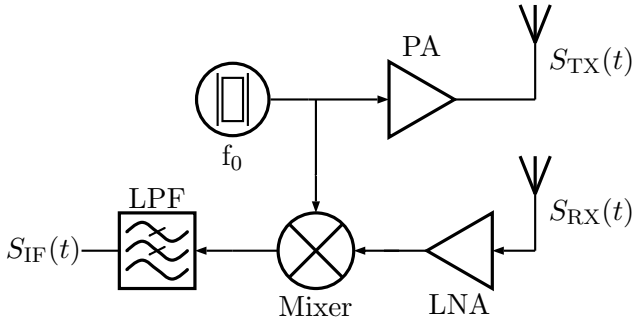


Figure 2.3: CW Doppler radar

According to the Doppler effect, the relationship between the observed frequency f and the emitted frequency f_0 when the transmitter and the observer are in relative motion is given by

$$f = \frac{v + v_{\mathrm{r}}}{v + v_{\mathrm{t}}} f_0 \tag{2.13}$$

where

- v is the velocity of the wave in the medium (here assumed to be equal to the speed of light in the vacuum c),
- v_r is the radial velocity of the receiver/observer relative to the medium assumed positive for a receiver moving towards the transmitter, and
- v_t is the radial velocity of the transmitter relative to the medium assumed positive for a transmitter moving away from the transmitter.

Let's assume that the transmitting radar is stationary $v_\mathrm{t} = 0$ whilst the target is moving toward the transmitter with a radial velocity v_r; assuming that the radar irradiates a signal with frequency f_0, the frequency f_1 received by the target is

$$f_1 = \frac{c + v_\mathrm{r}}{c + 0} f_0. \tag{2.14}$$

The echoed signal with frequency f_1 is reflected back to the radar. The frequency f_rx received by the radar is

$$f_\mathrm{rx} = \frac{c + 0}{v - v_\mathrm{r}} f_1 = \frac{c + v_\mathrm{r}}{c - v_\mathrm{r}} f_0. \tag{2.15}$$

The difference between the frequency received by the radar f_rx and the transmitted frequency f_0, called the Doppler frequency f_d, is

$$f_\mathrm{d} = f_\mathrm{rx} - f_0 = \frac{2v_\mathrm{r}}{c - v_\mathrm{r}} f_0 \approx \frac{2v_\mathrm{r}}{c} f_0 \tag{2.16}$$

where $v_\mathrm{r} \ll c$ is reasonably assumed. Recasting eqn. (2.16) we can express the target radial velocity v_r as

$$v_\mathrm{r} = \frac{c}{2} \frac{f_\mathrm{d}}{f_0}. \tag{2.17}$$

Two fundamental observation follows:

- only the radial component of the target velocity v_r can be determined, whilst nothing can be said about the transverse velocity v_t, and
- the distance between the radar and the target can not be determined.

To overcome the second limitation, a frequency modulation of the transmitted signal is required.

2.1.4 Determination the target distance: the FMCW radar

In a Frequency-Modulated Continuous-Wave (FMCW) radar, the transmitted signal is frequency modulated according to a given law. Both the target radial velocity and its distance can be determined [Lübbert 05], [Stove 92]. The architecture of a FMCW Doppler radar is depicted in Figure 2.4.
In a Frequency-Modulated Continuous-Wave the transmitted signal $S_\mathrm{TX}(t)$ has the form

$$S_\mathrm{TX}(t) = S_\mathrm{TX} \cdot \cos\left(\varphi_\mathrm{TX}(t)\right), \tag{2.18}$$

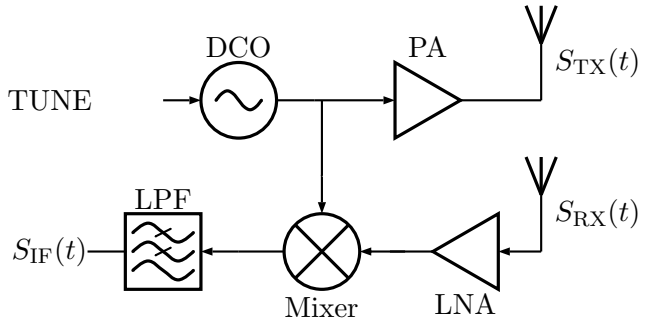


Figure 2.4: FMCW radar

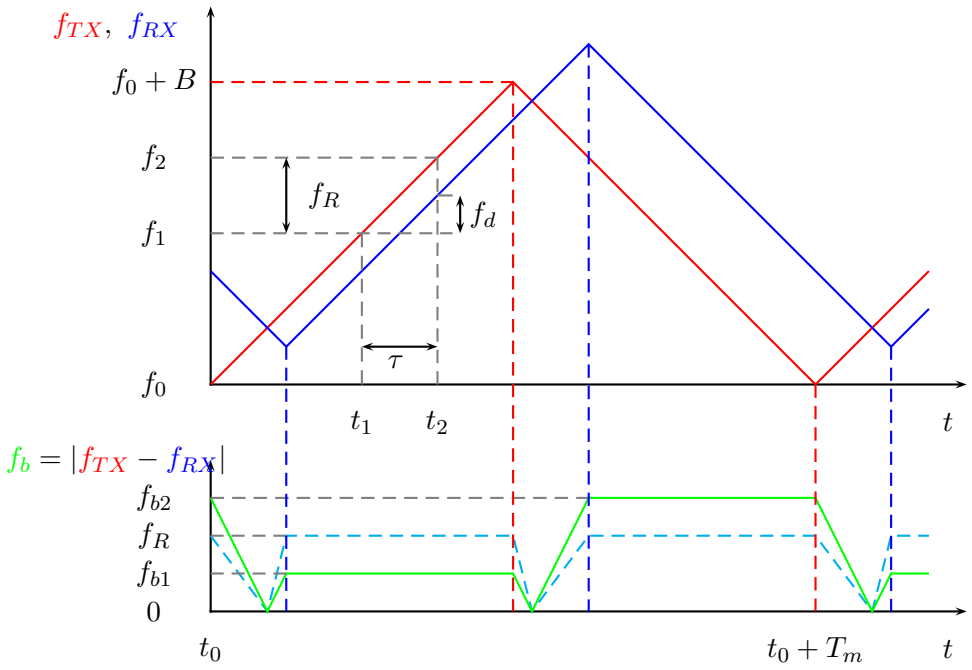


Figure 2.5: Linear FMCW waveforms

i.e. a sinusoid with a constant amplitude S_{TX} and an instantaneous phase $\varphi_{\mathrm{TX}}(t)$ given by

$$\varphi_{\mathrm{TX}}(t) = 2\pi \int_{t_0}^{\mathrm{t}} f(\tau) d\tau. \tag{2.19}$$

The most common kind of Frequency Modulation is the Linear Frequency Modulation, in which the carrier frequency increases linearly with time:

$$f(t) = f_0 + \alpha t. \tag{2.20}$$

We will assume for the moment that the frequency increases of B Hz in an interval of length $T_{\mathrm{m}}/2$ sec; the motivation of this choice will become clear later. The slope α is therefore

$$\alpha = \frac{2B}{T_{\mathrm{m}}}. \tag{2.21}$$

The phase $\varphi_{\mathrm{TX}}(t)$ of the transmitted signal becomes

$$\varphi_{\mathrm{TX}}(t) = 2\pi \left[f_0 t_0 - f_0 t + \alpha \frac{t_0^2}{2} - \alpha \frac{t^2}{2} \right]. \tag{2.22}$$

The received signal $S_{RX}(t)$ is a delayed and attenuated version of the transmitted signal

$$S_{\mathrm{RX}}(t) = S_{\mathrm{RX}} \cdot \cos\left(\varphi_{\mathrm{TX}}(t-\tau)\right) \tag{2.23}$$

where τ is the signal time of flight from the transmitter to the target and back; assuming a target moving with constant radial velocity v_{R}, the signal time of flight τ results in

$$\tau = 2\frac{r_0 + v_{\mathrm{R}} t}{c}, \tag{2.24}$$

where r_0 is the distance at time t_0 and c the speed of light. With the linear modulation given by (2.20) and (2.21), the instantaneous phase of the received signal $\varphi_{\mathrm{RX}}(t)$ becomes

$$\varphi_{\mathrm{RX}}(t) = \varphi_{\mathrm{TX}}(t-\tau) = 2\pi \left[f_0 t_0 - f_0 (t-\tau) + \alpha \frac{t_0^2}{2} - \alpha \frac{(t-\tau)^2}{2} \right] \tag{2.25}$$

The IF signal at the output of the receiver mixer is

$$S_{\mathrm{IF}}(t) = S_{\mathrm{IF}} \cdot \cos\left(\varphi_{\mathrm{TX}}(t) - \varphi_{\mathrm{RX}}(t)\right), \tag{2.26}$$

with an instantaneous phase $\varphi_{\mathrm{IF}}(t) = \varphi_{\mathrm{TX}}(t) - \varphi_{\mathrm{RX}}(t)$ of

$$\varphi_{\mathrm{IF}}(t) = 2\pi \left[f_0 \tau + \alpha \tau t - \alpha \frac{\tau^2}{2} \right] \tag{2.27}$$

$$\approx 2\pi \left[f_0 \tau + \alpha \tau t \right] \tag{2.28}$$

where the approximation holds for $\tau / T_{\mathrm{m}} \ll 1$, which is typically the case. Substituting the expression of τ and α leads to

$$\varphi_{\mathrm{IF}}(t) = 2\pi \left[\frac{2 f_0 r_0}{c} + \left(\frac{2 f_0 v_{\mathrm{R}}}{c} + \frac{4 B r_0}{T_{\mathrm{m}} c} \right) t + \frac{4 B v_{\mathrm{R}}}{T_{\mathrm{m}} c} t^2 \right]. \tag{2.29}$$

The last term in (2.29) is called Range-Doppler Coupling and can be neglected; the intermediate frequency f_{IF} is therefore

$$f_{\mathrm{IF}} = \frac{1}{2\pi} \frac{\partial}{\partial t} \varphi_{\mathrm{IF}}(t) = \frac{2 f_0}{c} v_{\mathrm{R}} + \frac{4B}{T_{\mathrm{m}}} \frac{r_0}{c}, \tag{2.30}$$

which can be rearranged as

$$v_{\mathrm{R}} = \frac{c}{2 f_0} f_{\mathrm{IF}} - \frac{2B}{T_{\mathrm{m}}} \frac{r_0}{f_0}. \tag{2.31}$$

For a given measured f_{IF}, infinite solutions (v_{R}, r_0) are possible. This can also be observed in the range-velocity diagram of figure Figure 2.6. For the resolution of the ambiguity, a second frequency sweep with different slope is needed. Let's assume, for simplicity, that in the next $T_{\mathrm{m}}/2$ interval the frequency of the modulated decreases linearly with an inverse slope, i.e. $\alpha_{\mathrm{down}} = -\alpha_{\mathrm{up}}$; let's further assume the period T_{m} is small enough such that the target velocity v_{R} and distance r_0 is not varied significantly. With reference

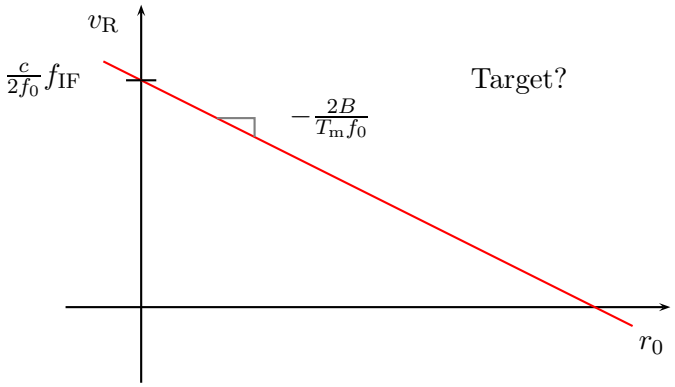


Figure 2.6: Single chirp range-velocity diagram

to Fig. 2.5, during the first semiperiod (called *up-chirp*) the frequency slope is positive and the intermediate frequency $f_{\mathrm{IF,up}}$ is measured, leading to

$$v_\mathrm{R} = \frac{c}{2f_0} f_{\mathrm{IF,up}} - \frac{2B}{T_\mathrm{m}} \frac{r_0}{f_0}; \tag{2.32a}$$

During the second semiperiod (called *down-chirp*) the frequency slope is negative and the intermediate frequency $f_{\mathrm{IF,down}}$ is measured; a similar calculation leads to

$$v_\mathrm{R} = -\frac{c}{2f_0} f_{\mathrm{IF,down}} + \frac{2B}{T_\mathrm{m}} \frac{r_0}{f_0}. \tag{2.32b}$$

Combining (2.32a) and (2.32b), we are finally able to determine both the target radial velocity v_R and its distance r_0:

$$v_\mathrm{R} = c\,\frac{f_{\mathrm{IF,up}} - f_{\mathrm{IF,down}}}{4f_0} \tag{2.33a}$$

$$r_0 = c\,\frac{f_{\mathrm{IF,up}} + f_{\mathrm{IF,down}}}{8B} T_\mathrm{m}. \tag{2.33b}$$

Graphically, the resolution of the ambiguity leads to the range-velocity diagram of Figure 2.7.

Being the received beat signals at $f_{\mathrm{IF,up}}$ and $f_{\mathrm{IF,down}}$ rectangular signals with period $T_\mathrm{m}/2$, their Fourier transform are $\mathrm{sinc}(\cdot)$ functions centered at f_0 with the first zero crossing at $2/T_\mathrm{m}$ from the peak. The minimum resolvable frequency is therefore given by

$$\Delta f = 2/T_\mathrm{m}. \tag{2.34}$$

Combining (2.34) with (2.33a) and (2.33b) leads to the determination of the target radial velocity resolution Δv_r

$$\Delta v_\mathrm{r} = \frac{c}{f_0} \frac{1}{T_\mathrm{m}} \tag{2.35a}$$

and the target distance resolution Δr_0

$$\Delta r_0 = \frac{c}{2B}. \tag{2.35b}$$

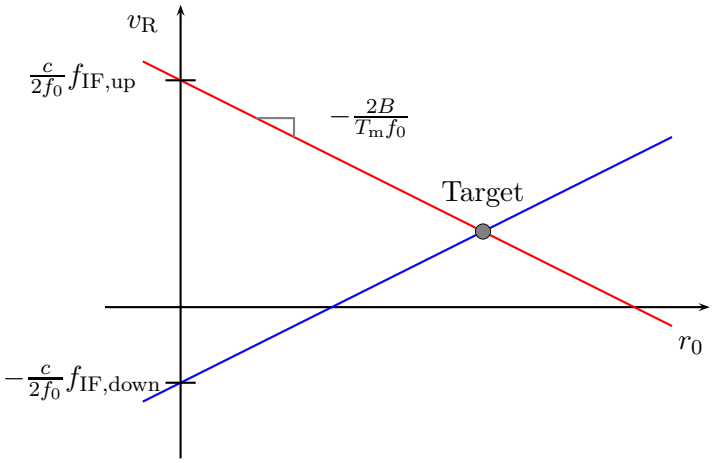


Figure 2.7: Two chirp range-velocity diagram

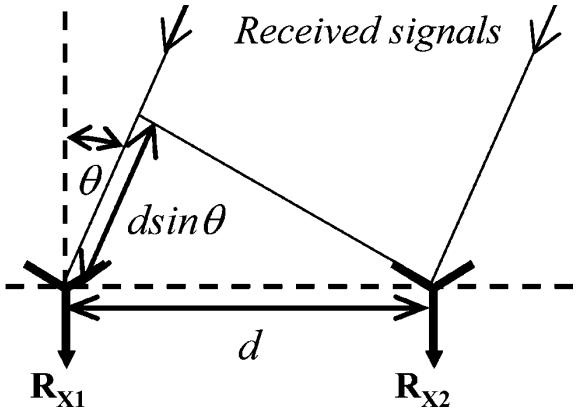


Figure 2.8: Phase difference in a receiver array

2.1.5 Determination the target direction: receiver array

In a radar with multiple receiver paths the angle of arrival of the incoming wave can be determined, and thus the direction of the target.

Assume for simplicity that the radar has two receivers R_{X1} and R_{X2} separated by a distance d, as in Figure 2.8. If θ is the angle of arrival and λ_0 is the wavelength, the phase difference $\delta\phi$ between the two received signal is

$$\delta\phi = \frac{2\pi}{\lambda_0} d \sin\theta. \tag{2.36}$$

Assuming that $C_{1\text{-}2}$ is the mutual coupling coefficient between the receivers (due, for example, to substrate coupling), each received signal has the form

$$R_{X1} = Ae^{j(\phi+\delta\phi/2)} + AC_{1\text{-}2}e^{j(\phi-\delta\phi/2)} \tag{2.37a}$$

$$R_{X2} = Ae^{j(\phi-\delta\phi/2)} + AC_{1\text{-}2}e^{j(\phi+\delta\phi/2)} \tag{2.37b}$$

with A the received signal amplitude and ϕ a reference phase. The angle of arrival can be easily computed by measuring the monopulse ratio R_{m}, defined as the ratio between the sum Σ and the difference Δ signals:

$$\begin{aligned} R_{\mathrm{m}} &= \frac{\Delta}{\Sigma} = \frac{R_{\mathrm{X1}} - R_{\mathrm{X2}}}{R_{\mathrm{X1}} + R_{\mathrm{X2}}} \\ &= \frac{e^{j\delta\phi/2} - e^{-j\delta\phi/2}}{e^{j\delta\phi/2} + e^{-j\delta\phi/2}} \cdot \frac{1 - C_{\text{1-2}}}{1 + C_{\text{1-2}}} \\ &\approx j\frac{\delta\phi}{2}\frac{1 - C_{\text{1-2}}}{1 + C_{\text{1-2}}} \\ &\approx \frac{\pi}{\lambda_0} d \frac{1 - C_{\text{1-2}}}{1 + C_{\text{1-2}}}\,\theta \end{aligned} \tag{2.38}$$

showing that, for $\theta \ll 1$, the angle of arrival θ is proportional to the monopulse ratio R_{m}.

2.1.6 Multiple targets detection

The up-chirp/down-chirp modulation scheme described so far can determine the velocity and the distance of a single target. In the case of two targets, there are four crossings in the range-velocity diagram; two crossings correspond to the real targets, the other two solutions are fictitious and are called ghost targets. In general, n targets produces $n^2 - n$ ghost targets. To distinguish between real targets and ghost targets, a multi-chirp modulation approach is necessary [Stove 92],[Lübbert 05]. For example, with a 4-chirp modulation (with different sweep rates) each target produces in the range-velocity diagram 4 lines (with different slopes) crossing in a single point; this is sufficient to distinguish between 2 targets.

The multi-chirp approach can be extended to more than 4 chirps; the analysis of the trade-off between the probability of wrong detection and the acquisition time is beyond the aim of this introduction to FMCW radars, and can be found in [Lübbert 05].

2.2 X-band upconverter for FMCW radars

The system diagram of a FMCW radar is reported in Figure 2.9, whilst the typical implementation of the carrier modulator is sketched in Figure 2.10. The modulating (BB) signal is generated in digital domain by a Direct Digital Synthesizer (DDS) because the extremely fast changes in the BB frequency required in radar applications cannot be achieved by analog synthesizers. I/Q modulation signals are applied to two DACs and processed by a SSB upconverter; the analysis and design of the analog upconverter is the object of this work.

As explained in the previous sections, radar performances are essentially determined by the characteristics of the transmitted waveform; the upconverter must therefore satisfy challenging specifications in term of high output power, clean spectrum, low phase noise. There are several causes for the generation of spurious tones in the output spectrum:

Image rejection. When a baseband tone at ω_{BB} is multiplied by the local oscillator tone at ω_{LO}, both the tones at the sum and at the difference frequencies appear at RF; if $\omega_{LO} \gg 2\omega_{BB}$ the suppression of the image term by filtering becomes impractical due to the excessive quality factor required. An alternative approach for image rejection

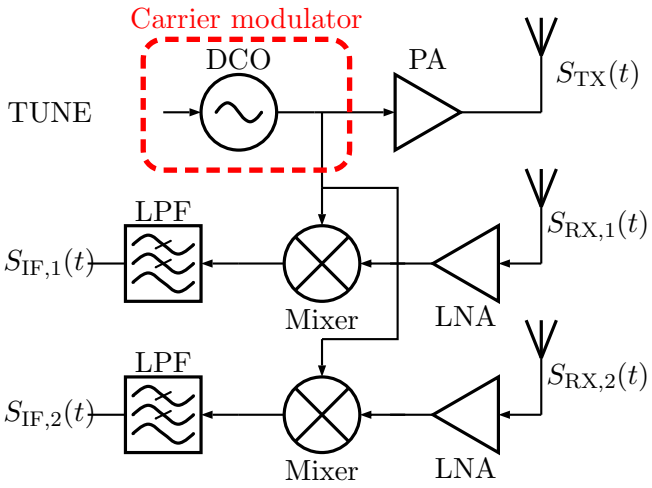


Figure 2.9: Radar system diagram

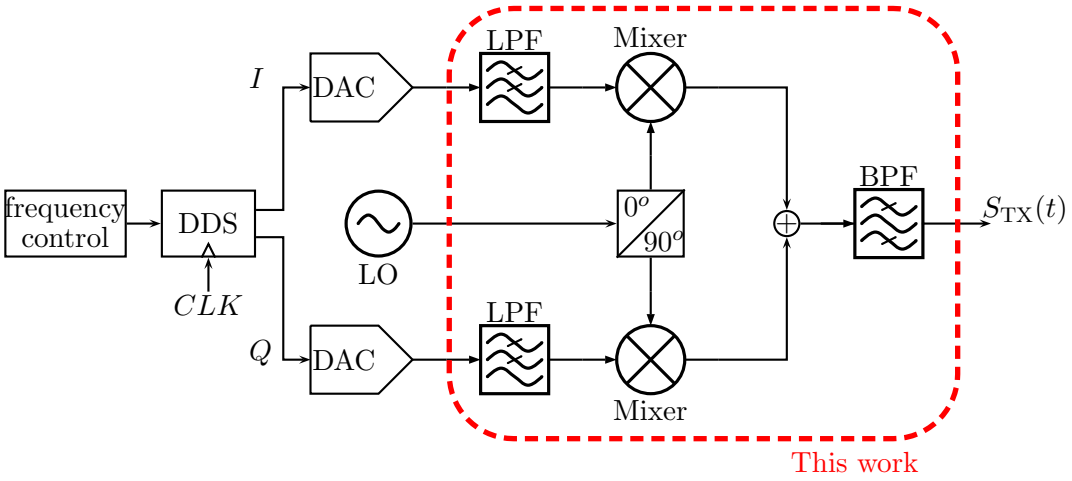


Figure 2.10: Radar modulator: DDS with SSB upconversion

is that of combining the outputs of two balanced mixers driven by quadrature LO signals; this solution shifts the problem to the I/Q LO signals generation, since good image rejection requires quadrature signals with low amplitude mismatch and low phase deviation from ideal $\pi/2$ rads in a wide LO bandwidth. The LO chain needs to deliver sufficient power to the mixers to guarantee correct switching, so signal amplification and LO buffering is necessary. The design of the LO path easily becomes the critical bottleneck of the whole upconverter.

Generation of unwanted harmonics. When the baseband input at ω_{BB} is applied to the upconverter interface, harmonic at $k\omega_{BB}$ are generated. Assuming a fully differential interface and no mismatches, the tones with odd k, $k \geq 3$ can have large amplitudes. Since the mixers are driven by a large LO signal with a rich harmonic content, the BB spectrum is upconverted around $n\omega_{LO}$, where again it is reasonable to assume odd n and $n \geq 3$. This spectrum is than applied to a RF amplifier stage

which further generates harmonic distortion at the output at $j \times (n\omega_{LO} \pm k\omega_{BB})$ (see Figure2.11). Again, RF filtering can somewhat lower the LO and RF harmonics but is ineffective for BB distortion; the key point is that of developing a highly linear interface (which is critical since in an upconverter we are dealing with large tones at the input) and being able to deliver a high power to the LO port of the mixers to assure a linear upconversion.

LO feedthrough. Solid-state mixers require a high power at the LO port to assure the correct switching of the active devices and to perform a linear frequency shift. To prevent this signal to reach the output, doubly-balanced mixers are adopted; a high mixer port isolation requires low mismatches between devices and a careful routing of signals through the upconverter; a good chip floorplan is mandatory.

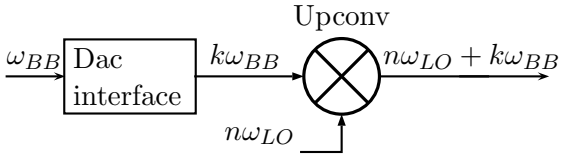


Figure 2.11: Harmonic distortion in the upconverter

Concerning the noise performance, the noise introduced by the upconverter directly adds to the input signals and increase the output phase-noise:

- the required output phase noise has to satisfy a mask which is application-dependent. Generally speaking, the floor phase noise at large frequency offsets is typically dominated by thermal noise while at small offset flicker noise is dominant; flicker noise is a major concern is CMOS technologies, and its reduction starts from a good choice of the upconverter architecture.
- for noise optimization signal amplification must be assured in the first stages of the signal chain; this approach however causes a higher distortion, requiring a careful balance between the noise and linearity.

2.2.1 Proposed circuit

In this project we propose a high linearity low phase noise X-band solid-state upconverter. From an architecture perspective, the key features of the proposed circuit are:

- wideband operation, with a DC-1 GHz baseband input bandwidth, and a $9-11$ GHz LO/RF bandwidth;
- quadrature architecture for image rejection; each path comprises a linear baseband interface with a DC-coupled double-balanced mixer. After mixing and I/Q signal recombination a RF amplifier boosts the signal to a target output power of approximately 0 dBm @ 100 Ω;
- on chip I/Q LO signal generation (from an external LO reference) performed with a wideband polyphase filter. A possible modification of the polyphase filter to control the I/Q phase difference between the I and Q paths and correct mismatches was also investigated (see Appendix A).

Two circuits are developed with a MOS and a bipolar SiGe technology respectively. From a design perspective, these different technologies offer devices with different performances in term of intrinsic gain, noise and linearity, therefore leading to different implementations of the upconverter core (i.e. the mixers) to meet the design goals:

CMOS upconverter (simulations and on-board measurements). The circuit was developed in a 65 nm digital CMOS technology with thick top metal for high-Q inductors. The MOS technology is well suited to build voltage-controlled resistors; two passive double-balanced mixers with zero bias current were chosen to reach a better linearity and reduce the flicker noise at the output. To the author's best knowledge, it is the first time that a zero bias current passive mixer is applied in a transmitter; DC coupling to the baseband interface is made possible by a common-mode feedback loop.

SiGe:C upconverter (post-layout simulations only). The circuit was developed in a 0.35 μm bipolar SiGe:C technology. Bipolar technology is not suitable to build passive switches; the circuit is therefore based on two active double-balanced Gilbert mixers (a solution based on a passive diode mixer was also investigated). The linearity of an active mixer is limited by the distortion introduced by the input baseband transconductor; advanced linearization techniques based on predistortion, feedback or feedforward were discarded due to the impossibility to accommodate them with the required DC-coupled baseband input and/or for technological limitations (the lower performances of the vertical *pnp* BJT impose the realization of an all-*npn* upconverter).

2.2.2 Image-rejection architecture

General considerations. An image-rejection architecture is mandatory to cancel the image frequency out of the mixer, since filtering at $2 \cdot \omega_{\mathrm{BB}}$ can not be effective.

Let's assume that the signals at the output of the baseband DACs $x_{\mathrm{BB,I}}(t)$ and $x_{\mathrm{BB,Q}}(t)$ are ideal tones with no amplitude mismatch and with the ideal $\pi/2$ rad phase shift. Then

$$x_{\mathrm{BB,I}}(t) = X_{\mathrm{BB}} \cos(\omega_{\mathrm{BB}} t + \varphi) \tag{2.39a}$$

and

$$x_{\mathrm{BB,Q}}(t) = X_{\mathrm{BB}} \cos(\omega_{\mathrm{BB}} t + \pi/2 + \varphi) \tag{2.39b}$$

respectively; X_{BB} is the signal amplitude and φ is the initial phase.

In an image-rejection upconverter, the baseband signals are multiplied by two quadrature LO tones, i.e.

$$x_{\mathrm{LO,I}}(t) = X_{\mathrm{LO}} \cos(\omega_{\mathrm{LO}} t + \pi/2 + \phi) \tag{2.40a}$$

and

$$x_{\mathrm{LO,Q}}(t) = X_{\mathrm{LO}} \cos(\omega_{\mathrm{LO}} t + \phi). \tag{2.40b}$$

Performing the multiplication between the baseband and the LO signals for the I channel, we get

$$\begin{aligned} x_{\mathrm{RF,I}}(t) =& X_{\mathrm{LO}} \cos(\omega_{\mathrm{LO}} t + \pi/2 + \phi) \cdot X_{\mathrm{BB}} \cos(\omega_{\mathrm{BB}} t + \varphi) = \\ =& \frac{X_{\mathrm{BB}} X_{\mathrm{LO}}}{2} \left[\cos((\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}}) t + \pi/2 + \phi + \varphi) \right. \\ & \left. + \cos((\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}}) t + \pi/2 + \phi - \varphi) \right], \end{aligned} \tag{2.41a}$$

while for the Q channel

$$\begin{aligned} x_{\mathrm{RF,Q}}(t) =& X_{\mathrm{LO}} \cos(\omega_{\mathrm{LO}} t + \phi) \cdot X_{\mathrm{BB}} \cos(\omega_{\mathrm{BB}} t + \pi/2 + \varphi) = \\ =& \frac{X_{\mathrm{BB}} X_{\mathrm{LO}}}{2} \left[\cos((\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}})t + \phi + \pi/2 + \varphi) \right. \\ & \left. + \cos((\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}})t + \phi - \pi/2 - \varphi) \right]. \end{aligned} \tag{2.41b}$$

Being the instantaneous phase difference of the tones at $\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}}$ equal to 0, and the phase difference of the tones at $\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}}$ equal to π, after I/Q recombination

$$\begin{aligned} x_{\mathrm{RF}}(t) &= x_{\mathrm{RF,I}}(t) + x_{\mathrm{RF,Q}}(t) = \\ &= X_{\mathrm{BB}} X_{\mathrm{LO}} \cos((\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}})t + \phi + \pi/2 + \varphi) \end{aligned} \tag{2.42}$$

showing that the tone at $\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}}$ is canceled.

Amplitude/phase errors. If the LO signals show amplitude and/or phase mismatch, the cancellation is not complete. Without loss of generality, assume $\phi = 0$ and $\varphi = 0$; in presence of both amplitude and phase mismatch, the LO signals assume the form

$$x_{\mathrm{LO,I}}(t) = X_{\mathrm{LO}} \cos(\omega_{\mathrm{LO}} t + \pi/2) \tag{2.43a}$$

and

$$x_{\mathrm{LO,Q}}(t) = X'_{\mathrm{LO}} \cos(\omega_{\mathrm{LO}} t + \delta); \tag{2.43b}$$

the baseband signals are still

$$x_{\mathrm{BB,I}}(t) = X_{\mathrm{BB}} \cos(\omega_{\mathrm{BB}} t) \tag{2.44a}$$

and

$$x_{\mathrm{BB,Q}}(t) = X_{\mathrm{BB}} \cos(\omega_{\mathrm{BB}} t + \pi/2). \tag{2.44b}$$

The upconverted I/Q tones becomes

$$x_{\mathrm{RF,I}}(t) = \frac{X_{\mathrm{BB}} X_{\mathrm{LO}}}{2} \left[\cos((\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}})t + \pi/2) + \cos((\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}})t + \pi/2) \right], \tag{2.45a}$$

and

$$x_{\mathrm{RF,Q}}(t) = \frac{X_{\mathrm{BB}} X'_{\mathrm{LO}}}{2} \left[\cos((\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}})t + \pi/2 + \delta) + \cos((\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}})t - \pi/2 + \delta) \right], \tag{2.45b}$$

respectively. After I/Q recombination the radio-frequency signal $x_{\mathrm{RF}}(t)$ becomes

$$\begin{aligned} x_{\mathrm{RF}}(t) =& \{x_{\mathrm{sig}}(t)\} + \{x_{\mathrm{img}}(t)\} \\ =& \left\{ \frac{X_{\mathrm{BB}} X_{\mathrm{LO}}}{2} \cos((\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}})t + \pi/2) + \frac{X_{\mathrm{BB}} X'_{\mathrm{LO}}}{2} \cos((\omega_{\mathrm{LO}} + \omega_{\mathrm{BB}})t + \pi/2 + \delta) \right\} \\ &+ \left\{ \frac{X_{\mathrm{BB}} X_{\mathrm{LO}}}{2} \cos((\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}})t + \pi/2) + \frac{X_{\mathrm{BB}} X'_{\mathrm{LO}}}{2} \cos((\omega_{\mathrm{LO}} - \omega_{\mathrm{BB}})t - \pi/2 + \delta) \right\} \end{aligned} \tag{2.46}$$

The Image Rejection Ratio (IRR) is defined as the ratio between the power of the signal tone P_{sig} and the power of the image P_{img}

$$IRR \triangleq \frac{P_{\text{sig}}}{P_{\text{img}}} = \frac{\overline{x}^2_{\text{sig}}/2}{\overline{x}^2_{\text{img}}/2}. \tag{2.47}$$

The squared of the signal tone $x^2_{\text{sig}}(t)$ is

$$\begin{aligned} x^2_{\text{sig}}(t) =& \frac{X^2_{\text{BB}}X^2_{\text{LO}}}{4}\cos^2((\omega_{\text{LO}}+\omega_{\text{BB}})t+\pi/2) + \frac{X^2_{\text{BB}}X'^2_{\text{LO}}}{4}\cos^2((\omega_{\text{LO}}+\omega_{\text{BB}})t+\pi/2+\delta) \\ &+ \frac{X^2_{\text{BB}}X_{\text{LO}}X'_{\text{LO}}}{2}\cos((\omega_{\text{LO}}+\omega_{\text{BB}})t+\pi/2)\cos((\omega_{\text{LO}}+\omega_{\text{BB}})t+\pi/2+\delta) \\ =& \frac{X^2_{\text{BB}}X^2_{\text{LO}}}{4}\cos^2((\omega_{\text{LO}}+\omega_{\text{BB}})t+\pi/2) + \frac{X^2_{\text{BB}}X'^2_{\text{LO}}}{4}\cos^2((\omega_{\text{LO}}+\omega_{\text{BB}})t+\pi/2+\delta) \\ &+ \frac{X^2_{\text{BB}}X_{\text{LO}}X'_{\text{LO}}}{4}\left[\cos(2(\omega_{\text{LO}}+\omega_{\text{BB}})t+\pi+\delta)+\cos(\delta)\right] \end{aligned} \tag{2.48}$$

while for the image $x^2_{\text{img}}(t)$ we get

$$\begin{aligned} x^2_{\text{img}}(t) =& \frac{X^2_{\text{BB}}X^2_{\text{LO}}}{4}\cos^2((\omega_{\text{LO}}-\omega_{\text{BB}})t+\pi/2) + \frac{X^2_{\text{BB}}X'^2_{\text{LO}}}{4}\cos^2((\omega_{\text{LO}}-\omega_{\text{BB}})t-\pi/2+\delta) \\ &+ \frac{X^2_{\text{BB}}X_{\text{LO}}X'_{\text{LO}}}{4}\left[\cos(2(\omega_{\text{LO}}-\omega_{\text{BB}})t+\delta)+\cos(\delta-\pi)\right]. \end{aligned} \tag{2.49}$$

The average signal and image power $\overline{x}^2_{\text{sig}}$ and $\overline{x}^2_{\text{img}}$ are therefore

$$\overline{x}^2_{\text{sig}} = \frac{X^2_{\text{BB}}X^2_{\text{LO}}}{8} + \frac{X^2_{\text{BB}}X_{\text{LO}}X'_{\text{LO}}}{4}\cos\delta + \frac{X^2_{\text{BB}}X'^2_{\text{LO}}}{8} \tag{2.50}$$

and

$$\overline{x}^2_{\text{img}} = \frac{X^2_{\text{BB}}X^2_{\text{LO}}}{8} - \frac{X^2_{\text{BB}}X_{\text{LO}}X'_{\text{LO}}}{4}\cos\delta + \frac{X^2_{\text{BB}}X'^2_{\text{LO}}}{8} \tag{2.51}$$

respectively, finally leading to the final expression of the IRR:

$$IRR = \frac{1+2\Delta X_{\text{LO}}\cos\delta+\Delta X^2_{\text{LO}}}{1-2\Delta X_{\text{LO}}\cos\delta+\Delta X^2_{\text{LO}}}, \qquad \Delta X_{\text{LO}} = X_{\text{LO}}/X'_{\text{LO}}. \tag{2.52}$$

If only the amplitude mismatch is considered, $\delta = 0$ and

$$IRR = \left(\frac{1+\Delta X_{\text{LO}}}{1-\Delta X_{\text{LO}}}\right)^2; \tag{2.53}$$

for a small amplitude mismatch we can set $\Delta X_{\text{LO}} = 1+\varepsilon$, $|\varepsilon| \ll 1$ and the image rejection (2.53) reduces to

$$IRR = \left(\frac{1+(1+\varepsilon)}{1-(1+\varepsilon)}\right)^2 \approx \frac{4}{\varepsilon^2}. \tag{2.54}$$

If only the phase mismatch is taken into account, $\Delta X_{\text{LO}} = 1$ and

$$IRR = \frac{1+\cos\delta}{1-\cos\delta} = \cot^2\frac{\delta}{2}; \tag{2.55}$$

for a small phase error $\sin\delta \approx \delta$ and we get

$$IRR = \frac{1+\cos\delta}{1-\cos\delta} = \left(\frac{1+\cos\delta}{\sin\delta}\right)^2 \approx \frac{4}{\delta^2}. \tag{2.56}$$

Assuming small amplitude and phase error together, we can express the image rejection with the approximate expression

$$IRR \approx \frac{4}{\varepsilon^2+\delta^2} \tag{2.57}$$

which is usually adopted for hand calculations.

2.2.3 I/Q LO signal generation

Having discussed the fundamental properties of quadrature systems, let's briefly take into consideration the problem of the generation of the quadrature signals to drive these systems [Lee 04], [Razavi 98].
Quadrature signals are traditionally generated in one of these three ways:

With Quadrature Voltage-Controlled Oscillator (QVCO). This method consists in the realization of two Voltage-Controlled Oscillators (VCOs) running at ω_{LO} locked to oscillate in quadrature.

- Advantages: no LO reference is needed, power consumption can be kept quite low.
- Disadvantages: large area is required, possible introduction of a systematic phase error due to magnetic coupling if LC oscillators are used.

By frequency division (VCO + DIV2). This method requires a single VCO running at twice the required frequency (i.e. $2\omega_{\mathrm{LO}}$) followed by a divide-by-two circuit for the generation of the quadrature signals.

- Advantages: smaller area is required with respect to the QVCO solution.
- Disadvantages: requires a reference LO at a frequency higher than that needed, the divider usually consumes a significant amount of power due to the high input frequency.

With RC-CR filters / polyphase filter (VCO + RC/PPF). Starting from a reference signal at ω_{LO}, this method uses passive RC network to phase-shifting the reference LO and generate quadrature signals.

- Advantages: passive (reliable) structure, easy implementation, phase and gain mismatch can be kept under control.
- Disadvantages: requires a reference LO, inherently narrowband, introduces signal losses.

The choice of the best method for quadrature generation strongly depends on the specifications of the particular application to be fulfilled.

2.2.4 Upconverter linearity

General considerations. A nonlinear time-invariant system can be described as a truncated power series:

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \dots \tag{2.58}$$

For $x(t) = A\cos(\omega t + \varphi)$ (2.58) becomes

$$y(t) = \alpha_0 + \alpha_1 A\cos(\omega t + \varphi) + \alpha_2 A^2 \cos^2(\omega t + \varphi) + \alpha_3 A^3 \cos^3(\omega t + \varphi) + \dots \tag{2.59}$$

Recalling that

$$\cos^2\theta = \frac{1 - \cos 2\theta}{2} \tag{2.60a}$$

and that

$$\cos^3\theta = \frac{3\cos\theta + \cos 3\theta}{4} \tag{2.60b}$$

the input-output relationship (2.58) becomes

$$\begin{aligned} y(t) = &\left[\alpha_0 + \frac{\alpha_2 A^2}{2}\right] + \left[\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right]\cos(\omega t + \varphi) + \left[-\frac{\alpha_2 A^2}{2}\right]\cos^2(2\omega t + 2\varphi) \\ &+ \left[\frac{\alpha_3 A^3}{4}\right]\cos^3(3\omega t + 3\varphi) + \dots . \end{aligned} \tag{2.61}$$

In a fully differential system $\alpha_{\mathrm{i}} = 0$ for all even indexes i, leading to a simplified expression for the harmonic distortion

$$y(t) = \beta_1\cos(\omega t + \varphi) + \beta_3\cos^3(3\omega t + 3\varphi) + \beta_5\cos^3(5\omega t + 5\varphi) + \dots . \tag{2.62}$$

Mixer linearity. In an upconverter mixer distortion occurs for both the baseband BB signal and the local oscillator LO signal, and a large number of output tones appears at angular frequencies

$$\omega_{\mathrm{RF}} = (2n+1)\omega_{\mathrm{BB}} + (2m+1)\omega_{\mathrm{LO}}, \tag{2.63}$$

assuming a fully differential architecture for both the BB and the LO. Since $\omega_{\mathrm{BB}} \ll \omega_{\mathrm{LO}}$, the terms near ω_{LO} cannot be filtered.

Linearity of the image-rejection architecture. We will now proof that in a quadrature image-rejection architecture the third order harmonic distortion generated at the baseband directly translate to the output. Specifically, assume that the I/Q baseband tones at the output of the DAC interface are

$$x_{\mathrm{BB,I}}(t) = X_{\mathrm{BB}}\cos(\omega_{\mathrm{BB}} t) \tag{2.64a}$$

$$x_{\mathrm{BB,Q}}(t) = X_{\mathrm{BB}}\cos(\omega_{\mathrm{BB}} t + \pi/2). \tag{2.64b}$$

Distortion at the (differential) baseband interface generates

$$y_{\mathrm{BB,I}}(t) = Y_1\cos(\omega_{\mathrm{BB}} t) + Y_3\cos(3\omega_{\mathrm{BB}} t) + \dots \tag{2.65a}$$

$$y_{\mathrm{BB,Q}}(t) = Y_1\cos(\omega_{\mathrm{BB}} t + \pi/2) + Y_3\cos(3\omega_{\mathrm{BB}} t + 3\pi/2) + \dots , \tag{2.65b}$$

where only the tones up to $3\omega_{\mathrm{BB}}$ were included. The baseband HD_3 is simply

$$HD_{3,\mathrm{BB}} = \frac{Y_3}{Y_1} \tag{2.66}$$

After upconversion, at the RF output of the I/Q mixers $x_{\mathrm{RF,I}}(t)$ and $x_{\mathrm{RF,Q}}(t)$ are given by

$$\begin{aligned} x_{\mathrm{RF,I}}(t) =& X_{\mathrm{LO}} \cos(\omega_{\mathrm{LO}} t + \pi/2) \cdot [Y_1 \cos(\omega_{\mathrm{BB}} t) + Y_3 \cos(3\omega_{\mathrm{BB}} t) + \ldots] \\ =& \frac{X_{\mathrm{LO}} Y_1}{2} [\cos(\omega_{\mathrm{LO}} t + \omega_{\mathrm{BB}} t + \pi/2) + \cos(\omega_{\mathrm{LO}} t - \omega_{\mathrm{BB}} t + \pi/2)] \\ &+ \frac{X_{\mathrm{LO}} Y_3}{2} [\cos(\omega_{\mathrm{LO}} t + 3\omega_{\mathrm{BB}} t + \pi/2) + \cos(\omega_{\mathrm{LO}} t - 3\omega_{\mathrm{BB}} t + \pi/2)] \end{aligned} \tag{2.67a}$$

$$\begin{aligned} x_{\mathrm{RF,Q}}(t) =& X_{\mathrm{LO}} \cos(\omega_{\mathrm{LO}} t) \cdot [Y_1 \cos(\omega_{\mathrm{BB}} t + \pi/2) + Y_3 \cos(3\omega_{\mathrm{BB}} t + 3\pi/2) + \ldots] \\ =& \frac{X_{\mathrm{LO}} Y_1}{2} [\cos(\omega_{\mathrm{LO}} t + \omega_{\mathrm{BB}} t + \pi/2) + \cos(\omega_{\mathrm{LO}} t - \omega_{\mathrm{BB}} t - \pi/2)] \\ &+ \frac{X_{\mathrm{LO}} Y_3}{2} [\cos(\omega_{\mathrm{LO}} t + 3\omega_{\mathrm{BB}} t + 3\pi/2) + \cos(\omega_{\mathrm{LO}} t - 3\omega_{\mathrm{BB}} t - 3\pi/2)] \\ =& \frac{X_{\mathrm{LO}} Y_1}{2} [\cos(\omega_{\mathrm{LO}} t + \omega_{\mathrm{BB}} t + \pi/2) - \cos(\omega_{\mathrm{LO}} t - \omega_{\mathrm{BB}} t + \pi/2)] \\ &+ \frac{X_{\mathrm{LO}} Y_3}{2} [-\cos(\omega_{\mathrm{LO}} t + 3\omega_{\mathrm{BB}} t + \pi/2) + \cos(\omega_{\mathrm{LO}} t - 3\omega_{\mathrm{BB}} t + \pi/2)], \end{aligned} \tag{2.67b}$$

which, after I/Q signal recombination, leads to an RF signal $x_{\mathrm{RF}}(t)$ with the form

$$\begin{aligned} x_{\mathrm{RF}}(t) &= x_{\mathrm{RF,I}}(t) + x_{\mathrm{RF,Q}}(t) \\ &= X_{\mathrm{LO}} Y_1 \cos(\omega_{\mathrm{LO}} t + \omega_{\mathrm{BB}} t + \pi/2) + X_{\mathrm{LO}} Y_3 \cos(\omega_{\mathrm{LO}} t - 3\omega_{\mathrm{BB}} t + \pi/2). \end{aligned} \tag{2.68}$$

Computing now the radio-frequency HD_3 we get

$$HD_{3,\mathrm{RF}} = \frac{X_{\mathrm{LO}} Y_3}{X_{\mathrm{LO}} Y_1} = HD_{3,\mathrm{BB}} \tag{2.69}$$

i.e. the same HD_3 of the baseband signal. A high baseband linearity is therefore necessary to keep the output spurs below a target level.

2.3 65nm CMOS upconverter design

The first version of the upconverter was implemented in a standard 65nm CMOS technology with thick top metal for high Q inductors. This section deals with:

- the design of the modulator;
- the layout of the circuit;
- the simulation and (as will be explained later, only partial) measurement results.

2.3.1 Design/analysis

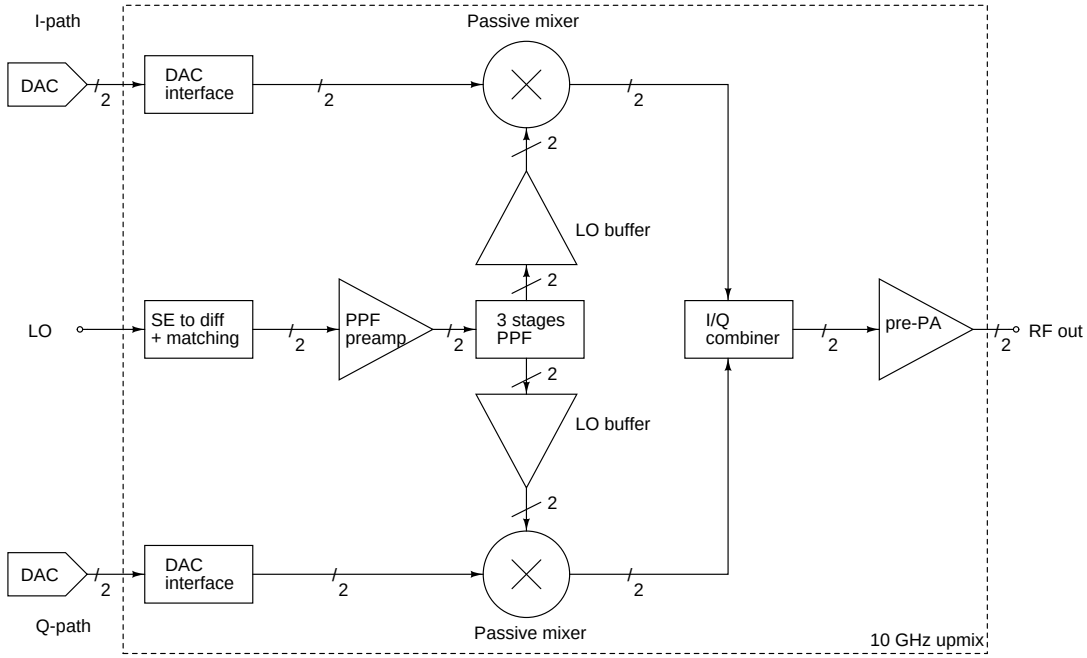


Figure 2.12: CMOS X-band upconverter architecture

The proposed CMOS upconverter architecture is shown in Figure 2.12 and summarized in table 2.1. Each building block will be described in the following sections.

block	description
mixer	passive current mixer
current buffer / combiner	cascode + RLC tank
DAC interface	current sink
pre-PA	differential pair
LO-path	PPF + preamp + LO buffers
bias	current mirrors + OTA-based CMFB

Table 2.1: X-band upconverter building blocks

Passive mixer

The core of the upconverter is, obviously, the mixer; the design goals of the mixer are:

- maximize the mixer linearity, and
- reduce the flicker-noise produced by the mixer itself.

In a CMOS technology it is possible to implement a mixer in two ways:

- as a Gilbert active mixer, or
- as a passive switch-based mixer.

While the use of Gilbert active mixers is advantageous because they provide conversion gain, they suffer from bad linearity originating in the V/I transconductor stage and generation of flicker-noise in the switching cell.

A passive mixer was therefore designed. A doubly balanced structure (Figure 2.3.1) was chosen to suppress the LO signal at the output; the mixer works in the current domain and no transconductance IF stage is needed, improving linearity. The differential baseband

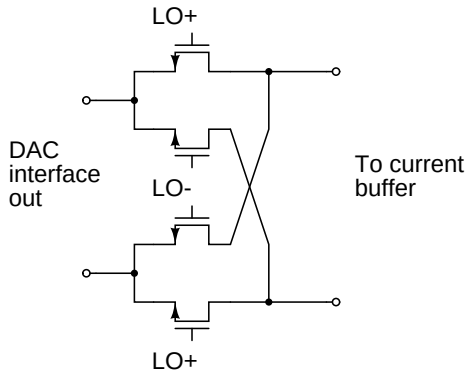


Figure 2.13: Passive Mixer

signal is applied to the sources of the transistors, the LO signal drives the gates while the $RF = LO \pm IF$ upconverted tone is taken from the drains. The size of the transistors is a compromise between the ON resistance and the capacitive load they provide to the LO buffers. The ON resistance can be easily computed; in the case of an nMos transistor, when the gate is high the transistor channel is formed and V_{ds} is small (linear region). Being the drain current

$$I_{\mathrm{ds}} = \frac{\mu_{\mathrm{n}} C_{\mathrm{ox}} W}{L} \left[(V_{\mathrm{gs}} - V_{\mathrm{th}}) V_{\mathrm{ds}} - \frac{V_{\mathrm{ds}}^2}{2} \right] \tag{2.70}$$

where μ_{n} is the electron mobility, C_{ox} the oxide capacitance per unit area, W and L the mos width and length respectively, V_{th} the threshold voltage, the ON resistance r_{on} results in

$$r_{\mathrm{on}} = \frac{1}{\partial I_{\mathrm{ds}} / \partial V_{\mathrm{ds}}} = \frac{L}{\mu_{\mathrm{n}} C_{\mathrm{ox}} W (V_{\mathrm{gs}} - V\mathrm{th}) - V_{\mathrm{ds}}} \approx \frac{L}{\mu_{\mathrm{n}} C_{\mathrm{ox}} W V_{\mathrm{ov}}} \tag{2.71}$$

with $V_{\rm ov} = V_{\rm gs} - V{\rm th}$ the overdrive voltage. The ON resistance $r_{\rm on}$ can be reduced increasing the W/L ratio and the overdrive $V_{\rm ov}$, but large transistors increase the capacitive loading of the LO buffer, while a large overdrive improves the linearity but increases the noise folding of the mixer, rising the output noise.

The nonlinear source / drain diffusion capacitances play an important role in the linearity of the passive mixer. Theoretically, substituting each transistor with a parallel combination of an nMos and a pMos transistor could cancel the distortion introduced by the modulation of the source/drain voltages; in practice, the lower mobility $\mu_{\rm p}$ of pMos transistors and the higher oxide capacitance $C_{\rm ox}$ proved to be detrimental at X-band.

To reduce the noise introduced by the mixer, a zero-DC current biasing was adopted to remove the flicker noise. This approach is widely used in dowconversion stages with the insertion of a capacitor in series to the mixer; in the case of out upconverter mixer a blocking capacitor can't be used because would introduce a high-pass filter at baseband, which is not allowed by specification. To overcome the problem, we introduced a common mode feedback circuit which senses the voltage at the drain of the switches and regulates the source voltage such that $V_{\rm ds} \approx 0$. This common mode feedback circuit will be shown later, once the DAC interface before the mixer and the current buffer after the mixer will be described.

Current buffer / combiner

According to the theory of current-commutating passive CMOS mixers, maximum linearity is obtained when the mixer is driven by a large source impedance $Z_{\rm s}$ and loaded by a low load impedance $Z_{\rm l}$ [Khatri 09], [Mirzaei 09]. In our architecture, the source impedance $Z_{\rm s}$ is determined by the DAC interface and, as will be seen in the next section, is ultimately limited by the (low) DAC output impedance of 50Ω; the only possible optimization can therefore be obtained by lowering the load impedance $Z_{\rm l}$. The low input impedance current buffer of Figure 2.3.1 was therefore inserted following the upconverter mixer. The current buffer/combiner stage accomplishes four goals:

- increases the mixer linearity,
- recombines the I/Q signal paths for image rejection,
- assures a high level of isolation between the I and Q mixers, and
- sets the drain voltages of the mixer transistors to a constant value, $\approx 270 - 300mV$.

The current buffer is constituted by a common-gate (CG) stage stacked above a nMos mirror in a cascode fashion. The biasing circuit, based on a high swing current mirror, sets the common-gate bias current and ultimately its transconductance $g_{\rm m,CG}$, and keep the voltage at the sources of the CG stage equal to the desired reference voltage $V_{\rm CM,ref}$. The output currents coming from the I and Q current buffer are finally recombined in a low-Q RLC tank, which also resonates the input capacitance of the AC-coupled pre power amplifier output stage. The poly resistor R was intentionally inserted to reduce the quality factor of the tank and to make the buffer output resistance more stable to process spreads.

The size and biasing of the common-gate stages set the buffer input impedance to $1/g_{m,CG}$; maximum linearity requires $1/g_{m,CG} \ll r_{\rm on}$ (the more, the better) where $r_{\rm on}$ is the mixer ON resistance. Large nMos transistors must be avoided since they increase the

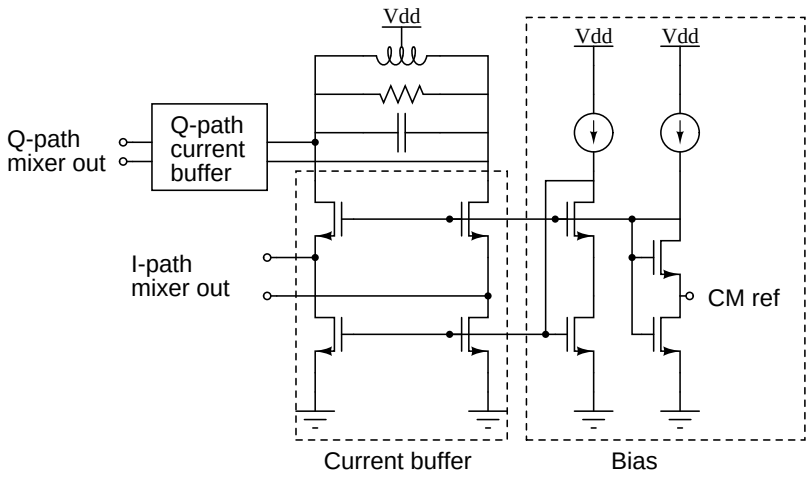


Figure 2.14: Current buffer/combiner

input capacitance of the stage, limiting the RF input bandwidth and the overall conversion gain of the upconverter.

DAC interface / CMFB circuit

The baseband I/Q sources are assumed to be two DACs with pseudo-differential current outputs driven by a DDS delivering a current

$$I_{\mathrm{DAC,I+}} = I_0\,[1 + \sin(\omega_{\mathrm{BB}} t)] \tag{2.72a}$$
$$I_{\mathrm{DAC,I\text{-}}} = I_0\,[1 - \sin(\omega_{\mathrm{BB}} t)] \tag{2.72b}$$
$$I_{\mathrm{DAC,Q+}} = I_0\,[1 + \cos(\omega_{\mathrm{BB}} t)] \tag{2.72c}$$
$$I_{\mathrm{DAC,Q\text{-}}} = I_0\,[1 - \cos(\omega_{\mathrm{BB}} t)] \tag{2.72d}$$

with $I_0 = 6\ mA$ to a $R_{\mathrm{S}} = 50\ \Omega$ load.

The passive mixers require a zero-DC current through the switches. We want to guarantee a DC coupled input, so decoupling caps are not allowed. The interface is therefore constituted by current sinks which removes the DC component of the input current while passing the AC component to the mixer, as depicted in Figure 2.3.1; since the DC input current $I_{\mathrm{in,DC}}$ depends on the input voltage V_{DAC}, a CMFB loop at the input is required. Assuming a high interface input impedance (i.e. sacrificing the input matching for linearity), calling V_{DAC} the input voltage the fraction of the DAC DC current flowing into the current sinks in the interface is

$$I_{\mathrm{in,DC}} = I_0 - V_{\mathrm{DAC}}/R_{\mathrm{S}}. \tag{2.73}$$

The task of the CMFB is that of sensing the input voltage at the node $CM, sense$ and regulating $I_{\mathrm{in,DC}}$ such that

$$V_{\mathrm{DAC}} \approx V_{\mathrm{CM,ref}} \tag{2.74}$$

i.e. such that the source-drain voltage in the mixer switch is zero, $V_{\mathrm{ds}} \approx 0$. The CMFB loop amplifier is composed by a pMos current source cascaded by a nMos common-source stage with RC compensation [Gray 01].

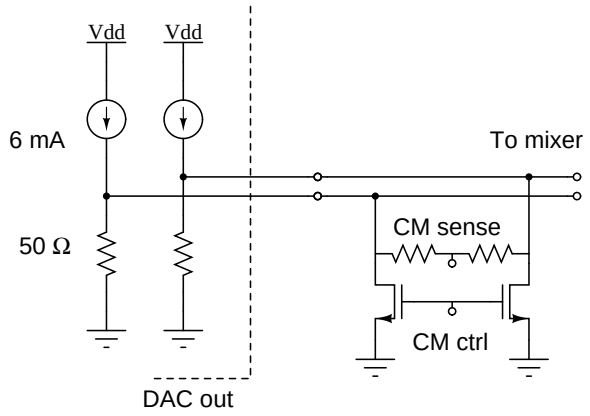


Figure 2.15: Baseband interface

Pre power amplifier

The output stage comprise an AC-coupled X-band amplifier to boost the radio-frequency signal to a target 0 dBm power level and drive a differential 100Ω load which, in a final upconverter implementation, will be the input impedance of the differential power amplifier of the radar transmitter. The on-chip RF amplifier, sketched in Figure 2.3.1 is a classic differential pair with a resonant low-Q load tuned at $\omega_{RF} \approx 2\pi \cdot 10\ GHz$. A cascode level,

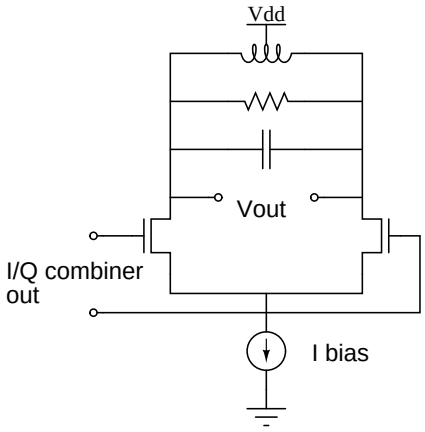


Figure 2.16: Pre-power amplifier

even if beneficial to increase the reverse isolation and hence the stability of the circuit, was not inserted to avoid signal clipping at the output nodes. The differential pair and tail transistor were sized to reduce their flicker noise contribution to the output.

Local Oscillator path

The Local Oscillator (LO) path has a critical impact on the performance of the whole upconverter. The local oscillator path must

- provide power matching to a single-ended 50Ω LO (external) source,
- generate accurate quadrature differential LO signals in the X-band, and

- drive the LO ports of the I/Q mixers.

In the proposed CMOS implementation, the generation of wideband quadrature signal is assigned to a polyphase filter (PPF), which offers several advantages [Kaukovuori 08]:

- PPFs are passive RC structures, whose behavior in presence of process spreads and/or circuit mismatches can be easily predicted,
- wideband behavior can easily be obtained by cascading several stages, and
- the design of the filter is immediate once the source impedance, load impedance, center frequency and bandwidth are determined.

Polyphase filters have also some design issues:

- require a differential input signal,
- each polyphase stage attenuates the signal, and
- the filter performance is strongly influenced by the actual parasitic in the layout.

In the proposed implementation, a three stage polyphase filter was required to guarantee the target image-rejection in the $9 \div 11\ GHz$ LO bandwidth in presence of process spreads.

The requirement of a differential input signal is here solved with the adoption of a LO transformer; even if a fully-integrated solution based on an active single-ended-to-differential phase splitter can be adopted (as in [Kodkani 08]), the use of a passive transformer has several advantages, since it can provide

- single-ended to differential conversion,
- impedance transformation for input power matching,
- passive voltage gain, and
- convenient ESD protection since an effective protection can be obtained if the ESD device is connected to the center tap of the differential coil, without loading the signal terminals.

The second PPF-based approach problem, i.e. the signal attenuation, is more critical. To obtain a good modulator linearity, a LO signal with a sufficient amplitude must be provided to the mixer; if this voltage is excessive, noise folding increases worsening the noise performance. This optimum LO signal amplitude must be guaranteed almost constant in the whole LO bandwidth (at least $9 \div 11\ GHz$ for every process corner). From a design perspective:

- in the particular CMOS technology in use, it was not possible to obtain signal amplification at X-band without inductors;
- low-Q tanks have to be used due to the large relative bandwidth $\Delta f / f_0$ that must be covered, decreasing the attainable voltage gain in amplifying each stage;
- several gain stages must be used to balance the PPF losses, meaning the need for more current, more inductors, and a more complex signal routing.

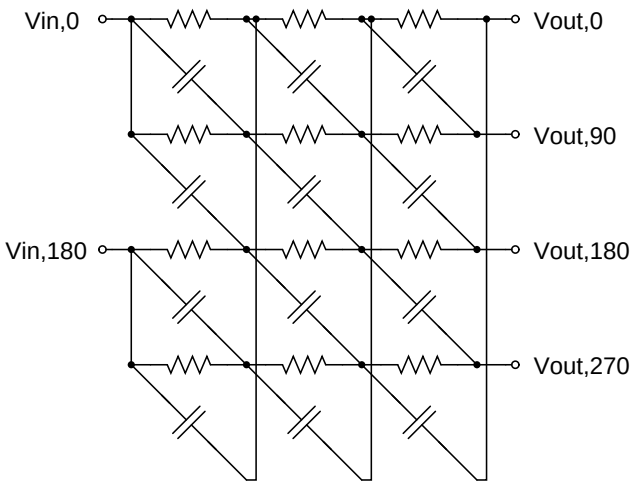


Figure 2.17: 3 stages polyphase filter

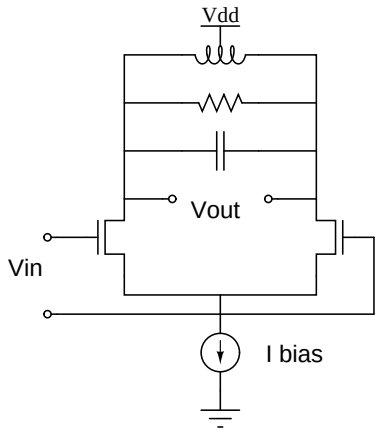


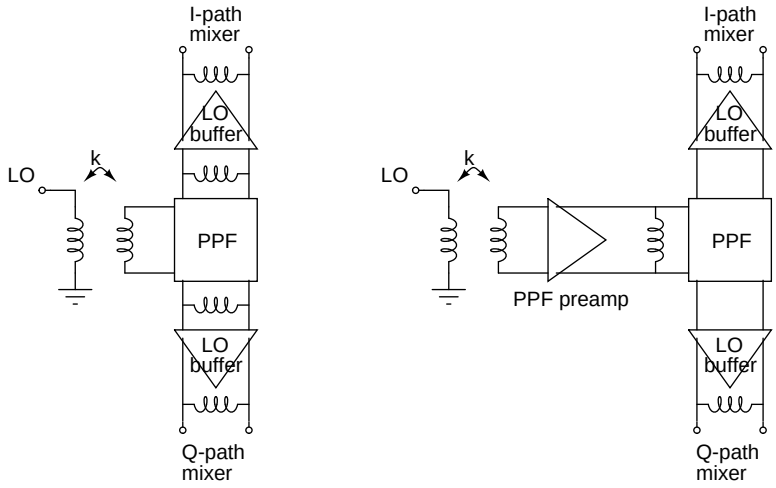
Figure 2.18: Pre/post ppf LO amplifiers

To overcome the losses introduced by the polyphase filters, resonant amplifiers are required in our 65nm CMOS technology; the amplifying stages are conventional RLC loaded differential pairs as illustrated in Figure 2.3.1.

The (complex) Local Oscillator path circuitry can be optimized by a proper disposition of the various building blocks; consider the two possible implementation of Figure 2.19. The implementation of Figure 2.19(a) is the most straightforward approach: first, a transformer converts the reference single-ended LO signal to a differential signal, possibly providing voltage amplification; then a polyphase filter generates the wideband quadrature signals required by the upconverter; finally two branches of LO buffers boost the signals to the required levels to drive the mixers.

This approach has several drawbacks, most of them appearing at the interface between the PPF output and the input of the LO buffers:

- the quadrature LO signal amplitudes at the output of the polyphase filter are quite small due to the filter attenuation; moreover, the capacitive loading of the LO buffers to the PPF further decreases the signal amplitude. This implies that a buffer chain



(a) Implementation # 1 (b) Implementation # 2

Figure 2.19: Possible LO path implementations

with increasing transistor width should be used;

- an inductor should be inserted at the filter / buffer interface to resonate the buffer capacitive loading and boost the signal levels; this is critical a problem in the layout of the LO path since the size of the PPF is smaller than the coils of the required inductors. Moreover, the I/Q coils have to be placed at sufficient distance to minimize the mutual coupling that could easily destroy the attainable image rejection of the modulator;
- finally, being the LO signal is first attenuated by the PPF and than amplified by the buffer, the distribution of the gain is not optimal in terms of noise.

Splitting the LO buffer chain in two and moving one amplifier stage before the polyphase filter as in Figure 2.19(b) solves the above issues:

- the pre-amplifier increases the signal levels before the PPF and, hence, at its output;
- moving the inductors from the output of the PPF to its input does not affect the signals amplitude but results in a more compact layout (one inductor less), easier routing at the PPF output, and minimizing the risk of mutual coupling;
- the pre-amplifier can exploit the secondary of the input transformer to resonate its input capacitance at X-band;
- the pre-amplifier lowers the NF of the LO chain.

The second implementation was therefore designed and layouted.

Biasing circuit and additional structures

The biasing of the chip is obtained with a combination of pMos/nMos current mirrors with a 1:3 mirroring ratio; mirrors are grouped into four families (LO circuitry, DAC interface, current mirrors and PA biasing respectively) based on “current routing” [Gray 01]

to reduce mismatches due to process variations with spatial distance. External voltage references are required to set the correct biasing.

Two separated voltage supplies are used to reduce the coupling between the LO circuitry and the RF amplifier; a common ground is used for the whole chip. All pads are ESD protected, with power clamps between the supplies and ground; decoupling capacitors were also added to filter the supplies and to distribute the VDDs and GND in the chip.

Compact inductors layout

To reduce the area requirements of the various inductors, each differential inductor was split into two symmetrical halves kept at distance (see Figure 2.3.1) to simplify the routing between the blocks of the system; each coil is connected by a "distributed" center tap. A wideband lumped-element inductor model was derived for accurate harmonic-balance

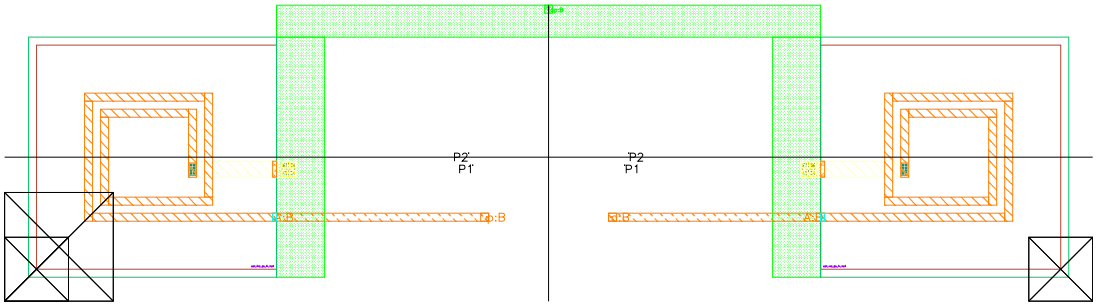


Figure 2.20: Compact inductor layout

upconverter simulations. The model, depicted in Figure 2.3.1, was fitted to EM data obtained from the actual layout; it includes substrate coupling, skin effect and parasitic inductance due to the wiring among the coils. Its accuracy is better than 5% in the X-band + DC operating point.

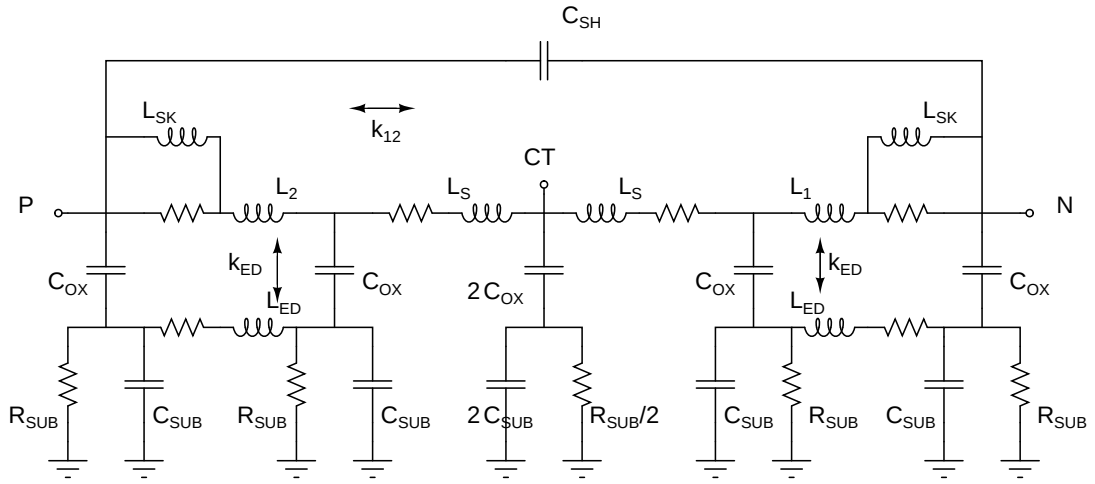


Figure 2.21: Wideband equivalent inductor lumped model

An inductors/transformers summary of the on-chip passive structures is reported in

table 2.2.

#	inductance $[pH]$	$\varnothing$ $[\mu m]$	
1 LO xfrm	640/760	120	
1 LO pre-amp ind	330	40	$[\times 2]$
2 LO buffer ind	1200	45×85	
1 I/Q combiner ind	300	32	$[\times 2]$
1 PA output ind	300	32	$[\times 2]$

Table 2.2: Inductors/Tranformers summary

2.3.2 Results

The CMOS version of the proposed upconverter was designed to be cascaded to two quadrature current DACs (for baseband signal generation) and to be measured with probes. Being this measurement setup quite complex and not available at the moment this dissertation was written, we decided to bond some chip samples to standard boards and feed the baseband inputs of the circuit with standard 50Ω signal generators.

In this way we were able to check the basic functionality of the circuit, keeping in mind that bonding inductors compromised the power port matching and that the chip interface was designed to operate from a current source.

For these motivations we here present both simulation and measurement results, premising that a certain degree of performance loss is to be expected due to the measurement setup; we start this section discussing the post-layout simulation results.

CMOS post-layout simulations

A 25-iterations Montecarlo post-layout simulation was performed to evaluate the performance of the upconverter (unless otherwise stated), at $T_{\text{nom}} = 125$ deg. The number of iterations, necessarily low due to the simulation time, is not high enough to structure an accurate statistical analysis but is however sufficient to show the potentialities of the CMOS upconverter.

Output spectrum ($f_{\mathbf{LO}} = 10\ GHz$, $f_{\mathbf{BB}} = 100\ MHz$)

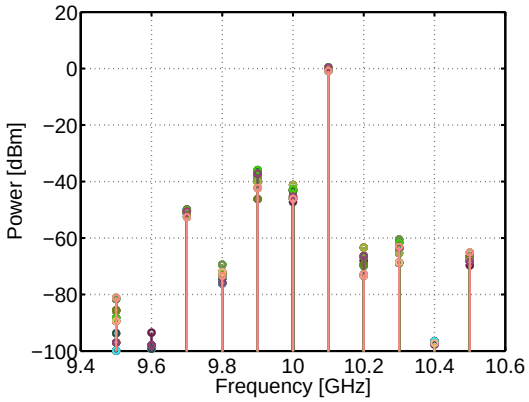


Figure 2.22: CMOS output spectrum

Output power	$-0.1\ dBm$
LO leak. suppr.	$43.9\ dBc$
Image rejection	$38.5\ dBc$
RF HD_3	$50.5\ dBc$

Table 2.3: CMOS output spectrum

BB sweep ($f_{\mathbf{LO}} = 10\ GHz$, slow corner)

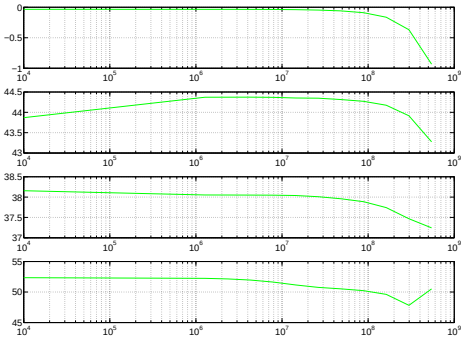


Figure 2.23: CMOS BB sweep

Output power	$-0.1\ dBm$
LO leak. suppr.	$> 43.3\ dBc$
Image rejection	$> 37.2\ dBc$
RF HD_3	$> 47.9\ dBc$
$-3\ dB$ BB bandwidth	$> 1\ GHz$

Table 2.4: CMOS BB sweep

LO sweep ($f_{\mathbf{BB}} = 100\ MHz$, slow corner)

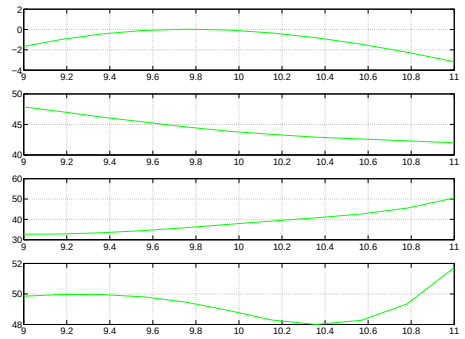


Figure 2.24: CMOS LO sweep

Output power	$-0.1\ dBm$
LO leak. suppr.	$> 42.5\ dBc$
Image rejection	$> 33.0\ dBc$
RF HD_3	$> 48.0\ dBc$
$-3\ dB$ RF bandwidth	$> 2.5\ GHz$

Table 2.5: CMOS LO sweep

Phase noise ($f_{\mathbf{LO}} = 10\ GHz$, $f_{\mathbf{BB}} = 100\ MHz$)

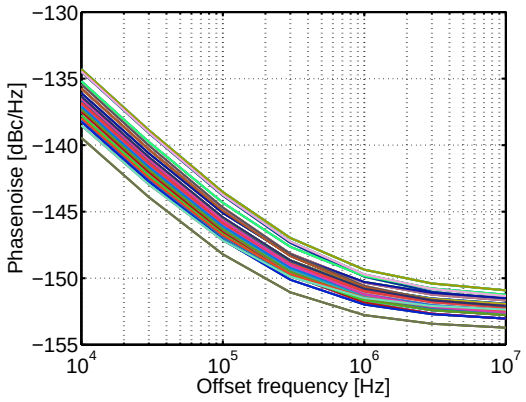


Figure 2.25: CMOS phase noise

Offset freq.	Phase noise
10 kHz	-136.5 dBc/Hz
100 kHz	-145.6 dBc/Hz
1 MHz	-150.9 dBc/Hz
10 MHz	-152.2 dBc/Hz

Table 2.6: CMOS phase noise

RF/LO matching

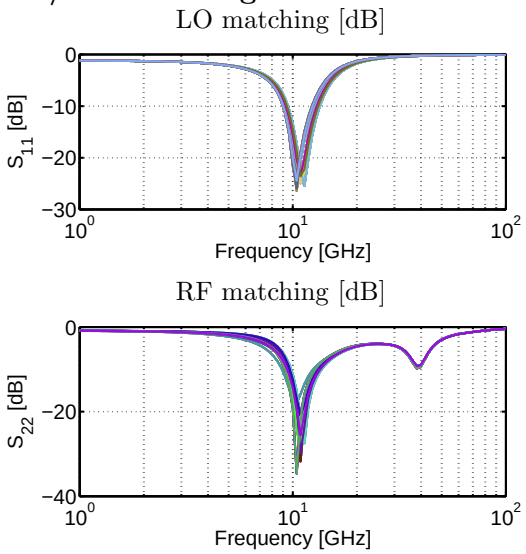


Figure 2.26: CMOS RF/LO matching

LO matching
$< -8\ dB \in [9 - 12]$
RF matching
$< -8\ dB \in [913]$

Table 2.7: CMOS RF/LO matching

The output spectrum evaluated for a Local Oscillator frequency $f_{\mathrm{LO}} = 10\ GHz$ and for an input baseband frequency $f_{\mathrm{BB}} = 10\ MHz$ is plotted in Figure 2.22. The output power at the center of the RF bandwidth is approximately 0 dBm, with an image rejection better than 37 dBc and a LO leakage below 41 dBc; the RF HD_3, i.e. the tone at $f_{\mathrm{LO}} - 3f_{\mathrm{BB}}$ is approximately at $-50\ dBc$.

The large signal behavior of the modulator for a sweep of the baseband frequency f_{BB} and for a sweep of the LO frequency f_{LO} is depicted in Figure 2.23 and Figure 2.24 respectively. The performance of the upconverter with respect to f_{BB} is almost constant for $f_{\mathrm{BB}} < f_{\mathrm{BB,\ -3dB}} \approx 1\ GHz$; the variation of the spectrum with f_{LO} is more significant, confirming that the generation of wideband quadrature LO signals is critical. As can be seen in Figure 2.24, the polyphase filter was centered at a slightly higher frequency than the center LO frequency. The LO leakage decreases with the LO frequency, indicating that the capacitive couplings between the mixer's port are critical at high f_{LO}.

The excellent phase noise, evaluated for $f_{\mathrm{LO}} = 10\ GHz$ and $f_{\mathrm{BB}} = 100\ MHz$, is reported in Figure 2.25; the expected noise floor at large offsets is better than $-152\ dBc/Hz$, with a flicker corner frequency of approximately 300 kHz, indicating that the input common-mode feedback loop effectively lowers the flicker noise by removing almost completely the (large) DC input current coming from the baseband DACs.

The port matching (Figure 2.26) is better than $-8\ dB$ in the $9 - 11\ GHz$ frequency interval; the circuit was not designed for input matching at the baseband input port.

The power dissipation of the circuit blocks is reported in table 2.8.

Interface	$2 \cdot 4\ mA$
Current Buffer	$2 \cdot 21\ mA$
Power Amplifier	$21\ mA$
LO pre-amp	$27\ mA$
LO Buffer	$2 \cdot 10\ mA$
CMFB	$2 \cdot 1\ mA$
Total	$144\ mW$

Table 2.8: Power dissipation

The complete layout of the CMOS upconverter is reported in Figure 2.27; the chip area is $700\mu m \times 1300\mu m$ pads included.

Board measurement results

Some chip samples were bonded to a test board built on a Roger® RO4003 substrate to interface the chip to the measurement setup (Figure 2.28).

The output spectrum variation with f_{LO} for $f_{\mathrm{BB}} = 10\ MHz$ and $p_{\mathrm{LO}} = 3\ dBm$ is plotted in Figure 2.29. The center RF frequency is shifted to a frequency higher than expected, i.e. $\approx 10.6\ GHz$; the nominal output power is $\approx -5\ dBm$, indicating that the losses in the RF bonding inductors compromised the RF port matching and markedly decreased the expected output power. The circuit linearity (RF HD_3) is approximately 5 dB higher than simulated. This higher distortion originates at baseband inputs between the chip interface and the 50Ω ac-coupled signal generators. The quadrature signal generation provided by the polyphase filter is effective and leads to an image-rejection better than $-40\ dBc$ in the required 2 GHz bandwidth. The LO leakage at the output is higher than expected in all the frequency range; this phenomenon was investigated and is not related to mismatches in the doubly-balanced mixers but is due to a direct signal feedthrough from the LO to the RF port, probably due to signal coupling among the bonding inductances.

The measured output spectrum variation with f_{BB} with $f_{\mathrm{LO}} = 10.75\ GHz$ is reported in Figure 2.30; due to limitations in the measurement instrumentation, a maximum f_{BB} of 80 MHz was attainable.

The measured phase noise of the circuit (blue curve in Figure 2.31) is limited by the phase noise introduced by the baseband generators (red dash-dotted line) and by the local oscillator (green dashed line). The 3 dB in phase noise improvement with respect to the baseband noise at large offsets is due to the I/Q architecture of the upconverter. The phase noise introduced by the CMOS circuit is therefore below that measured at the output.

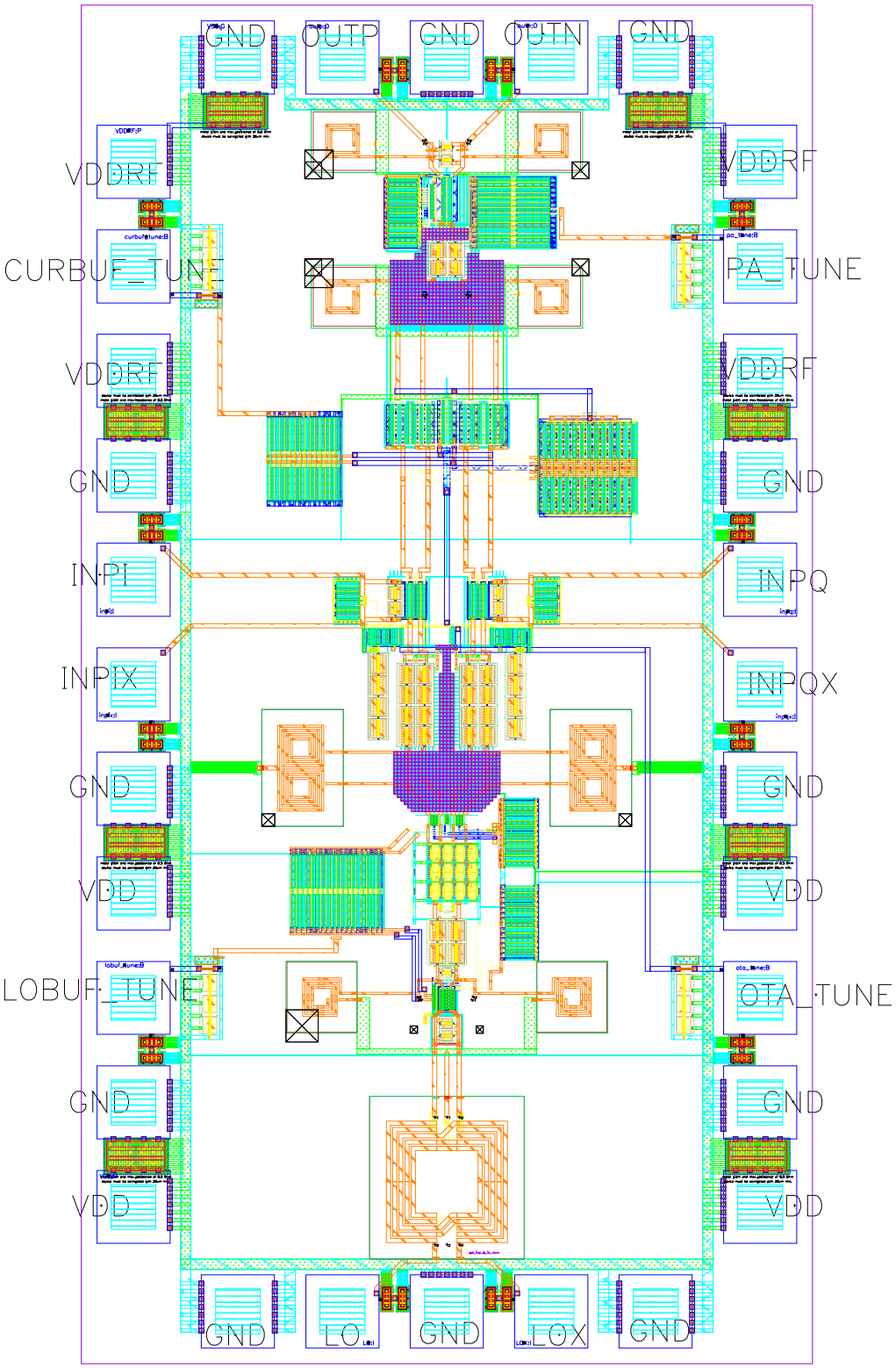


Figure 2.27: CMOS X-band upconverter layout ($700\mu m \times 1300\mu m$)

Figure 2.28: CMOS X-band upconverter chip mounted on the test board

Care was taken when bonding the circuit to the test board to minimize the length of the bonding inductances at the LO port, since it was preferable to introduce a higher parasitic inductance at the RF port (which causes power losses at the output) than at the LO port (which, decreasing the LO amplitude at the LO port and therefore at the mixer's LO port, would have caused a bad switching impacting noise and linearity). For this motivation, only the LO port matching was achieved (Figure 2.32).

The output IP_3 reaches a value of +14.5 dBm at $f_{\mathrm{LO}} = 10.6\ GHz$(Figure 2.33); the whole upconverter draws 150 mA from a 1.2 V supply.

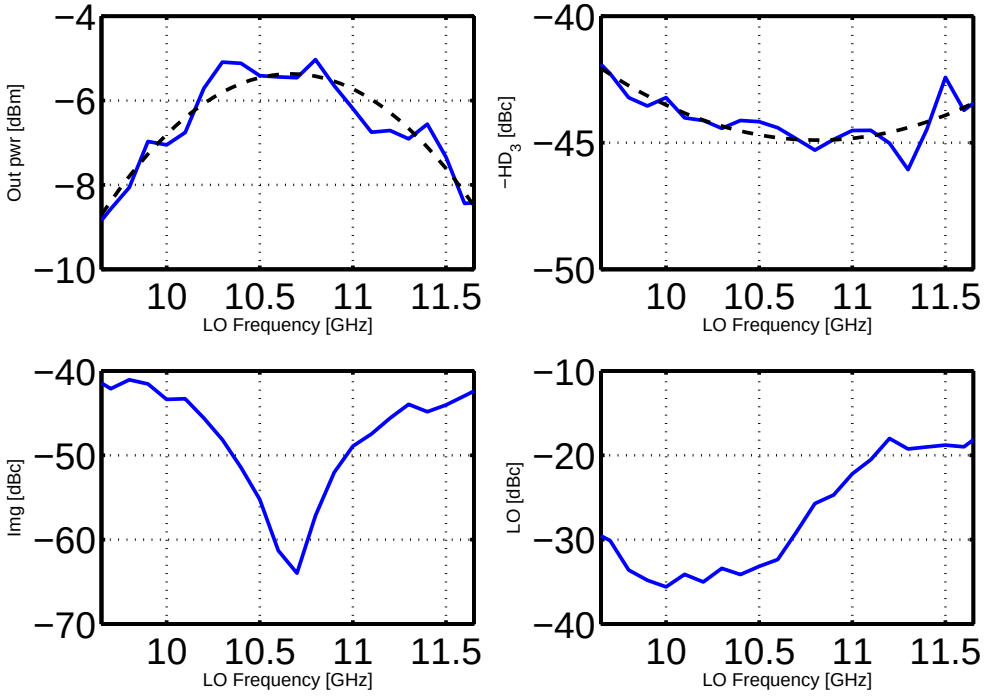


Figure 2.29: CMOS X-band upconverter measured LO sweep

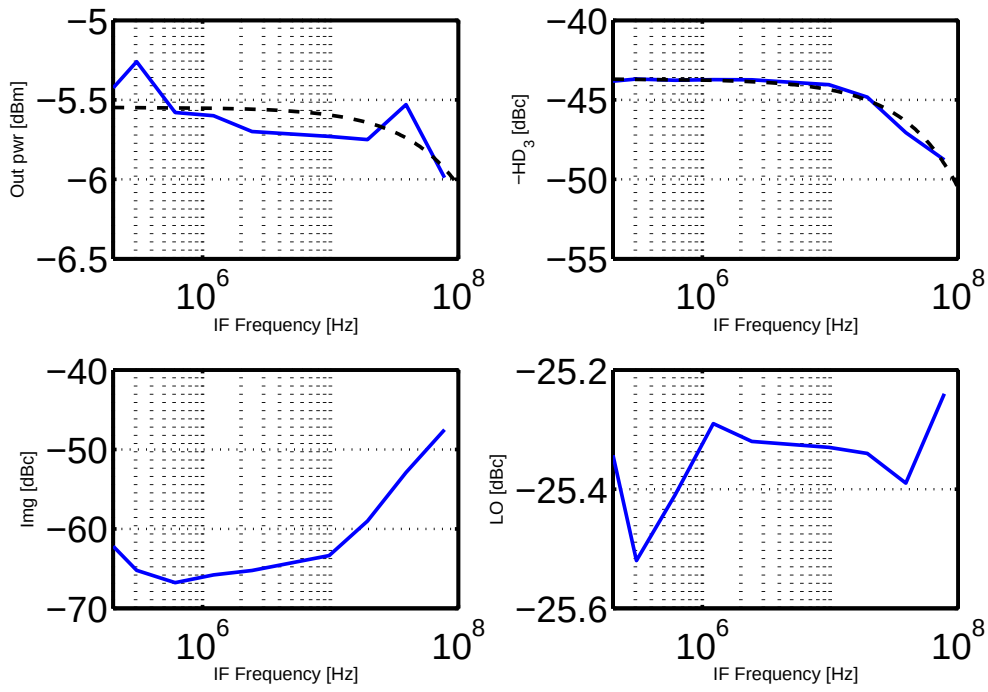


Figure 2.30: CMOS X-band upconverter measured IF sweep

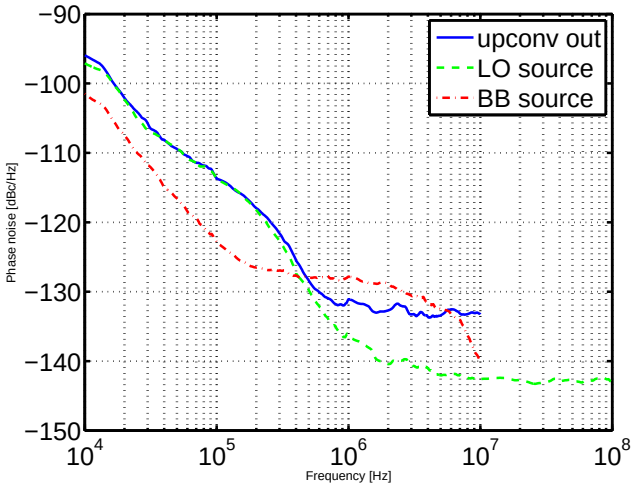


Figure 2.31: CMOS X-band upconverter phase noise (limited by source's pn)

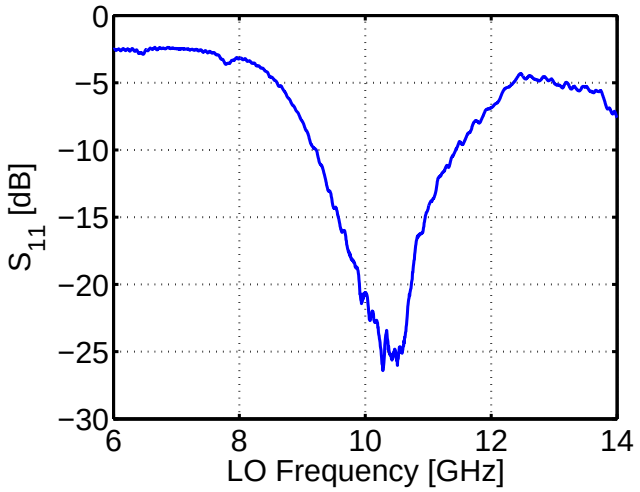


Figure 2.32: CMOS X-band upconverter LO port matching

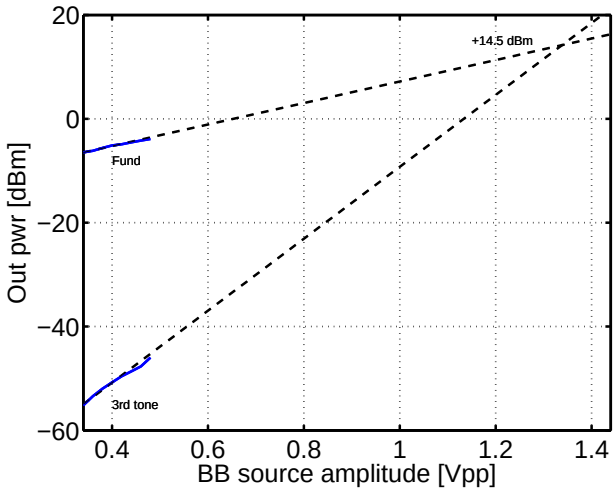


Figure 2.33: CMOS X-band upconverter output IP_3

2.4 0.35μm SiGe:C upconverter design

The second version of the upconverter was implemented in a 0.35μm Silicon-Germanium bipolar technology. This section includes:

- the design of the upconverter;
- the layout of the circuit;
- the simulation results only; the chip samples are currently in production and no measurement result is thus available.

2.4.1 Design/analysis

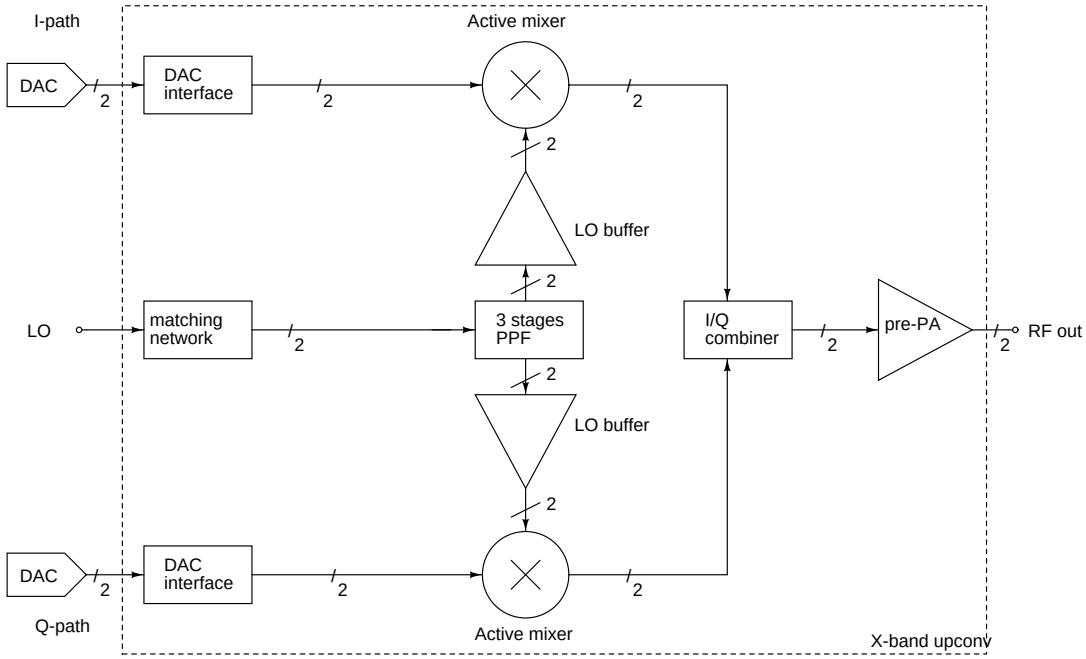


Figure 2.34: SiGe:C X-band upconverter architecture

The proposed SiGe:C upconverter architecture is reported in Figure 2.34; the main building blocks are reported in table 2.9. The main differences with respect to the CMOS version are the following:

Active mixer. The upconverter is based on an active doubly-balanced Gilbert mixer with linearized transconductor, with a shunt-peaking load acting as a combiner for the I/Q paths.

DAC interface. The DAC interface was simplified with respect to the CMOS upconverter, and now consists of a DC-coupled PNP emitter follower stage with a 50 Ω resistor in parallel at the input for power matching; no CMFB loop is thus required.

LO path. The same three stages polyphase filter is employed. A single amplifying stage is sufficient to boost the LO signal to the required level; the pre amplifier stage is thus not needed.

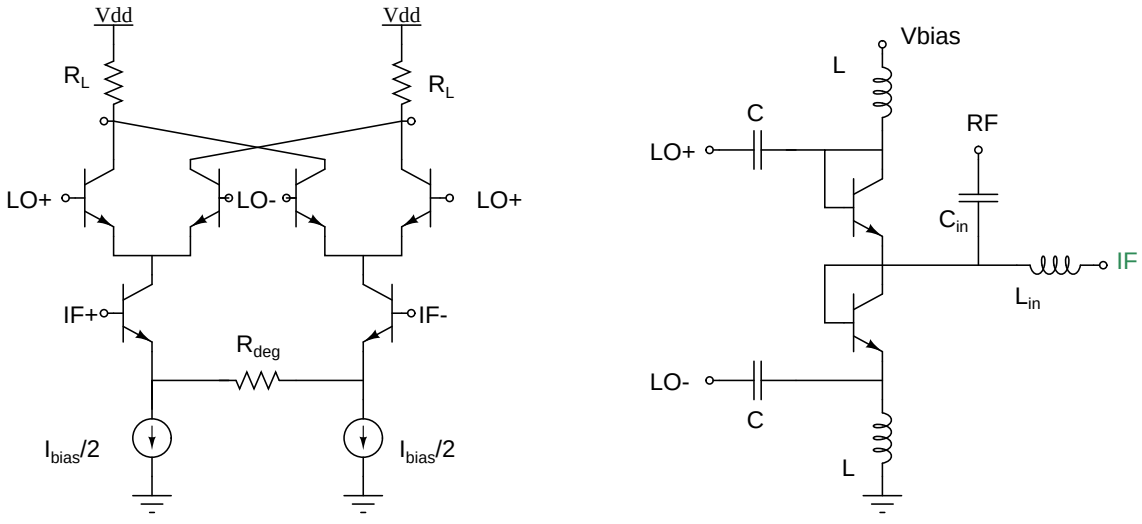
block	description
mixer	active Gilbert mixer
combiner	shunt-peaking load
DAC interface	pnp level shifter
pre-PA	differential pair
LO-path	PPF + LO buffers
bias	current mirrors

Table 2.9: SiGe:C upconverter building blocks

Mixer

In a bipolar technology it is not possible to implement a passive switch-based mixer due to the lack of good switches. Common ways to design a bipolar mixer are therefore:

- as an active Gilbert mixer (Figure 2.35(a)), or
- as a passive diode mixer (Figure 2.35(b)).



(a) Active mixer

(b) Passive diode mixer

Figure 2.35: SiGe X-band upconverter core

The diode mixer approach was investigated and its analysis is reported in Appendix B. Since Schottky diodes were not available in our bipolar technologies, diode connected transistor were employed; a biasing is required to reduce the LO amplitude needed for the mixer switching. The analysis performed shows that this kind of mixer suffer from high sensitivity to process spreads and a poor (and narrowband) port isolation, making it not suitable for our application.

The 0.35μm SiGe:C technology in use offers bipolar transistors with an extremely low flicker noise corner, making the implementation of an active low-noise mixer considerably

easier than in the case of a CMOS technology; for the SiGe:C bipolar mixer the design goal thus becomes the optimization of the linearity of the circuit.

Assuming ideal switching, the nonlinear behavior of the Gilbert mixer is due to the imperfect V/I conversion in the transconductor. There are basically two ways to improve the transconductor linearity:

- use a conventional differential-pair based transconductor with source degeneration and increase the DC current in the gm-cell to reduce the peak i_{ce}/I_{ce}, improving the HD_3 (small signal linearity), or
- substitute the simple transconductor with a more linear gm-cell, based on the v_{be} cancellation technique (large signal linearity).

In the first solution, the source degeneration lowers the effective transconductance of the V/I stage; the effect, combined with an increase of the DC current, is that of lowering the amplitude of the small signal current with respect to the bias current so that the circuit works in a deeper small-signal regime [Sansen 99]. The better linearity comes at the expense of a greater power dissipation and of the subsequent need to amplify the signal once upconverter, and is only a partial solution to the problem.

As an alternative approach, the v_{be} cancellation technique consists in building a transconductor in which the distortion introduced by the V/I conversion in a bipolar transistor are combined to cancel the distortion. The implementations proposed in literature are based on current mirroring [Chung 90] or bipolar transistor stacking [Caprio 73] (with a possible additional current mirror to improve the circuit stability as in [Iizuka 07]); alternative approaches have been shown to increase the input voltage swing [Pan 07]. All these solutions are however not applicable in our circuit because require precise and wide-band pnp mirrors (not available in our technology), or a excessive number of stacked transistors (three including the biasing) making impossible to guarantee a large voltage swing at the baseband input nodes.

The actual implementation of the mixer consist in the "classic" active Gilbert mixer with resistive source degeneration of Figure 2.35(a); despite the non-optimal power efficiency, this circuit offers the designer the best balance between conversion-gain, noise and linearity.

Combiner

Due to the smaller parasitic of the bipolar process when compared to the CMOS process, a common shunt-peaking load for both the I/Q Gilbert active mixers is chosen as a combiner, as in Figure 2.4.1.

DAC interface

The active mixer of the SiGe upconverter needs baseband inputs in the voltage domain; being the upconverter driven by quadrature baseband DACs in the current domain, a simple single-ended 50Ω resistor was chosen for I/V (linear) conversion and input power matching. A combined pnp/npn level shifter is adopted to accommodate the DAC DC output level to that required by the Gilber mixer; the bipolar transistors where biased with low DC current to maximize the transistors cutoff angular frequency ω_T. The resulting DAC interface, reported in Figure 2.4.1, is biased through the same pnp mirror which

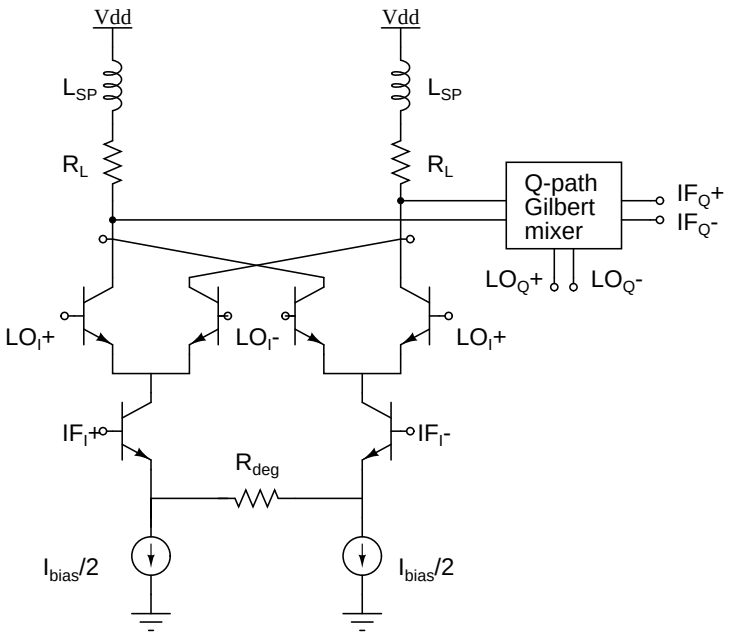


Figure 2.36: SiGe X-band shunt-peaking combiner

also biases the active mixers to reduce process mismatches between the two circuits. The second voltage level shift is obtained with a npn bjt to better track the mixer v_{be} variation with temperature.

Pre power amplifier

An ac-coupled fully differential RF amplifier follows the passive combiner to boost the output signal level. The proposed circuit (Figure 2.4.1) is the bipolar version of the CMOS differential-pair based amplifier used for the MOS implementation of the upconverter. An additional resistive emitter degeneration was employed to increase the amplifier linearity.

Local Oscillator path

The Local Oscillator path underwent substantial review from the CMOS to the SiGe:C implementation. From an architectural point of view, it was decided to keep a simpler differential LO input to a 100Ω differential source, avoiding the need for the single-ended to differential conversion and, hence, for the LO transformer.

The LO path still features a three stages polyphase filter for wideband quadrature signal generations and amplifiers to restore the LO signal levels. The simulated image rejection is plotted in Figure 2.39. According to [Gingell 75], the amplitude difference between positive and negative frequency equals the attainable image rejection.

Due to the lower LO amplitude needed to drive a bipolar active mixer compared to the corresponding CMOS implementation [Razavi 98], and given the better RF performance of the SiGe:C bipolar technology in use, a single stage of amplification was sufficient in the LO path to restore the polyphase filter losses; the LO pre-amplifier was therefore removed. The power matching at the LO port is obtaining resonating the input polyphase

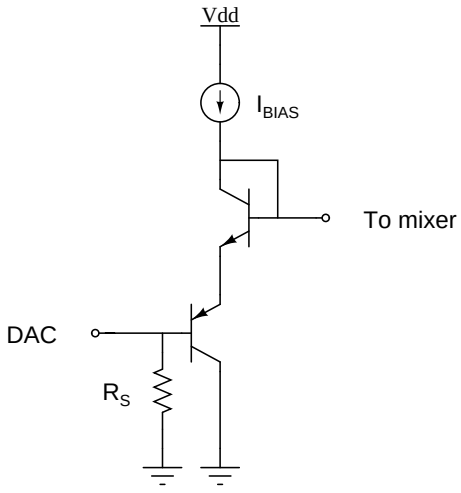


Figure 2.37: SiGe X-band DAC interface (half circuit)

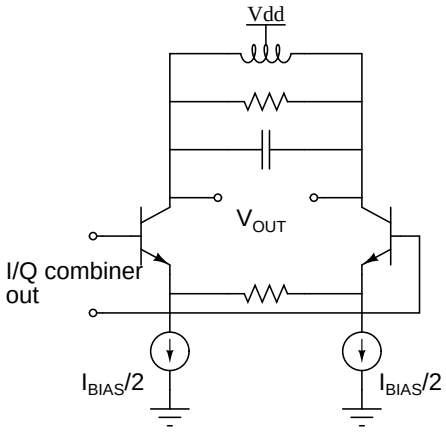


Figure 2.38: SiGe X-band RF amplifier

impedance (calculated in the Appendix A) with an inductor in the X-band; the center tap of the LO inductor sets the input LO driver common-mode voltages and is connected to ESD protection devices. The LO path schematic of the bipolar upconverter is reported in Figure 2.4.1. Each LO driver is composed by a resistively loaded differential pair followed by an emitter follower to drive the mixer LO port (Figure 2.4.1).

Biasing circuit and additional structures

The biasing of the chip is based on pnp/npn current mirrors in a way similar to the CMOS version; no external references are here required. As in the previous design, the LO circuitry and the RF amplifier use two different supplies; all pads are ESD protected and decoupling caps between the supply and ground are used to filter these global signals.

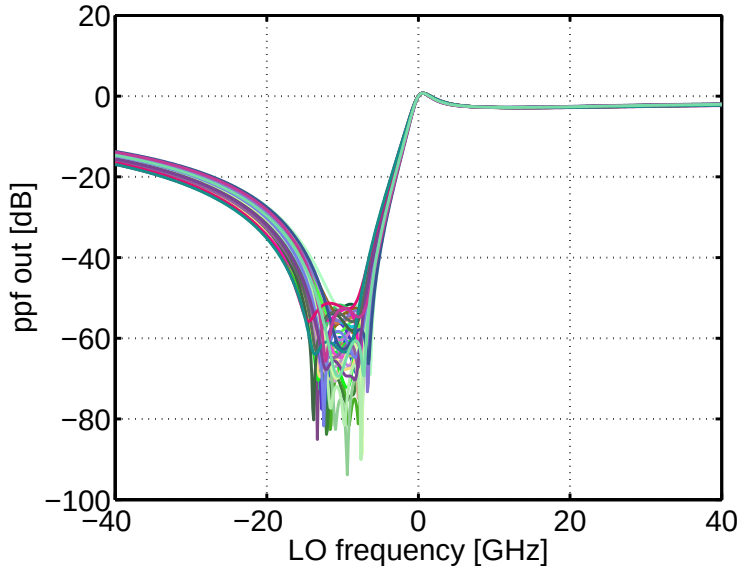


Figure 2.39: PPF image-rejection [200 mc iters] [Gingell 75]

LO freq [GHz].	8.528	9.009	9.489	9.970	10.450	10.931	11.411
min img. rej. [dB]	46.351	46.248	46.503	46.062	45.733	45.673	45.629
mean img. rej. [dB]	60.816	60.880	60.364	60.193	60.586	60.712	60.618

Table 2.10: Expected image rejection from a 200 iterations mc simulation

Inductors

Two inductors are used for the LO and RF power matching to a differential 100Ω port; a third inductor is used in the combiner as shunt peaking; the inductors summary is reported in Table 2.11.

#	inductance [pH]	⌀ [μm]	
1 LO in ind	1000	60	[×2]
1 RF out ind	1000	60	[×2]
1 I/Q combiner ind	200	30	[×2]

Table 2.11: Inductors summary

2.4.2 Results

Being the chip samples in production at the moment this dissertation was written, we only present the simulated performance of the SiGe:C upconverter; post-layout Montecarlo simulations, temperature behavior of the circuit and change in the circuit performance with the voltage supply was evaluated.

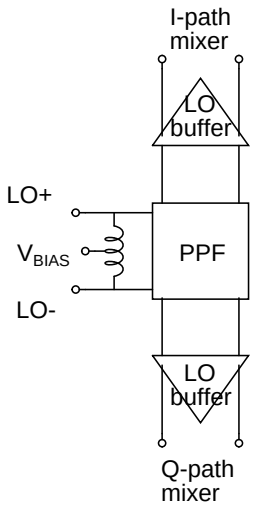


Figure 2.40: SiGe Local Oscillator path

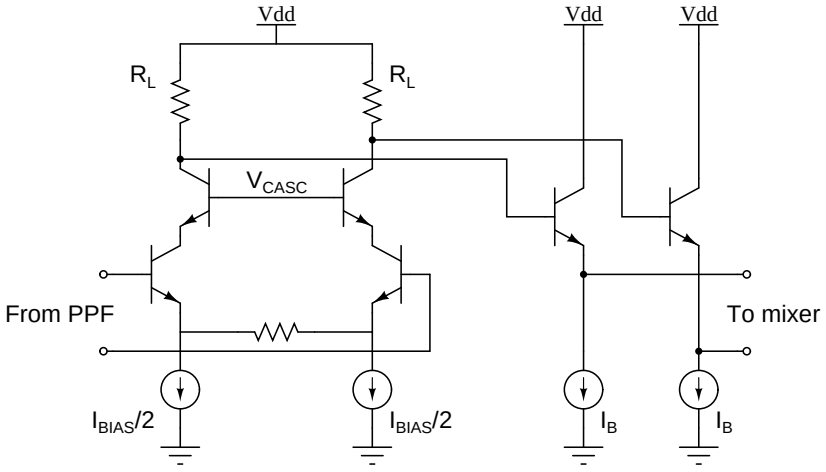


Figure 2.41: SiGe LO amplifier

Each simulation was performed in the following condition:

- 65 mA + 35 mA of total current consumption (LO+IF and RF circuit, respectively),
- 1 nH bonding inductor $\forall$ pad, and
- lumped inductors model derived from EM simulations.

Montecarlo simulations

The performance of the upconverter is evaluated against process spreads and mismatches by means of a 50 iterations Montecarlo simulation (except for the BB and LO sweep simulations).

The simulation results show that the same performances of the CMOS upconverter can be reached with a simpler circuit architecture. The peak RF output power is $-2\ dBm$ at 10 GHz, with an expected LO leakage of 42.7 dBc, an image rejection of 55.9 dBc

and a RF HD_3 of 56.9 dBc (Figure 2.42). A greater variance with respect to the CMOS upconverter is to be expected due to the generation of an on chip current reference for the circuit biasing. The excellent low flicker noise corner of SiGe:C bipolar transistors directly translates into a very low phase noise of the RF tone at small offsets, which reaches a value of -123 dBc/Hz at a 10 Hz offset as reported in Figure 2.45. Port matching in the X-band (Figure 2.46 and Figure 2.47) and circuit stability (Figure 2.48 and Figure 2.49) was assured.

RF output spectrum ($f_{BB} = 10MHz$, $f_{LO} = 10GHz$)

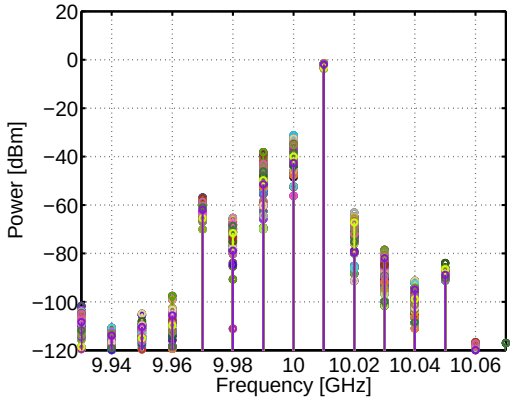


Figure 2.42: SiGe:C output spectrum

Output power	-2.3 dBm
LO leak. suppr.	42.7 dBc
Image rejection	55.9 dBc
RF HD_3	56.9 dBc

Table 2.12: SiGe:C output spectrum

BB/LO frequency sweep

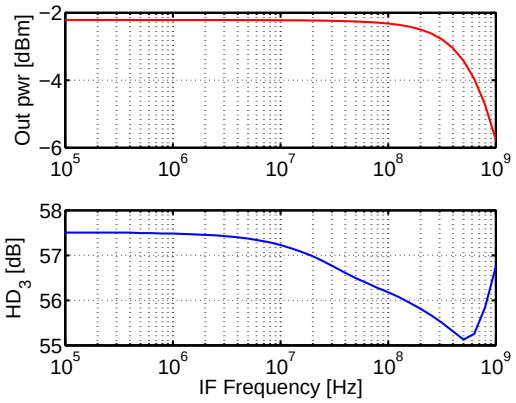


Figure 2.43: BB sweep ($f_{LO} = 10$ GHz)

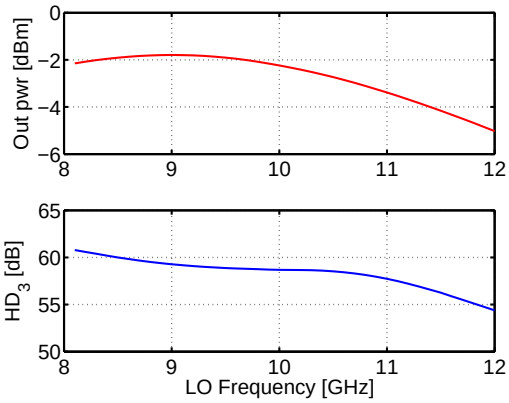


Figure 2.44: LO sweep ($f_{BB} = 10$ MHz))

Phase noise ($f_{LO} = 10GHz$)

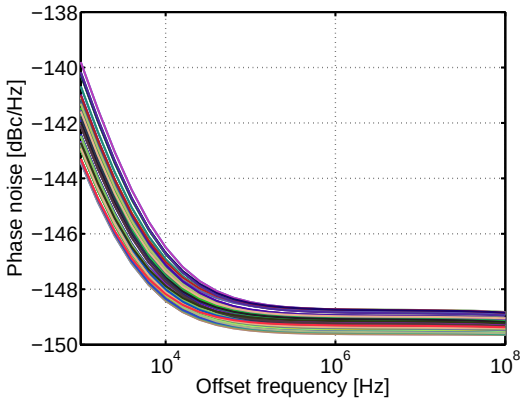


Figure 2.45: SiGe:C phase noise

Offset freq.	Phase noise
10 Hz	-123.07 dBc/Hz
100 Hz	-132.97 dBc/Hz
1 kHz	-142.12 dBc/Hz
10 kHz	-147.69 dBc/Hz
100 kHz	-149.03 dBc/Hz
1 MHz	-149.19 dBc/Hz
10 MHz	-149.21 dBc/Hz
100 MHz	-149.27 dBc/Hz

Table 2.13: SiGe:C phase noise

Port matching

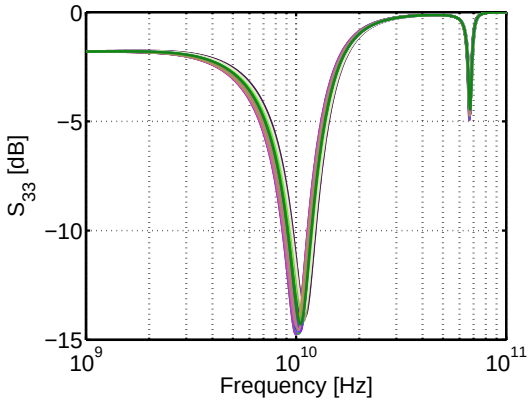


Figure 2.46: LO port matching

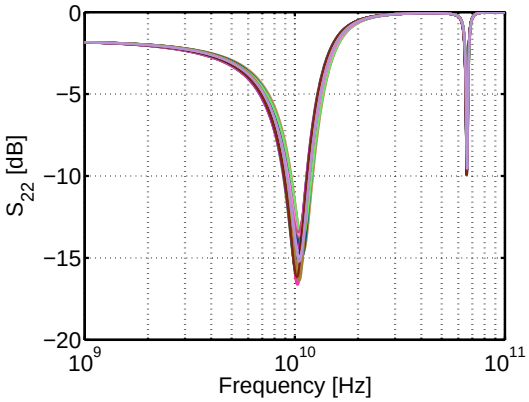


Figure 2.47: RF port matching

Stability

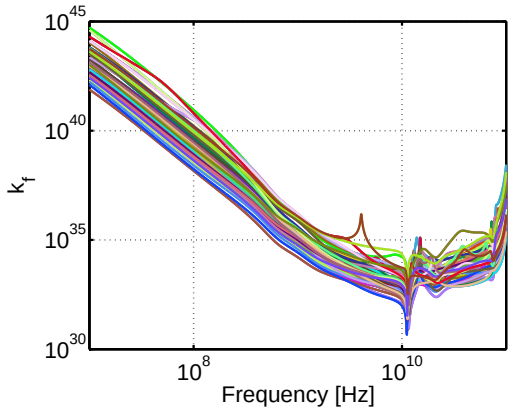


Figure 2.48: k_f stability factor ($> 1 \; \forall$ freq)

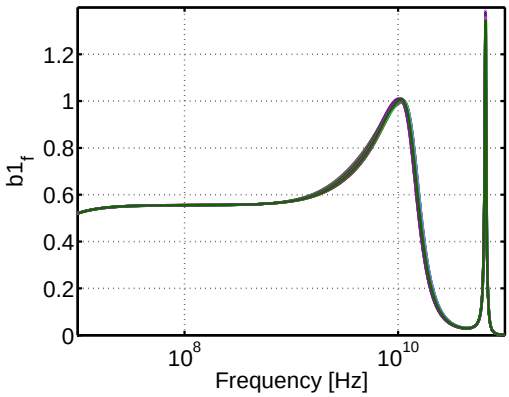


Figure 2.49: $b1_f$ stability factor ($> 0 \; \forall$ freq)

Temperature dependence

Temperature variation has a little influence on the gain, the port matching and the circuit stability. An improvement on the phase noise is to be expected at lower temperatures due to the reduced thermal noise generated by the devices.

RF output spectrum ($f_{BB} = 100MHz$, $f_{LO} = 10GHz$)

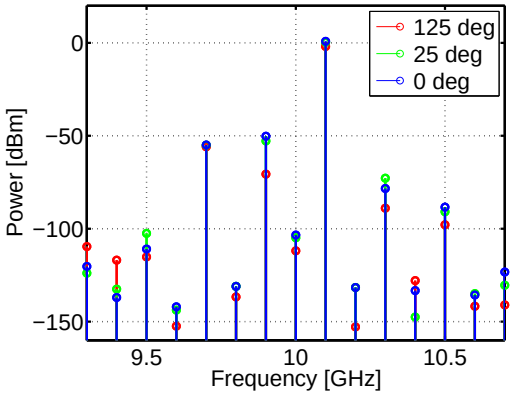


Figure 2.50: SiGe:C temperature dependence of the output spectrum

Output power	$> -1.9\ dBm$
Image rejection	$> 51.0\ dBc$
RF HD_3	$> 53.9\ dBc$

Table 2.14: SiGe:C temperature dependence of the output spectrum

Phase noise ($f_{LO} = 10GHz$))

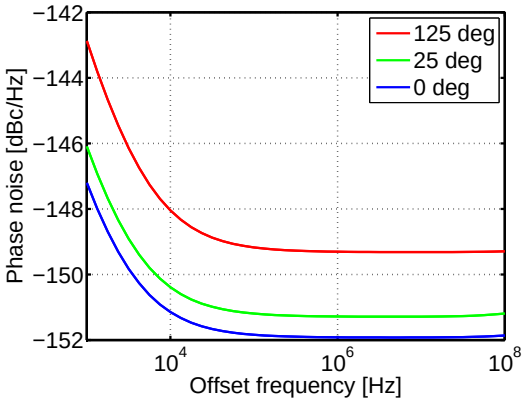


Figure 2.51: SiGe:C temperature dependence of the phase noise

Offset freq.	Phase noise
10 Hz	< -124.0 dBc/Hz
100 Hz	< -133.9 dBc/Hz
1 kHz	< -142.9 dBc/Hz
10 kHz	< -148.0 dBc/Hz
100 kHz	< -149.2 dBc/Hz
1 MHz	< -149.3 dBc/Hz
10 MHz	< -149.3 dBc/Hz
100 MHz	< -149.3 dBc/Hz

Table 2.15: SiGe:C temperature dependence of the phase noise

Port matching

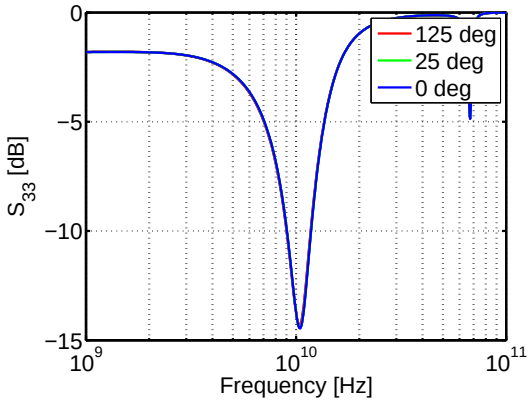


Figure 2.52: SiGe:C temperature dependence of the LO port matching

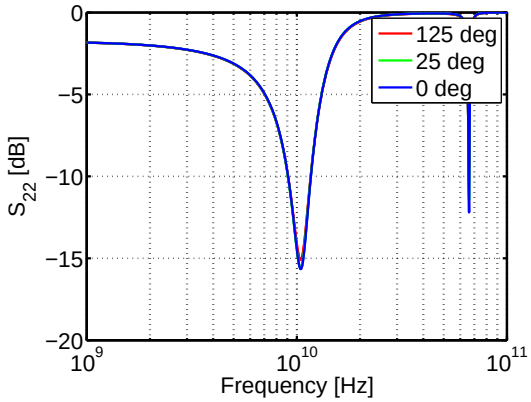


Figure 2.53: SiGe:C temperature dependence of the RF port matching

Stability

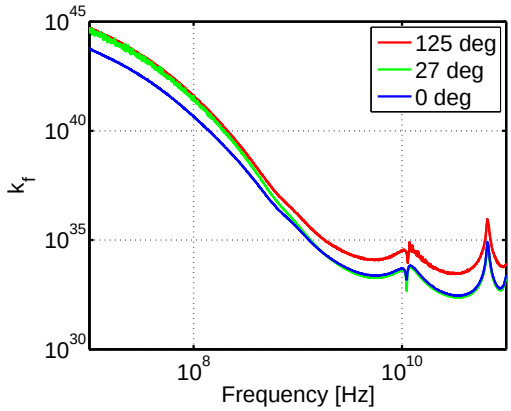


Figure 2.54: SiGe:C temperature dependence of the k_f stability factor ($> 1 \; \forall$ freq)

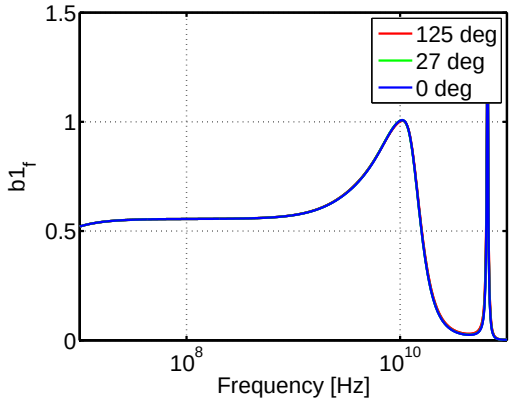


Figure 2.55: SiGe:C temperature dependence of the $b1_f$ stability factor ($> 0 \; \forall$ freq)

Supply voltage dependence

The circuit performance is maintained for a supply voltage variation from 3.0 V to 3.6 V.

RF output spectrum ($f_{BB} = 100MHz$, $f_{LO} = 10GHz$)

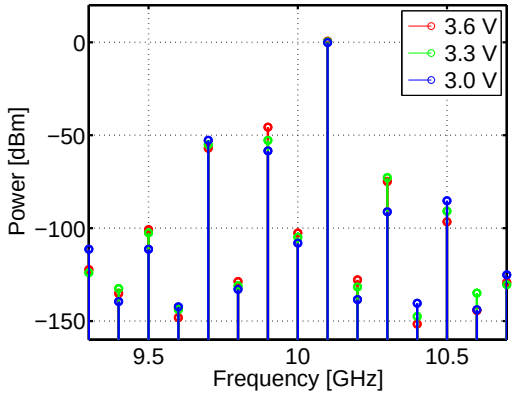


Figure 2.56: SiGe:C supply voltage dependence of the output spectrum

Output power	$> -0.1\ dBm$
Image rejection	$> 46.2\ dBc$
RF HD_3	$> 52.7\ dBc$

Table 2.16: SiGe:C supply voltage dependence of the output spectrum

Phase noise ($f_{LO} = 10GHz$))

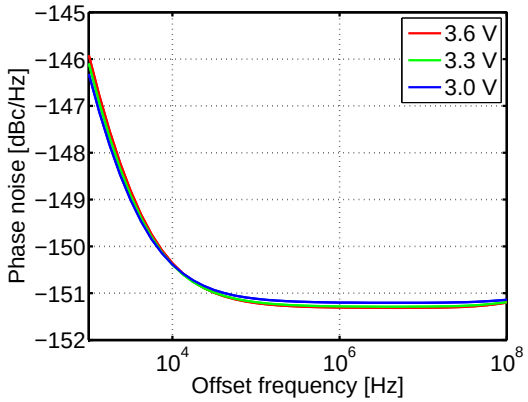


Figure 2.57: SiGe:C supply voltage dependence of the phase noise

Offset freq.	Phase noise
10 Hz	< -127.4 dBc/Hz
100 Hz	< -137.2 dBc/Hz
1 kHz	< -145.9 dBc/Hz
10 kHz	< -150.4 dBc/Hz
100 kHz	< -151.1 dBc/Hz
1 MHz	< -151.2 dBc/Hz
10 MHz	< -151.2 dBc/Hz
100 MHz	< -151.1 dBc/Hz

Table 2.17: SiGe:C supply voltage dependence of the phase noise

Port matching

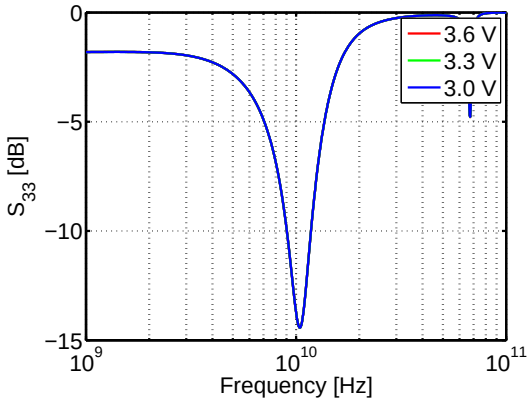


Figure 2.58: SiGe:C supply voltage dependence of the LO port matching

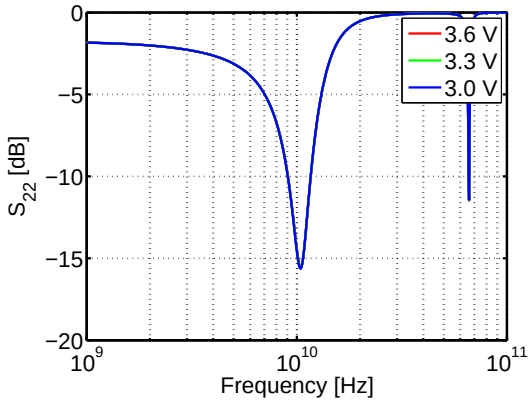


Figure 2.59: SiGe:C supply voltage dependence of the RF port matching

Stability

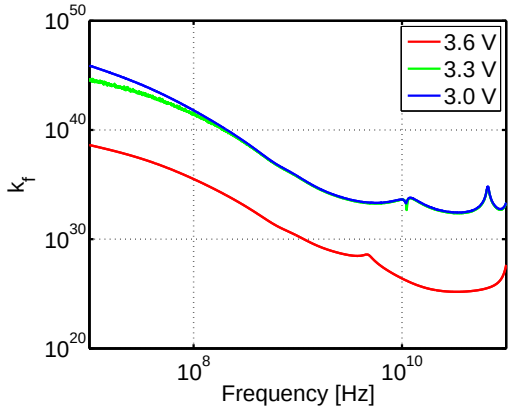


Figure 2.60: SiGe:C supply voltage dependence of the k_f stability factor ($> 1 \; \forall$ freq)

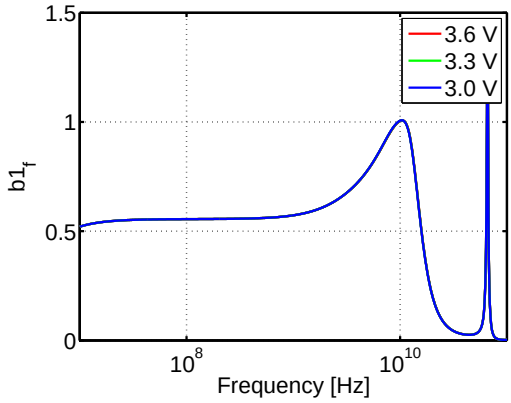


Figure 2.61: SiGe:C supply voltage dependence of the $b1_f$ stability factor ($> 0 \; \forall$ freq)

Summary

The chip layout is reported in Figure 2.62; chip size is $728\mu m \times 1028\mu m$ pads included. The simulated circuit performance is summarized in table 2.18; the clear major limitation of the design is the required total power consumption.

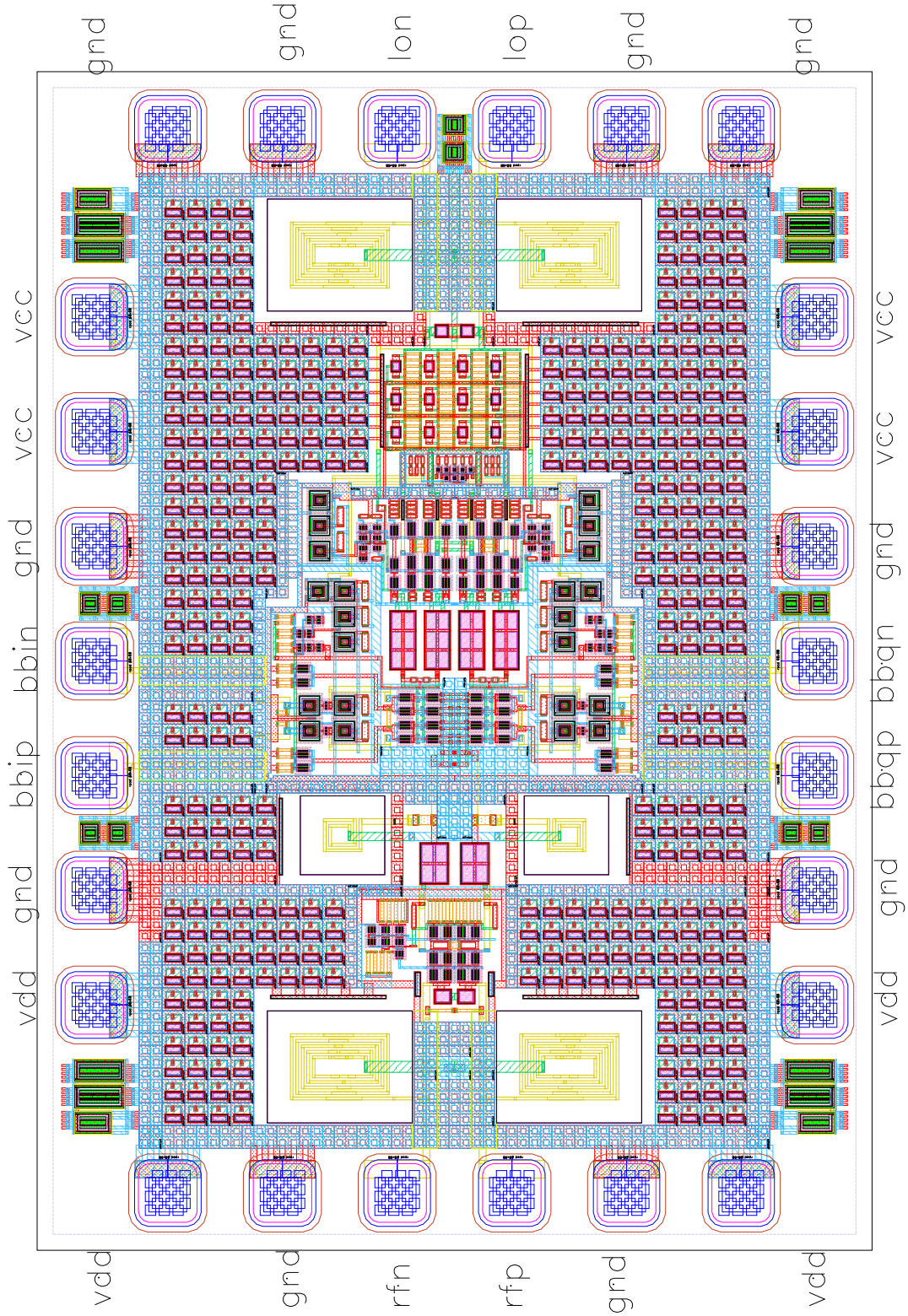


Figure 2.62: SiGe:C X-band upconverter layout ($728\mu m \times 1028\mu m$)

Parameter	Simulation(*)	Comment
BB bandwidth	0–1 GHz	-3dB bw
LO bandwidth	8–13 GHz	-3dB bw
RF bandwidth	7–14 GHz	-3dB bw
RF output power	-2.0 ± 0.5 dBm	
LO power	< -3 dBm	
BB amplitude	400 mVpp	
BB common mode	200 mV	
LO leakage	-43 ± 5 dB	
Image rejection	-56 ± 7 dB	
HD_3	-57 ± 3 dB	baseband HD_3 at RF
Phase noise @ 10 Hz	-123.1 ± 1.1 dBc/Hz	DAC and LO sources
Phase noise @ 100 Hz	-133.0 ± 1.1 dBc/Hz	assumed ideal
Phase noise @ 1 kHz	-142.1 ± 0.9 dBc/Hz	
Phase noise @ 10 kHz	-147.7 ± 0.5 dBc/Hz	
Phase noise @ 100 kHz	-149.3 ± 0.3 dBc/Hz	
Phase noise @ 1 MHz	-149.2 ± 0.3 dBc/Hz	
Phase noise @ 10 MHz	-149.2 ± 0.3 dBc/Hz	
Corner freq	≈ 5 kHz	
BB impedance match	< -8 dB ∈ [0–600] MHz	50Ω s.e. with 6 pF DAC out cap
LO impedance match	< -8 dB ∈ [8.5–12.0] GHz	100Ω differential
RF impedance match	< -8 dB ∈ [8.5–12.0] GHz	100Ω differential
Voltage	3.3 V	
Pdc	360 mW	total
Layout size	$728\mu m \times 1028\mu m$	chipframe size
Layout pads	26	8 I/O - 10 gnd - 4+4 supply

(*) 50 iters montecarlo simulation, Tnom=125deg, 1nH bondwire ∀ pad
LO freq: 10 GHz; BB freq: 10 MHz

Table 2.18: SiGe:C upconverter performance

2.5 Comparison and discussion

The CMOS and SiGe:C upconverters presented in the previous sections present very similar performances in term of output power, spectrum cleanliness, linearity and phase noise.

Frequency modulators for radar applications found in literature are usually implemented only in SiGe or GaInP/GaAs; in this work we show that the standard CMOS technology can be adopted to successfully implement these systems.
There are however some differences between the two modulators.
Advantages of CMOS upconverter:

- cheaper technology;
- better integration with analog baseband/digital radar subsystems;
- better power consumption.

Advantages of SiGe:C upconverter:

- smaller chip size;
- easier architecture;
- smaller layout.

A comparison between the upconverters proposed in this work and the state-of-the-art found in literature is summarized in Table 2.19; apart from a complete FMCW transceiver chip [Wang 09], the comparison is primarily done with doubly-balanced up-conversion mixers optimized for the output power and/or the linearity. Some works include the mixer only while other works also include BB/IF amplifiers or LO generation circuitry, so a comparison in terms of power consumption or chip area makes little sense due to the different type and number of building blocks placed on chip. The key point is that the overall performance our CMOS modulator is comparable with the other SiGe implementations, while having advantages in term of cost and a higher level of integration in a complete mixed-signal system.

Table 2.19: Upconverter comparison.

	[Syu 07]	[Comeau 06]	[Wang 09]	[Lim 09]	[Grau 00]	[Meng 03]	[Italia 04]	This #1 (meas)	This #2 (sim)
Freq. [GHz]	2.4/5.7	19–31	10.5	1.22	5.8	5.2	5.25	10.6	10
Conversion gain [dB]	1.5/-0.2	-0.8	–	6	-17	-2.5	11	–	–
Output power [dBm]	–	–	1	–	–	–	–	-5	-2
LO leak [dBc]	38/43	–	> 40	–	42	–	25	25	43
oP1dB [dBm]	-10.5/-9	-8.6	–	–	-15.5	-12.5	4	–	–
oIP3 [dBm]	12/13	1.4	–	22	–	–	–	14.5	24
Supply [V]	3.5	3.3	3	1.8	2.7	–	–	1.2	3.3
Power [mW]	45[1]	38[2]	350[3]	39.6[4]	17[2]	–[2]	102[5]	180	360
Chip size [mm^2]	0.56	1	8.58	0.58	0.38	1	4	0.91	0.75
Technology	0.35μm SiGe	0.12μm SiGe	0.18μm CMOS	0.18μm CMOS	0.8μm SiGe	2μm GaInP/GaAs	0.8μm SiGe	65 nm CMOS	0.35μm SiGe

[1] Doubly balanced downconversion mixer only.
[2] Doubly balanced mixer only.
[3] Complete transceiver, on wafer probing.
[4] Heterodyne receiver with upconversion of the received RF signal.
[5] I-path only.

Conclusions

Summary of the work, original contribution and future work.

Low-power 2.4 GHz receiver:

- a novel architecture for power consumption reduction is proposed;
- an accurate time-variant analysis is performed for circuit optimization;
- a 2.4 GHz receiver front-end was implemented in a digital 90 nm CMOS technology.

The work shows the effectiveness of the proposed receiver architecture. The measured performance of the front-end complies with the ZigBee standard; our chip has one of the lowest power consumption and smallest area than what is currently present in the literature. A possible future work could be that of integrating a transmitter in the chip and ADCs/DACs to build the complete analog part of the wireless subsystem.

Linear low-noise X-band upconverter:

- an analysis of the I/Q upconverter is proposed;
- a CMOS upconverter and a SiGe:C upconverter for FMCW radar systems are designed, layouted and compared;
- a novel PPF-based tunable phase-shifter to correct I/Q imbalance is proposed.

Most of the upconverters/modulators for radar applications found in the literature up to now are built with SiGe, GaInP or GaAs technologies. The work shows that a pure CMOS implementation compliant with the requirements of Frequency-Modulated Continuous-Wave radar systems can be realized. To complete the work, the CMOS upconverter needs to be fully characterized once driven by the current baseband DACs; moreover, measurements of the SiGe:C bipolar upconverter should confirm the chip simulations which are here reported.

Conclusioni

Conclusione del lavoro, contributi originali e lavoro futuro.

Ricevitore low-power a 2.4 GHz:

- In questo progetto è stata presentata un'innovativa architettura per la riduzione del consumo di potenza;
- è stata condotta un'approfondita analisi tempo-variante per l'ottimizzazione del circuito;
- un prototipo del ricevitore a 2.4 GHz è stato implementato in una tecnologia CMOS digitale a 90 nm.

Il lavoro dimostra la validità dell'architettura proposta. Le prestazioni misurate del front-end rispettano lo standard ZigBee; il nostro chip possiede uno dei più bassi consumi di potenza a l'area più piccola tra tutti i ricevitori low-power al momento presentati in letteratura. Una possibile continuazione del lavoro potrebbe prevedere la realizzazione del trasmettitore, da integrare nello stesso chip, e degli ADC/DAC richiesti per completare la sottosezione analogica del ricetrasmettitore.

Upconverter lineare a basso rumore in banda X:

- Il progetto presenta un'analisi degli upconverter in quadratura;
- il lavoro ha riguardato design, layout e confronto di due versioni di upconverter per sistemi radar FMCW, il primo in tecnologia CMOS ed il secondo in tecnologia SiGe:C;
- viene proposto un innovativo tipo di phase-shifter accordabile basato su filtro polifase.

La maggior parte degli upconverter/modulatori per applicazioni radar attualmente presenti in lettereratura sono costruiti con tecnologie SiGe, GaInP o GaAs. Questo lavoro mostra che è possiblile realizzare un modulatore per Frequency-Modulated Continuous-Wave radar con una tecnologia puramente CMOS. Per completare il lavoro occorre caratterizzare l'upconverter CMOS con gli ingressi in banda base pilotati dai DAC in corrente;

le misure della versione bipolare dell'upconverter dovrebbero infine confermare i risultati di simulazione mostrati in questa tesi.

List of publications

1. Bevilacqua, A.; Camponeschi, M.; Tiebout, M.; Gerosa, A.; Neviani, A.: "Design of broadband inductorless LNAs in ultra-scaled CMOS technologies", *IEEE International Symposium on Circuits and Systems (ISCAS), 2008;* Page(s): 1300-1303.

2. Camponeschi, M.; Bevilacqua, A.; Andreani, P.: "Analysis and Design of a Low-Power Single-Stage CMOS Wireless Receiver", *NORCHIP, 2009;* Page(s): 1-4.

3. Camponeschi, M.; Bevilacqua, A.; Neviani, A.; Andreani, P.; "Accurate Time-Variant Analysis of a Current-Reuse 2.2 GHz 1.3 mW CMOS Front-End", *IEEE International Symposium on Circuits and Systems (ISCAS), 2010;* Page(s): 2063-2066.

4. Camponeschi, M.; Bevilacqua, A.; Andreani, P.; "Time-Variant Analysis and Design of a Power Efficient ISM-Band Quadrature Receiver", *Analog Integrated Circuits and Signal Processing, 2010;* Springer Netherlands; Page(s): 1-10.

Appendix A

Polyphase filter as a phase shifter

In this chapter an analysis of the phase/amplitude imbalance in a multi-stage polyphase filter (PPF) is performed. With respect to a classical PPF, in which the capacitors are equal, we want to estimate the frequency response of the circuit in the presence of a desired *spread in the capacitances. Our goal is to use this desired spread to balance the unavoidable mismatch in the real circuit, and keep the IRR of the I/Q path high.*

A.1 Principle

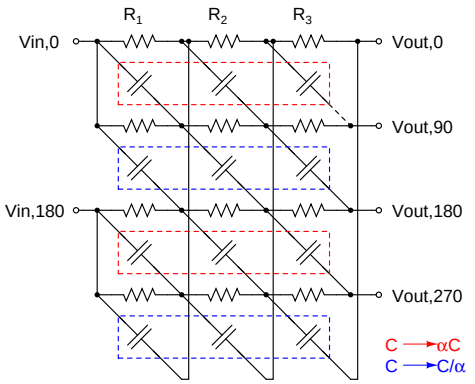
A polyphase filter (PPF) is formed by a cascade of RC stages to generate quadrature signals in a wide bandwidth starting from a differential input signal. In a conventional PPF, the capacitors have all the same value while the resistors are scaled to enhance the bandwidth in which the quadrature signals are generated and to increase the quadrature accuracy [Kaukovuori 08].

In this section we are going to show that it is possible to control the phases of the output signals with a proper control of the capacitors; the proposed principle is shown in Figure A.1(a). The values of the capacitors are controllable and can be varied "by rows" around their nominal values; at the output

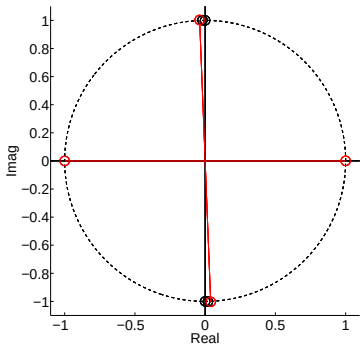
- the differential outputs between out 0 / out 180 and out 90 / out 270 are kept,
- the relative phase among the differential outputs can be controlled and varied around the nominal $\pi/2$ phase difference (see Figure A.1(b)).

In the following, we will derive the phase imbalance (i.e. the phase deviation from nominal $\pi/2$) in the case of a single stage PPF and a two-stages PPF. In the case of the single stage PPF the inputs are driven differentially and the exact value of the amplitude and phase imbalance can be derived. To analyze a two-stages filter, we have to:

- determine the input impedance of the second stage;
- determine the phase/amplitude imbalance of the first stage loaded by the impedance calculated before;
- determine the imbalance introduced by the second stage, driven by the "*quasi*-quadrature" inputs determined in the previous analysis.



(a) PPF tuning



(b) Output phasor representation ($\alpha = 1.1$)

Figure A.1: PPF as phase shifter

A.2 Single stage ppf

We will assume that the single stage ppf has a purely capacitive load; the stage is driven by ideally differential signals.

A.2.1 Input impedance

Consider the single-stage polyphase filter of figure A.2. The calculation of the input

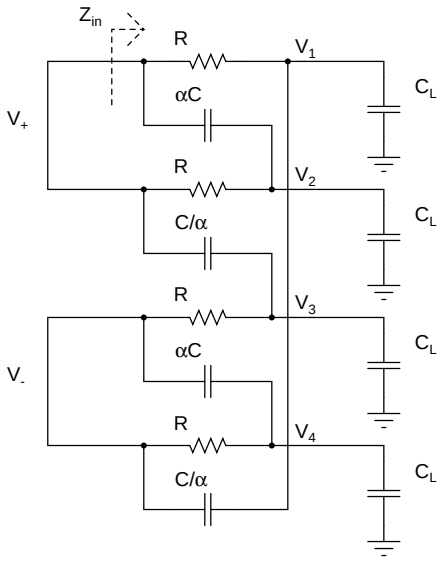


Figure A.2: Single stage polyphase filter with IRR compensation.

impedance $Z_{in}(s)$ is performed grounding all the inputs different from the upper v_+ node, as in figure A.3. Suppose $\alpha = 1$. The input impedance is given by the parallel of two impedances

$$Z_{in}(s) = Z_A(s) \| Z_B(s) \tag{A.1}$$

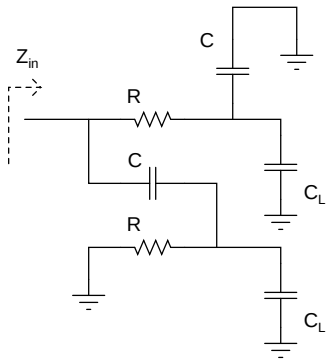


Figure A.3: Polyphase filter cell.

where

$$Z_A(s) = R + \frac{1}{s(C_L + C)} = \frac{1 + s(C_L + C)R}{s(C_L + C)} \tag{A.2}$$

$$Z_B(s) = \frac{1}{sC} + \frac{R}{1 + sRC_L} = \frac{1 + s(C_L + C)R}{sC(1 + sRC_L)}. \tag{A.3}$$

The input admittance is

$$Y_{in}(s) = Y_A(s) + Y_B(s) = s(C_L + 2C)\frac{1 + sR\frac{CC_L}{C_L+2C}}{1 + s(C_L + C)R} \tag{A.4}$$

and the impedance is given by

$$Z_{in}(s) = \frac{1}{s(C_L + 2C)}\frac{1 + s(C_L + C)R}{1 + sR\frac{CC_L}{C_L+2C}} \tag{A.5}$$

which shows a zero at

$$\omega_z = \frac{1}{R(C_L + C)} < \frac{1}{RC} \tag{A.6}$$

and a pole at

$$\omega_p = \frac{C_L + 2C}{RC_LC} > \frac{C_L}{RC_LC} = \frac{1}{RC}. \tag{A.7}$$

For frequencies below ω_p, we can approximate the input impedance as

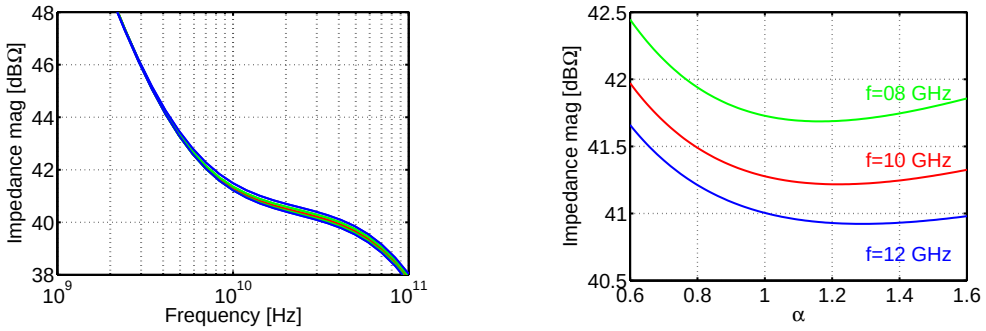
$$Z_{in}(s) \approx \frac{1 + s(C_L + C)R}{s(C_L + 2C)} \approx \frac{1}{s(C_L + 2C)} + \frac{s(C_L + C)R}{s2(C_L + C)} = \frac{R}{2} + \frac{1}{s(C_L + 2C)} \tag{A.8}$$

i.e. as a series of a resistance $R/2$ and a capacitance $C_L + 2C$.

For $\alpha \neq 1$ the expression of the input impedance becomes of third order and offers little design insight:

$$Z_{in,\alpha}(s) = \frac{\left[1 + s\left(C_L + C/\alpha\right)R\right]\left[1 + s\left(C_L + \alpha C\right)R\right]}{s\alpha C(1 + sRC_L)\left[1 + s(C_L + C/\alpha)R\right] + s\left(C_L + C/\alpha\right)\left[1 + s(C_L + \alpha C)R\right]}. \tag{A.9}$$

The change in input impedance for $\alpha \pm 20\%$ is small (Figure A.4), so the approximated value $Z_{in}(s)$ given by A.8 can be assumed valid also for $\alpha \neq 1$.



(a) $\alpha = (\ 0.8\ 0.9\ 1\ 1.1\ 1.2\ )$ (b) $f = (\ 8\ 10\ 12\ )$ GHz

Figure A.4: PPF input impedance, $R = 200\Omega, C = 150fF, C_L = 15fF$

A.2.2 Phase shifting

With reference to the previous circuit, superposition allows us to write:

$$v_1 = v_+ \frac{1}{1 + s(C_L + C/\alpha)R} + v_- \frac{sRC/\alpha}{1 + s(C_L + C/\alpha)R} \tag{A.10a}$$

$$v_2 = v_+ \frac{sR\alpha C}{1 + s(C_L + \alpha C)R} + v_+ \frac{1}{1 + s(C_L + \alpha C)R} \tag{A.10b}$$

Recalling that the circuit is driven differentially, $v_+ = v/2$ and $v_- = -v/2$, from which

$$\frac{v_1}{v} = \frac{1}{2} \frac{1 - sRC/\alpha}{1 + s(C_L + C/\alpha)R} \tag{A.11a}$$

$$\frac{v_2}{v} = \frac{1}{2} \frac{1 + sR\alpha C}{1 + s(C_L + \alpha C)R}. \tag{A.11b}$$

For $s = j\omega$

$$\frac{v_1}{v} = \frac{1}{2} \frac{1 - \omega^2 C/\alpha (C_L + C/\alpha)R^2 - j\omega(C_L + 2C/\alpha)R}{1 + \omega^2 (C_L + C/\alpha)^2 R^2} \tag{A.12a}$$

$$\frac{v_2}{v} = \frac{1}{2} \frac{1 + \omega^2 \alpha C (C_L + \alpha C)R^2 - j\omega C_L R}{1 + \omega^2 (C_L + \alpha C)^2 R^2}. \tag{A.12b}$$

We whish to evaluate the phase/amplitude imbalance at a frequency in general different from $\omega_0 = 1/RC$, so we define a factor, k, defined as

$$\omega = k\omega_0 = \frac{k}{RC}. \tag{A.13}$$

The above equations thus become

$$\frac{v_1}{v} = \frac{1}{2} \frac{1 - k^2(\beta/\alpha + 1/\alpha^2) - jk(\beta + 2/\alpha)}{1 + k^2(\beta + 1/\alpha)^2} \tag{A.14a}$$

$$\frac{v_2}{v} = \frac{1}{2} \frac{1 + k^2(\beta\alpha + \alpha^2) - jk\beta}{1 + k^2(\beta + \alpha)^2} \tag{A.14b}$$

where $\beta = C_L/C$ was defined.

Phase Imbalance

The phase difference ϕ is defined as

$$\phi = \angle\frac{v_1}{v} - \angle\frac{v_2}{v} = \arctan\left[\frac{\Im(v_1/v)}{\Re(v_1/v)}\right] - \arctan\left[\frac{\Im(v_2/v)}{\Re(v_2/v)}\right]. \tag{A.15}$$

Given the following trigonometric identity

$$\arctan a - \arctan b = \arctan\frac{a-b}{1+ab} \tag{A.16}$$

we can rewrite the phase imbalance as

$$\tan\phi = \frac{\Im(v_1/v)\cdot\Re(v_2/v) - \Im(v_2/v)\cdot\Re(v_1/v)}{\Im(v_1/v)\cdot\Im(v_2/v) + \Re(v_1/v)\cdot\Re(v_2/v)}. \tag{A.17}$$

Since

$$\Re(v_1/v) = \frac{1}{2}\frac{1-k^2(\beta/\alpha+1/\alpha^2)}{1+k^2(\beta+1/\alpha)^2} \tag{A.18a}$$

$$\Im(v_1/v) = -\frac{1}{2}\frac{k(\beta+2/\alpha)}{1+k^2(\beta+1/\alpha)^2} \tag{A.18b}$$

$$\Re(v_2/v) = \frac{1}{2}\frac{1+k^2(\beta\alpha+\alpha^2)}{1+k^2(\beta+\alpha)^2} \tag{A.18c}$$

$$\Im(v_2/v) = -\frac{1}{2}\frac{k\beta}{1+k^2(\beta+\alpha)^2} \tag{A.18d}$$

the tangent of the phase imbalance becomes

$$\begin{aligned}\tan\phi &= \frac{-k(\beta+2/\alpha)\cdot[1+k^2(\beta\alpha+\alpha^2)] + k\beta\cdot[1-k^2(\beta/\alpha+1/\alpha^2)]}{k(\beta+2/\alpha)\cdot k\beta + [1-k^2(\beta/\alpha+1/\alpha^2)]\cdot[1+k^2(\beta\alpha+\alpha^2)]} \\ &= \frac{k^3\beta + k(2+k^2\beta^2)\alpha + 2k^3\beta\alpha^2 + k^3(2+\beta^2)\alpha^3 + k^3\beta\alpha^4}{k^2 - k^2\beta(1-k^2)\alpha - (1+k^2\beta^2-k^4\beta^2-k^4)\alpha^2 - k^2\beta(1-k^2)\alpha^3 - k^2\alpha^4}.\end{aligned} \tag{A.19}$$

The phase imbalance Φ, i.e. the deviation of the phase from ideal $\pi/2$, can be easily determined. Let $\Phi = \phi - \pi/2$; then the cotangent of Φ is simply given by

$$\cot\Phi = \cot(\phi - \pi/2) = -\tan\phi. \tag{A.20}$$

The deviation Φ can thus be expressed as

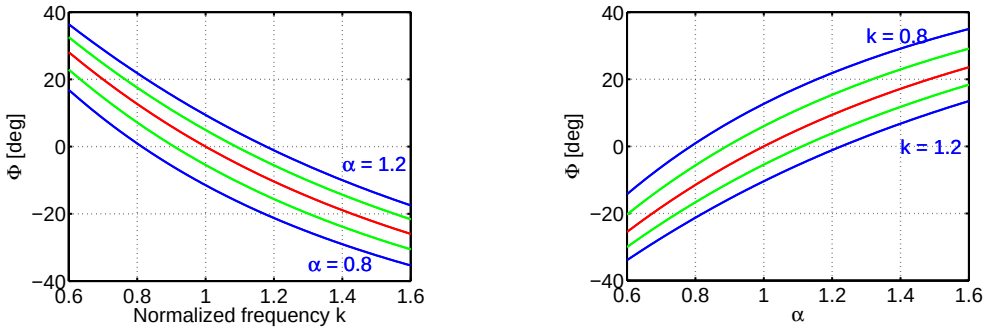
$$\cot\Phi = -\frac{k^3\beta + k(2+k^2\beta^2)\alpha + 2k^3\beta\alpha^2 + k^3(2+\beta^2)\alpha^3 + k^3\beta\alpha^4}{k^2 - k^2\beta(1-k^2)\alpha - (1+k^2\beta^2-k^4\beta^2-k^4)\alpha^2 - k^2\beta(1-k^2)\alpha^3 - k^2\alpha^4}. \tag{A.21}$$

Evaluated at $\omega = \omega_0$, i.e. for $k = 1$, the above equation reduces to

$$\begin{aligned}\cot\Phi\big|_{k=1} &= -\frac{\beta + (2+\beta^2)\alpha + 2\beta\alpha^2 + (2+\beta^2)\alpha^3 + \beta\alpha^4}{1-\alpha^4} = \\ &= \frac{\beta(1+\alpha^2) + \alpha(2+\beta^2)}{\alpha^2-1}\end{aligned} \tag{A.22}$$

from which it can be observed that

$$\Phi(\alpha^{-1})\big|_{k=1} = -\,\Phi(\alpha)|_{k=1}\,. \tag{A.23}$$



(a) $\alpha = (\ 0.8\ 0.9\ 1\ 1.1\ 1.2\ )$ (b) $k = (\ 0.8\ 1\ 1.2\ )$

Figure A.5: Phase imbalance in the single stage PPF, $\beta = 0.1$

Amplitude Imbalance

The amplitude ratio imbalance A_{bal} is defined as

$$A_{bal} = \frac{|v_1/v|}{|v_2/v|}. \tag{A.24}$$

To keep the notation simple, the square of the amplitude imbalance is actually determined

$$\begin{aligned} A_{bal}^2 &= \frac{|v_1/v|^2}{|v_2/v|^2} = \frac{|1 - k^2(\beta/\alpha + 1/\alpha^2) - jk(\beta + 2/\alpha)|^2}{|1 + k^2(\beta + 1/\alpha)^2|^2} \cdot \frac{|1 + k^2(\beta + \alpha)^2|^2}{|1 + k^2(\beta\alpha + \alpha^2) - jk\beta|^2} \\ &= \frac{[1 - k^2(\beta/\alpha + 1/\alpha^2)]^2 + [k(\beta + 2/\alpha)]^2}{[1 + k^2(\beta\alpha + \alpha^2)]^2 + [k\beta]^2} \cdot \frac{[1 + k^2(\beta + \alpha)^2]^2}{[1 + k^2(\beta + 1/\alpha)^2]^2} \\ &= \frac{k^2(\alpha + \beta)^2 + 1}{k^2(\alpha\beta + 1)^2 + \alpha^2} \cdot \frac{\alpha^2 + k^2}{\alpha^2 k^2 + 1} \end{aligned} \tag{A.25}$$

which for $k = 1$ becomes

$$A_{bal}^2\big|_{k=1} = \frac{(\alpha + \beta)^2 + 1}{(\alpha\beta + 1)^2 + \alpha^2}. \tag{A.26}$$

In this case we observe that

$$A_{bal}(\alpha^{-1}) = A_{bal}^{-1}(\alpha). \tag{A.27}$$

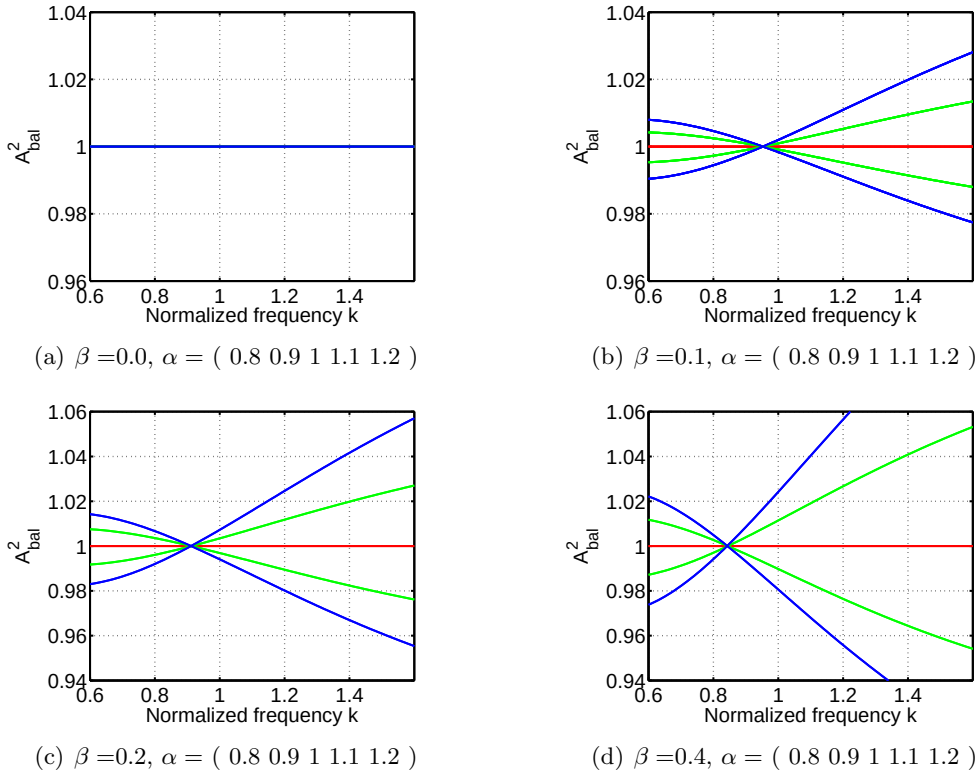
The frequency behavior of the squared amplitude imbalance A_{bal}^2 for various combinations of α and β is plotted in Figure A.6.
Interestingly, increasing the capacitive load β

- the frequency for which $A_{bal}^2 = 1$ decreases;
- the slope of the curves for a given α increases.

The behavior of the squared amplitude imbalance A_{bal}^2 with α for various combinations of k and β is plotted in Figure A.7.

A.3 Two stages ppf

In a two stages PPF, the first stage (R_1, C) is driven differentially and loaded by the second stage, while the second stage (R_2, C) is driven by "quasi quadrature" inputs.



(a) β =0.0, α = (0.8 0.9 1 1.1 1.2)

(b) β =0.1, α = (0.8 0.9 1 1.1 1.2)

(c) β =0.2, α = (0.8 0.9 1 1.1 1.2)

(d) β =0.4, α = (0.8 0.9 1 1.1 1.2)

Figure A.6: Amplitude imbalance in the single stage PPF vs k

A.3.1 Phase shifting in the first stage

The phase shifting θ of the first stage can be determined from the previous analysis. Assuming for simplicity that the input impedance of the second stage is purely capacitive, the phase and amplitude imbalances of the second stage can be derived from the case of the single stage PPF providing that the following substitutions are made:

$$C_{\mathrm{L}} \Rightarrow C_{\mathrm{L}} + 2C \tag{A.28a}$$

$$R \Rightarrow R_1, \text{ i.e. } k \Rightarrow k_1 \tag{A.28b}$$

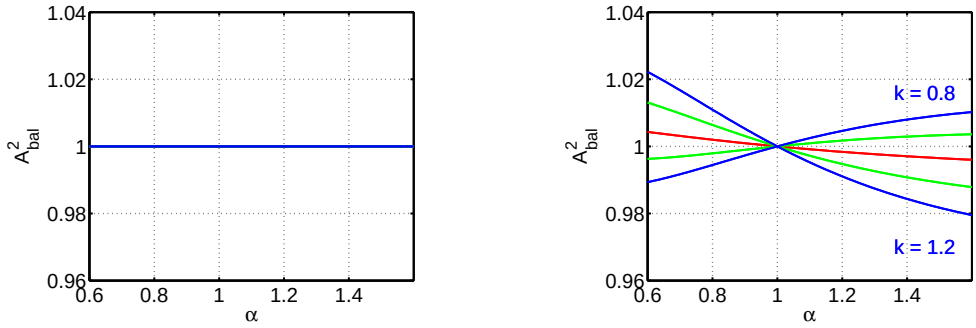
$$\beta \Rightarrow 2 + \beta \tag{A.28c}$$

$$\Phi \Rightarrow \theta \tag{A.28d}$$

Phase imbalance

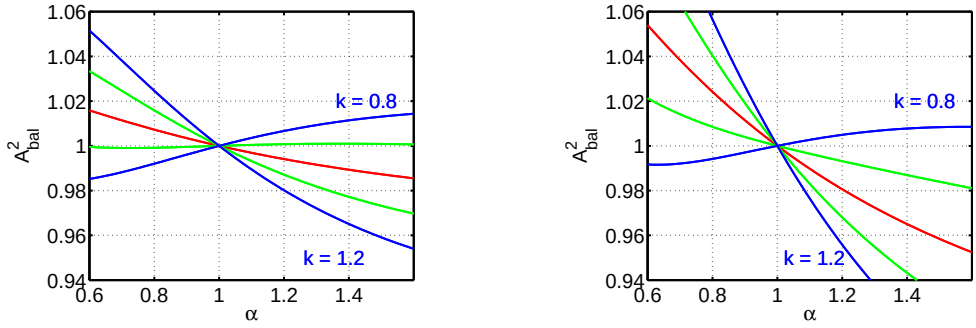
The cotangent of the phase imbalance θ is given by

$$\cot\theta = \frac{a_4\alpha^4 + a_3\alpha^3 + a_2\alpha^2 + a_1\alpha + a_0}{b_4\alpha^4 + b_3\alpha^3 + b_2\alpha^2 + b_1\alpha + b_0} \tag{A.29}$$



(a) β =0.0, k = (0.8 0.9 1 1.1 1.2)

(b) β =0.1, k = (0.8 0.9 1 1.1 1.2)



(c) β =0.2, k = (0.8 0.9 1 1.1 1.2)

(d) β =0.4, k = (0.8 0.9 1 1.1 1.2)

Figure A.7: Amplitude imbalance in the single stage PPF vs α

where

$$
\begin{aligned}
a_4 &= k_1^3(2+\beta)\\
a_3 &= k_1^3[2+(2+\beta)^2]\\
a_2 &= 2k_1^3(2+\beta)\\
a_1 &= k_1[2+k_1^2(2+\beta)^2]\\
a_0 &= k_1^3(2+\beta)\\
b_4 &= k_1^2\\
b_3 &= k_1^2(2+\beta)(1-k_1^2)\\
b_2 &= (1-k_1^2)[1+k_1^2+k_1^2(2+\beta)^2]\\
b_1 &= k_1^2(2+\beta)(1-k_1^2)\\
b_0 &= -k_1^2.
\end{aligned}
$$

Amplitude imbalance

The amplitude imbalance is

$$A_{bal}^2 = \frac{k_1^2[\alpha+(2+\beta)]^2+1}{k_1^2[\alpha(2+\beta)+1]^2+\alpha^2} \cdot \frac{\alpha^2+k_1^2}{\alpha^2 k_1^2+1}. \tag{A.30}$$

A.3.2 Phase shifting in the second stage with ideal input amplitudes

The inputs of the second stages are in "quasi quadrature", i.e. show amplitude and phase imbalance as in table A.3.2.

input #	amplitude	phase
1	$\sqrt{\eta}A$	θ_0
2	$A/\sqrt{\eta}$	$\theta_0 + \pi/2 + \theta$
3	$\sqrt{\eta}A$	$\theta_0 + \pi$
4	$A/\sqrt{\eta}$	$\theta_0 + 3\pi/2 + \theta$

Table A.1: Quasi-quadrature inputs

Without loss of generality, it can be assumed that $A = 1$ and $\theta_0 = 0$, since this does not impact the amplitude ratio η and the phase difference Φ among mismatched outputs.

In the following, we will consider separately the effects of phase and amplitude imbalance: in a first calculation, we will assume no amplitude mismatch (i.e. $\eta = 1$) and a general phase offset θ; in a second case, we assume $\eta \neq 1$ but $\theta = 0$. Here, we assume that the phases of the of the four inputs of a polyphase stage are 0, $\pi/2 + \theta$, π and $3\pi/2 + \theta$, respectively.

The output voltages are given by

$$v_1 = v\frac{1}{1 + s(C_L + C/\alpha)R_2} - v\frac{je^{j\theta}sR_2C/\alpha}{1 + s(C_L + C/\alpha)R_2} \tag{A.31a}$$

$$v_2 = v\frac{sR_2\alpha C}{1 + s(C_L + \alpha C)R_2} + v\frac{je^{j\theta}}{1 + s(C_L + \alpha C)R_2} \tag{A.31b}$$

so that

$$\frac{v_1}{v} = \frac{1 - je^{j\theta}sR_2C/\alpha}{1 + s(C_L + C/\alpha)R_2} \tag{A.32a}$$

$$\frac{v_2}{v} = \frac{sR_2\alpha C + je^{j\theta}}{1 + s(C_L + \alpha C)R_2}. \tag{A.32b}$$

For $s = j\omega$

$$\begin{aligned}\frac{v_1}{v} =& \frac{1 - j(\cos\theta + j\sin\theta)j\omega R_2C/\alpha}{1 + j\omega(C_L + C/\alpha)R_2} \\ =& \frac{1 + \omega\cos\theta R_2C/\alpha + \omega^2\sin\theta C/\alpha(C_L + C/\alpha)R_2^2}{1 + \omega^2(C_L + C/\alpha)^2R_2^2} \\ & - j\frac{\omega(C_L + C/\alpha)R_2 + \omega^2\cos\theta C/\alpha(C_L + C/\alpha)R_2^2 - \omega\sin\theta R_2C/\alpha}{1 + \omega^2(C_L + C/\alpha)^2R_2^2}\end{aligned} \tag{A.33a}$$

$$\begin{aligned}\frac{v_2}{v} =& \frac{j\omega R_2\alpha C + j(\cos\theta + j\sin\theta)}{1 + j\omega(C_L + \alpha C)R_2} \\ =& \frac{-\sin\theta + \omega\cos\theta(C_L + \alpha C)R_2 + \omega^2\alpha C(C_L + \alpha C)R_2^2}{1 + \omega^2(C_L + \alpha C)^2R_2^2} \\ & + j\frac{\omega\sin\theta(C_L + \alpha C)R_2 + \cos\theta + \omega R_2\alpha C}{1 + \omega^2(C_L + \alpha C)^2R_2^2}.\end{aligned} \tag{A.33b}$$

For $\omega = k_2\omega_0 = k_2/(R_2C)$ we obtain

$$\frac{v_1}{v} = \frac{\alpha^2 + k_2\alpha\cos\theta + k_2^2\sin\theta(\alpha\beta+1) - j[k_2\alpha(\alpha\beta+1) + k_2^2\cos\theta(\alpha\beta+1) - k_2\alpha\sin\theta]}{\alpha^2 + k_2^2(\alpha\beta+1)^2} \tag{A.34a}$$

$$\frac{v_2}{v} = \frac{-\sin\theta + k_2\cos\theta(\beta+\alpha) + k_2^2\alpha(\beta+\alpha) + j[k_2\sin\theta(\alpha+\beta) + \cos\theta + k_2\alpha]}{1 + k_2^2(\beta+\alpha)^2}. \tag{A.34b}$$

Phase Imbalance

For the phase imbalance Φ we obtain

$$\cot\Phi = \frac{a_4\alpha^4 + a_3\alpha^3 + a_2\alpha^2 + a_1\alpha + a_0}{b_4\alpha^4 + b_3\alpha^3 + b_2\alpha^2 + b_1\alpha + b_0} \tag{A.35}$$

where

$$\begin{aligned}
a_4 &= k_2^3\beta \\
a_3 &= -k_2(k_2^2-1)\sin\theta + \beta k_2^2(k_2^2+1)\cos\theta + k_2(1+k_2^2+\beta^2k_2^2) \\
a_2 &= (k_2^2+1)(k_2^2+\beta^2k_2^2+1)\cos\theta + 2\beta k_2^3 \\
a_1 &= k_2(k_2^2-1)\sin\theta + \beta k_2^2(k_2^2+1)\cos\theta + k_2(k_2^2+\beta^2k_2^2+1) \\
a_0 &= k_2^3\beta \\
b_4 &= k_2^2 \\
b_3 &= \beta k_2^2(k_2^2-1)\sin\theta + k_2(k_2^2+1)\cos\theta \\
b_2 &= (k_2^2-1)(k_2^2+\beta^2k_2^2+1)\sin\theta \\
b_1 &= \beta k_2^2(k_2^2-1)\sin\theta - k_2(k_2^2+1)\cos\theta \\
b_0 &= -k_2^2.
\end{aligned}$$

For $k_2 = 1$ the above expression reduces to

$$\cot\Phi = \frac{\alpha^2\beta + \alpha\beta^2 + 2\alpha + \beta}{(\alpha-1)(\alpha+1)}. \tag{A.36}$$

Observation. For $\theta = 0$ (A.35) simplifies in

$$\cot\Phi = \frac{k_2^2(\alpha\beta+1)(\alpha+\beta) + \alpha}{k_2(\alpha-1)(\alpha+1)}. \tag{A.37}$$

Once again

$$\Phi(\alpha^{-1})\big|_{k_2=1} = -\,\Phi(\alpha)|_{k_2=1}\,. \tag{A.38}$$

Amplitude imbalance

The square of the amplitude imbalance is

$$A_{bal}^2 = \frac{\alpha^2 + 2k_2\cos\theta\alpha + k_2^2}{k_2^2\alpha^2 + 2k_2\cos\theta\alpha + 1} \cdot \frac{k_2^2(\alpha+\beta)^2 + 1}{k_2^2(\alpha\beta+1)^2 + \alpha^2} \tag{A.39}$$

so that

$$A_{bal}(\alpha^{-1}) = A_{bal}^{-1}(\alpha). \tag{A.40}$$

Observation. For $\theta = 0$

$$A_{bal}^2 = \frac{(\alpha + k_2)^2}{(\alpha k_2 + 1)^2} \cdot \frac{k_2^2(\alpha + \beta)^2 + 1}{k_2^2(\alpha\beta + 1)^2 + \alpha^2}. \tag{A.41}$$

A.3.3 Phase shifting in the second stage with ideal input phases

Assuming no phase shift but only amplitude imbalance, the output voltages are

$$v_1 = \sqrt{\eta} v \frac{1}{1 + s(C_L + C/\alpha)R_2} - v/\sqrt{\eta} \frac{jsR_2C/\alpha}{1 + s(C_L + C/\alpha)R_2} \tag{A.42a}$$

$$v_2 = \sqrt{\eta} v \frac{sR_2\alpha C}{1 + s(C_L + \alpha C)R_2} + v/\sqrt{\eta} \frac{j}{1 + s(C_L + \alpha C)R_2} \tag{A.42b}$$

so that

$$\frac{v_1}{v} = \frac{\sqrt{\eta} - jsR_2C/(\sqrt{\eta}\alpha)}{1 + s(C_L + C/\alpha)R_2} \tag{A.43a}$$

$$\frac{v_2}{v} = \frac{\sqrt{\eta} sR_2\alpha C + j/\sqrt{\eta}}{1 + s(C_L + \alpha C)R_2}. \tag{A.43b}$$

For $s = j\omega$

$$\frac{v_1}{v} = \frac{\sqrt{\eta} + \omega R_2C/(\sqrt{\eta}\alpha) - j[\omega\sqrt{\eta}(C_L + C/\alpha)R_2 + \omega^2 C/(\sqrt{\eta}\alpha)(C_L + C/\alpha)R_2^2]}{1 + \omega^2(C_L + C/\alpha)^2 R_2^2} \tag{A.44a}$$

$$\frac{v_2}{v} = \frac{\omega/\sqrt{\eta}(C_L + \alpha C)R_2 + \omega^2\sqrt{\eta}\alpha C(C_L + \alpha C)R_2^2 + j[\omega\sqrt{\eta}R_2\alpha C + 1/\sqrt{\eta}]}{1 + \omega^2(C_L + \alpha C)^2 R_2^2}. \tag{A.44b}$$

With $\omega = k_2\omega_0 = k_2/(R_2C)$ we get

$$\frac{v_1}{v} = \frac{1}{\sqrt{\eta}} \cdot \frac{\eta\alpha^2 + k_2\alpha - j[k_2\eta\alpha(\alpha\beta + 1) + k_2^2(\alpha\beta + 1)]}{\alpha^2 + k_2^2(\alpha\beta + 1)^2} \tag{A.45a}$$

$$\frac{v_2}{v} = \frac{1}{\sqrt{\eta}} \cdot \frac{k_2(\beta + \alpha) + k_2^2\eta\alpha(\beta + \alpha) + j[k_2\eta\alpha + 1]}{1 + k_2^2(\beta + \alpha)^2}. \tag{A.45b}$$

Phase Imbalance

The cotangent of the phase imbalance is found to be

$$\cot\Phi = \frac{k_2^2(\alpha\beta + 1)(\alpha + \beta) + \alpha}{k_2(\alpha - 1)(\alpha + 1)},$$

independent on the input amplitude mismatch η and therefore equal to (A.37).

Amplitude Imbalance

The squared amplitude imbalance is

$$A_{bal}^2 = \frac{(\alpha\eta + k_2)^2}{(\alpha k_2 \eta + 1)^2} \cdot \frac{k_2^2(\alpha+\beta)^2 + 1}{k_2^2(\alpha\beta+1)^2 + \alpha^2} \tag{A.46}$$

Observation. For $\eta = 1$

$$A_{bal}^2 = \frac{(\alpha + k_2)^2}{(\alpha k_2 + 1)^2} \cdot \frac{k_2^2(\alpha+\beta)^2 + 1}{k_2^2(\alpha\beta+1)^2 + \alpha^2}, \tag{A.47}$$

which is (A.41).

A.3.4 Overall phase shifting in the second stage

The calculation of the overall phase shift requires to calculate the phase shift $\Phi(\omega)$ introduced by the first stage with (A.29), which is frequency dependent, and than fed it into (A.35) to determine the additional phase shift introduced by the second stage. The complete expression is quite complex and gives little design insight.

To simplify the problem, we calculate the phase shift at the two angular frequencies $\omega = 1/(R_1C)$ and $\omega = 1/(R_2C)$, i.e. for $k_1 = 1$ and $k_2 = 1$. We further assume that

- $C_L = 0 \Rightarrow \beta = 0$;
- $\theta \ll 1 \Rightarrow \sin\theta \approx \theta, \cos\theta \approx 1, \cot\theta \approx 1/\theta$.

The phase imbalance θ introduced by the first stage (A.29) becomes

$$\frac{1}{\theta} \approx \frac{2k_1^3\alpha^4 + 6k_1^3\alpha^3 + 4k_1^3\alpha^2 + 2k_1(1+2k_1^2)\alpha + 2k_1^3}{k_1^2\alpha^4 + 2k_1^2(1-k_1^2)\alpha^3 + (1-k_1^2)(1+5k_1^2)\alpha^2 + 2k_1^2(1-k_1^2)\alpha - k_1^2}, \tag{A.48}$$

while the overall phase imbalance Φ (A.35) satisfies

$$\cot\Phi \approx \alpha \frac{[k_2(k_2^2-1)\theta - k_2(k_2^2+1)]\alpha^2 - (k_2^2+1)^2\alpha - k_2(k_2^2-1)\theta - k_2(k_2^2+1)}{-k_2^2\alpha^4 - k_2(k_2^2+1)\alpha^3 + (1-k_2^2)(1+k_2^2)\alpha^2 + k_2(1+k_2^2)\alpha + k_2^2}. \tag{A.49}$$

Phase imbalance at $\omega = 1/(R_1C)$

For $\omega = 1/(R_1C)$ than $k_1 = 1$ and $k_2 = R_2/R_1 \triangleq r$. The phase imbalance θ from the first stage is

$$\theta \approx \frac{\alpha^2 - 1}{2(\alpha^2 + 3\alpha + 1)} \approx \frac{\alpha - 1}{2(\alpha + 1)}, \tag{A.50}$$

which, plugged into (A.49), leads to

$$\begin{aligned}\cot\Phi_1 &\approx \frac{\alpha(\alpha+1)[r(r^2+1)\alpha^2 + 2(r^4+r^3+2r^2-r+1)\alpha + r(r^2+1)]}{(\alpha-1)[(2r^2)\alpha^4 + 2r(r+1)^2\alpha^3 + (r^4+4r^3+4r^2+4r-1)\alpha^2 + 2r(r+1)^2\alpha + 2r^2]} \\ &\triangleq \frac{\alpha}{\alpha-1} \cdot P_k(\alpha).\end{aligned} \tag{A.51}$$

To get more insight into the previous equation, let's assume $\alpha \approx 1$ and suppose $P_k(\alpha) \approx P_k(1)$. The phase imbalance reduces to

$$\cot\Phi_1 \approx \frac{4\alpha}{\alpha-1} \cdot \frac{(r^2+1)(r+1)}{r^3+7r^2+9r-1}. \tag{A.52}$$

Phase imbalance at $\omega = 1/(R_2C)$

For $\omega = 1/(R_2C)$ than $k_1 = R_1/R_2 \stackrel{\triangle}{=} 1/r$ and $k_2 = 1$. Regardless of the phase imbalance θ introduced by the first stage, the overall phase imbalance at $\omega = 1/(R_2C)$ reduces to

$$\cot \Phi_2 = \frac{2\alpha}{\alpha^2 - 1}. \tag{A.53}$$

Observation. If $R_1 = R_2$ then $r = 1$; in the assumption that $\alpha \approx 1$ (A.52) becomes

$$\cot \Phi_1 \approx \frac{\alpha}{\alpha - 1} \approx \frac{\alpha}{\alpha - 1} \cdot \frac{2}{\alpha + 1} = \cot \Phi_2 \tag{A.54}$$

validating the approximations carried out in the calculation of the phase shift at $1/(R_1C)$.

A.3.5 Implementation

In a real desgin of the proposed phase shifter, it's easier to implement a linear tuning of the capacitances. The above calculations can be easily adapted with the substitution $\alpha = 1 + \varepsilon$. Indeed, if $\alpha \approx 1$ then $\varepsilon \approx 0$ and

$$C\alpha \Rightarrow C(1 + \varepsilon), \tag{A.55a}$$

$$C/\alpha \Rightarrow C/(1 + \varepsilon) \approx C(1 - \varepsilon) \tag{A.55b}$$

indicating that all the required capacitance are linearly spaced and can be realized with a proper digitally controlled capacitor bank.

Limiting our analysis to the single stage polyphase filter, the phase and amplitude imbalance with the propose linear tuning can be easily derived from (A.21) and (A.25) respectively. With the substitutions

$$\alpha^p = (1 + \varepsilon)^p \approx 1 + p\varepsilon \qquad p = 1 \dots 4 \tag{A.56}$$

the phase imbalance (A.21) becomes

$$\begin{aligned} \Phi &\approx 1/\cot \Phi \\ &\approx \frac{2(-\beta^2k^4+\beta^2k^2-2\beta k^4+2\beta k^2-k^4+2k^2+1)\varepsilon-\beta^2k^4+\beta^2k^2-2\beta k^4+2\beta k^2-k^4+1}{2(2\beta^2k^3+4\beta k^3+3k^3+k)\varepsilon+2(\beta^2k^3+2\beta k^3+k^3+k)} \end{aligned} \tag{A.57}$$

while the amplitude imbalance (A.25) is

$$A^2_{bal} \approx \frac{2(\beta^2k^2+\beta^2k^4+3\beta k^2+k^4+2k^2+1)\varepsilon+\beta^2k^4+\beta^2k^2+2\beta k^4+2\beta k^2+k^4+2k^2+1}{2(2\beta^2k^4+\beta^2k^2+3\beta k^4+\beta k^2+k^4+2k^2+1)\varepsilon+\beta^2k^4+\beta^2k^2+2\beta k^4+2\beta k^2+k^4+2k^2+1}. \tag{A.58}$$

Substituting $\alpha = 1 + \varepsilon$ in (A.21) and (A.25) and assuming $\omega = 1/(RC)$ (i.e. $k = 1$), we get

$$\Phi \approx \frac{\varepsilon(\varepsilon + 2)}{\varepsilon^2\beta + \varepsilon\beta^2 + 2\varepsilon\beta + 2\varepsilon + \beta^2 + 2\beta + 2} \tag{A.59}$$

and

$$A_{bal}^2 = \frac{\varepsilon^2 + 2\varepsilon\beta + 2\varepsilon + \beta^2 + 2\beta + 2}{\varepsilon^2\beta^2 + \varepsilon^2 + 2\varepsilon\beta^2 + 2\varepsilon\beta + 2\varepsilon + \beta^2 + 2\beta + 2}. \tag{A.60}$$

If $\varepsilon \ll 1$ then ε^2 is negligible, leading to

$$\begin{aligned} \Phi &\approx \frac{\varepsilon}{(1+\varepsilon)(1+\beta+\beta^2/2)} \\ &\approx \frac{\varepsilon}{1+\beta+\beta^2/2} \end{aligned} \tag{A.61}$$

and

$$A_{bal}^2 = \frac{2\varepsilon + 2\beta + 2\varepsilon\beta + \beta^2 + 2}{2\varepsilon + 2\beta + 2\varepsilon\beta + 2\varepsilon\beta^2 + \beta^2 + 2} \tag{A.62}$$

respectively. Further assuming no capacitive load, i.e. $\beta = 0$, we simply get

$$\Phi \approx \varepsilon \tag{A.63}$$

and

$$A_{bal}^2 = 1, \tag{A.64}$$

indicating that for small variations of the tuned capacitance the attainable phase shifting Φ is linear whilst the amplitude is unaffected.

A.4 Conclusion

A novel use of a polyphase filter as a phase shifter is introduced. Basic equations for the amplitude and phase imbalances were derived in the case of a single stage filter and of a two stage filter with a capacitive loading. A possible implementation with a linear tuning is discussed and analyzed, showing the validity of the proposed concept.

Appendix B

Bipolar diode mixer

A diode mixer for frequency conversion in bipolar integrated circuit was investigated.

The conceptual schematic of the mixer core is sketched in Figure B; the circuit is the integrated counterpart of the common discrete microwave passive Schottky diode mixers, implemented with diodes which can be found in any bipolar standard library, without (optional) process improvements.

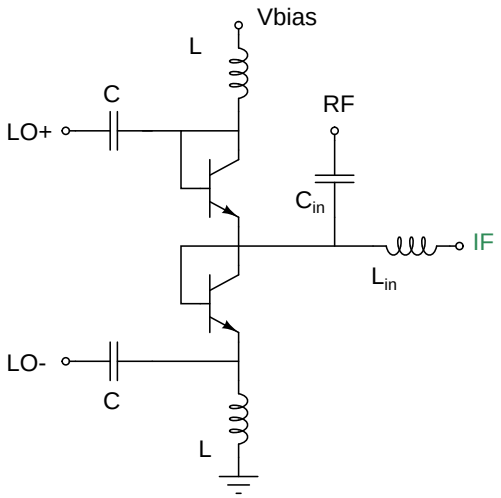


Figure B.1: SiGe passive diode mixer

Two diode-connected npn bipolar transistors are connected in series; the baseband (DC-coupled) input IF signal drives the common node, while the differential local oscillator signal is applied to the core by means of LC high-pass filters. Diodes nonlinearities produce the sum (RF + IF) and difference (RF - IF) upconverted tones at the common diode node, which is eventually made available to the RF port through a second LC high pass filter.

Mixer transistors are designed with minimum size to reduce the parasitic and increase the linearity; npn transistors are biased with a $v_{\mathrm{be}} \approx v_{\mathrm{be,ON}} \approx 800mV$ to reduce the required LO amplitude [Maas 92]. The baseband input is DC-coupled as required in our application.

Advantages:

- by properly combining four cores a doubly balanced mixer with LO rejection and suppression of the image can be obtained;
- power consumption is very low;
- each core requires a small area.

Disadvantages:

- negative conversion gain;
- poor/narrowband IF-to-RF port isolation;
- LO suppression is sensitive to mismatches in the layout;
- linearity is very sensitive to device parasitic;
- moderate temperature variation of the circuit performance.

In conclusion, the passive bipolar mixer described in this section can be implemented in a very compact area. The negative conversion gain can not be as issue depending on the application, but the low power consumption vanishes when the subsequent RF amplification is included.

This kind of mixer proved to be unsuitable for our Frequency-Modulated Continuous-Wave radar application: the insufficient port isolation translates into a not acceptable level of spurious tone suppression in the X-band. The sensitivity of the linearity to the device parasitic were too high for out performance-driven design.

Appendix C

Overview of ESD Protection Strategies in Radio-Frequency CMOS Circuits

The ESD protection of CMOS Radio-Frequency circuits is a critical issue, since the common ESD clamps tend to degrade the performances of such circuits in terms of power matching, gain and noise figure. In this section we give a brief overview of these problems and presents the state-of-the-art RF-ESD protection strategies.[1]

C.1 Introduction

The technological scaling of the recent years made the CMOS technology suitable for the implementation of fully integrated RF transceivers. The downscaling led to the realization of CMOS transistor with even higher cut-off frequency (well above 100 GHz for a 90 nm tech), making the design of CMOS wireless devices operating into the gigahertz range of frequencies possible.

On the other hand, the protection of Radio-Frequency circuits from ElectroStatic Discharge events is becoming even and even critical as technology scales. To understand the problem, consider that in a typical 90 nm CMOS technology the gate oxide (1.2 nm of thickness) can only withstand an instantaneous V_{gs} of $+4.5\ V$ / -5.25 V before breakdown [Thijs 05], posing serious reliability problems. Moreover, we have to consider the fact in a typical RF wireless front-end a common source amplification stage (part of the Low Noise Amplifier) is the first block after the antenna: the gate of such transistor is therefore directly connected to an IO pin.

While the power clamp is not of concern since it is not directly connected to any signal path, the RF pads are critical and an ESD protection is thus mandatory to guarantee the survival of the circuit. An ideal protection:

- should not to be visible at the RF frequency of operation to preserve the input matching, the bandwidth and the gain of the RF transceiver unchanged,
- should have a high quality factor, since lossy reactive components placed in front of the RF chain increase the noise figure of the system, and

[1] The section reports some general considerations and a summary of significant contributions relative to ESD protection strategies found in literature. Shown data, figures and plots belong to the respective authors.

- should obviously be an effective ESD protection.

Meeting all these constraints at the same time is not trivial. The problem therefore is: How to assure that the protection does not degrade the performances of the RF blocks?

Several different approaches have been proposed in the last few years; these approaches can be divided into two main categories:

- the plug-and-play method, that consists on developing a typology of ESD protection, with minimum impact on the performances on the circuit, that can be selected from a library and included into the RF design once this design is completed; and

- the co-designed methodology, in which the design of the circuit and that of the ESD protection scheme is concurrent.

This report is organized as follows. The *"Low-C"* approach, in which the maximum parasitic capacitance that can be tolerated in the circuit with minimum impact is determined, is initially presented in Section C.2; Sections C.3 and C.4 present two narrowband techniques whose aim is that of hiding the parasitic capacitance introduced by the protection at the RF operating frequency, namely the *cancellation* and the *isolation* techniques. Section C.5 gives insight into the *co-design* approach, while Section C.6 deals with *inductor-based* protection strategies. Section C.7 provides some additional insight into the problems of ESD protection for *broadband* circuits, while Section C.8 draws the conclusions on the topic.

C.2 "Low-C" approach

This is the traditional and straightforward strategy; it consists on determining the maximum parasitic capacitance that the circuit can sustain and therefore insert a proper protection that doesn't exceed this limit.

A simple calculation can show how much capacitance can be tolerated. Consider the circuit in figure C.1, representing a Low Noise Amplifier (a cascode LNA with inductive degeneration in this particular case) driven by a 50 Ω source (an antenna), with an ESD protection drawn as a "black box" Z_{esd}.

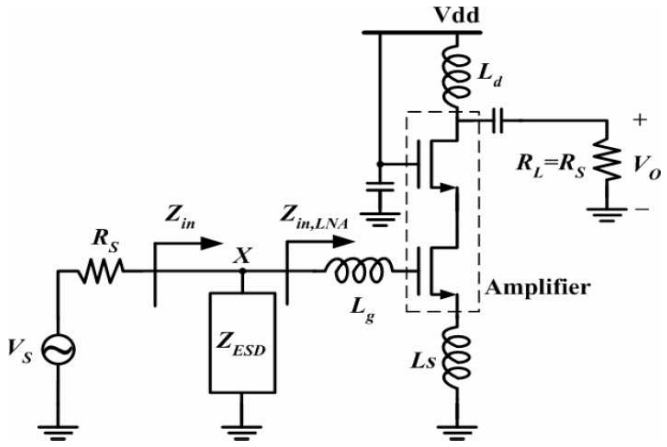


Figure C.1: ESD protected inductive degenerated LNA

The LNA is typically designed to assure a 50 Ω impedance in the bandwidth of interest to assure power matching with the source; we can therefore assume $Z_{in,LNA} = 50\ \Omega \triangleq R_s$ at the frequency of operation. We model the ESD protection simply with its parasitic capacitance shunting the input, i.e. $Z_{esd}(s) = 1/sC_{par}$; its main undesired effect is that of lowering the value of the input impedance increasing the power reflected toward the antenna. The input impedance $Z_{in}(s)$ in this case is given by

$$Z_{in}(s) = \frac{R_s}{1 + sR_sC_{par}}. \tag{C.1}$$

To assure an adequate input matching Γ we must guarantee

$$|\Gamma|_{dB} \triangleq 20 \log \left| \frac{Z_s - Z_{in}(s)}{Z_s + Z_{in}(s)} \right| \leq -10\ dB \tag{C.2}$$

where Z_s is the source impedance, equal to R_s. Finding the expression of $Z_{in}(s)$ in the above expression, substituting into (C.1) and resolving for C_{par}, we find the maximum capacitance that that can be tolerated:

$$C_{par} = \frac{1}{\pi R_s f} \sqrt{\frac{|\Gamma|^2}{1 - |\Gamma|^2}}. \tag{C.3}$$

At 5 GHz this translates into a 400 fF total capacitance; with ≈ 70 fF for the input pad and ≈ 200 fF for the input stage, only ≈ 130 fF remains for the ESD protection stage. This stage must guarantee protection against both positive and negative stresses of the I/O pad; typically a dual-diodes stage is chosen, in which one diode conducts current from ground to the pad in case of a negative stress of the input, while a second diode conducts from the pad to V_{DD} in case of a positive stress. At small signal these diodes appear in parallel and must satisfy the above limit; it is therefore critical to guarantee a sufficient robustness.

The "Low-C" approach can thus only be applied as protection scheme in the lower GHz range of operating frequency [Soldner 05]; at higher frequency the problem becomes unsolvable and other protection strategies are required.

C.3 ESD cancellation technique

A possible solution to the aforementioned problems could be the use of an inductor as protecting element. The basic idea [Leroux 01] is that of resonating the parasitic capacitance introduced by the pad and by the input stage, as in figure C.2(a): at the operating frequency the shunt impedance is sufficiently high and gives minimal impact on RF performances, while protecting the circuit from HBM-type events (which frequency is limited in the low MHz range). Unfortunately this solution is not effective for CDM stresses, which can resonate at RF frequency and cause voltage peaks damaging the circuit (green curve in figure C.3).

The solution is that of inserting explicitly an ESD protection device in the tank [Hyvonen 03], obtaining what is known as the "cancellation circuit" (figure C.2(b)-(d)). The inductor again resonates with the parasitic capacitance at RF, but during an ESD event the protection devices enter in conduction lowering the shunt resistance and thus dumping the high-frequency oscillation during a CDM stress (blue curve in figure (C.3)).

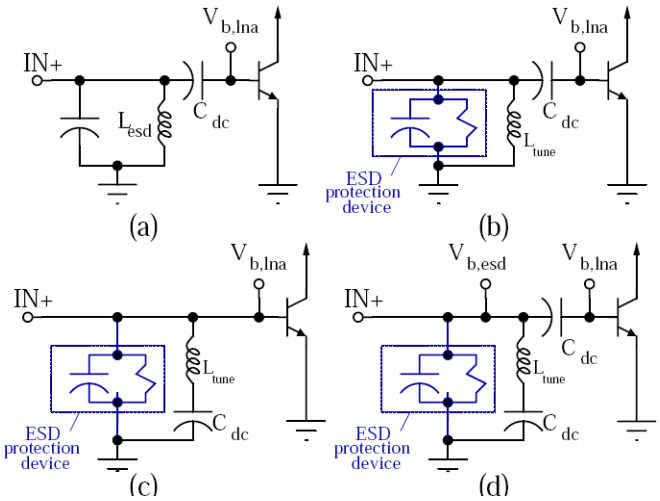


Figure C.2: Cancellation techniques

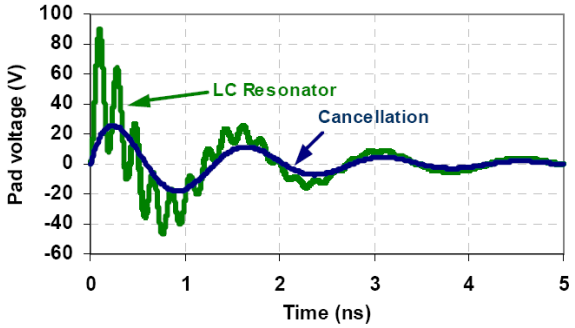


Figure C.3: Simulation Results

Figure C.2 shows various practical implementations of the biasing of the circuit when the cancellation technique is adopted: in figure (b) a dc-blocking capacitor is required in the signal path, which may introduce losses; in figure (c) the capacitor is placed in series with the inductor, and the same biasing voltage is used for both the circuit and the protection stage; finally, in figure (d), the two approaches are combined allowing an optimal polarization of the ESD element giving an extra degree to the designer.

To evaluate the performances of this kind of protection and its impact on the RF circuit, the following Figure of Merit can be defined,

$$FoM = Z_{shunt} \cdot V_{HBM} = \frac{V_{HBM}}{\omega C_{ESD}} \tag{C.4}$$

where V_{HBM} is the level of HMB robustness and $Z_{shunt} = 1/sC_{ESD}$ is the parasitic shunt impedance introduced.

At resonance, the equivalent shunt resistance can be expressed as

$$R_{shunt} = \frac{Q_{canc}}{\omega_0 C_{esd}}, \tag{C.5}$$

where

$$Q_{canc} = \frac{1}{\frac{1}{Q_{ind}} + \frac{1}{Q_{esd}}} \tag{C.6}$$

is the quality factor of the cancellation circuit, Q_{ind} is that of the shunting inductor, Q_{esd} that of the ESD device and C_{esd} is the maximum parasitic capacitance that can be sustained. The FoM becomes:

$$FoM = Q_{canc}\frac{V_{HBM}}{\omega C_{esd}} \tag{C.7}$$

In order to minimize the degradation of the performances of the RF circuit it is therefore necessary to maximize Q_{canc}. [Hyvonen 03] and [Hyvonen 05] analyze in detail the performances obtainable with various kind of ESD protection devices usually available in a CMOS technology; measurements show that:

1. Grounded-Gate NMOS: GGNMOS built into an isolated deep trench have an excellent quality factor ($Q = 17.5$@5 GHz in a 0.35 μm tech), while triggered GGNMOS should be avoided since the trigger NMOS have a finite resistance which lowers the attainable quality factor ($Q = 4.4$);

2. dual-diodes: for the top diode, a P^+ diffusion in an N-well is a good choice since good a quality factor can be obtained ($Q = 18.9$@5 GHz in a 0.18 μm tech); for the bottom diode both a pn diode built directly on the substrate and a diode built in an isolated P-well have high Q ($Q = 17.3$ and 20.3 respectively), while a P^+ diffusion in an N-well should be avoided ($Q = 10.2$) since the low-Q pn junction formed between the N-well and the P-substrate appears in parallel with the P^+-N-well junction, increasing the overall parasitic capacitance.

Measurement carried out on a test 5.25 GHz LNA show that a TLP failure current of 2.4 A (equivalent to 3.6 kV HBM stress) can be sustained with modest RF performance degradation (0.2 dB worsening of noise figure relative to the same unprotected LNA which, for comparison, fails already at a 0.7 A TLP current) once a proper high-Q protection is used.

In the case the technology library doesn't provides devices with sufficiently high quality factor, or the designer decides not to use such devices[2], the isolation technique could be considered.

C.4 ESD isolation technique

The isolation technique has been developed to isolate the (typically low-Q) ESD protection element from the RF circuit. It consists on a shunt equivalent LC resonating at the operating frequency of the RF circuit put in series with a conventional ESD protection diode [Ker 03] (see figure C.4).

Since only the resonant frequency is fixed, the designer has a degree of freedom in choosing the optimized value of the inductor and the capacitor. With respect to the cancellation technique, the LC tank is now in series with the ESD protection rather than in parallel, so the HBM protection level is reduced [Hyvonen 03]. Moreover the designer must beware that an high-Q LC tank will give rise to large voltage peaks during a ESD

[2]high Q devices have an increased sensibility to process variations.

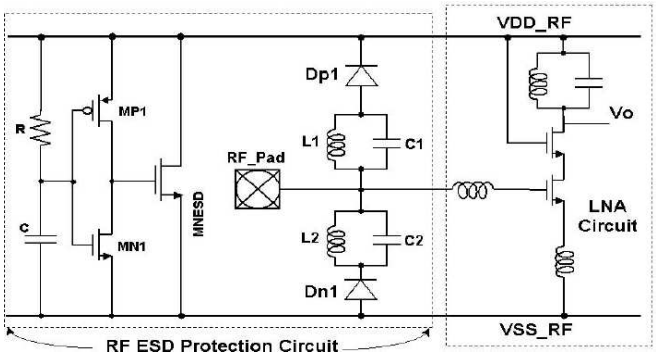


Figure C.4: Isolation techniques

stress; as in the case of the cancellation technique, substituting the capacitor with a pair of diodes in antiparallel damps the oscillation and gives the structure a better robustness even for fast CDM current pulses.

Two kind of isolation strategies can be adopted: in the LCD structure, the equivalent LC is connected to the RF path while the ESD circuit is connected to a supply; conversely, in the DLC structure it is the ESD protection to be connected to the RF pad; the latter strategy usually leads to worse performances due to the increased parasitic capacitance it introduces at the input node.

Experimental results carried out on a 0.25 μm CMOS test LNA working at 2.7 GHz show that choosing larger inductors ($8 \div 12$ nH) has a minor impact on the power gain S_{21}. With the LCD structure the degradation in the power gain is substantially independent on the sizing of the ESD devices, so larger diodes can be inserted assuring a better ESD protection; on the contrary, in the DLC structure the gain worsens increasing the size of the protection diodes; the loss is however below 1 dB even when a 1.2 pF diode is selected.

As for the noise figure, the use of the isolation technique improves the performances attainable with respect to the unprotected case; again, larger inductors give better performances and larger diodes can be inserted when the LCD structure is adopted, assuring a better ESD protection.

The measured ESD robustness shows a tight dependence with the number of coils of the integrated inductor: the same LCD structure with a $C_{diode} = 600$ fF passes a 5.7 kV HBM test when an inductor with 2.5 turns is adopted, but drops to 2.8 kV when in the case of 6.5 turns. On the contrary, once the sizing of the LC tank is chosen, higher level of protection are obtained increasing the diode sizing; target 2 kV HBM and 200 V MM ESD protection level are reached when $C_{diode} = 300$ fF and $L = 5.88$ nH (4.5 turns), with a power gain loss below 0.7 dB at 2.7 GHz and a Noise Figure increase of approximately 0.6 dB. The main drawback of this approach is the larger area occupation required by the integrated inductors, which makes this kind of protection less attractive with technology scaling.

C.5 Co-design of the protection

Co-design of protection is an improved technique with respect to the cancellation circuits, that consists on merging the protection devices into the input matching network of the RF circuit. This method requires a deep knowledge of both ESD and RF design problems

and their (usually complementary) requirements. The effect of all nonidealities in both the matching network and protection circuit must be taken into account, leading to a quite expensive effort in the design [Vassilev 03]. The main advantage is that very little performance degradation can be assured; moreover, for circuits operating above 5 GHz, this seems to be the only feasible way to ensure suitable protection [Soldner 05].
From RF signal prospective, the ESD devices appear as pure passive RLC components present at the input/output nodes. As such, they attenuate the RF signal, effectively degrading the circuit signal to noise ratio. Co-design approach does not consider ESD protection devices as parasitic components, affecting the RF core functionality; on the other hand, the ESD RLC network is integrated into the RF circuit. There are potentially two main difficulties: a) the nonidealities of the real ESD structures, which complicate equivalent RLC network to resonate and, b) the general sensitivity to process variations of the device parameters. These are, however, common problems in the RF field that should be addressed in any design.

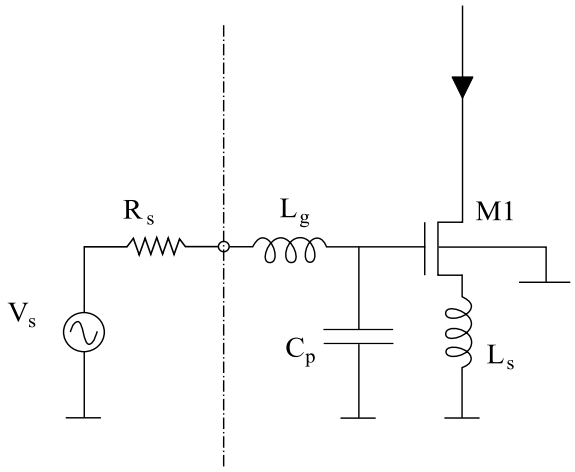


Figure C.5: Input matching principle of common source LNA.

Figure C.5 sketches the typical input stage of a LNA:

- R_s denotes the source impedance (50 Ω);
- C_p collects the parasitic capacitance at the gate node (gate-drain, gate-bulk and possibly ESD capacitances);
- L_s set the real part of the input impedance equal to R_s at the desired frequency;
- L_g is used to adjust the series resonance, diminishing the circuit imaginary input impedance;

It is important to note that the presence of C_p imposes an upper limit on R_s, above which the source degeneration direct power match would not be possible, as approximated by:

$$R_s = \frac{1}{2\omega C_p(1 + \frac{C_p}{C_{gs}})}, \tag{C.8}$$

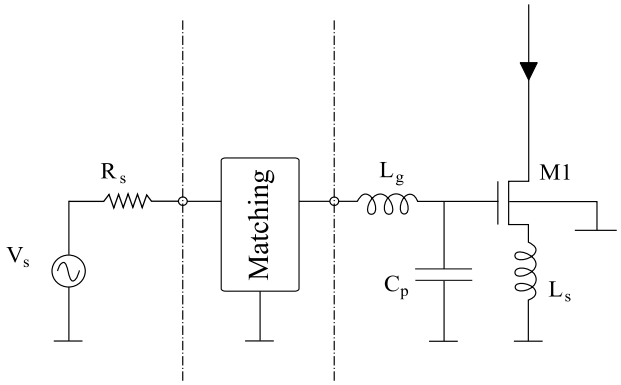


Figure C.6: Additional input matching circuit.

The consequence is that when the frequency or the input capacitance increase, the mismatch causes gain and noise figure degradation. To avoid this effect, the interposition of an external matching circuit is necessary, as shown in fig. C.6.
The aim of the matching network is to transform R_s to a lower intermediate impedance, comparable with the right term of the previous equation.
For the impedance transformation from R_s, a classical L-match circuit can be used (fig. C.7). In this case, the capacitance C_1 can be considered as another ESD protection element, including the bond pad capacitance: the following approximation holds:

$$R_{eq} \approx \frac{1}{R_s(\omega C_1)^2}, \tag{C.9}$$

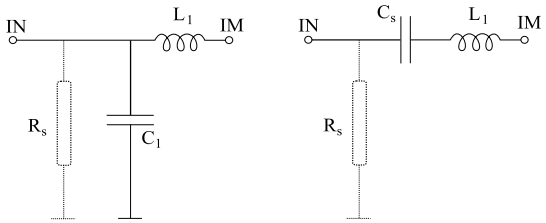


Figure C.7: L-match impedance transformer: the equivalent impedance at node IM is lower than the source initial impedance at node IN, due to the LC resonance at the given frequency.

The combination of the topologies sketched in fig. C.6 and fig. C.7 lead to another impedance matching circuit, as shown in figure C.8: here, C_1 and C_p are represented by the ESD snapback devices ME1 and ME2, while the two inductors are merged in a single one with a total impedance Z. The resistive and high frequency impedance of the inductor(s) allow de-biasing the input and core nodes in ESD conditions, providing at the same time very good current discharge conditions through ME1 and ME2: this is a good solution, especially to protect MOSFET gate.
Typically, in a bulk 0.25 μm process substrate, for an ESD optimized grounded gate

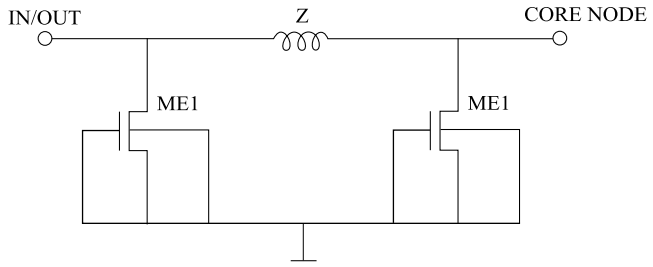


Figure C.8: Two stage ESD protection circuit.

NMOS to withstand about 2 kV HBM stress, its equivalent capacitance is $600 - 800\ fF$, providing total impedance to ground 300 Ω at 2.5 GHz.
Measurements on a 1.9 GHz LNA built with a 0.25 μm CMOS tech show that protection levels higher than 3 kV HBM can be achieved [Vassilev 03]; this work shows however a quite large degradation in the power gain S_{21} with respect to the unprotected reference LNA (19.6 dB versus 25.73 dB) which causes in turn a worsening of the noise figure of 1.3 dB.

C.6 Inductor based protection

In this kind of approach an inductor is used as a protection element; since the HBM ESD pulse has typically lower frequency when compared to radio-frequency signals, it is possible to insert in the design a shunt inductor at the input node which diverts the ESD current to the power lines, behaving as an open at the operating frequency [Thijs 05]. The advantage of this technique is that of finding a way of inserting an effective protection with minimal design effort (the so called "plug-and-play" class of protection); typically, only a minimal intervention on the polarization circuit is required.

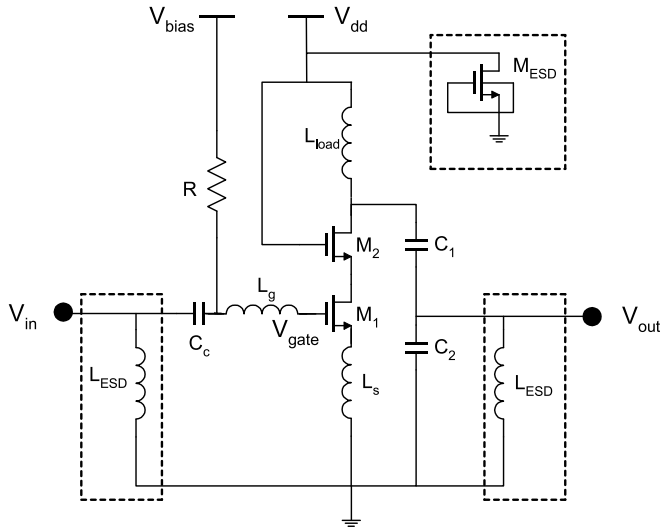


Figure C.9: Schematic of ESD-protected LNA.

Fig. C.9 well exemplifies a typical topology of an inductor ESD protected LNA. As

visible, ESD protection devices are added as "plug-and-play" components: inductors are placed at both input and output, in order to divert the ESD current away from the LNA core to the power lines. This is obviously true within the assumption that the ESD pulse has low frequency compared to the RF operating frequency.
It is should be noted that the grounded gate NMOS (used as power clamp at the power supply node) can be sized as big as desired because no RF signal is present at power node. Since all used ESD protection devices work bi-directionally, all possible pin-to-pin combinations are protected against ESD stress.
Circuits as in fig. C.9 can be easily simulated, and results are important hints to choose the right inductor. At low frequencies, a low resistance must be seen instead of an open circuit; on the other hand, impedance matching must be guaranteed at the working frequency. This is a quite simple constrain that must be respected. The second step concerns the evaluation of reflection parameters that must be maintained under imposed limits: it is worth noting that the presence of a shunt inductor can enhance matching parameters.
Since the noise of the LNA is mostly determined by the elements at its inputs, an increase in noise figure (NF) is to be expected by adding the additional inductor; fig. C.10 shows the worsening of the noise figure of a LNA for increasing values of the protection inductors.

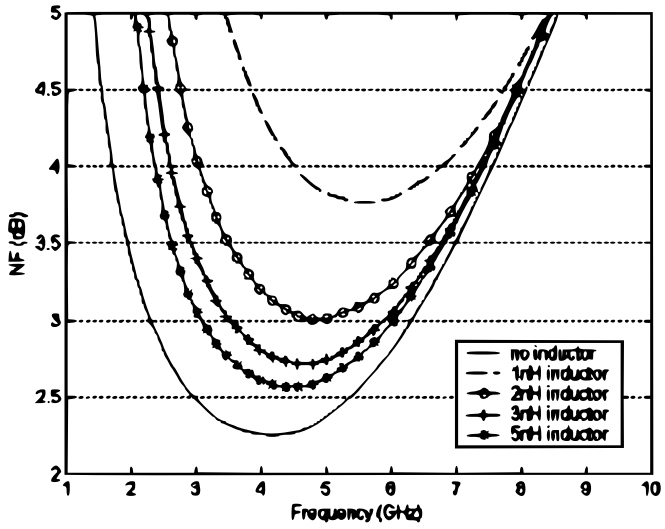


Figure C.10: Simulated noise figure for different values of ESD inductors. For a NF of maximum 3 dB, all inductors except 1 nH can be used.

Transient simulations need to be performed, to determine which inductor provides the best ESD protection. When an ESD event occurs, its fast rising edge will cause a voltage overshoot across the inductor (node Vin), as the instantaneous current through it cannot be changed. Capacitor C_C couples the transient voltage onto the node V_{gate}, as a capacitive divider. After the overshoot, the voltage across the inductor is determined by its on-resistance. Therefore, an inductor with low on-resistance is preferable; this is a mandatory condition in order to reduce the voltage drop as much as possible since a DC voltage can damage the gate oxide of input transistor; larger inductors have a greater series resistance and give rise to a higher voltage at the gate of the input transistor.
The latter sentence suggests that additional precautions have to be taken, such that the voltage at the gate oxide always is clamped at a safe value, in order to prevent any degra-

dation: the most effective solution is a simple fast clamp placed close to the gate (fig. C.11).

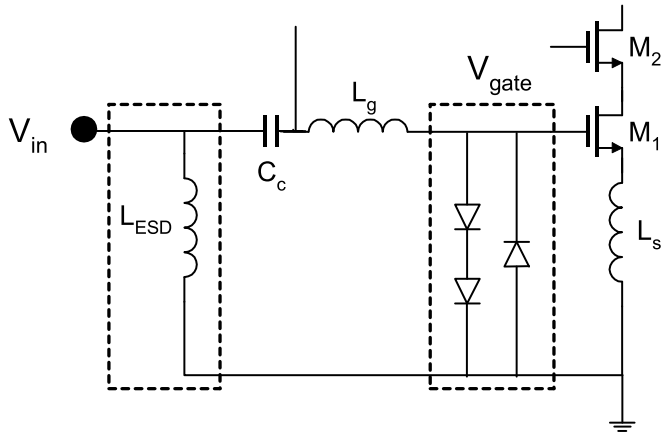


Figure C.11: Schematic with additional diodes to clamp the gate voltage of M_1.

Diodes do not conduct any significant current an can therefore be sized very small from a ESD point of view, introducing a minor impact the RF frequency due to the negligible additional parasitic capacitance introduced at the gate node. Fig. C.12 compares a 2 kV HBM simulation with and without the additional diodes; with the diodes, the voltage at the gate is clamped to a safe value of maximum 1.4 V. This prevents failure of the gate oxide, and will result in a drastic improvement of ESD robustness, since the limiting factor is shifted to the current capability of the ESD inductor or most likely to the voltage across the decoupling capacitor. Further, these diodes are also very beneficial for CDM stress protection.

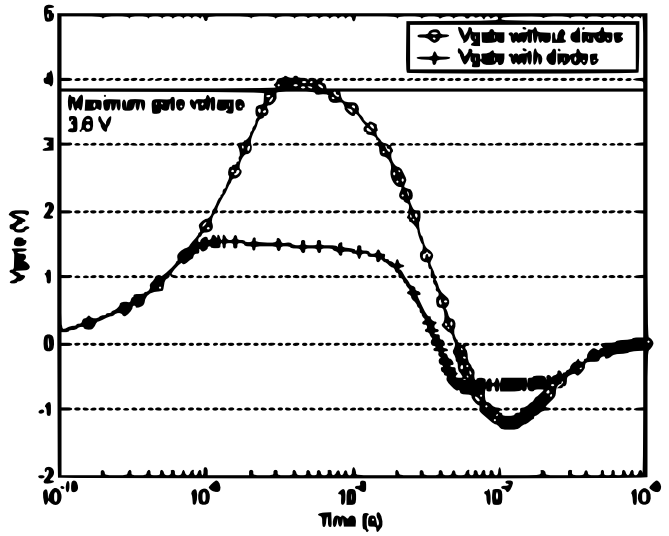


Figure C.12: 2 kV HBM transient simulation, stressed input to ground, for LNA with and without additional diodes at the gate of M_1. With the diodes, the voltage at the gate of M_1 is clamped to a safe value.

The inductor-based protection method has been extended with the use of above-IC inductors [Thijs 05], i.e. high quality inductors build with thin-film wafer-level packaging; the cited work shows that a great improvement with respect to the use of standard integrated inductors can be obtained, primary thanks to the much higher quality factor of the above-IC inductors (40 for a 3 nH inductor). The main drawbacks are the use of a non standard fabrication process, which increases the final cost of the chip, and area requirements (the technique was in fact applied only for the RF input pin).

C.7 Broadband protections strategies

Among the above analyzed protection scheme, the cancellation and the isolation techniques can be used only for narrowband circuits. The "low-C" approach is wideband but has a low-pass effect and can't be adopted for high frequency applications (as a rough guide, not suitable when the circuit is operating approximately above 5 GHz [Soldner 05]). A broadband protection with little performance degradation can be obtained when a structure similar to a transmission line is inserted before the RF stage; two approaches are analyzed in the following sections: the one called "distributed" and the novel "T-diodes".

C.7.1 Distributed

The basic idea of the distributed approach is that of splitting a single "big" ESD device into many smaller devices and inserting them into a transmission line; π-model [Ker 04] or complex multi-stage [Ito 01] distributed ESD protection schemes have been proposed in the literature (see figure C.13).

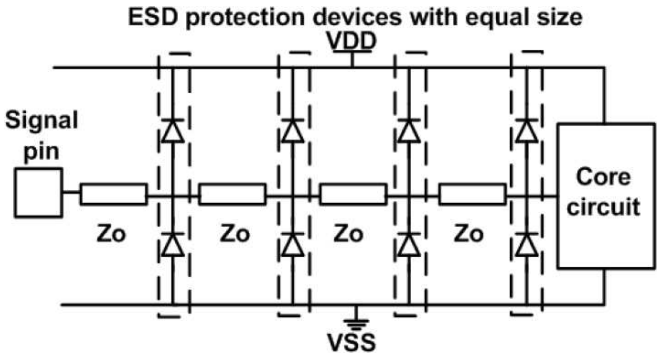


Figure C.13: Distributed protection scheme

In [Ker 04] a coplanar wave guide (CPWG) is built in a 0.25 μm CMOS technology with 5 level of metal; the signal line is made in the top metal layer, while the bottom metal is used as grounded shield; the CMOS process fixes the thickness and the conductivity of the metal layers, their spacing and the dielectric constant of the intra-metal dielectric; the characteristic impedance of the transmission line is obtained selecting the right width of the CPWG. Two dual-diodes structures are placed at the sides of the wave guide, in order to offer protection for both positive and negative ESD stresses.

Very high protection levels can be obtained (> 8 kV HBM) over a wide bandwidth since the ESD protection is distributed between several stages; an active VDD-to-VSS

clamp circuit was proven to be necessary to reach this high robustness. The wide area required by the CPWG (approx. 1800 μm of length) make this kind of protection not attractive in high integration chips.

C.7.2 T-diodes

The "T-diode" protection published in [Linten 07] consists in an integrated transformer and a pair of diodes arranged in a structure that approximates a lossless transmission line (figure C.14). Once the characteristic impedance Z_c and the level of the protection (pro-

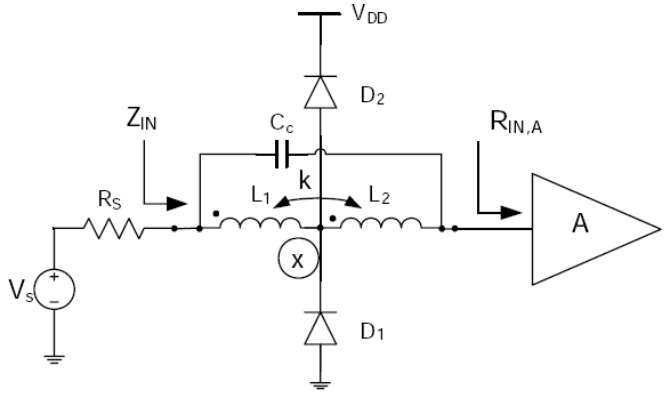


Figure C.14: T-diodes protection scheme

portional to the size of the diodes C_D) are chosen, the electrical delay τ of this equivalent transmission line is determined and the sizing of the protection scheme is easily derived with the following equations:

$$C_D = \tau / Z_c \tag{C.10a}$$

$$L = Z_c \tau (1/4 + 1/\pi^2) \tag{C.10b}$$

$$M = Z_c \tau (1/4 - 1/\pi^2) \tag{C.10c}$$

$$C_c = \tau / (Z_c \pi^2) \tag{C.10d}$$

$$k = \sqrt{M/L^2} \tag{C.10e}$$

where L is the inductance of both the primary and the secondary of the transformer, M is the mutual inductance, k is the coupling factor and C_c is the parasitic capacitance between the two set of coils; the structure can be placed "as-is" directly in front of the RF circuit with very little modifications of this block.

The impact of this protection on the input matching is given by:

$$S_{11,tot} = S_{11,LNA} \cdot e^{-j2\omega\tau},$$

so the magnitude is unaffected and the bandwidth is preserved.

Experimental results of this protection scheme applied to a 0.18 μm wideband $1 \div 5\ GHz$ cascode low noise amplifier when a $C_D = 460\ fF$ is chosen show that the bandwidth and the input matching of the LNA are practically not affected while the noise figure degradation is below 1 dB. The structure achieved a robustness of 4.6 kV HBM. The area requirement of this structure is substantially given by that of the transformer (4 turns, external radius $r = 75\ \mu m$ in the design), i.e. appreciably lower than the previous "distributed" approach.

C.8 Conclusion and current trends

The ESD protection of radio-frequency circuits is becoming more critical at every technological step since thinner gate-oxide has a low breakdown voltage. The analysis performed in this report shows that a classic approach aimed to minimize the parasitic capacitance of a standard ESD protection is not sufficient to preserve the RF performances, especially at high frequency.

Several improved techniques have been analyzed, both for narrowband and wideband circuits. The general picture is that a "universal" ESD protection for RF circuits does not exist, and the designer has to choose the most suitable kind of protection depending on the particular design.

Generally speaking, it is clear that RF and ESD design cannot proceed in a separate way but a co-design approach has to be adopted in order to obtain an effective ESD protection at high frequency.

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