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Characterization and modeling of GaN-based transistors for power applications

Thesis written with the financial contribution of Fondazione Cariparo

Coordinator: Andrea Neviani

Supervisor: Enrico Zanoni

Ph.D. Student: Matteo Borga

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Abstract

GaN-based devices have emerged as a promising solution for power management applications. The intrinsic physical properties of the Gallium Nitride are exploited in order to considerably improve the efficiency and to reduce the volume of the next generation power switching converters. The wide energy gap allows to fabricate high voltage-rate devices with a reduced area consumption, whereas the high mobility guarantees a considerably low on-Resistance of the transistor. Moreover, thanks to the reduced parasitic capacitances, the operating frequency of the devices can be higher than conventional Silicon based transistors.

In order to ensure a wide spreading of Gallium Nitride technology in the power transistors market, the price of the devices needs to be kept as low as possible. The costs of native substrates for the fabrication of GaN transistors are nowadays prohibitive, so that the epitaxial growth of Gallium Nitride on Silicon substrates has been developed. GaN-on-Silicon is the most suitable technology to fabricate GaN-based devices on a cheap and large area wafers (up to 200 mm), resulting in a significant reduction of the production costs.

On the other hand, growing GaN on a foreign substrate results in high dislocation and defect densities which could affect the performance of the devices in terms of both losses and reliability issues. A so-called "buffer decomposition experiment" allowed to evaluate the role of the different layers which compose the vertical stack of a GaN-on-Silicon wafer by characterizing samples obtained by stopping the epitaxial growth at different stages of the process. It is demonstrated that both the thickness and the composition of the epitaxial stack, beside enhancing the breakdown voltage, improve the material quality by limiting the propagation of defects and dislocations. Moreover, a study on the reliability of the Aluminum Nitride layer grown on silicon is presented,

showing that the AlN fails due to a wear-out process following a Weibull distribution. Furthermore, an extensive analysis on the reliability of the GaN-on-Silicon vertical stack is presented, as well as a systematic study on the failure statistic. It is shown that the time to failure of the GaN-on-Silicon stack is Weibull distributed, and, although it is weakly temperature-activated, it exponentially depends on the applied voltage. Moreover, the expected lifetime of the tested devices at the operating voltage is extracted.

Aiming to further improve the performance of lateral High Electrons Mobility Transistors (HEMTs) in terms of vertical robustness and losses reduction, the impact of the resistivity of the silicon substrates has been evaluated. It is shown that highly resistive p-doped substrate results in a plateau region in the IV characteristic which considerably increases the vertical breakdown voltage of the devices. Nevertheless, the existence of a trade-off between the vertical robustness and the stability of the threshold voltage is demonstrated. A set of electrical characterization ascribes the threshold voltage shift to the positive backgating effect possibly related to the capacitive coupling of the partially depleted substrate which only occurs if lowly p-doped silicon is used. The origin of the plateau region is further investigated by means of a set of TCAD simulations, allowing to develop a two-diodes model which confirms the hypothesis on the substrate depletion.

Even if stable and reliable lateral HEMTs are commercially available, their operating voltage is limited to ~ 900 V. In order to expand the applications field of the GaN-based devices to higher operating voltage, different device concepts have been developed so far. A promising solution is represented by (semi-)vertical trench gate devices, which are characterized by a thick drift layer where the OFF-state electric field spreads vertically in a bulky region, thus avoiding surface effects. Thanks to the vertical architecture, the OFF-state breakdown only depends on the thickness of the epitaxial stack, thus allowing to reach high breakdown voltages with a limited area consumption.

Since the carriers must flow vertically, the gate of the devices lies in an etched trench, and it consists of a Metal Oxide Semiconductor (MOS) system. Within this thesis the gate leakage is deeply studied on devices with different gate dielectric, by means of electrical characterizations performed with different connection configurations and

different bias polarities. Moreover, the gate capacitance is analytically calculated, and the experimental behavior observed for the Gate-Source and Gate-Drain capacitances over the applied voltage is discussed and modeled considering the GaN bias condition close to the dielectric interface. Lastly, a preliminary dielectric trap characterization is performed by evaluating the capacitance hysteresis induced by the electric field within different gate oxide materials.

The last section of this work presents a custom setup developed for the characterization of the threshold voltage variations over the time. The stability of the threshold voltage is fundamental for allowing a device to operate properly in a switching converter. Standard pulsed systems used for the characterization of the threshold voltage allow to evaluate the impact of the bias level on the threshold variation, but no details on the time evolution can be obtained. The presented threshold transient setup monitors the threshold voltage variation over a wide time-interval, ranging from 10 μs to 100 s, allowing the analysis of the trapping and detrapping kinetics. Moreover, by monitoring the transient variation as a function of the temperature it is possible to full characterize (energy level and cross section) the traps involved in the observed instabilities.

Sommario

I dispositivi in GaN sono una soluzione promettente per applicazioni di potenza. Le proprietà fisiche intrinseche del nitruro di gallio consentono di migliorare notevolmente l'efficienza e di ridurre il volume della prossima generazione di circuiti switching per la conversione dell'energia.

Crescere il GaN su substrati non nativi comporta la presenza di alte densità di dislocazioni e difetti, che compromettono le performance dei dispositivi in termini di perdite ed affidabilità. Un esperimento detto "buffer decomposition experiment" ha permesso di valutare l'impatto dei diversi strati che compongono lo stack verticale di un wafer GaN-on-Silicon tramite la caratterizzazione di campioni ottenuti fermando il processo di crescita epitassiale in diversi momenti del processo. È dimostrato che sia lo spessore che la composizione dello stack verticale, oltre a migliorare la tensione di breakdown, migliora la qualità dei materiali, limitando la propagazione di dislocazioni e difetti. Inoltre, viene presentato uno studio sull'affidabilità dello strato in nitruro di alluminio (AlN) depositato su silicio; si dimostra che l'AlN si rompe per un processo percolativo, e i tempi di fallimento seguono una distribuzione di Weibull. Inoltre, viene discussa un'estesa analisi sulla affidabilità di uno stack GaN-on-Silicon, comprensiva di uno studio sistematico sulla statistica dei fallimenti. È dimostrato che il tempo di fallimento segue una distribuzione di Weibull, e, nonostante sia poco dipendente dalla temperatura, è esponenzialmente accelerato dalla tensione applicata. Infine, viene estratto il tempo di vita atteso in condizioni operative nominali.

Con l'obiettivo di migliorare ulteriormente le performance degli HEMT laterali in termini di robustezza e di riduzione delle perdite, è stato valutato il ruolo della resistività del substrato in silicio. È dimostrato che substrati di tipo p altamente resistivi causano una regione di "plateau" nella caratteristica IV del dispositivo, la quale aumenta

considerevolmente la tensione di breakdown del dispositivo. Nonostante questo, è stato evidenziato un trade-off tra la robustezza dello stack verticale e la stabilità della tensione di soglia. L'origine fisica della regione di plateau è stata inoltre investigata tramite simulazioni TCAD, che hanno permesso di sviluppare un modello a due diodi.

Nonostante siano disponibili nel mercato dispostivi laterali stabili e affidabili, la loro tensione nominale non supera i 900V. Nei dispositivi con architettura verticale, il breakdown in off-state dipende solo dallo spessore dello stack epitassiale, consentendo di raggiungere alte tensioni di fallimento con un consumo di area limitato. In questa tesi la corrente di leakage di gate viene dettagliatamente studiata in dispositivi verticali con diversi dielettrici di gate, tramite caratterizzazioni effettuate con diverse configurazioni di connessioni e diverse polarità. Inoltre, la capacità di gate è calcolata analiticamente, e l'andamento sperimentale osservato per le capacità Gate-Source e Gate-Drain al variare della tensione di gate sono analizzate e modellizzate considerando il potenziale del GaN vicino all'interfaccia con il dielettrico.

Nell'ultima parte della tesi viene presentato un setup custom sviluppato per caratterizzare le variazioni della tensione di soglia nel tempo. La stabilità della soglia è fondamentale per assicurare che il dispositivo funzioni correttamente in un convertitore switching. I sistemi impulsati convenzionali utilizzati per la caratterizzazione della soglia permettono di valutare l'effetto del bias sulle variazioni della soglia, ma non danno nessuna informazione sull'evoluzione temporale. Il setup presentato monitora le variazioni della tensione di soglia in un intervallo temporale ampio, che spazia dai 10 µs ai 100 s, consentendo di analizzare le cinetiche di intrappolamento e detrappolamento. Inoltre, monitorando i transienti di soglia in funzione della temperatura si possono caratterizzare (energia e sezione di cattura) le trappole che causano le instabilità osservate.

Introduction

The electrical energy is nowadays extensively used around the word, and it is expected to be the most widespread form of energy by 2040. Eco-friendly and high-efficiency systems are helping us to reduce energy wasting; nevertheless, the digital society that is developing will required within few years new power-consuming services (communications, digital services, data storage, logistics, transport…). This progression is pushing the market to develop advanced systems for the production, the distribution, the storage and the conversion of the electrical energy.

The electrical energy is always stored or delivered in a different form with respect what needed by the final device. For example, the electrical grid provide an AC voltage, while most of electronic appliance (TV, PC, smartphone, LED laps…) require a relatively low DC voltage; another example is the electric cars, in which the energy is stored in high voltage DC batteries, and it needs to be converted into AC power to be supplied to the AC motors; a third case is the DC output of the photovoltaic systems, which must be converted into AC voltage to be released into the high voltage electrical grid. All these electrical conversions are assigned to complex switching electronic circuits (DC-DC converters, inverters…) which needs to be as more efficient as possible, to minimize the power losses and the wasting of energy.

The active component of these switching converters is a transistor that, driven by a controller, operates like a switch. This latter during the operation go from on OFF-state condition, in which it must block a high voltage with very low current losses, to an ON-state condition, where the current that flows into the devices should give a negligible voltage drop, minimizing the resistive losses. Silicon-based devices are approaching the theoretical limits of the semiconductor material, and no significant improvements can be obtained. In order to improve the efficiency of the new-generation conversion systems

and to fit the market demand, new devices based on novel materials have been developed over the last years.

One of the most promising technology is based on the (Al)GaN material system. Gallium nitride is a wide bandgap semiconductor material that, thanks to its intrinsic properties, is intended to significantly increase the performance not only of switching converters, but also of high-frequency power amplifiers. Thanks to the high saturation velocity GaN-based transistors can operate to higher frequency and lower resistive losses with respect to the silicon-based ones. In addition, the wide bandgap brings to a high breakdown electric field, which allows the development of small-size devices suitable for high voltage application. Moreover, thanks to its direct energy gap, also high-efficiency optoelectronics devices and light sources (i.e. LEDs) have been developed based on (Al)GaN material system.

An example of performing devices based on Gallium Nitride is provided by the High Electron Mobility Transistor (HEMT). This device is a field effect transistor based on an AlGaN/GaN heterostructure. The intrinsic properties of the materials cause a strong piezoelectric and spontaneous polarization charges to appear at the junction between these materials, thus creating a triangular potential well in which electrons are gathered. This high-density sheet of charge, also known as bi-Dimensional Electron Gas (2DEG), forms the channel of the transistor. The transport in the 2DEG is a low-scattering phenomenon, since it occurs in a undoped semiconductor material; this guarantees the high mobility of the electrons within channel. The high carrier density and the high mobility allow to achieve an overall reduction of the resistive losses of the transistor.

Although this promising technology is already available on the market, there is still some limitation on these lateral devices concerning the reliability, the costs, and the low voltage-rate (< 900 V). In order to increase the spread of GaN-based transistors, higher operating voltage devices must be developed. A promising approach is the developing of a vertical GaN-based transistor. This device is not based on a heterojunction, but on a Metal-Oxide-Semiconductor (MOS) gate. The drain is not placed on the gate-source top plane, but on the back-side of the device, separated by a thick low-doped drift region from the channel region. This architecture allows the development of high operating-voltage devices, with all the advantage given by Gallium

Nitride. Nevertheless, several aspects need to be investigated and improved on these novel devices in order to obtain stable and reliable devices in a voltage range higher than 1 kV.

This thesis summarizes the main achievement and outcomes obtained during my three years Ph.D. research working on GaN-based devices for power applications. The manuscript is composed by five chapters.

Chapter one consists of a general introduction on Gallium Nitride and on the architecture of the devices. Moreover, an overview on the state of the art of the different topics discussed in the following chapters will be presented.

Chapter two presents an analysis on the reliability of the vertical stack of GaN on Silicon power HEMTs. The so-called "Buffer Decomposition Experiment" allows to evaluate the role of the different layers of a standard GaN-on-Si platform. Moreover, the failure statistic of the AlN nucleation layer grown on Silicon is analyzed. The second part of the chapter is focused on the reliability study and on the time to failure (TTF) evaluation of a full GaN-on-Si stack.

In **chapter three** the impact of the silicon substrate resistivity on the performance of lateral HEMTs is evaluated. The analysis is focused on both the vertical leakage, which is a critical OFF-state loss, and on the stability of the devices. It is demonstrated that using highly resistive silicon results in a plateau region on the I-V curve, and that a trade-off between the robustness and the stability is pointed out. Moreover, an investigation on the origin of the plateau is carried out by means of TCAD simulations, and a two-diodes model describing the experimentally observed behavior is proposed.

Chapter four focuses on the study of the gate module of novel vertical trench-gate GaN-based devices. The gate leakage is studied by characterizing the devices in different connection configuration and bias polarities. Moreover, a comparison among different gate dielectrics in terms of leakage currents and robustness is presented. Beyond the gate leakage, the gate capacitance is analytically calculated and modeled, discussing the dependence of the gate capacitance behavior on the gate bias and measurement configuration. Finally, a preliminary gate trap-density evaluation is performed by means of capacitance-voltage hysteresis measurements.

Lastly, in **chapter five** a novel setup allowing the monitoring of the threshold voltage variations over a wide time range (from 10 μs to 100 s) is presented. The details on the measurement technique and on the setup will be widely discussed. Moreover, two examples of application of the setup are shown, demonstrating the improvement on the device characterization obtained thanks to the presented technique.

Chapter 1:

Gallium Nitride and its applications

1.1 Gallium Nitride

Nitride-based semiconductors are suitable materials for the fabrication of high-performance transistors for both power and radiofrequency applications, allowing to overcome the limitations related to the silicon devices in term of efficiency and volume. High carrier mobility and high breakdown field are the key features to reduce the losses and to shrink the devices size. Moreover, thanks to their the direct energy gap, high efficiency white LEDs, UV LEDs and lasers have been developed based on these materials. In addition, by alloying different Nitride-based materials (i.e. AlN and GaN), the electro-physical properties of the resulting semiconductor (AlGaN) can be engineered by acting on the concentration of the alloy.

Despite the high knowledge reached in growing the Gallium Nitride, there are still some issues related to the material that limit the performance of the devices in term of both stability and reliability. Due to the prohibitive cost and limited availability of native substrates, Gallium Nitride is commonly growth hetero-epitaxially on Sapphire or Silicon; this latter has the advantage of being extremely cheap and to be available in wafer up to 200mm, guaranteeing good scalability and cost reduction. The main drawback of using non-native substrates is related to the remarkably differences in term of physical properties (lattice constant, thermal expansion coefficients, …) that results in a high defectivity of the lattice of the epitaxial layers which cause issue of stability of the final devices.

Another issue is the growth of high-quality dielectrics for the fabrications of vertical MOS devices based on Gallium Nitride. The gate dielectric plays a key role on several aspects of the devices, like the static losses, the reliability, the stability of the gate, thus indicating the necessity to improve the knowledge on the insulating materials and on their deposition techniques.

1.1.1 Crystal structure and band diagram

Gallium Nitride is a compound semiconductor composed by Gallium and Nitrogen, which are respectively in the 3rd and in the 5th group of the periodic table of the elements. For this reason, GaN is part of the so-called III-V materials. Gallium Nitride can have three different crystal structures, which are wurtzite, zincblende and rock-salt. This latter cannot be grown epitaxially, thus it is unsuitable for the fabrication of electronics devices.

In the zincblende structure, also known as sphalerite, the Gallium atoms, which are shared with adjacent cells, compose a face-centered cubic structure ($a = b = c$, $\alpha = \beta = \gamma = 90°$), while the Nitrogen atoms (4 per unit cell) are packed in the tetrahedral hole along the cube diagonal at the same distance from the Gallium atom at the corner and to the three ones place in the faces center. This crystal configuration is thermodynamically metastable, thus the zincblende slowly transform over the time to the wurtzite structure, which is a stable crystal configuration. In this latter, each type of atoms (i.e. Gallium and Nitrogen) form a hexagonal close-packed sub-lattice ($a \neq c$, $\alpha = 120°$, $\beta = 90°$). The two sub-lattices are interpenetrated with an offset along the z-axis of 5c/6. In this configuration there is a clear sequence of Gallium-atoms planes and N-atoms planes.

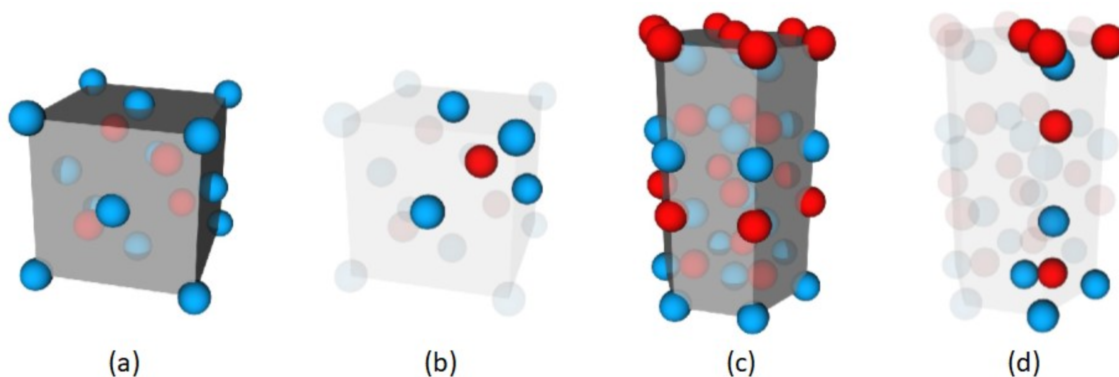


Figure 1.1 – Schematic representation of the two possible crystal structures of GaN: (a) zincblende and (c) wurtzite. (b) and (d) highlight the Nitrogen atoms occupying the tetrahedral hole formed by Gallium atoms (and vice versa in wurtzite crystal).

The atomic bonds between atoms of GaN are mixed ionic-covalent bonds. The strength of the atomic bonds is the key for the high breakdown electric field of this semiconductor. Moreover, the lattice properties of gallium nitride have a direct impact on its energy gap, which is the feature which make GaN a suitable material for the

fabrication of either power transistors and optoelectronic devices such as blue and UV LEDs.

The band structure of GaN in both zincblende and wurtzite configuration is shown in Figure 1.2; both zincblende and wurtzite GaN have a direct energy gap, meaning that the minimum of the conduction band and the maximum of the valence band are aligned at the same value of the vector k, which is proportional to the particle momentum. This peculiarity, which make GaN ideal for optoelectronic applications, results in a high probability that a radiative recombination between an electron and a hole occurs, with the resulting emission of a photon. A second important property of Gallium nitride is the high value of the energy gap, which has been demonstrated to be 3.39 eV at 300 K [1]. This remarkably high energy value, which is related to the relatively low lattice constant, results in a high critical electric field of GaN (3.3 MV/cm).

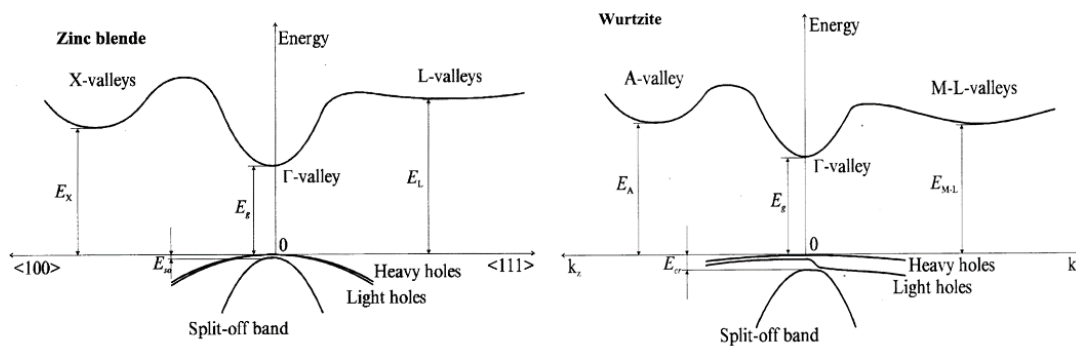


Figure 1.2 – band structure of zincblende GaN (left) and wurtzite GaN (right) [2].

Gallium Nitride is also suitable to create alloys with other Nitride-based semiconductors, for example Aluminum Nitride (AlN), which has a higher energy gap than GaN and a higher breakdown field. The compound semiconductor obtained by alloying GaN and AlN is the Aluminum-Gallium Nitride ($Al_xGa_{(1-x)}N$), which electrical properties can be tuned by changing the aluminum concentration in the alloy. This feature of the compound semiconductors is very important because allow the grown of "ad hoc" materials with adjustable lattice constant and energy gap.

1.1.2 Polarization effects on GaN

Polarization effect is an important characteristic that unites all the III-N materials. The intrinsic asymmetry of the lattice bonds, as well as the high ionicity of the III-N

bond, result in a respectively spontaneous and piezo charge distribution at the two sides of a III-N semiconductor layer.

Gallium nitride crystal lattice is characterized by an alternating sequence of planes respectively composed by Gallium atoms and by Nitrogen atoms. Especially in the wurtzite crystal configuration, since these planes are not uniformly spaced (asymmetry along the c direction), the Ga-N bond dipole moment (caused by the partial ionicity of the Ga-N bond) is not self-compensating, thus resulting in a net dipole moment originating along the growth direction.

Beyond the spontaneous polarization, which is ascribed to the crystal asymmetry, all III-N materials exhibit piezoelectric capability. Once the semiconductor is submitted to a tensile- or compressive-stress, its lattice gets deformed, and two opposite charge distributions appear on the two sides of the semiconductor layer. The orientation of the piezoelectric charge strongly depends whether the stress is tensile or compressive. Piezoelectric effect is typically observed when a relatively thin semiconductor layer is grown over a material with a different lattice constant, thus creating a heterojunction. The thin layer lattice deforms in order to accommodate the lattice constant of the bulky semiconductor layer.

This characteristic of the (Al)GaN material system allows to obtain a high charge-density layer well confined in a potential well. As it will be discussed in the following, this is the basis for the High Electron Mobility Transistors (HEMTs).

1.1.3 Growth techniques

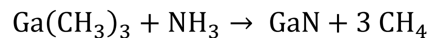
Gallium Nitride is a semiconductor which must be grown by means of an epitaxial deposition process, thus depositing thin films of atoms on a pre-existing substrate. Several techniques were developed to grow GaN films, aiming to deposit a high-quality semiconductor thus guaranteeing to exploit all the intrinsic properties of the material: in fact, poor crystal quality of the deposited layer results in a reduced performance of the final devices caused by defects, cracks and dislocations in the crystal lattice.

In the following a brief overview on the two most commonly used growing methods, which are MOCVD (Metal Organic Chemical Vapor Deposition) and MBE (Molecular Beam Epitaxy), will be given.

MOCVD

In the MOCVD deposition technique the precursors are injected into a growth chamber where a heated substrate is positioned. The main source gas is the ammonia NH_3, which represents the source of Nitrogen, while the Gallium or the Aluminum are obtained by their respective metalorganic compounds, which are Trimethyl-Gallium (TMGa) or Trimethyl-Aluminum (TMAl), carried into the chamber by a gas, usually Hydrogen, whose percentage depends on the growing pressure [3].

The gases injected into the reactor react over the heated substrate, so that a semiconductor layer is formed. The chemical reaction allowing the GaN growth is:



$$Ga(CH_3)_3 + NH_3 \rightarrow GaN + 3\ CH_4$$

The same reaction allows the growth of the Aluminum Nitride (AlN), by substituting the Gallium with the Aluminum [4]. Moreover, by combining both TMGa and TMAl, AlGaN can be obtained. N-type and p-type doping in GaN can be achieved by using respectively silane/di-silane (SiH_4/Si_2H_6) or cyclopenta-dienylmagnesium (Cp_2Mg) [5].

The substrate, which is positioned at the base of the reactor, is heated up while the precursors are evaporated within the growth chamber. The substrate temperature needs to be high enough so that the growth rate is not limited by the surface reaction rate but by the precursors injection rate, thus allowing to better control the layer thicknesses and composition [5]. Furthermore, substrate temperature (which ranges between 700 °C and 1100 °C [4]) plays a key role on the strain management, which is fundamental when GaN is deposited over a foreign substrate characterized by a different thermal expansion coefficient. High temperature also guarantees higher crystal quality.

MOCVD is the preferred technique to fabricate devices for commercial purpose. With the described method a high yield is achievable by growing several wafers simultaneously in the same chamber with a relatively high deposition rate as well as a good uniformity of the deposited layers.

MBE

A second growing technique which deserves to be presented is the Molecular Beam Epitaxy (MBE). Unlike MOCVD, MBE allows to grow high crystal quality GaN films on foreign substrate, with a considerably reduced impurity concentration and well controlled material composition. Moreover, very sharp interfaces between different semiconductor materials can be obtained [6].

For the MBE growth, an extremely clean ultra-high vacuum environment is needed. Beams of the constituent materials obtained by sublimation or evaporation performed by effusion cells, are collimated over the heated substrate where they chemically react forming the semiconductor crystal. Within the effusion cells, also called Knudsen cells, a highly purified solid source is used, and no engineered precursors is needed (as in MOCVD growth). This fact, combined with the lack of particles within the growth chamber (high-vacuum), guarantees a considerably low impurity density and a high crystal quality.

The effusion cells are paired with mechanical shutters, which can selectively run or block the beams. This mechanical action is considerably faster than the growth of a single atom layer, so that the layer thickness is precisely controlled. Moreover, by setting the temperature of the solid source material, the beam flux can be regulated so that the layer composition is well controlled [6].

Although the high performance in terms of crystal quality and low impurities density, MBE technique is mainly used in academic and material characterization fields, since for high yield, high throughput and cost-effective purpose (fabrication of commercial devices) MOCVD is the preferred solutions.

1.1.4 Substrates for GaN growth

As previously discussed, Gallium Nitride is commonly growth epitaxially over a pre-existing substrate by means of different deposition techniques. The choice of the substrate for the fabrication of GaN wafer is a trade-off between the final device performance and cost, and it must be done considering the actual application.

Two main parameters must be considered when choosing a substrate for the GaN growth, which are the lattice constant and the thermal expansion coefficient. The lattice

mismatch between the substrate and the epitaxial layer results in a defective substrate/epitaxy interface, and a consequent formation of dislocations which penetrate the epitaxial layers. On the other hand, also the growth temperature must be considered: as previously discussed, a high substrate temperature is needed in order to enhance the growth rate, to reduce the impurity incorporation and to improve the overall crystal quality. At the end of the epitaxial growth, which usually requires a temperature higher than 1000 °C, the substrate and the epitaxial layers need to be cooled down to room temperature. During the cool down phase, the lattice constant of each material tens to decrease. The mismatch between the thermal expansion coefficients results in bowing of the wafer which could lead to a crack of the wafer.

Several substrate materials have been proposed over the years for the GaN growth. The ideal solution in order to minimize the lattice constant and the thermal expansion coefficient mismatch is the use of Gallium Nitride substrates. Although the development of native Gallium Nitride substrates is improving, the fabrication costs and the limited wafer size achievable limit this solution to be exploited expect for research purpose.

The first material used for growing GaN was the Sapphire (Al_2O_3). The latter has a hexagonal lattice configuration, similar to the wurtzite configuration of the GaN lattice. On the other hand, it has a considerably different thermal expansion coefficient and lattice constant. Moreover, its reduced thermal conductivity makes sapphire substrates not the ideal substrate material for high power applications [7]. Nevertheless, Al_2O_3 are commonly used for growing optoelectronic devices, such as LEDs.

Silicon carbide (SiC) substrate is the best choice for the epitaxial growth of (Al)GaN, thanks to both its remarkably high heat conductivity and its low lattice mismatch with GaN. Unfortunately, SiC substrates size is limited to 6 inches diameter, and their costs is extremely high. The resulting high cost of the final devices cannot be suitable for power devices. Nevertheless, SiC substrates are commonly used for the fabrication of GaN based RF devices, where high power dissipation is involved and a high amount of heat needs to be sank.

Nowadays, the most common solution for growing GaN based power devices is Silicon (Si). Silicon substrates fabricated with the Czochralski process are commercially available with diameter higher than 200 mm (8 inches). Even if the complexity of

growing thick epitaxial layers increases with the increasing wafer diameter, mainly due to the severe lattice and thermal mismatch between the silicon and the III-V [8], the high yield, high scalability and the remarkably cost reduction make silicon substrates the preferred solution for the epitaxial growth of GaN-based devices for power applications.

Between the silicon substrate and the gallium nitride active region, several layers need to be interposed (Figure 1.3). The first layer grown over the silicon substrate is called nucleation layer and is usually an aluminum nitride (AlN) layer which thickness is in the order of the hundreds of nanometers. The role of this layer is to prevent the gallium-silicon eutectic reaction, also known as melt-back etching [9]. Although the high lattice constant mismatch between the two materials, the material quality of the AlN is sufficient for the epitaxial growth of the subsequent layers.

Over the aluminum nitride nucleation layer, an engineered transition layer is grown. The role of the transition layer is to create a compressive stress on the lattice which prevents the cracking of the wafer due to the thermal expansion coefficients mismatch during the cooling-down phase, which occurs once the epitaxial growth is completed. A widely adopted solution is to grown a series of AlGaN layer with a decreasing aluminum concentration, to accommodate the lattice mismatch [10]. Another proposed solution is the growth of a GaN/AlN superlattice over the nucleation layer: this solution allows to fabricate thicker epitaxial layers over silicon substrates thanks to a more evolved strain engineering [11].

Between the transition layer and the undoped GaN region, which constitutes the active region of the final device, a buffer layer must be interposed. The buffer layer for power devices is usually a thick (> 2 μm) GaN layer intentionally doped with carbon (C). The carbon, which is a deep acceptor in GaN, compensates for the intrinsic conductivity of the undoped GaN. As a result, a thick semi-insulting layer divides the active region of the device from the highly defective substrate/epi interface. There are two main reason why using a carbon doped buffer layer, which are the lowering of the vertical conductivity of the vertical stack [12] and the prevention of punch-through effects [13][14].

Over the carbon doped GaN layer, a thin layer of undoped GaN is grown. This layer is the active layer of the final device, where the channel is formed. As will be

discussed in the following paragraph, the electron channel in a High Electron Mobility Transistor (HEMT) is formed thanks to the piezoelectric charge of an AlGaN barrier layer grown over the undoped GaN layer.

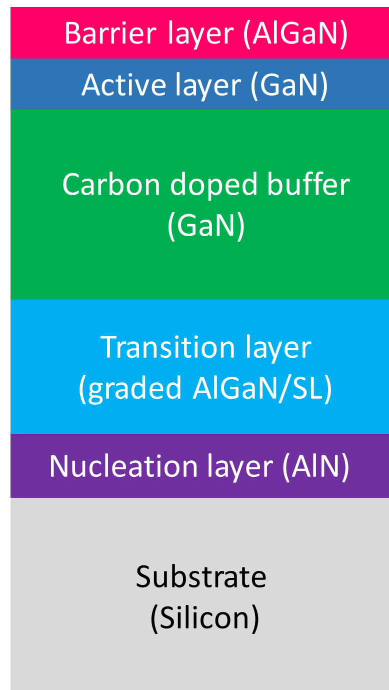


Figure 1.3 – Schematic representation of a standard GaN-on-Silicon epitaxial stack.

1.2 GaN-based Devices

The physical properties of gallium nitride are extensively exploited in order to develop new devices for power application, which allow to improve the conversion systems efficiency by reducing the power losses. Moreover, thanks to the high breakdown strength of the gallium nitride, the dimension of the final circuits can be reduced allowing higher operating frequency. In the following a brief overview on the two GaN-based devices discussed within this thesis is presented.

1.2.1 Lateral devices: HEMTs

The High Electron Mobility Transistor (HEMT) is a n-channel device based on the GaN/AlGaN heterojunction. It exploits the polarization properties of the (Al)GaN material system to form an electron layer which acts as the channel of the device.

Due to the lattice constant mismatch, the AlGaN barrier layer grown over the GaN active layer is submitted to a tensile stress, and the whole layer is strained. This condition causes two piezoelectric charge distributions to be present at the two opposite interfaces of the AlGaN barrier layer; at the AlGaN/GaN interface a strong positive piezo-charge appears, which, added to the positive spontaneous polarization charge of the GaN, over-compensates the spontaneous polarization of the underlying GaN layer and results in a net positive charge at the material interface Figure 1.4.

The abovementioned positive charge attracts the electrons of the undoped GaN layer toward the interface. The resulting high-density accumulation layer extends in a plane parallel to the heterointerface and is strictly confined within a triangular potential well; for these reasons, it is defined 2-Dimensional Electron Gas (2DEG). This sheet of free electrons lies in an undoped semiconductor, meaning that, unlike silicon MOSFETS where the inversion channel is formed in a doped region, there are no scattering phenomena with the doping. This allows the carriers of the 2DEG to have mobility as high as 2000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [15].

The density of the 2DEG can be controlled by applying a potential over the AlGaN barrier layer by means of a gate contact which depletes the underlying semiconductor when a negative voltage is applied.

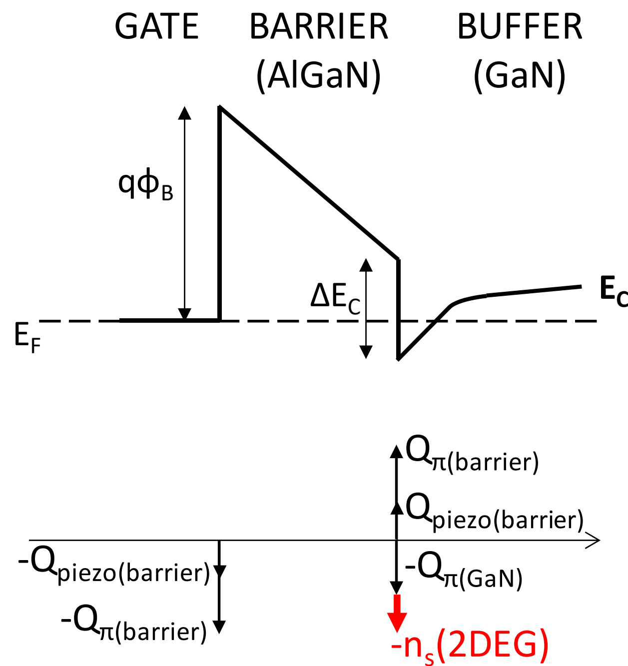


Figure 1.4 – Schematic band diagram and charges distribution in a AlGaN/GaN junction.

By processing two ohmic contacts (source and drain) on the AlGaN barrier layer on the two sides of the gate metal, a transistor is obtained. The electrons flow within the 2DEG from the source ohmic contact (grounded) toward the drain ohmic contact (positive potential); by acting on the gate potential the density of the electron channel can be modulated, thus biasing the device in on-state or off-state.

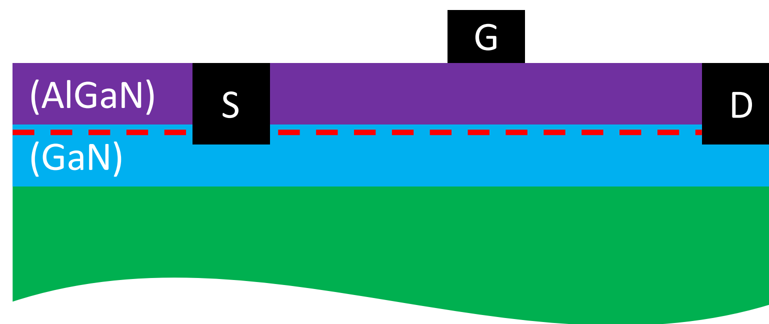


Figure 1.5 – schematic cross section of a HEMT device.

As previously discussed, the devices based on the AlGaN/GaN heterojunction have a normally-on behavior, meaning that a negative gate voltage is necessary in order to deplete the 2DEG and to switch off the device. This characteristic is not suitable for a device supposed to operate in a power conversion circuit. In fact, for safety reasons, the device must be in an off-state condition when its gate contact is biased to 0 V. Although several solutions have been developed in order to achieve the normally-off behavior, the

use of a p-doped gate is the most commonly used for power devices. During the epitaxial growth of the wafers, a layer of magnesium (Mg) doped GaN is placed above the barrier layer. This layer is selectively etched during the fabrication of the device in the whole active region except for the area below the gate metal contact. This leads to a partial depletion of the 2DEG in the gate region under equilibrium condition ($V_G = 0$ V). In order to turn-on the device a positive gate bias is needed.

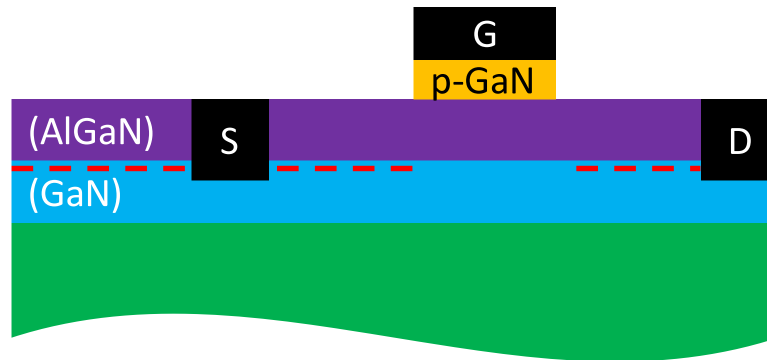


Figure 1.6 – schematic cross section of a normally-off HEMT device with the p-GaN gate.

In the final application, that is a switching converter, the device operates either in on-state and in off-state condition. During the on-state, when the gate voltage is higher than the threshold voltage and the highly conductive electron channel is formed in the whole drain-source region, the device is biased in linear region, and it can be modeled with a (low) resistance, which determines the on-state losses. On the other hand, when the gate bias is lower than the threshold voltage of the device, the 2DEG do not connect the drain and the source. When the device is in this bias regime, the drain voltage is usually high (due to the circuit operations), and the materials must sustain high electric fields. Several breakdowns might occurs during the off-state condition of the device [16], including vertical breakdown between the drain and the substrate, and lateral breakdown between either drain-gate and drain-source. To avoid lateral breakdown, some design rules must be followed, such as increasing the gate-drain length in order to reduce the electric field within that region of the device. Concerning the improvement of the vertical breakdown, the epitaxial stack thickness and crystal quality need to be optimized.

1.2.2 Vertical Devices: Trench Gate MOSFET

Beside the significant improvement obtained so far, lateral devices suffer of trapping phenomena (mainly related to surface effects) and their breakdown is limited by the device layout (drain-gate length). For considerably-high voltage applications (> 1000 V), new device architectures have been developed.

One example is the vertical trench gate Metal Oxide Semiconductor transistor. These devices are based on a $n^-/p/n^+$ GaN structure obtained by sequentially growing the three layers epitaxially over a substrate. The drain contact is placed on the bottom of the three GaN layers, while the source is electrically connected with the top n-doped layer. The gate MOS module of the device is placed on a vertical etched surface, and it penetrates the n^+ layer and the p layer thus modulating the bias condition and the charge density at the dielectric/semiconductor interface in the p-doped layer.

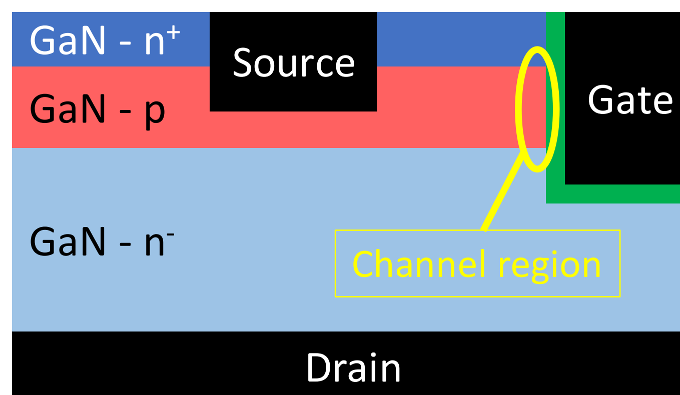


Figure 1.7 – schematic cross section of a vertical trench gate MOS device.

As a positive gate bias is applied to the gate contact, an inversion layer is created in the semiconductor, thus shorting the two n^+ and n^- layers. On the other hand, for low gate biases, there is no inversion channel, and the p/n^- junction might deplete according to the applied drain bias. The bottom n-doped layer is called drift layer and it is typically lowly doped and considerably thick: the role of this layer is to accommodate the off-state electric field by distributing it in a wide depleted region.

The distribution of the electric field during the off-state condition in a vertical device is crucial to obtain high breakdown voltage. Despite lateral devices, where the breakdown is limited by the lateral gate/drain distance, in the vertical architecture the off-state voltage mainly drops in the bulky lightly-doped GaN layer. This means that the vertical breakdown depends on both the thickness of the drift layer and on its doping

level. Moreover, since the electric field is distributed in a bulk semiconductor, there are no issues related to the interfaces trapping.

Since the off-state robustness is mainly related to the thickness of the epitaxial stack (and of the drift region), it is important to grow high quality thick epitaxial stacks. As discussed in the previous paragraph, GaN substrate is the most suitable solution to obtain high quality and thick epitaxy, and several works in literature demonstrate the advantages of fabricating GaN-on-GaN vertical devices [17], [18]. Nevertheless, the fabrication of vertical devices on foreign substrates is promising, since it allows to reduce the costs of the final devices [19], [20].

Chapter 2:

Reliability of the GaN-on-Si vertical stack

Part of the discussions, data and figures presented within this chapter have been previously published in:

M. Borga, M. Meneghini, D. Benazzi, E. Canato, R. Püsche, J. Derluyn, I. Abis, F. Medjdoub, G. Meneghesso and E. Zanoni "Buffer Beakdown in GaN-on-Si HEMTs: a comprehensive study based on a sequential growth experiment", Microelectron. Reliab., 2019, special issue ESREF 2019, DOI:*10.1016/j.microrel.2019.113461* [21].

M. Borga, M. Meneghini, I. Rossetto, S. Stoffels, N. Posthuma, M. Van Hove, D. Marcon, S. Decoutere, G. Meneghesso, E. Zanoni, "Evidence of Time-Dependent Vertical Breakdown in GaN-on-Si HEMTs," in IEEE Transactions on Electron Devices, vol. 64, no. 9, pp. 3616-3621, Sept. 2017. DOI: 10.1109/TED.2017.2726440 [22]

2.1 Buffer decomposition experiment

As widely discussed in the previous chapter, GaN is commonly grown on foreign substrates, thus guaranteeing good scalability and cost reduction of the final devices. The need to growth gallium nitride over silicon substrates leads to the development of complex buffer and transition layer architectures which allow to obtain a good crystal quality thus an improved electrical performance of the devices.

In this paragraph the results of a so-called "buffer decomposition experiment" will be discussed. Three different samples were fabricated, where the epitaxial growth was interrupted at different stages. In this way we are able to separately evaluate the role of the AlN nucleation layer, of the AlGaN buffer, and of the vertical stack up to the C-doped layer on the conduction and breakdown processes of the vertical stack. Moreover, a reliability analysis on the Aluminum Nitride nucleation layer will be discussed.

2.1.1 Devices description

In this experiment three different samples are tested and studied. The first sample, hereinafter referred as Sample A, consists of a 200 nm thick layer of AlN epitaxially grown on a conductive p-doped silicon substrate. In a GaN-on-Si platform, the AlN layer, beside avoiding the Ga-Si eutectic reaction, acts as a base layer for the growth of the subsequent (Al)GaN layers. The second sample, Sample B, has a similar structure to sample A, but over the thin AlN layer, an additional 350 nm thick $Al_{70}Ga_{30}N$ layer is grown. Usually, in a GaN-on-Si stack, several AlGaN layers are interposed between the nucleation layer and the GaN layer; the aim of these layers is to generate compressive stress to compensate for the thermal-mismatch-induced tensile stress that is generated during cool-down phase. At the same time, the strain fields at the layer transitions cause some of the threading dislocations to bend and thereby limit the density of the dislocations that propagate from the defective nucleation layer toward the subsequent layers. This guarantees a reduced defect and trap densities close to the active region of the final devices.

Lastly, sample C is made up of a p-doped silicon substrate, a 200 nm AlN layer, a 2350 nm thick multi-layer AlGaN backbarrier, which prevents the dislocation to propagate through the epitaxial stack, and a 2450 nm thick carbon doped GaN layer. The aim of the C-doped layer is to prevent punch-through effect on the final devices, and to reduce the intrinsic conductivity of the GaN. Several works in literature show that this layer plays a crucial role not only in the vertical robustness but also in the stability of the devices under dynamic bias conditions [23][24][25]. A schematic representation of the tested structures is shown in Figure 2.1.

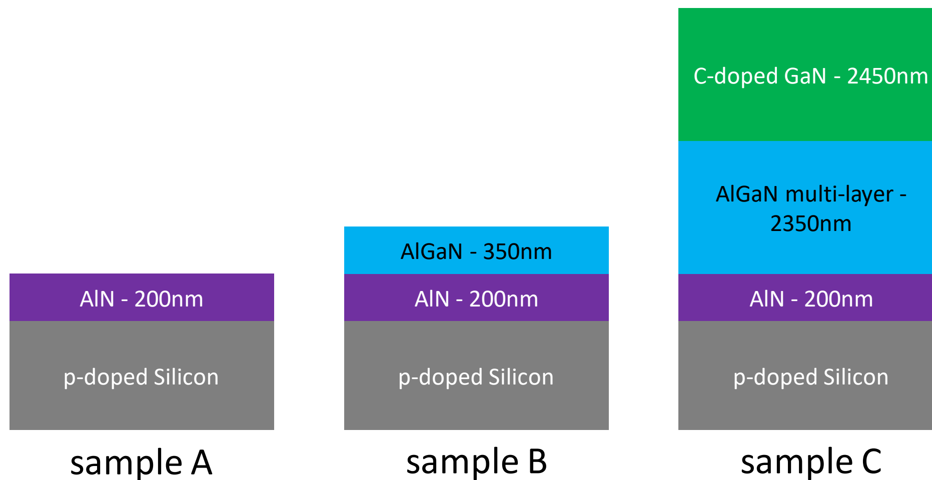


Figure 2.1 – Schematic representation of the three fabricated samples within the buffer decomposition experiment: Sample A (left), Sample B (center) and sample C (right). [21]

The electrical characterizations have been carried out by biasing a set of top ohmic Ti(40nm)/Au(20nm) contacts, defined by photolithography; the contact area is 95x95 μm.

2.1.2 Leakage and breakdown analysis

In a complex semiconductor stack, such as the samples under analysis, where different semiconductor materials with different doping either type and levels are involved, the transport mechanisms of the charges are difficult to fully-comprehend. Moreover, the role of the polarization charge in an atypical junction as the one formed between the Silicon substrate and the AlN nucleation layer is not clear and could strongly affect the leakage and the failure behavior of the stack. A schematic band diagram, which facilitates the comprehension of the energy configuration of the three samples under analysis, is shown in Figure 2.2. It is worth noticing that a high potential barrier prevents electron to be injected from the silicon substrate into the AlN nucleation

layer. Moreover, as suggested in several papers in literature [3][4], an inversion electron layer is formed in the p-doped substrate at the silicon/AlN interface. The AlN is the material with the higher energy gap in the stack on all the three tested samples, and it has a very low density of free charges; for this reason, the nucleation layer is often considered as an insulating layer, and its conduction and valence bands are represented bending linearly and not quadratically. The AlGaN layer(s) has a smaller energy gap compared to the AlN, but, due to the absence of an extrinsic doping, its conductivity is relatively limited. Lastly, the thick GaN layer is doped with Carbon atoms. The aim of this doping is to compensate the intrinsic conductivity of the Gallium Nitride, by introducing deep acceptor-like atoms. The resulting layer can be described as a lowly-doped p-type semiconductor layer. At the AlGaN/GaN junction a p/n heterojunction is formed.

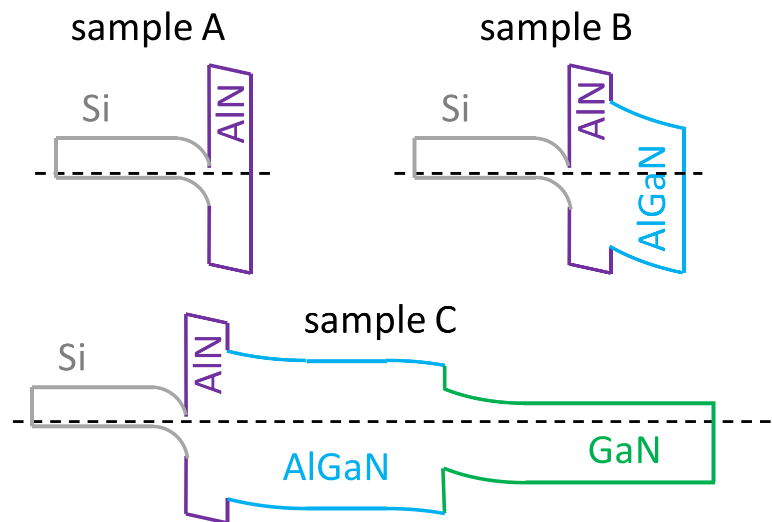


Figure 2.2 – schematic equilibrium band diagram of the studied samples: sample A (top-left), sample B (top-right) and sample C (bottom). [21]

Several devices on each sample are submitted to a voltage sweep on the ohmic pad by means of the High Voltage SMU (±3 kV, 4 mA) of a Keysight B1505A, while the substrate was grounded. These measurements have been carried out at 30 °C, 100 °C, and 170 °C thanks to a ceramic heater driven by a Thorlabs TC200 PID controller. The applied voltage was swept from 0 V up to the failure of the device (step 1 V, integration time 20 ms), so that both the leakage current behavior and the failure voltage are monitored on a single measurement as a function of the ambient temperature.

In Figure 2.3 the current-voltage characteristics at low- and at high-temperature of the three analyzed samples are compared. The leakage current on sample A is not strongly affected by the ambient temperature, meaning that the conduction is limited by a tunneling processes which allows current injection from the electron inversion layer formed in the silicon, at the Si/AlN interface, toward a defect-related deep level within the AlN. This process strongly depends on the availability of states within the AlN close to the material interface, therefore on the local defectivity of the AlN. Once the carriers are injected into the AlN, they easily reach the top ohmic contact thanks to a trap-related conduction favored by the high dislocation density of the AlN.

Unlike sample A, the leakage current on sample B has a higher dependence on the ambient temperature, meaning that the limiting conduction mechanisms is temperature dependent. The electrons are injected from the silicon substrate to the AlN layer by means of a temperature independent tunneling mechanism, as described in sample A discussion. The carriers injected in the AlN move toward the top ohmic contact by means of defects-assisted conduction mechanisms, which are temperature enhanced. Moving from the AlN to the AlGaN layer, the dislocations and defects densities reduce. As a consequence, even if a high amount of electrons is tunneling-injected into the AlN, the conduction within the AlGaN, which is temperature dependent, limits the overall current flowing through the vertical stack of sample B.

Lastly, Blue lines in Figure 2.3 show the strong impact of the ambient temperature on the vertical leakage of the sample C. The high temperature dependence is compatible with the presence of a deep acceptor level (i.e. carbon); the holes located in the C-doped GaN can easily flow toward the substrate (where they recombine) due to the absence of high potential barriers in the valence band moving from the epitaxial layers toward the substrate. The hole current that originates from this process considerably enhances the total current at high temperature due to the higher amount of free holes thermally generated within the C-doped GaN layer at 150 °C. The higher current of the sample C with respect to both sample A and sample B in the voltage range of 0 V - 100 V at high temperature confirms that the parallel holes current becomes even higher than the electron current as the temperature increases.

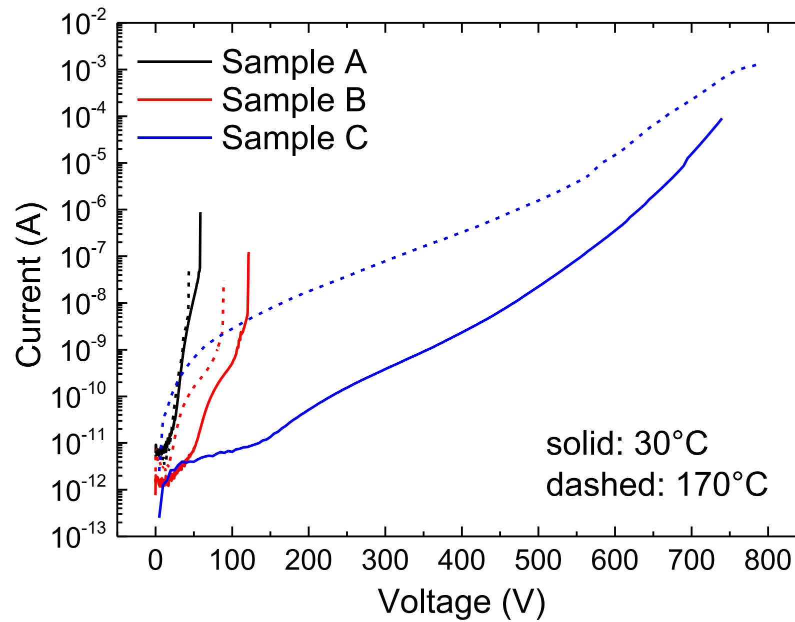


Figure 2.3 – Current-voltage characteristics carried out at both low- and high-temperature in the three samples under analysis.

In order to further investigate the conduction processes, the three samples under analysis are submitted to a double voltage sweep (upward and backward) at both low and high temperature. The aim of the measurement is to evaluate the presence of a hysteresis between the upward and backward curves. The hysteresis is an indicator of the trapping phenomena: the electrostatic potential of the trapped charges, which are injected during the upward voltage sweep, affects the behavior of the current during the backward sweep. The voltage step was 1 V, while the integration time was 20 ms. The maximum voltage is chosen in order to avoid the breakdown of the devices, and it is respectively for sample A, sample B and sample C of 40 V, 80 V and 600 V.

Experimental results which are shown in the following pages, prove how each samples feature is directly linked to its trapping behavior:

- On sample A (Figure 2.4), as the ambient temperature increases from 30 °C to 150 °C, the hysteresis is considerably reduced. This can be ascribed to the effect of the temperature on the detrapping kinetic, which results in a lower amount of trapped charges during the backward sweep with respect to the upward sweep.
- Sample B (Figure 2.5) exhibits a comparable hysteresis at both room temperature and high temperature; it is worth noticing that, unlike sample

A in which the current level during the upward sweep is not depending on the ambient temperature, the leakage current in sample B strongly depends on the temperature, as discussed previously. This leads to a higher carrier injection, which results in an increased availability of charge that might be trapped. The higher density of trapped charges during the upward sweep, hinders the hopping conduction between deep states, thus causing the hysteresis to be higher than on sample A.

- Sample C (Figure 2.6), besides being the more complex structure within the experimental set, thanks to the carbon acceptor states, is the only structure where also a source of positive charges (holes) is present. The role of the carbon in the hysteresis of the leakage current through the stack is clear in Figure 2.6 (a): the current during the backward sweep is higher than the current during the upward sweep, meaning that positive charges, which promote the carrier injection, are trapped within the stack. The high temperature even enhances this phenomenon, thanks to the higher availability of positive charges within the epitaxial layers.

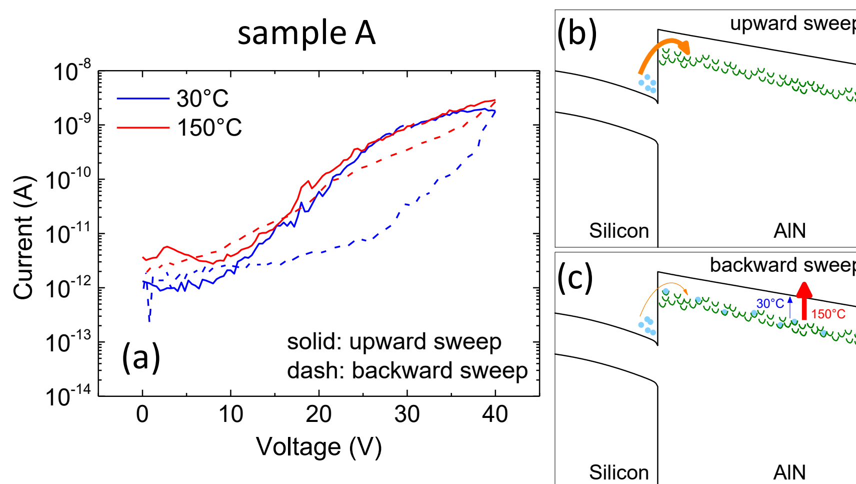


Figure 2.4 – (a) Double sweep (upward: solid, backward: dashed) current-voltage characterization on sample A at both room- and high-temperature. Figures (b) and (c) represent a schematic band diagram during respectively the upward sweep and the backward sweep.

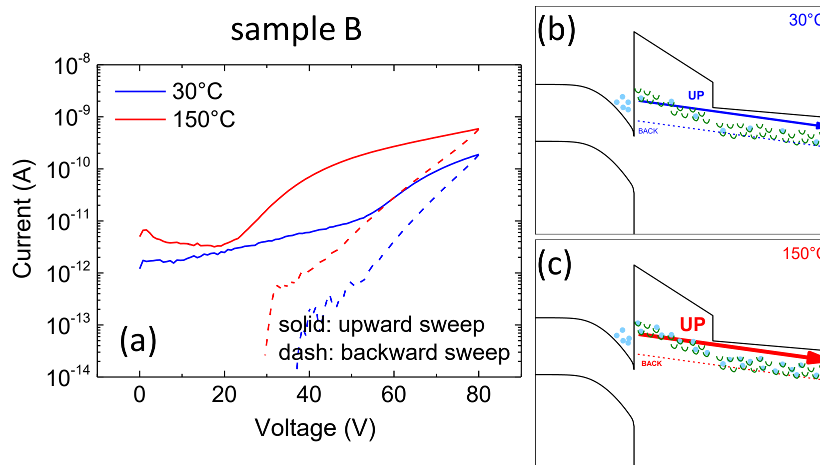


Figure 2.5 – (a) Double sweep (upward: solid, backward: dashed) current-voltage characterization on sample B at both room- and high-temperature. Figures (b) and (c) represent a schematic band diagram respectively at room and high temperature.

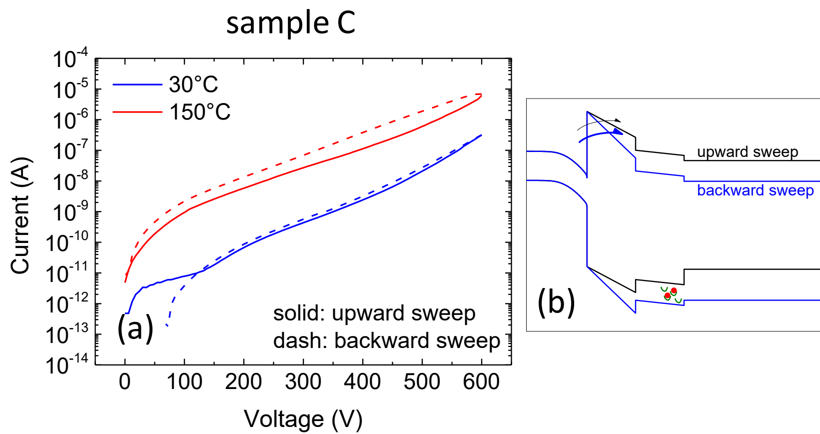


Figure 2.6 – (a) Double sweep (upward: solid, backward: dashed) current-voltage characterization on sample C at both room- and high-temperature. Figure (b) represent a schematic band diagram where the electrostatic effect of the positive trapped charges is highlighted.

After focusing on a single device behavior, a more statistical approach was adopted. Several devices were tested on each sample at 30 °C, 100 °C and 170 °C, by sweeping the voltage on the top ohmic contact from 0 V, with a step of 1 V, up to the catastrophic failure of the device.

The electrical characterizations performed on sample A, show an unstable current-voltage characteristic of the devices and a high device-to-device variability (Figure 2.7 (a)). As discussed before, the current of sample A strongly depends on the local defectivity of the AlN layer caused by both the remarkably high lattice mismatch between the Aluminum Nitride and the Silicon as well as the low surface mobility of Al species during the epitaxial growth. Moreover, also the presence of impurities might play a role in increasing the leakage current through the AlN, as cussed in [28]. The latter

also demonstrate that the leakage current through the AlN layer as well as its robustness can be improved by carefully optimizing the growth temperature of the AlN layer itself.

Lastly, the leakage current behavior through the AlN shows a low dependency on the ambient temperature, since the tunneling current mostly depends on the local defectivity of the material. The same dependence of the breakdown electric field on the ambient temperature was also shown in [29] with a more statistical approach; the temperature weakly affects the critical mean electric field, but, by testing several devices, it was demonstrated that there is a higher spread on the failure electric field at high temperature.

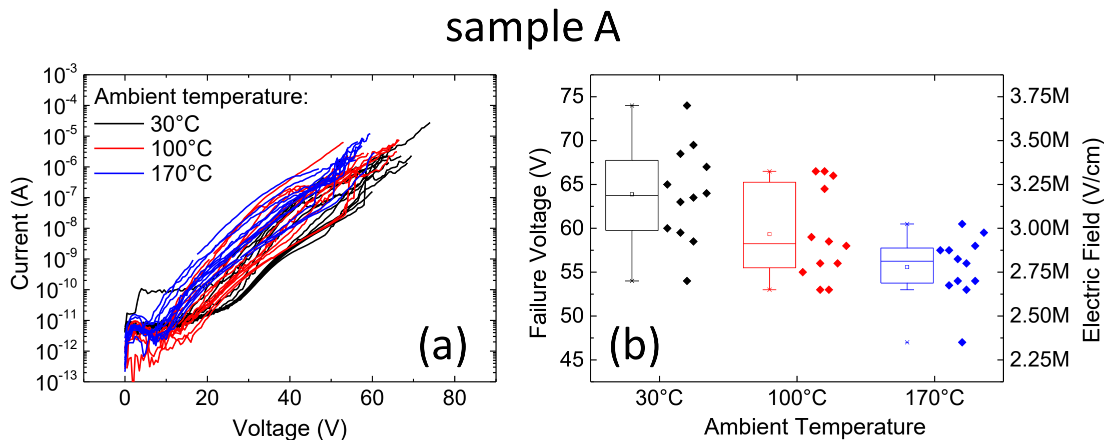


Figure 2.7 – Current-voltage characteristics performed on several devices of sample A at different ambient temperatures. Plot (b) summarizes the failure voltage of the tested devices as a function of the ambient temperature; right-axis shows the equivalent failure electric field. [21]

By comparing the current-voltage characteristics of the devices grown on sample B (Figure 2.8 (a)) with those grown on sample A, it is clear the role of the AlGaN layer: the current-voltage curves of sample B result more stable and the device-to-device variability is considerably reduced. Moreover, due to the higher total thickness of the epitaxial layers, the breakdown voltage of the devices on sample B is considerably higher with respect to the failure voltage of the devices of sample A. In the case of sample B, the average electric field at the breakdown was calculated as the ratio of the failure voltage and the total thickness of the AlN and the AlGaN layers, and it results 2.58 MV/cm at 30°C. This calculation is a strong approximation, since a non-uniform partitioning of the applied voltage shall occur. The failure electric field of sample B is lower than the one calculated in sample A, meaning that the electric field is not uniformly distributed within the AlN/AlGaN stack. This can be ascribed either to the different dielectric constants and

the different conductivity of the two materials; moreover, also the piezoelectric charge may play a role in the voltage partitioning within the epitaxial layers. As on sample A, the higher ambient temperature results in a lowered breakdown voltage (Figure 2.8 (b)).

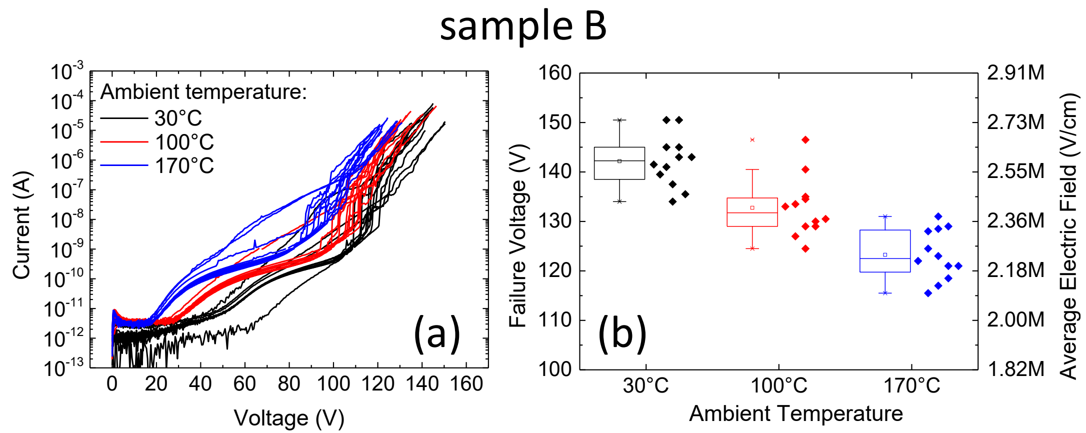


Figure 2.8 – Current-voltage characteristics performed on several devices of sample B at different ambient temperatures. Plot (b) summarizes the failure voltage of the tested devices as a function of the ambient temperature; right-axis shows a rough estimation of the failure electric field. [21]

The current-voltage characteristics of the sample C are shown in Figure 2.9 (a). The thick carbon doped layer, besides reducing the conductivity of the vertical stack, causes the carrier conduction not to be related to the local defectivity of the semiconductor but to the carbon doping of the buffer layer, which is a well-controlled parameter, thus resulting in a remarkably high repeatability of the IV characteristics of the devices over the whole sample area. As previously discussed, the ambient temperature has a clear impact on the current through the structure, causing this latter to be higher for increasing temperatures. Lastly, thanks to the thick epitaxial layer and thanks to the high material quality of the carbon doped GaN layer, the breakdown voltage is considerably improved, and it is higher than 700 V at room temperature (Figure 2.9 (b)). The breakdown voltage slightly decreases increasing the ambient temperature.

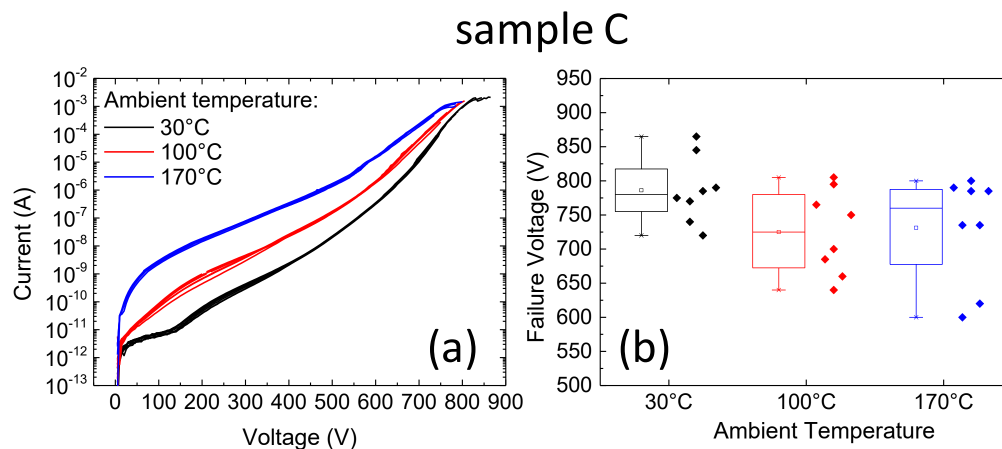


Figure 2.9 – Current-voltage characteristics performed on several devices of sample C at different ambient temperatures. Plot (b) summarizes the failure voltage of the tested devices as a function of the ambient temperature. [21]

2.1.3 Reliability of the AlN nucleation layer

This paragraph focuses on the failures of the AlN layer grown on a silicon substrate. The leakage characterizations at different ambient temperatures show a very unstable behavior of the current with the applied voltage, thus indicating the high defectiveness of the material. Studying the failure statistic of this sample allows us to better understand if the defects play a role in the breakdown of the devices.

Beyond the analysis on the conduction mechanisms and on the trapping phenomena, Sample A allows also an estimation of the breakdown electric field of the Aluminum Nitride grown on silicon. Thanks to the conductive nature of the silicon substrate, we can suppose that all the applied voltage drops on the AlN layer. Moreover, the AlN can be considered as an insulating material, meaning that the electric field through it is almost constant within the whole thickness. These two approximations allow us to estimate the maximum electric filed that causes the breakdown of the AlN layer by calculating the ratio between the failure voltage and the thickness of the AlN layer (Figure 2.7 (b)). At 30 °C the average breakdown electric field of the AlN layer results 3.2 MV/cm, and it drops to 2.78 MV/cm at 170 °C, showing a weak temperature dependence, in agreement with the analysis reported in [29]. These breakdown filed values are compatible with previous works in literature [26][27][28].

A set of constant voltage stresses are carried out by biasing at 50 V the ohmic contact on top of the AlN layer with a Keithley 2410, a high voltage source meter limited at 1.1 kV, 20 mA. The silicon substrate was grounded. Due to the high conductivity of

the silicon substrate, all the applied voltage drops on the AlN layer, thus allowing the study of its failure statistic. During these voltage stresses the ambient temperature was 30 °C. This TDDB-like analysis aims to extend the statistical study presented by Schneider at al. in [29], where the failure electric field of the AlN grown on Silicon was demonstrate to be Weibull distributed and weakly temperature dependent.

In Figure 2.10 the noisy behavior of the current through the AlN layer over the time can observed; this can be ascribed to the defectiveness of the material, which results in a dynamic formation and disruption of leakage paths. Once a set of defects is aligned, a conductive path gets formed between the ohmic contact and the silicon substrate, the device shows a catastrophic breakdown. This failure mechanism was previously defined as percolation [30], and it is typical of the breakdown of the dielectric materials.

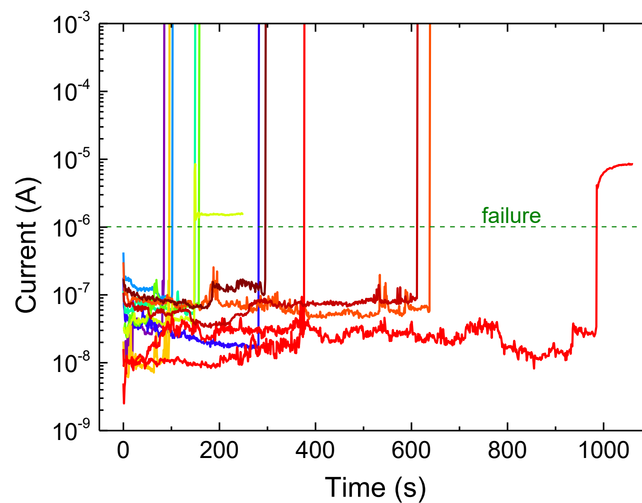


Figure 2.10 – Current behavior over the time during a constant voltage stress at 30°C performed on 10 devices of sample A. [21]

By plotting the time to failure of a set of 10 devices grown on sample A on a Weibull plot (Figure 2.11), it can be noticed that the points perfectly align, meaning that the failures are Weibull distributed.

The cumulative Weibull distribution is expressed as:

$$F_t = 1 - e^{\left(\frac{t}{a}\right)^{\beta}}$$

The distribution is characterized by two parameters; the shape parameter β and the scale parameter α. The shape parameter β gives a direct indication if the failure rate either decreases over the stress time (β < 1) or increases over the time (β > 1). If the failure rate decreases over the time, it means that the devices under test show early-life failures,

often caused by a latent defect related to the device itself. On the other hand, when the shape parameter is higher than 1, the failure rate increases over the time, meaning that the devices fail due to a degradation process.

The beta parameter value of the distribution extracted with 99% confidential level is 1.05, meaning that the failures are caused by a wear-out process that degrades the devices. The alpha parameter, which represents the time at which the 63.2% of the devices is expected to be failed, is equal to 189 s for the adopted stress condition. The Weibull distribution of the failures agrees with the percolation model, confirming the hypothesis made on the failure mechanism of the AlN layer.

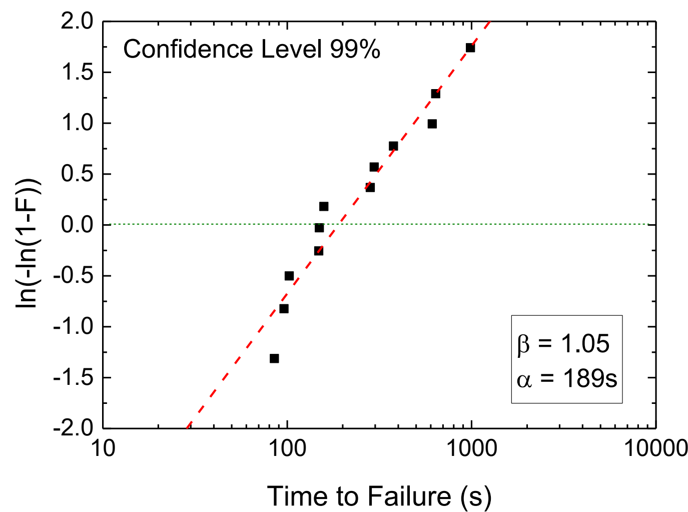


Figure 2.11 – Weibull plot of the failures recorded during the TDDB analysis performed on sample A. [21]

Lastly, the impact of the temperature on the failure voltage shown in Figure 2.7 can be used for the investigation of the failure process of the AlN nucleation layer. As the temperature increases, the energy of the bonds among the atoms which compose the crystal lattice of the material tends to decrease. This results in a reduction of the energy gap of the semiconductor, thus in a reduction of the critical electric field which leads to the breakdown of the material.

The energy gap reduction due to the temperature can be estimated thanks to either the Varshni Law and the Bose-Einstein relation[31]:

$$(Varshni) \qquad \Delta E_G(T) = \frac{\alpha\, T^2}{\beta + T} \qquad \alpha = 1.8\ \text{meV}, \qquad \beta = 1462$$

$$(Bose - Einstein) \qquad \Delta E_G(T) = a_\beta \frac{2}{e^{\frac{\theta}{T}} - 1} \qquad a_\beta = 471\text{meV} \qquad \theta = 725$$

Considering that the energy gap of AlN at 0 K is roughly 6.15 eV [31], the energy gap at 300 K (~ 30 °C) and at 450 K (~ 170 °C) results:

$$E_G(300\ K) = \begin{matrix} 6.058 & (Varshni) \\ 6.057 & (Bose - Einstein) \end{matrix}$$

$$E_G(445\ K) = \begin{matrix} 5.963 & (Varshni) \\ 5.920 & (Bose - Einstein) \end{matrix}$$

Furthermore, the value of the energy gap directly affects the critical breakdown field, which can be calculated as [32]:

$$E_{crit} = 1.73 \cdot 10^5 \cdot E_G^{2.5}$$

The analytical calculation of the critical electric field variation related to the reduction of the energy gap caused by the increasing temperature results:

$$\Delta E_{crit}(\%) = 1.73 \cdot 10^5 \cdot \frac{{E_G^{445K}}^{2.5} - {E_G^{300K}}^{2.5}}{{E_G^{300K}}^{2.5}} = \begin{matrix} -4.02\ \% & (Varshni) \\ -5.91\ \% & (Bose - Einstein) \end{matrix}$$

The theoretical variation of the critical electric field induced by the increasing temperature does not explain the experimental results, where the extrapolated critical electric field variation from 300 K to 445 K results above 12 %.

Nevertheless, by plotting the failure voltage over the leakage current of the device (Figure 2.12), a clear trend can be observed: devices with higher leakage current show a lower breakdown voltage (and consequently a lower breakdown field) of the AlN nucleation layer. This demonstrates that the breakdown process is current driven, meaning that the carriers flowing through the semiconductors locally damage the lattice leading to the failure of the layer, consistently with the percolation theory mentioned above.

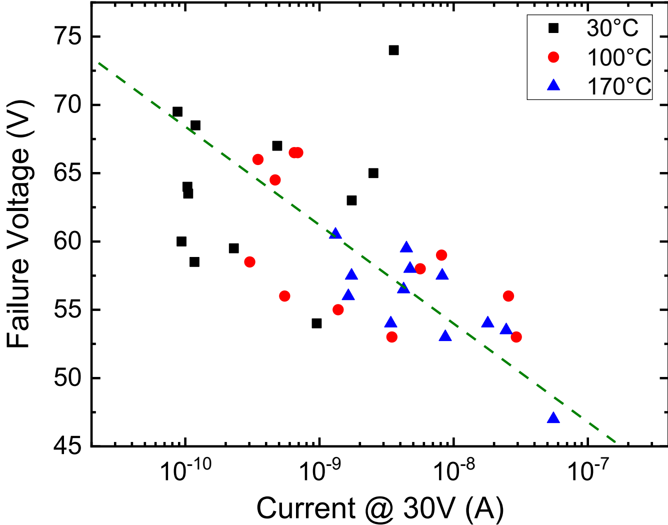


Figure 2.12 – Failure voltage vs the leakage current measured at 30 V on Sample A at different ambient temperatures.

2.2 Reliability analysis on a full GaN-on-Silicon stack

In the previous paragraph the leakage conduction and the reliability of three samples obtained by stopping the epitaxial growth of a GaN-on-Silicon stack at different stages was discussed. In this paragraph a similar analysis performed on a GaN-on-Silicon full stack is presented. Several breakdown mechanisms can occur in a GaN-based device when submitted to an OFF-state bias [16]: lateral breakdown at the drain edge of the gate (where the electric field peaks), due to converse piezoelectric effect [33] or to the time-dependent formation of traps and percolative paths [34]; lateral drain-source breakdown of the (Al)GaN buffer caused by sub-threshold leakage and punch-through effects [35]; lateral breakdown of the silicon nitride (passivation) layer due to the excessive electric field at the edge of the field-plate [36], [37]; vertical (buffer-related) breakdown ascribed to the increase of both the drain-to-substrate leakage [38]–[43] and the electric field.

The aim of this study is to investigate the vertical leakage and breakdown processes in GaN-based transistors by means of electrical characterizations, optical inspection, and failure statistics.

2.2.1 Devices description

The results presented in this paragraph were obtained on AlGaN/GaN normally-off HEMTs grown on a silicon substrate designed for 200 V operation. The normally-off condition has been obtained through the use of a p-GaN gate. Concerning the vertical breakdown, the most important aspect is the epitaxial stack of the devices, between drain and substrate contacts. Over the boron-doped silicon substrate with a resistivity comprised between 1 to 10 Ω·cm, a 200 nm AlN nucleation layer is grown. Graded backbarrier is composed by two 500 nm AlGaN layers with Al concentration respectively of 0.77 and 0.44. The 2000 nm thick carbon-doped buffer layer is an AlGaN alloy with 8% of Al concentration. Finally, on top of the C-doped buffer there are 300 nm of undoped GaN (channel layer), in which the two-dimensional-electron-gas (2DEG) is formed. The drain-contact width is 100 μm while its length is 47 μm. Gate-drain distance

is 0.85 μm. Even if the tested devices were provided with working gate-stack and source contact, all the measurements presented within this section were performed by only biasing the drain contact and keeping the substrate grounded (unless otherwise specified). This was useful to test the vertical leakage and robustness of the vertical stack in a condition as close as possible to the final device architecture.

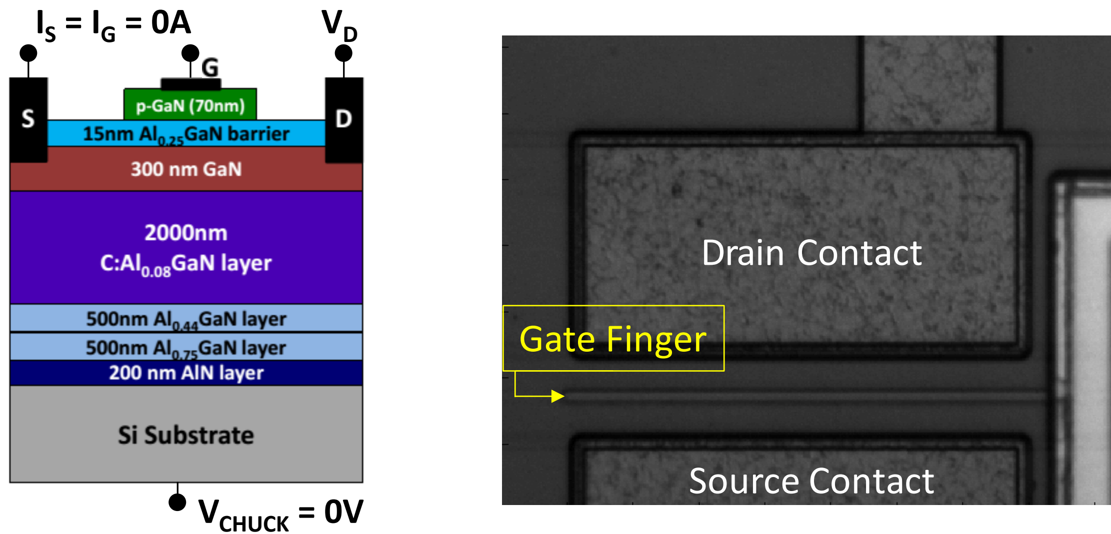


Figure 2.13 – schematic cross section (left) and top view (right) of the tested devices. Copyright © 2017, IEEE.

2.2.2 Leakage analysis and step-stress tests

Before the execution of the stress experiments, we investigated the physical origin of vertical leakage current. Figure 2.14 (a) shows the 2-terminal leakage measurements (between drain and source) performed on five devices belonging to the same wafer. The leakage curves were measured by sweeping, with the High Voltage SMU of a Keysight B1505A (±3 kV, 4 mA), the drain voltage from $V_D = 0$ V up to the failure of the device. The disrupting breakdown of the samples under test occurs at about 900 V. Moreover, two conduction mechanisms can be noticed (see the change in slope above $V_D = 300$ V in Figure 2.14). This result is consistent with previous studies [44], [39] and has been explained as follows: for $V_D < 200$ V, conduction is nearly ohmic (possibly involving dislocations), since the slope of the log-log I-V curves is nearly 1. For $V_D > 300$ V, the buffer is significantly depleted, and the defects (possibly C atoms on nitrogen sites, C_N) are ionized. As described in [39], the high electric field for $V_D > 300$ V may favor Poole-Frenkel emission processes, and allows the charge stored in the ionized C_N acceptors to leak out of the traps. This leads to a strong increase in vertical leakage for $V_D > 300$ V

(where I ~ V^k, k = 18). By increasing the ambient temperature, the leakage current increases (Figure 2.14 (b)), consistently with the paper of Moens *et al.* [39], due both to the increased availability of free carriers and to a stronger ionization of buffer traps.

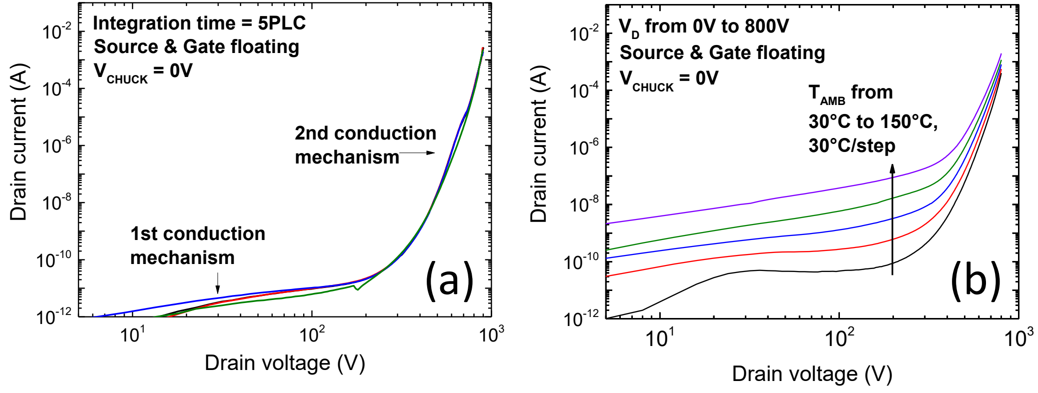


Figure 2.14 – (a) Vertical leakage current behavior at ambient temperature of several devices. (b) Vertical leakage current of the devices under test as a function of the ambient temperature. Copyright © 2017, IEEE.

In order to further investigate the field-enhanced emission process, the following Poole-Frenkel equation was considered:

$$I = A\, e^{-\Phi_B/kT} e^{\beta\sqrt{E}/kT}\, E$$

Where I is the Poole-Frenkel current, A is a constant value, β is the Poole-Frenkel parameter, k is the Boltzmann constant, Φ_B is the depth of the trap level, and E is the electric field. Due to the complexity of the vertical stack, the correlation between the applied voltage and the electric field is not clear. Taking into account that the depleted junction is the u.i.d-GaN/C:GaN interface and knowing that the C:GaN thickness is 2000 nm, as an approximation we can assume that the region where is located the electric field is 2000 nm. So that the electric field results to be proportional to the ratio between the applied voltage and 2000 nm. Moreover, the Poole-Frenkel current can be written as:

$$\ln\left(\frac{I}{E}\right) = \ln(A) - \frac{q\Phi_B}{kT} + \frac{q\beta\sqrt{E}}{kT} = (\beta\sqrt{E} - \Phi_B)\frac{q}{kT} + \ln(A)$$

Thanks to the leakage measurements in temperature (Figure 2.14 (b)), we are able to plot the ln(I/E) as a function of q/kT at different voltages (Figure 2.15 (a)). It is immediately clear that the set of points related to each drain bias is perfectly aligned; moreover, from the Poole-Frenkel equation, we can notice that the slope of the fitting line is:

$$\text{slope} = \beta\sqrt{E} - \Phi_B$$

Plotting the slopes of the fitting curves versus the square root of the applied electric field on the depleted junction (Figure 2.15 (b)), it is possible to determine both the β parameter and the Φ_B.

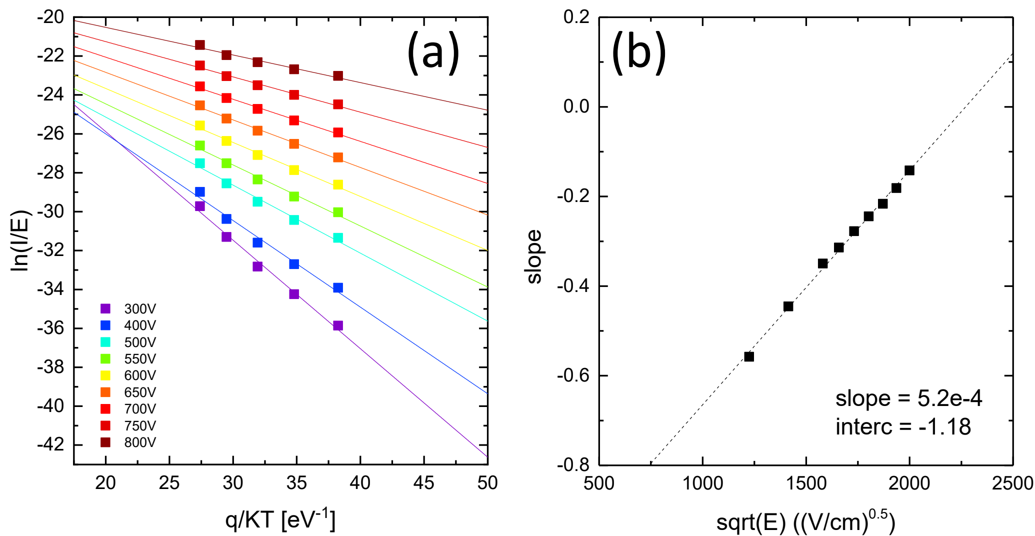


Figure 2.15 – (a): Poole-Frenkel plot at different electric field strength as a function of the ambient temperature; the experimental values lie on a line for each voltage bias. (b): slope of the fitting lines on the Poole-Frenkel plot as a function of the square root of the electric field. The slope gives an indication of the energy level of the states involved in the Poole-Frenkel effect.

Thanks to the described analysis, it was extracted the depth of the trap level involved in the conduction process, which results 1.18 eV. This value – considering the degree of approximation of this analysis – is consistent with the carbon related defects (C_N, 0.85-0.95 eV [45]).

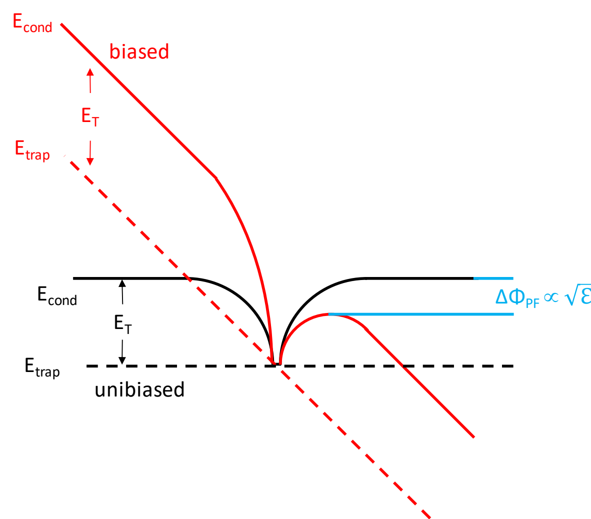


Figure 2.16 – schematic band diagram of the Poole-Frenkel emission at high drain bias. Copyright © 2017, IEEE.

In order to obtain a better understanding on the failure mechanisms and on the vertical robustness, step-stress experiments were performed. The voltage between drain and substrate was increased by 20 V every 120 s, from V_D = 0 V up to the failure of the device. All the measurements presented within this chapter were obtained by biasing the drain, with only the substrate grounded. The gate and the source were left disconnected. Representative results are reported in Figure 2.17 (a): the device showed a stable behavior up to a drain voltage of 700 V. For higher stress voltages, the noise superimposed to the drain leakage current showed a significant increase, indicating the generation of random conductive paths between adjacent defects [46], [47] (see also the enlargement of the last steps in Figure 2.17 (b)). Breakdown was found to occur at V_D = 870 V, which is lower than the breakdown voltage estimated by DC sweeps. The results in Figure 2.17 suggest that the vertical (drain-source) breakdown is a time-dependent process, that is driven by the high electric field.

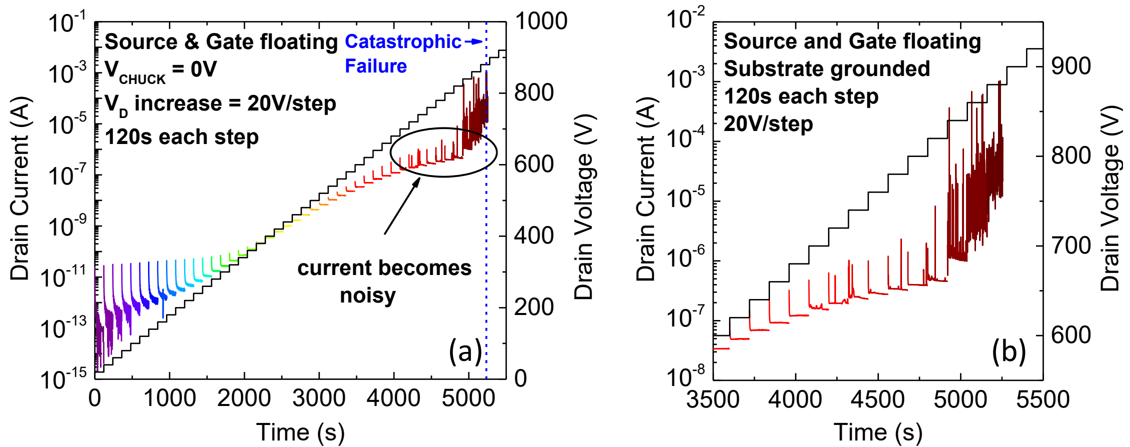


Figure 2.17 – (a) Drain current monitored during the step-stress (V_{CHUCK} = 0 V, V_D increases in 20 V steps). (b) Drain current monitored during the last 15 steps before failure occurs. Copyright © 2017, IEEE.

2.2.3 Time dependent breakdown and reliability analyses

To investigate the dependence of the degradation kinetics on voltage and temperature, a set of constant voltage stress tests were carried out. Based on the results of leakage measurements and step-stress tests, three drain voltages were imposed during the constant voltage stresses, namely 770 V, 800 V, 820 V. Figure 2.18 reports the variation of the leakage current measured during the stress of 18 identical samples at V_D = 800 V. Vertical leakage current is initially stable, and slightly decreases due to the occurrence of charge trapping effects. For sufficiently long stress times, the current

becomes noisy, suggesting the occurrence of a defect generation process. The failure consists in a sudden increase in the leakage current, that leads to the catastrophic failure of the devices. This behaviour is similar to the time-dependent breakdown of dielectrics, that is commonly explained by the defect percolation theory [30].

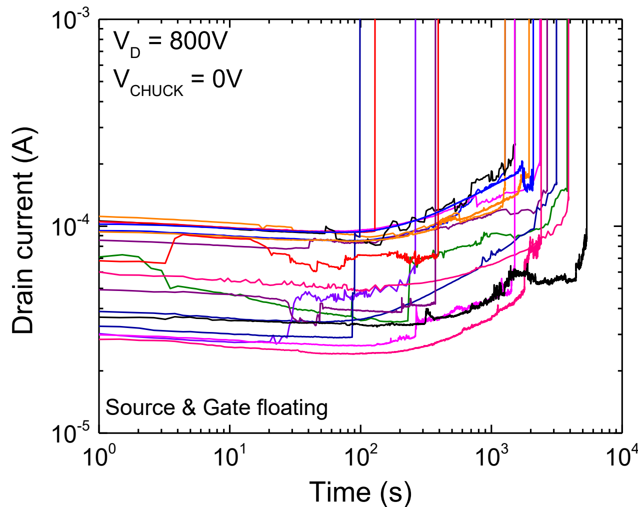


Figure 2.18 – Drain current monitored during a constant voltage stress (V_D = 800 V). Copyright © 2017, IEEE.

Figure 2.19 reports the time to failure and leakage current of several devices stressed at the three different voltage levels. With increasing stress voltage, an increase in leakage current and a decrease in TTF is observed.

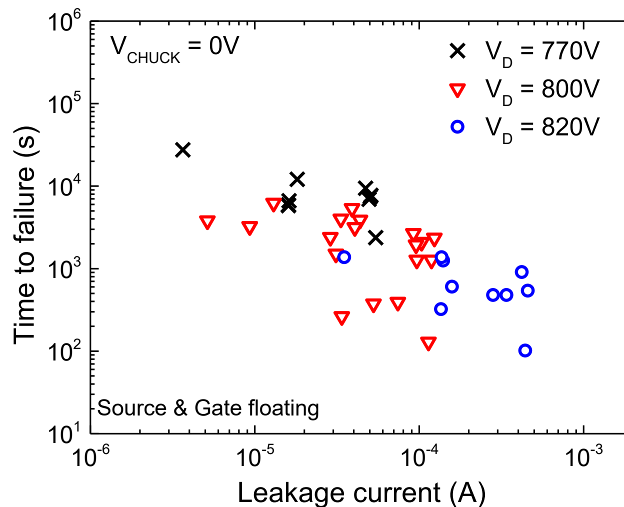


Figure 2.19 – time to failure dependence on the initial leakage for three drain bias levels applied during the constant voltage stress. Copyright © 2017, IEEE.

Figure 2.20 (a) shows that the TTF follows a Weibull distribution, which was previously presented in 2.1.3. The scale parameters, with 50% of confidence level, are 10511.5 s, 2868.5 s, 863.2 s respectively at drain bias of 770 V, 800 V, 820 V. In agreement

with the percolation theory [30], the drain voltage accelerates the failure mechanisms, resulting in a lower time to failure at higher voltages. Shape parameters are larger than 1 and range between 1.51 and 1.93, thus suggesting that the breakdown is related to the intrinsic properties of the material rather than to extrinsic factors [48]. Figure 2.20 (b) shows the box chart of the dependence of the time to failure on the applied voltage; the time to failure exponentially decreases with increasing stress bias, indicating that the degradation process is strongly field-dependent.

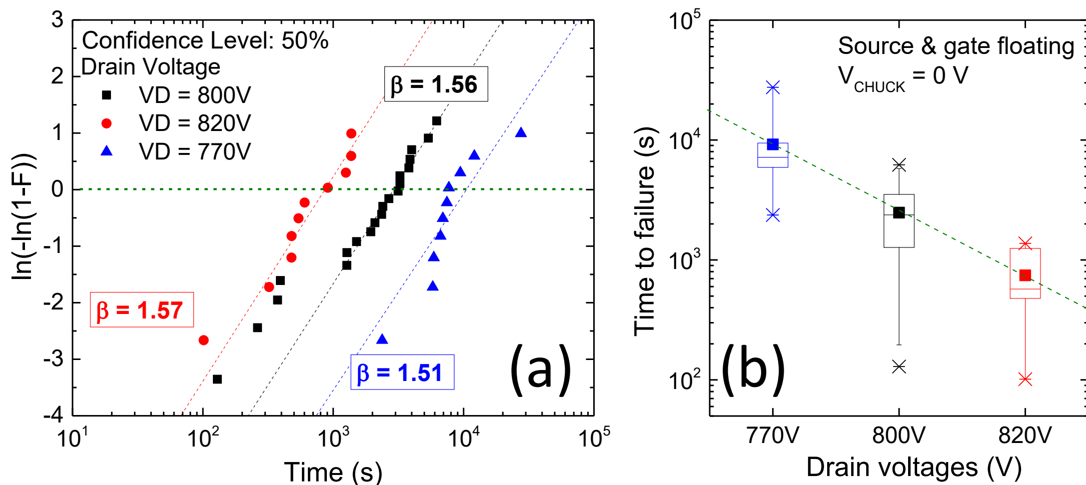


Figure 2.20 – (a): Weibull plot of the constant voltage stresses performed on several devices at three drain voltages, namely 770 V, 800 V, 820 V. (b): time to failure dependence on the applied drain voltage (box chart). Copyright © 2017, IEEE.

To evaluate the impact of temperature on TTF, we performed constant voltage stress tests (stress voltage = 770 V) at different ambient temperatures, namely 30 °C, 90 °C, 150 °C (Figure 2.21 (a)). Increasing stress temperature shortens the TTF: the activation energy of the failure mechanism was extracted, and it results E_a = 0.25 eV (Figure 2.21 (b)). Previous discussion indicates that TTF is strongly (exponentially) dependent on the electric field, indicating that the degradation process is field-dependent. On the other hand, a low thermal activation (E_a = 0.25 eV) was found. This result supports the hypothesis that degradation is primarily activated by voltage, while temperature acts only as a weak acceleration factor.

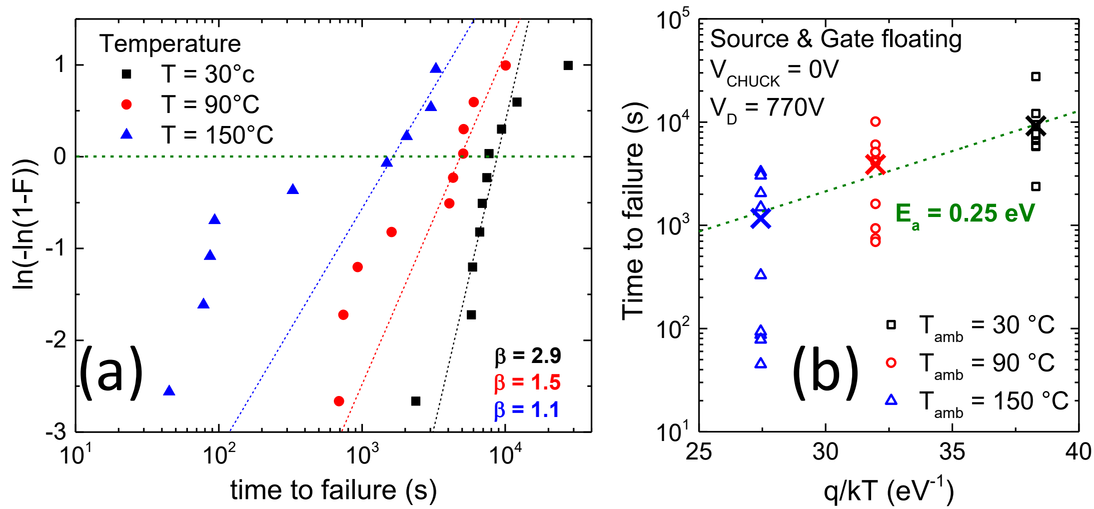


Figure 2.21 – (a) Weibull plot of constant voltage stress (V_D = 770 V, T_{amb} ranging from 30 °C to 150 °C). At high temperature a secondary failure mechanism shortens the lifetime of some devices. (b): corresponding Arrhenius plot. Copyright © 2017, IEEE.

The results obtained allowed us to evaluate the dependence of the time to failure on the applied voltage. Figure 2.22 shows that the maximum applicable voltage in order to obtain a lifetime of 20 years with 1 % failure rate is about 560 V at room temperature (T_{AMB} = 30 °C), considerably higher than the operating voltage of the devices under test (200 V). Consistently with the low activation energy of the failure mechanism, analogous results were estimated at higher temperature (150°C).

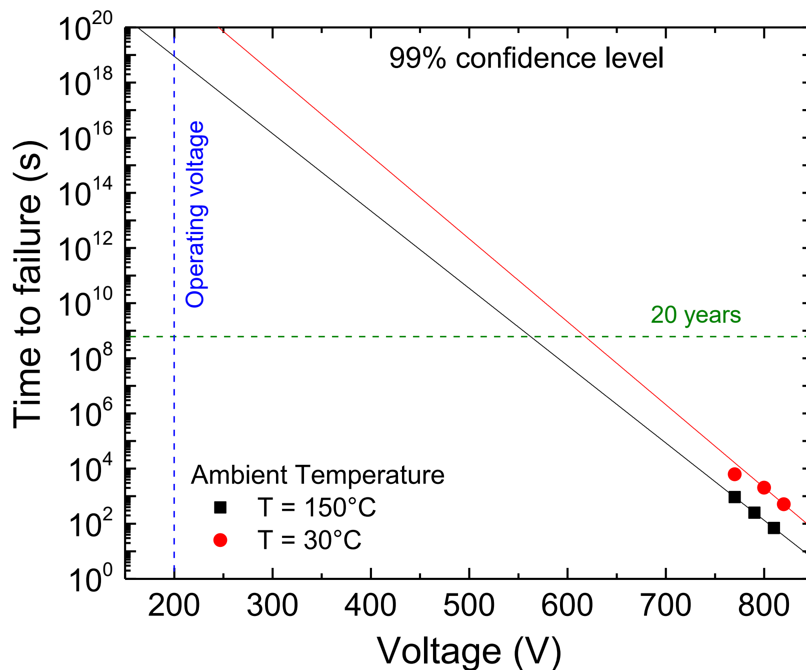


Figure 2.22 – Time to failure dependence on the drain voltage applied at ambient temperature of 30 °C and 150 °C. Each point represents the Weibull scale factor with a confidence level of 99%. Copyright © 2017, IEEE.

2.2.4 Electroluminescence (EL) and optical inspections

In order to collect more information on the physical origin of vertical breakdown, we investigated the EL pattern emitted by the devices during a step-stress test. This allows to investigate the presence of electroluminescence, and to identify the presence/position of the leakage paths responsible for breakdown. Figure 2.23 reports the false colour pattern of the electroluminescence measured during the stress experiment at three different drain voltages, namely 650 V, 850 V and 860 V. The stress/acquisition was changed accordingly, in order to avoid the saturation of the CCD camera. The EL patterns were taken under constant voltage conditions within a voltage step. The reason is that a stable voltage during a long exposure time is needed, due to the weak luminescence signal emitted by the devices. The leakage current monitored during the emission reveals results consistent to the step-stress analysis reported in the previous paragraph: for low drain voltage (V_D = 650 V) the current remains stable with a slight noise superimposed to the curve; at higher bias levels (V_D = 850 V, 860 V) the leakage current increases until the catastrophic failure occurs. The stress is applied in a 2-terminal configuration, between drain and substrate, by keeping the source and the gate terminal floating. As it can be noticed, a significant EL signal is detected all around the drain pad. Since the drain contact is ohmic, and since the field is applied vertically, we infer that the EL signal is emitted on the overall drain area, but visible only outside the thick drain metallization.

Failure occurs at random positions under the drain contact, either at the centre of the pad, or at the edges (see three representative examples in Figure 2.24). This suggests that failure is a random process.

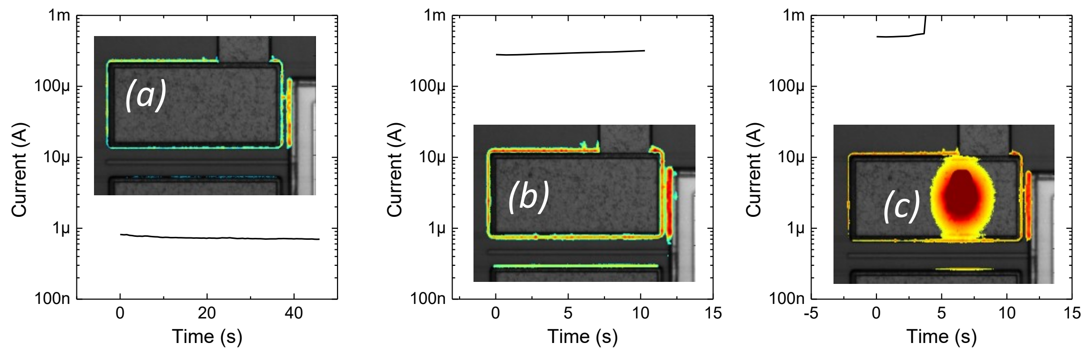


Figure 2.23 – Emission microscopy acquired at different drain bias levels, namely (a) V_D = 650 V, (b) V_D = 850 V, (c) V_D = 860 V (failure voltage). The EL pattern is reported along with the leakage current measured during the execution of the EL test (lasting few tens of seconds). Copyright © 2017, IEEE.

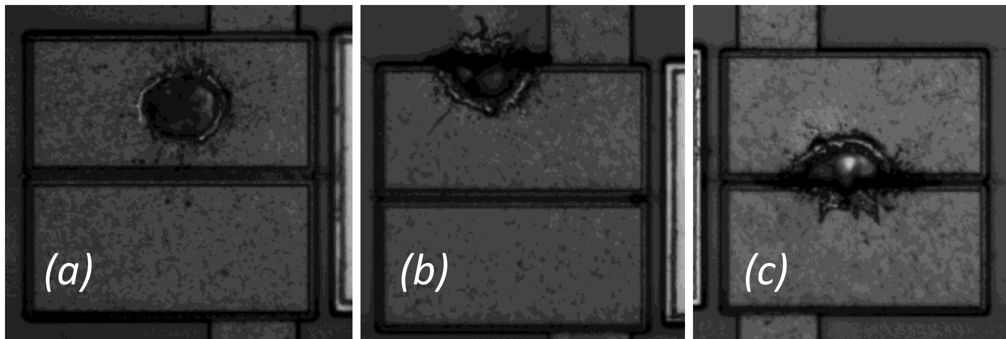


Figure 2.24 – photo taken after the catastrophic failure. Damage can be located: (a) in the middle of the drain pad; (b) at the edge of the gate pad; (c) in the edge of the drain pad next to the gate finger. Copyright © 2017, IEEE.

2.2.5 Outcomes of the analysis

As previously discussed, during a 2-terminal vertical stress, a high bias is applied between drain and substrate. Vertical leakage current flows mainly through dislocation-related paths [49], [50]; several works ascribe the conduction to the pure-screw dislocation [51], [52], but also a moderate bulk conduction is possible due to the non-ideal compensation of the buffer and the corresponding residual conductivity.

The deeply depleted buffer behaves as a leaky dielectric, and shows a time-dependent breakdown, similarly to what happens when dielectrics are subject to high electric field. The main difference between the TDDB of dielectrics and the process described within this chapter is that in the presented condition the failure is detected in a semiconductor (a wide bandgap semiconductor depleted) and not in an insulator. The results suggest that the breakdown could be facilitated in proximity of dislocations, where a higher (vertical) leakage might accelerate the defect generation process.

When the drain bias reaches 850 V, this voltage drops on the 3500 nm-thick buffer, resulting in an average electric field of 2.4 MV/cm (the breakdown field of GaN is 3.3 MV/cm). Under these conditions, two regions may be subject to a higher vertical field: (i) the AlN nucleation layer, that is located between the conductive silicon substrate and the AlGaN buffer, as was proposed in [43]; (ii) the undoped GaN channel layer that, due to the significantly low free charge density, is highly depleted at high drain voltages . We suggest that failure originates in one of these two regions: once a short circuit path is created through the GaN channel or the AlN layer, it propagates vertically thus leading to the creation of a shunt between the drain and the substrate. This process is promoted by the high electric field (consistently with the results in Figure 2.20 (b), while temperature has only a minor role in the degradation process (Figure 2.21 (b)).

2.3 Conclusions

This chapter presents a deep analysis on the reliability of the GaN-on-Silicon vertical stack. Growing gallium nitride on silicon substrates is the most suitable solution in order to reduce the costs thus allowing the power-semiconductor-market penetration of GaN-based devices.

In the first part of the chapter, the electrical behavior of three different structures obtained by stopping the epitaxial growth of a standard GaN-on-Silicon process at different stages was discussed, showing that both the thickness and the composition of the epitaxial stack, beside enhancing the breakdown voltage, improve the material quality by limiting the propagation of defects and dislocations. Furthermore, the critical electric field of the AlN nucleation layer grown on a silicon substrate was evaluated, and it results equal to 3.2 MV/cm. In addition, focusing on the Si/AlN sample, it has been showed that the nucleation layer presents a current driven wear-out process when submitted to a constant voltage stress, with Weibull-distributed times to failure, suggesting that the creation of a percolation process is the failure mechanism of the aluminum nitride layer.

In the second part of the chapter, the analysis was extended to a whole GaN-on-Silicon stack, showing that its degradation is time dependent, similar to the time-dependent breakdown of a dielectric material: TTF is Weibull distributed, with a shape factor greater than 1, indicating the existence of an intrinsic failure process. The failure mechanism is strongly field-dependent, and weakly thermally activated ($E_a < 0.25$ eV). The failure of the devices occurs due to the creation of a defect path (percolation path) between drain and substrate; the presence of defective leakage paths is confirmed by the electroluminescence analysis. The time-dependent failure is supposed to originate in the undoped GaN channel layer or in the AlN nucleation layer, due to a defect generation and percolation process enhanced by the electric field.

Chapter 3:

Doping of substrates for GaN-on-Si Growth

Part of the discussions, data and figures presented within this chapter have been previously published in:

M. Borga, M. Meneghini, S. Stoffels, X. Li, N. Posthuma, M. Van Hove, S. Decoutere, G. MEenghesso and E. Zanoni, "Impact of Substrate Resistivity on the Vertical Leakage, Breakdown, and Trapping in GaN-on-Si E-Mode HEMTs," in IEEE Transactions on Electron Devices, vol. 65, no. 7, pp. 2765-2770, July 2018. DOI: 10.1109/TED.2018.2830107 [53]

M. Borga, M. Meneghini, S. Stoffels, M. Van Hove, M. Zhao, X. Li, S. Decoutere, E. Zanoni, G. Meneghesso, "Impact of the substrate and buffer design on the performance of GaN on Si power HEMTs", Microelectronics Reliability, vol. 88–90, 2018, pp. 584-588, September 2018, DOI: 10.1016/j.microrel.2018.06.036 [54]

M. Borga, C. De Santi, S. Stoffels, B. Bakeroot, X. Li, M. Zhao, M. Van Hove, S. Decoutere, G. Meneghesso, M. Meneghini and E. Zanoni, "Modeling of the vertical leakage current in AlN/Si Heterojunctions for GaN Power Applications", under review.

3.1 The role of the substrate resistivity

The OFF-state losses of a transistor contribute to the efficiency drop of the power converter in which the device operates. One of the contributions to the device losses is the vertical leakage current, which needs to be minimized. Moreover, as discussed in Chapter 2:, the vertical leakage current can accelerate the defects generation which enhances the percolation process leading to the failure of the vertical stack.

In the following discussion the impact of growing GaN on differently doped silicon substrates is evaluated, taking into account both the vertical leakage related losses and the performance of the whole device.

3.1.1 Devices description

The devices tested within this activity are normally-off HEMTs based on an AlGaN/GaN heterostructure, with a p-type GaN gate (Figure 3.1). The active region is grown over a carbon doped GaN (C:GaN) layer that prevents punch-through effects. A 25x1.525 μm-thick superlattice is placed over the substrate in order to minimize the density of dislocations that propagate from the silicon substrate and AlN nucleation layer through the nitride-based semiconductor. Three silicon substrates were used for device fabrication, having increasing resistivity: $\rho = 0.01\ \Omega\cdot$cm, $\rho = 1\ \Omega\cdot$cm and $\rho = 6\ \Omega\cdot$cm. The substrates were boron-doped (p-type doping), where an increasing doping concentration results in a decreasing silicon resistivity.

The geometry of the devices is as follows: gate-drain length L_{GD}=10 μm, in order to avoid early lateral breakdown; gate width W_G=100 μm; gate-source distance is equal to L_{SG} = 0.75 μm.

The transition layers, the buffer and the devices geometry are optimized for 200 V operations. Nevertheless, within this work the devices are biased considerably beyond their nominal operating voltage, aiming to the study of the physical processes which affect the devices stability and reliability.

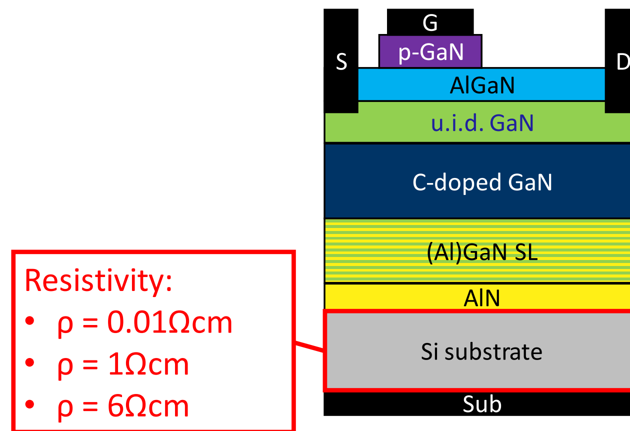


Figure 3.1 – Schematic cross section of the tested devices. Three doping levels were used for the substrates, so that the resistivity of the substrates varies from 0.01 Ω·cm (conductive silicon) to 6 Ω·cm.

3.1.2 Vertical leakage and EMMI analysis

To evaluate the impact of substrate resistivity on the vertical robustness and leakage current, we characterized the three wafers with different substrate resistivities by means of two terminal (drain-to-substrate) measurements (Figure 3.2).

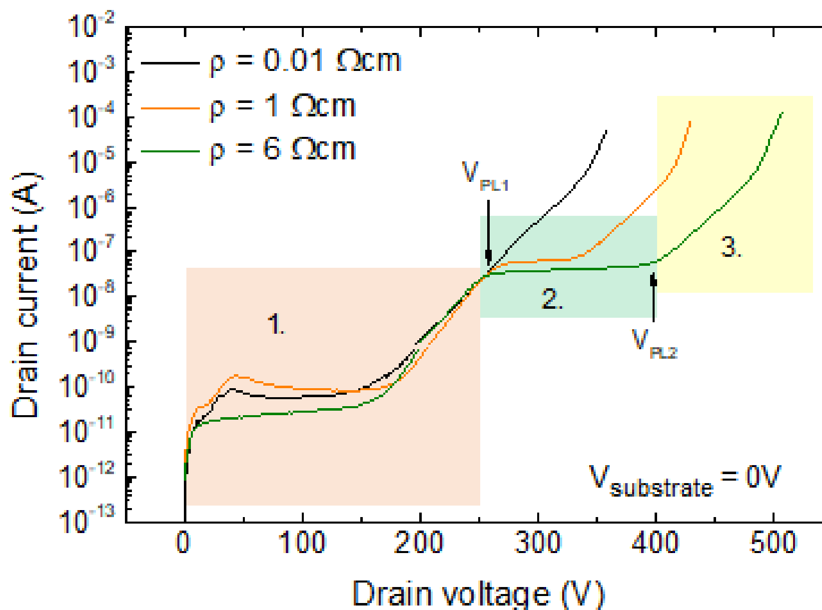


Figure 3.2 – 2-terminal vertical leakage measured on three wafers with different resistivity of the p-type silicon substrate. A "plateau" is observed only in the wafers having higher substrate resistivity. Copyright © 2018, IEEE.

Three different regions can be identified in Figure 3.2: in region 1, the vertical leakage through the structure is controlled by the voltage drop on the GaN buffer, while the voltage drop on the silicon substrate is minimum. For this reason, all three wafers show identical behavior, regardless of substrate resistivity. In region 2, the I-V curves of the devices with resistive substrate (ρ =1 Ω·cm and ρ =6 Ω·cm) show a significant change

in slope. A plateau, i.e. a region in which the current is nearly constant with increasing voltage, can be identified. We ascribe this plateau to the partial depletion of the silicon substrate, and a tentative explanation on the origin of the observed leakage current behavior will follow.

As the drain-substrate voltage increases beyond a certain value (V_{PL1} in Figure 3.2), a space-charge region starts building up in the silicon substrate. As a consequence, the voltage on the GaN buffer stops increasing, and so does the vertical leakage current. In this voltage range, the silicon substrate acts as a parallel plate capacitor, and charge builds up across it. The plateau ends at voltage V_{PL2} (indicated in Figure 3.2 for the wafer with the highest substrate resistivity using a black line), and the vertical leakage recovers the initial slope. We ascribe the end of the plateau to the injection of electrons from the silicon substrate to the GaN buffer. Recent studies [26], [41] pointed out that at high drain bias an electron inversion region is generated at the AlN/Si interface (see Figure 3.3). When the vertical voltage exceeds V_{PL2}, electron injection from substrate to the GaN-buffer (through the AlN layer) may occur via trap-assisted tunneling. A few tens of volts before the catastrophic failure the current further increases (showing a change in the slope) probably due to avalanche process in the Si substrate.

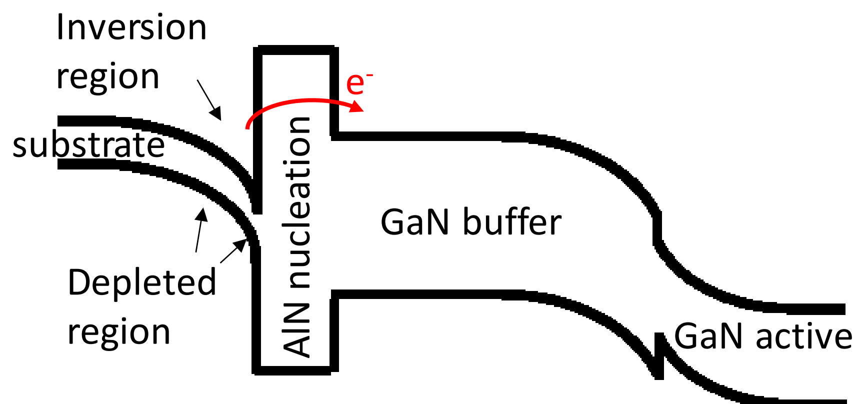


Figure 3.3 – schematic band diagram of the vertical stack, showing the depleted silicon substrate, and the generation of an inversion layer at the Si/AlN interface. Copyright © 2018, IEEE.

In order to better understand the origin of the "plateau" region, we carried out current-voltage-temperature characterization of the samples having the substrate with the highest resistivity. The results of this analysis (Figure 3.4) indicate the following: in region 1 ($V < 200$ V), leakage current increases with temperature due to the increase in conductivity of the buffer layer. In fact, at higher temperatures, conduction may be

favored by the increase in the free carrier density, and by the increase in the thermal energy of the carriers. The most interesting changes with temperature are noticed in the plateau region, i.e. between 250 V and 400 V. As can be noticed in Figure 3.4, with increasing temperature the voltage for the onset of the plateau (V_{PL1}) moves towards higher voltages.

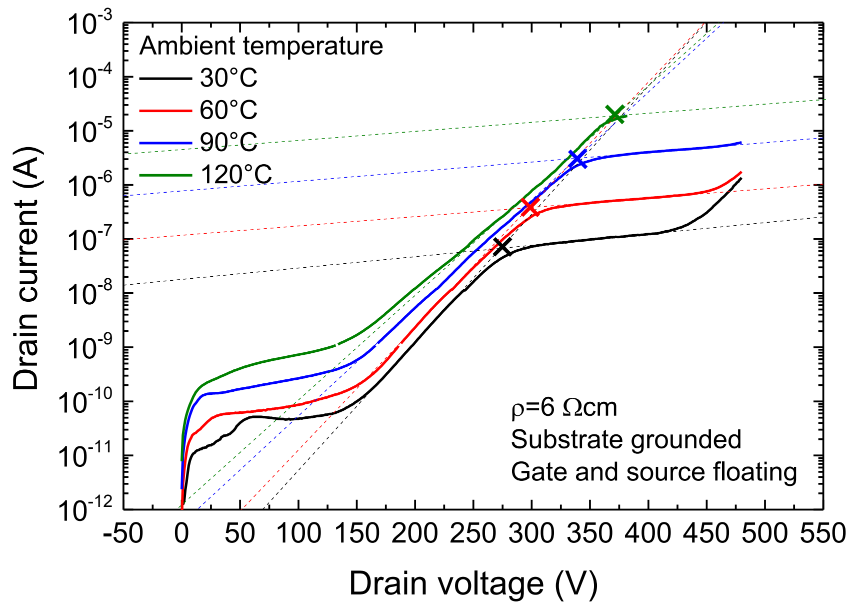


Figure 3.4 – 2-terminal vertical leakage current measured on the wafer with the highest substrate resistivity at different temperature levels. The voltage at which the plateau starts increases with temperature, consistently with a higher density of ionized doping in the buffer. Copyright © 2018, IEEE.

An estimate of the dependence of V_{PL1} on temperature was obtained by defining V_{PL1} as the x-coordinate of the intercept of the linear regression of the plateau region and the linear regression of the region where the current strongly increases, as shown in Figure 3.4. We found that V_{PL1} has an Arrhenius dependence on temperature, as shown in Figure 3.5, with an activation energy of 30 meV. This value is consistent with the ionization energy of p-type acceptors in the p-silicon substrate, thus supporting the hypothesis that the plateau could be related to the depletion of the substrate.

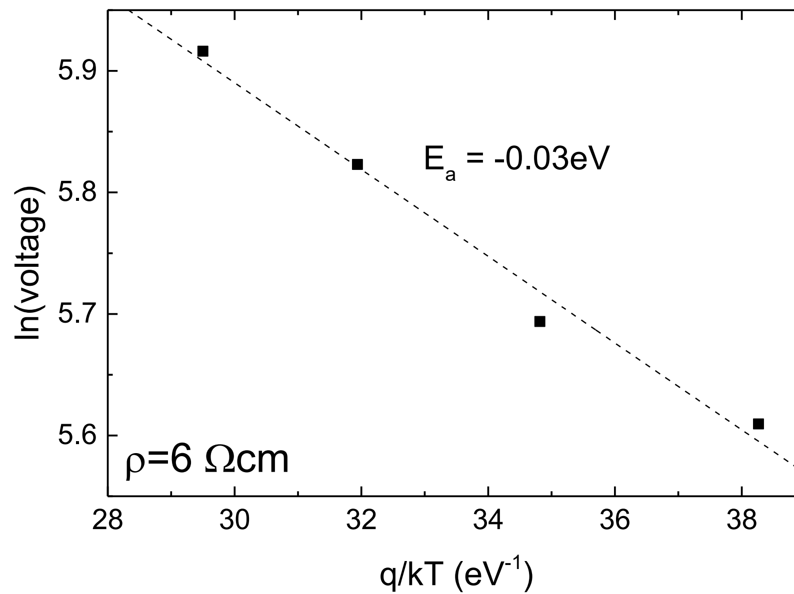


Figure 3.5 – Arrhenius plot of the voltage at which the plateau starts, with the corresponding activation energy. Copyright © 2018, IEEE.

In order to further investigate the origin of the plateau, an electroluminescence analysis was performed. We measured the dependence of the EL signal on drain-substrate voltage as follows: with substrate grounded, the drain voltage was increased from 0 V up to failure (step of 20 V every 120 s). During each step of the stress, an electroluminescence image was acquired with an exposure time of 10 s in order to avoid the saturation of the CCD sensor. Under high vertical bias, the electroluminescence signal originates from the flow of hot electrons within the GaN stack. The electrons injected from the substrate are accelerated by the high field across the GaN buffer [22]. The deceleration of such electrons (Bremsstrahlung) due to interaction with the lattice leads to the generation of a weak luminescence signal.

Figure 3.6 shows the current measured during the stair-case voltage sweep used for the EL characterization (thin solid line), along with the intensity of the EL signal collected from the sample (square dots). The inset of Figure 3.6 reports a micrograph of the drain pad, showing a false-color map of the luminescence signal. As can be noticed, during the EL measurements current shows the characteristic plateau at voltages between 250-300 V, consistently with the results in Figure 3.2 and Figure 3.4. A measurable EL signal starts being emitted at 200 V. Remarkably, also the EL signal shows a plateau for voltages higher than 250-300 V, exactly in the same voltage range as vertical leakage current. This is a further confirmation of the fact that within the plateau region,

the voltage drops on the GaN buffer (and the corresponding vertical leakage current) are constant. In fact, the intensity of luminescence depends on current (directly proportional to the number of hot electrons) and on the average energy of electrons (which is determined by the electric field). In the plateau, current is fixed, and an increase in voltage between drain and substrate does not lead to an increase in luminescence. This is explained by considering that during the plateau, the voltage across the GaN buffer stops increasing, while a considerable voltage drop starts building up across the silicon substrate. The EL signal starts increasing again once the end of the plateau is reached, since vertical leakage starts flowing again through the structure.

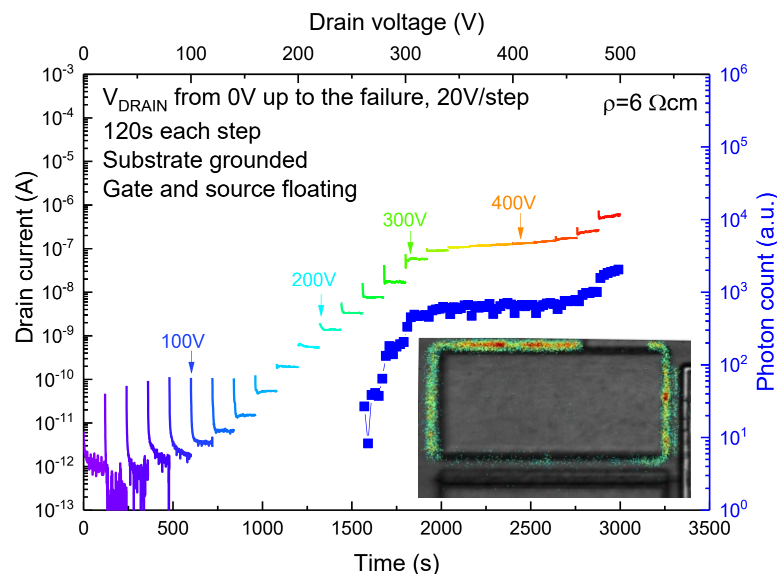


Figure 3.6 – comparison between drain current and EL signal during a step-stress experiment. EL signal has the same trend as drain current, indicating that when the plateau is reached, current and field stop increasing across the GaN buffer, and a significant depletion starts on the silicon substrate. (inset): false color EL pattern measured during a 2-terminal (drain-to-substrate) stress on one of the analyzed devices, at 480 V. EL signal is emitted under and around the drain contact, while the rest of device area is unaffected. Copyright © 2018, IEEE.

3.1.3 Step-stress test and evidence of Vth shift

In the previous sections (3.1.2) we have discussed the impact of substrate resistivity on breakdown voltage and vertical leakage of GaN-based transistors. In this section, we show that the use of a highly-resistive substrate may result in additional trapping processes that are not present in wafers with a low resistivity substrate. To evaluate these aspects, we executed a set of 4-terminal step-stress experiments. With source and gate grounded, the drain-to-substrate bias was increased by 20 V every 120 s, and the corresponding leakage current was measured. After each stage of the step-

stress experiments, we carried out a full characterization of the electrical properties of the transistors, to identify the changes in the electrical properties induced by stress. Representative results obtained on wafers with different substrate resistivity are reported in Figure 3.7. Figure 3.7 (a) reports the drain-to-substrate current measured during stress, while Figure 3.7 (b) reports the variation in threshold voltage induced by stress. The curve related to the wafer with a low resistivity substrate (black line in Figure 3.7) shows: the lower breakdown voltage (consistently with the results in Figure 3.2), no plateau above 250 V, and no shift in threshold voltage after each step of the stress. On the other hand, the devices with resistive substrate show: higher breakdown voltage, a significant plateau (i.e. a stress voltage range where current is constant during stress), and a considerable shift in threshold voltage induced by stress.

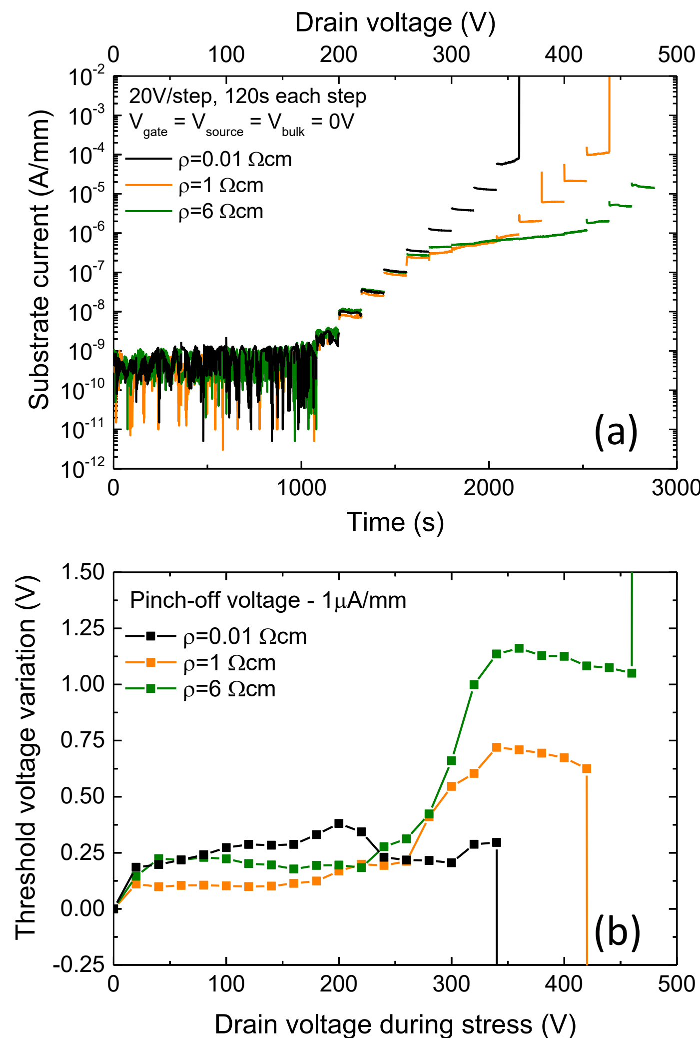


Figure 3.7 – results of step-stress experiments carried out on wafers with different resistivity of the p-type silicon substrate. (a) substrate current measured during the step-stress experiment. (b) variation in threshold voltage induced by stress. A significant threshold voltage shift is observed only on the wafers with highly resistive substrate. Copyright © 2018, IEEE.

Remarkably, the threshold variation occurs in correspondence of the plateau region (compare Figure 3.7 (a) and Figure 3.7 (b)). Since we ascribed the plateau region to the depletion of the Silicon/III-N junction, we suggest that the depletion of Si substrate leads also to the threshold voltage variation. We can explain this as follows: for stress voltage V_{STRESS} smaller than the onset of the plateau V_{PL1}, the voltage drops mostly on the GaN buffer, due to the depletion of the u.i.d-GaN/C-GaN junction. When V_{stress} is higher than the plateau onset V_{PL1}, the substrate starts depleting. As a consequence, the bottom of the buffer region moves to a positive potential, equal to $V_{STRESS}–V_{PL1}$. At the end of each stage of the step-stress experiment, the stress bias is removed, and the drain goes back to zero. Both junctions (silicon/III-N and u.i.d-GaN/C-GaN) are depleted: the u.i.d-GaN/C-GaN depletion region quickly recovers thanks to the high carrier availability in the active region. On the contrary, in the nucleation/superlattice layers the carrier's mobility is much lower due to the presence of several high-barrier heterojunctions. This causes a slow recovery (from the depletion) of the Silicon/III-N junction. It is worth noticing that during recovery, carrier supply may be provided also by the silicon substrate, through the AlN layer. Due to the low vertical leakage through the AlN layer, the space-charge-region in the substrate acts as a parallel-plate capacitor, charged at the voltage V_{STRESS}-V_{PL1} (in the range 100-200 V, depending on stress voltage). This means that when the drain bias goes to zero, the bottom of the buffer goes temporarily to a positive potential (around 100-200 V, depending on stress voltage). This brings to a positive voltage backgating effect, as shown schematically in Figure 3.8. A positive backgating potential may induce a significant buffer trapping [55], since the C-GaN/u.i.d-GaN diode (which behaves as a p/n junction) reaches a positive bias, and this leads to a significant electron injection into the C-doped buffer.

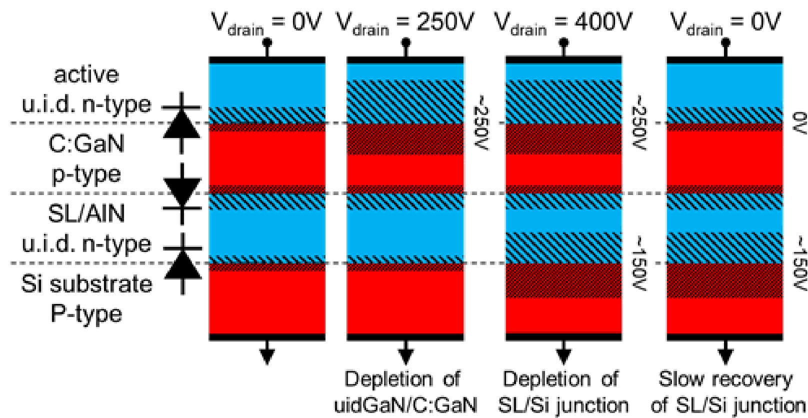


Figure 3.8 – schematic representation of the vertical stack interfaces in OFF-state condition with different drain voltages. At Vstress=250 V, the substrate starts depleting, and a space charge region is formed in the p-type substrate. For high stress voltages (e.g. 400 V) a considerable voltage drop appears across the depleted region of the p-type substrate. When the drain bias is brought back to zero (rightmost frame), the depleted region in the substrate acts as a parallel plate capacitor and – temporarily – keeps the voltage at the bottom of the buffer at a positive value (around 100-200 V). Such positive backgating effect leads to a significant threshold voltage shift. Copyright © 2018, IEEE.

3.1.4 Positive backgating transients

To confirm that a positive backgating can induce a significant charge trapping, we carried out a positive backgating ramp experiment. In this test, a HEMT is continuously biased in linear region, with a drain voltage of 1 V. At the same time, the substrate voltage is swept from 0 V to 200 V and backward to 0 V, with a ramp rate of about 25 V/s. Ideally, in absence of traps, a positive substrate bias would result in a slight and recoverable increase in 2DEG density, and this is consistent with the blue line (upwards sweep) in Figure 3.9 (inset).

Remarkably, the results shown in Figure 3.9 indicate that once a positive substrate potential higher than 150 V is reached, a significant charge trapping takes place. In fact, as the substrate bias returns to zero, drain current (and 2DEG resistivity) shows a strong decrease, which is ascribed to the trapping of electrons in the buffer (green line). Such trapping is induced by the exposure to positive substrate (and buffer) potential. It is worth noticing that the three wafers with different substrate behave in the very same way; in the following the experimental results obtained on wafer with substrate resistivity $\rho = 1\ \Omega\cdot\text{cm}$.

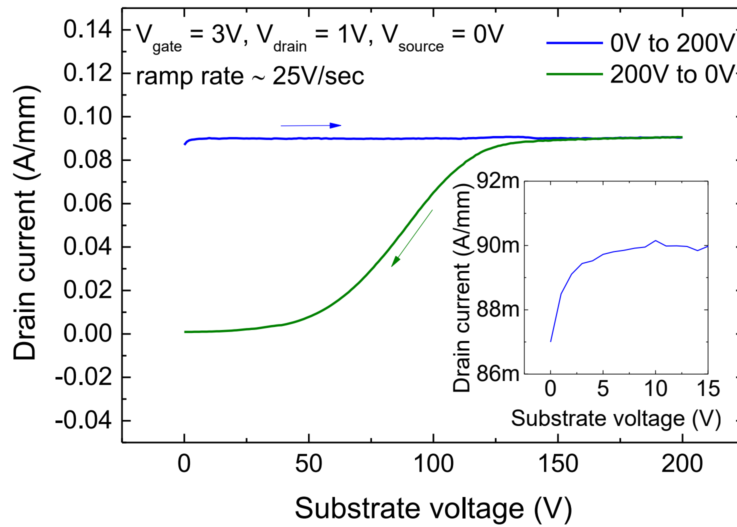


Figure 3.9 – drain current dependence on a positive substrate voltage sweep on a device fabricated on ρ = 1 Ω·cm substrate. A significant drop in current (hysteresis) is observed during the down-wards sweep, due to the trapping of electrons in the buffer induced by the positive backgating potential. The inset shows an enlarged view of the drain current during the upward sweep. Copyright © 2018, IEEE.

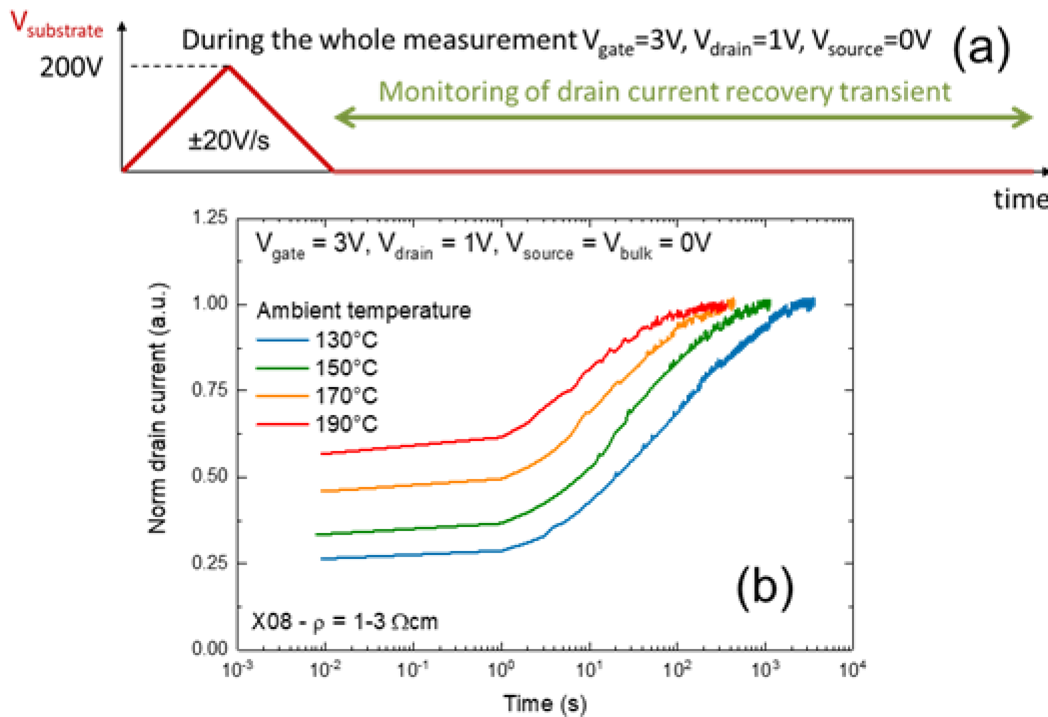


Figure 3.10 – (a) schematic representation of the measurement: positive backgating ramps induce trapping effects within the vertical stack that reduces the drain current. After the positive backgating, the recovery of the current is monitored during the time. (b) Recovery of the drain current over the time after a positive backgating ramp has been measured at different ambient temperature. Copyright © 2018, IEEE.

Temperature-dependent analysis was carried out to extract the activation energy of the defect filled by positive buffer potential. Specifically, we investigated the time-constant of the recovery from the trapped condition (induced by a positive substrate

ramp up to 200 V, 25 V/s), as a function of temperature. The results are shown in Figure 3.10, for one of the analyzed wafers. As can be noticed, once the positive substrate potential is removed, it takes a relatively long time (> 10 s) for the 2DEG conductivity to recover to the pristine value. The recovery (de-trapping) process is thermally activated, with activation energy in the range 0.5-0.66 eV (Figure 3.11). It is worth noticing that the three wafers with different substrate resistivities show a very similar behavior and Arrhenius plot (within process variability); this is consistent with the hypothesis that the charge trapping observed during positive backgating is related to buffer traps (which have – in a first order approximation – no dependence on substrate properties).

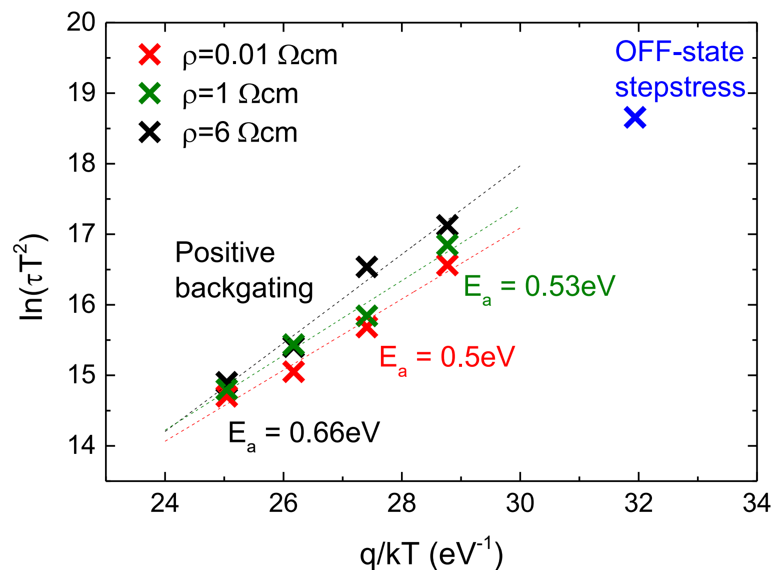


Figure 3.11 – Arrhenius plot of positive backgating and OFF-state recovery transients. The time constant of the trapping process induced by positive backgating and of the process induced by off-state stress are on the same Arrhenius plot, indicating the common physical origin. Copyright © 2018, IEEE.

In 3.1.3 we have demonstrated that a significant Vth shift is observed when the wafers with resistive substrate are stressed in the plateau region; we have ascribed this effect to the fact that when the drain bias is removed, the potential at the bottom of the buffer becomes temporarily positive (150-200 V), due to the depletion capacitance of the substrate. In section 3.1.4 we have demonstrated – by means of positive substrate ramps – that a positive back-bias can effectively lead to a significant buffer trapping. Now, we need to demonstrate that the trap states filled during the step-stress experiment are the same that are filled during the positive back-bias stress. To demonstrate this, we submitted a sample to a step-stress test; the final voltage was 440 V (well above V_{PL1}), in order to ensure a sufficient degradation and shift in Vth.

After reaching this trapping condition, both substrate and source potential were fixed at 0 V, and the transistor was biased in the linear region (V_{GS} = 3 V, V_{DS} = 1 V). The recovery of drain current (from the trapped condition to the fully recovered value) was measured (Figure 3.12), and the related time constant was extracted by fitting the recovery transient with a stretched exponential function [56] defined as:

$$I = I_0 + A_0 e^{-\left(\frac{t}{\tau}\right)^{\beta}}$$

As shown in Figure 3.11 the time constant of the recovery from step-stress is perfectly aligned (in the Arrhenius plot) with the time-constant of the recovery from positive backgating stress. This result supports the hypothesis on the role of positive buffer potential in the degradation of the devices: both OFF-state and positive backgating recovery are driven by the same detrapping process.

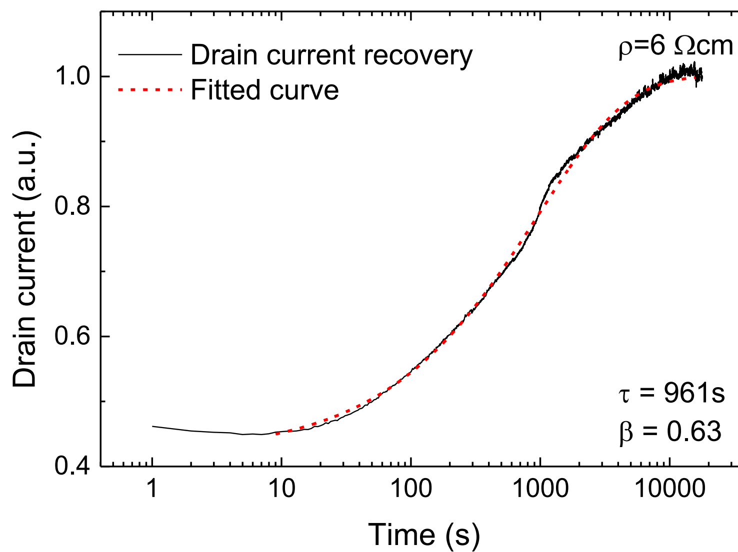


Figure 3.12 – Drain current recovery after a step stress up to 440 V. After the sample was step-stressed up to 440 V, the recovery of drain current (in the linear region) was monitored for several hours. Copyright © 2018, IEEE.

The band diagram in different bias condition is shown in Figure 3.13: (a) zero-bias condition; (b) plateau condition ($V_{DRAIN} > V_{PL1}$); (c) zero-bias after a drain bias higher than V_{PL1} is applied and substrate depletion occurs; (d) positive backgating bias. It is worth noticing that in Figure 3.13 (c) and Figure 3.13 (d) the band condition of the active/buffer junction is very similar, and the injection of electrons from the active region (n-type) to the buffer can occur easily.

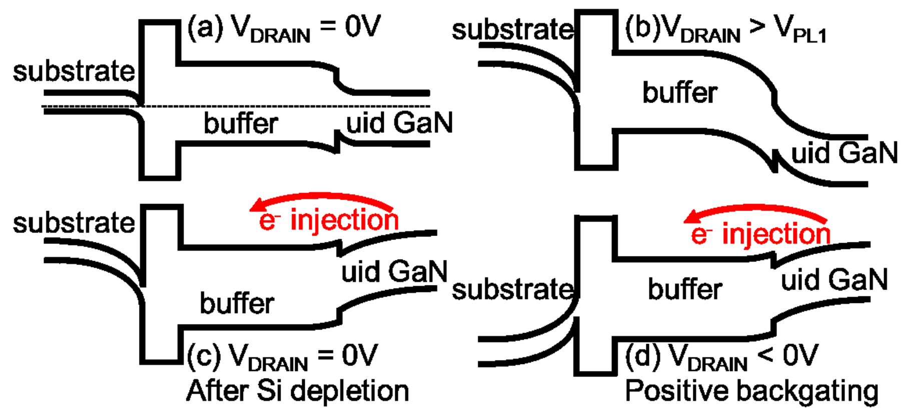


Figure 3.13 – Band diagrams of the vertical stack in different bias conditions. Charge injection from the active region to the buffer has been highlighted. Copyright © 2018, IEEE.

3.2 TCAD analysis on AlN/Si junction

In 3.1 the impact of the substrate resistivity on the device's performance was studied. A trade-off between the vertical stack robustness and the device stability has been pointed out. Moreover, the cause of the plateau region as well as the origin of the Vth shift were hypothesized to be the related to the depletion of the substrate.

Since the plateau region was also observed in the current-voltage characteristic of a sample composed by only the AlN nucleation layer grown over a p-doped highly resistive silicon substrate [57], a set of TCAD simulations on a Si/AlN structure was carried out in order to understand the origin of the observed phenomenon. In this section the results of these simulations will be shown and discussed, and a two-diodes model will be proposed.

3.2.1 Details on the measured and simulated structures

The characterized test structure consists of a 200 nm AlN layer grown by means of metalorganic chemical vapor deposition (MOCVD) on a lowly p-doped (~ 10^{15} cm^{-3}) 6 inches silicon substrate. The metal contact on the AlN consists of a Ti/Al/Mo/Au stack, with thicknesses of 30/60/35/50 nm, respectively. The area of the metal contact on the top of the AlN is 1.5 mm^2. Further details on the devices and on their fabrication can be found in [57]. The electrical characterization has been carried out by means of a Keysight B1505, by biasing a metallic contact on the AlN layer and keeping the substrate grounded.

The Technology Computer-Aided Design (TCAD) simulations have been performed with Sentaurus Device by Synopsys. The simulated structure was composed of a 200 nm AlN layer over a 5 μm thick silicon substrate. The thickness of the silicon has been considerably reduced in the simulated structures in order to minimize the computational load of the simulations; in any case, since in the worst case all the applied voltage drops within the first 2-3 μm from the interface, this does not affect the accuracy of the results.

The unintentionally doped nature of the AlN layer was taken into account by lightly n-doping the AlN layer. Charge density and distribution were calculated according to Fermi statistics, while generation and recombination rates were modeled

by thermal process. In order to consider both the impact of the defectivity of the materials near the interface and the effect of Al in-diffusions, a Shockley-Read-Hall (SRH) generation process was activated in a thin layer (100 nm) in the silicon close to the material interface, where the defect concentration is higher. In the silicon substrate, an avalanche generation process was taken into account as well. The electron injection rate from the substrate into the AlN was obtained by both thermionic emission over the potential barrier and direct non-local tunneling. The effective tunneling mass considered is $0.4 \cdot m_0$ [58] where m_0 is the electron's rest mass.

3.2.2 Two-diodes model

The measured I-V curve of the p-Si/AlN heterojunction is shown in Figure 3.14. As can be noticed, the increase in vertical leakage is interrupted by the presence of a plateau. As will be discussed below, and consistent with previous reports [57], [58], such a plateau originates from a partial depletion of the substrate. Understanding and modeling the origin of this plateau is of fundamental importance for the development of high voltage GaN devices. Some earlier descriptions have been presented on p-Si/AlN junctions [57], [58]; we build upon these previous studies, by proposing an alternative approach based on a two-diodes model, by demonstrating its validity, and by reporting the simulated band diagrams. The solid-red line in Figure 3.14, i.e. the simulation result, closely fits the current behavior of the real device (dashed-black line), reproducing the plateau region.

In order to match the measured current level, the conduction band offset at the AlN/Si heterojunction has been set to 1.08 eV, in good agreement with previous papers in literature (see for instance [58], [59]).

Due to the intrinsic polar property of AlN, the interface between Si and AlN is characterized by a positive fixed charge. This latter attracts electrons from the bulk silicon substrate toward the material interface. The high conduction band offset prevents electrons to be injected into the AlN through a thermionic emission process and forces the electrons to be confined in a triangular potential well, thus forming a sheet of charges (inversion layer) close to the junction in the p-Si.

A good understanding of the physical origin of the observed plateau can be obtained by looking at the schematic band diagram of the simulated structure shown in

the inset of Figure 3.14. An inversion layer in the Silicon at the Si/AlN interface acts as a source of electrons that are injected into the AlN layer [26], [40]. In absence of interface traps, the tunneling path is a straight line from the inversion layer to the conduction band of the AlN (iso-energetic process), whose length is defined, in the following discussion, as "tunneling distance".

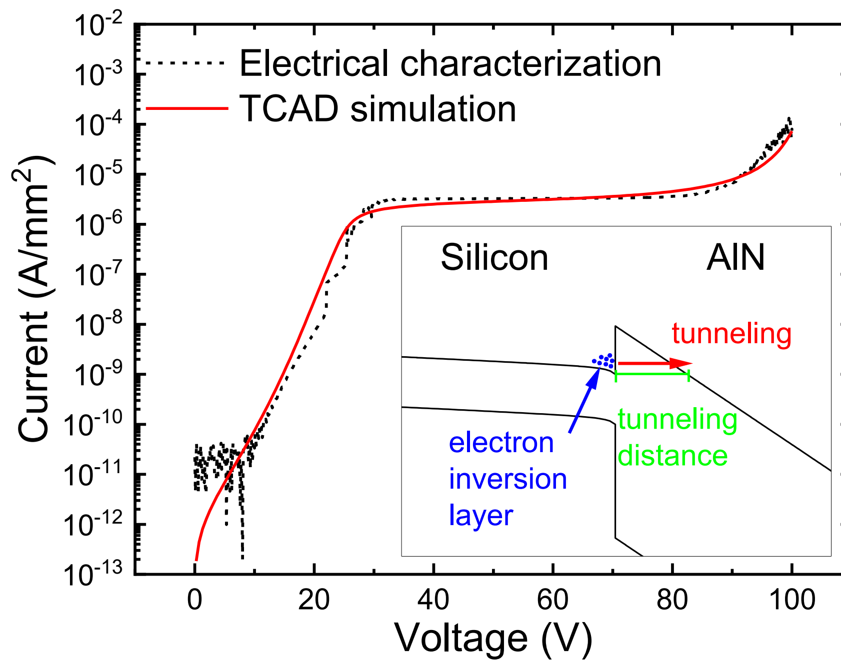


Figure 3.14 – Comparison between electrical characterization (dashed-black line) and TCAD simulation (solid-red line) of an AlN/p-Silicon junction. A plateau region can be observed in both electrical characterization and TCAD simulation, in the voltage range 25 V – 90 V. Inset: schematic band diagram of the Si/AlN junction; electrons tunnel to AlN from an inversion layer that is formed in the silicon at the Si/AlN interface.

In order to better understand the contribution of each layer to the leakage of the whole structure and to investigate the origin of the plateau, we propose to model the high free-charge density in the inversion layer as a highly n-doped silicon layer, as shown in Figure 3.15. This allows an analysis based on a simple two-diode model, which is a series connection of:

- An n+-Si/AlN (Figure 3.15 (b)), that can be thought of as an AlN Schottky diode
- An n+-Si/p-Si (Figure 3.15 (c)), that is a simple n^+/p silicon diode.

The n^+-Si layer doping level is 10^{20} cm^{-3}, and it has been chosen based on the electron density of the inversion layer of the p-Si/AlN junction. Its thickness was set to

10 nm (only a few nm close to the junction are involved in the injection/diffusion process).

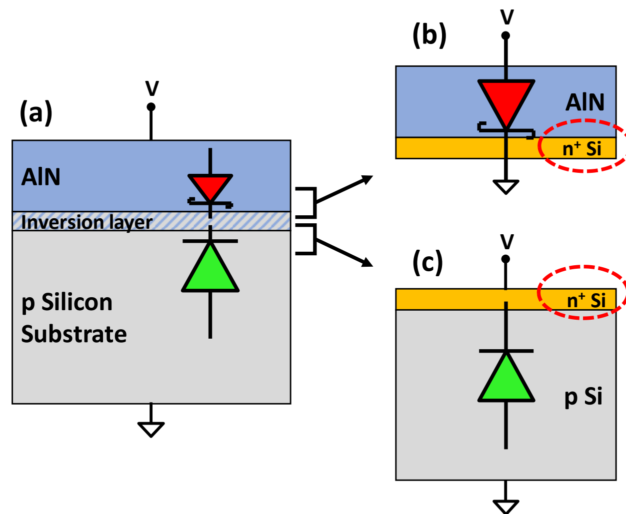


Figure 3.15 – (a) Structure of the measured AlN/p-Si junction. For modeling purposes, it can be decomposed in (b) an AlN/n+-Si junction that models the AlN layer and the electron inversion layer that originates in the silicon at the Si/AlN interface, and (c) a n+-p silicon diode that models the p-doped substrate and the inversion layer. The equivalent model diodes are shown in each part.

The first step is the simulation of the n^+-Si/AlN structure (Figure 3.15 (b)) whose I-V characteristic is the solid-green line in Figure 3.16 (a). The current through the structure originates from the electrons that move from the inversion layer towards the conduction band of the aluminum nitride by means of a tunneling process through a triangular potential barrier; such process may be enhanced by temperature (phonon-assisted tunneling). The tunneling probability, which strongly depends on the tunneling distance, increases as soon as the voltage drop on the aluminum nitride increases the band bending, thus bringing the conduction band edge closer to the inversion layer.

The high electron density in the inversion layer causes all the applied voltage to drop on the aluminum nitride, resulting in a monotonic and exponential increase in the current with the applied voltage (see Figure 3.16 (a) from 0 V to 30 V).

By comparing the I-V characteristic of the first diode (n+-Si/AlN, Figure 3.15 (b)) with that of the complete AlN/p-Si structure (Figure 3.15 (a)), it can be noticed that, in the voltage range 0 V-25 V, the two curves perfectly match (Figure 3.16 (a)). This proves that, in the low-voltage regime, the leakage current in the complete AlN/p-Si structure does not depend on the substrate characteristics but only on the tunneling barrier at the heterojunction, in agreement with [57].

The second diode in the proposed model is the n^+/p silicon diode (Figure 3.15 (c)), whose I-V characteristic is shown in Figure 3.16 (b) (solid-red line). Note that the I-V curve is shifted rightwards by 25 V, which is the onset voltage of the plateau region, in order to have a better comparison.

Two different regions can be identified:

- a lightly sloped region, between 25 V and 90 V
- a highly sloped region, above 90 V

Within the first region the current behavior is typical of a reverse biased p/n junction, where the current level weakly increases with the applied voltage. Under the applied conditions, the n^+/p junction is reversely biased, and there is a lack of free charges in the structure. Carriers can only be generated through a thermal generation process [58], possibly assisted by defects within the energy gap of the silicon. The latter can be native defects of the silicon as well as Al in-diffusion within the substrate, as reported in [60]. At higher voltages, the depletion region builds up within the weakly doped p-silicon, and the high electric field starts promoting avalanche generation in the substrate, thus causing a strong increase in the current through the structure (second slope, above 90 V).

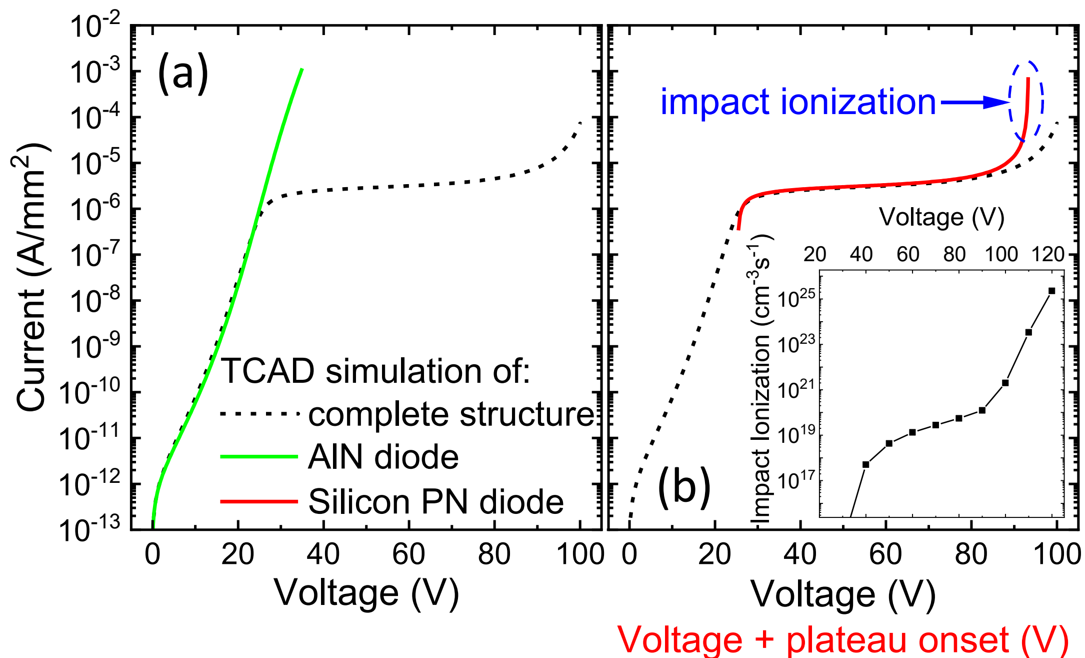


Figure 3.16 – (a) Simulated I-V characteristic of the complete AlN/p-Si junction (dashed-black line) and of the AlN/n+-Si structure (solid-red line). (b) simulated I-V characteristic of the complete AlN/p-Si junction (dashed-black line) and I-V characteristic of the n+-p silicon diode (solid-red line). The inset shows the impact ionization rate at the Si/AlN interface as a function of the applied voltage.

The presented analysis, carried out on the two diodes separately, clarifies the band diagram behavior of the complete AlN/p-Si structure shown in Figure 3.17 (a). In the low voltage regime (black lines), all the applied voltage drops on the AlN layer, causing the tunneling distance to decrease (Figure 3.17 (b)) and, consequently, the current level to increase.

As current reaches the reverse leakage current of the equivalent p/n$^+$ silicon diode, the substrate starts depleting (Figure 3.17 (a) – solid-red lines), whereas the voltage drop on the AlN gets pinned, and the tunneling distance stops decreasing (Figure 3.17 (b), red highlighted region).

Since the current of the series of two diodes is limited by the less conductive one, the total current remains almost constant despite the increasing voltage. For higher voltages (> 90 V), the avalanche generation process that takes place in the substrate, promoted by the electric field (Figure 3.17 (a) – blue lines), remarkably increases the conductivity of the substrate, thus leading the current through the complete AlN/p-Si structure to be limited again by the tunneling injection from the inversion layer into the AlN. At this stage, the voltage drop in the AlN starts increasing again whereas the tunneling length decreases (Figure 3.17 (b), blue highlighted region), enhancing the tunneling process.

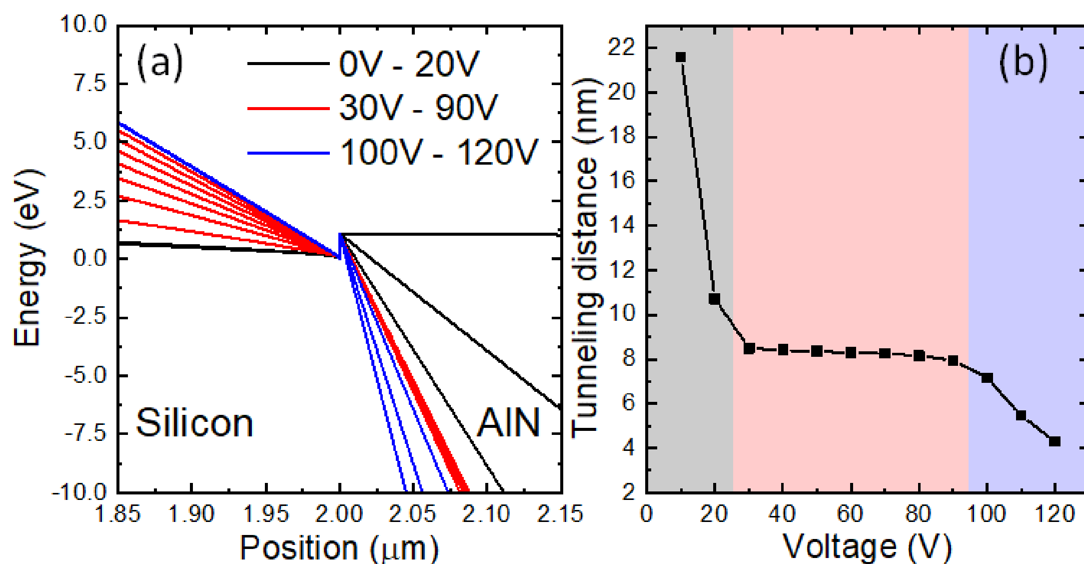


Figure 3.17 – (a) Conduction band of the Si/AlN junction; all the curves were shifted in order to have the same energy reference at the interface. (b) tunneling distance (as defined in Figure 3.14) as a function of the applied voltage.

The accuracy of the 2-diodes model proposed was proven by comparing the results with those obtained by a TCAD simulation of the complete structure (Figure 3.18). By combining the I-V characteristics that result from the TCAD simulation of the two sub-structures separately, we obtained a leakage current curve that perfectly matches the simulated I-V characteristic of the AlN/substrate complete structure.

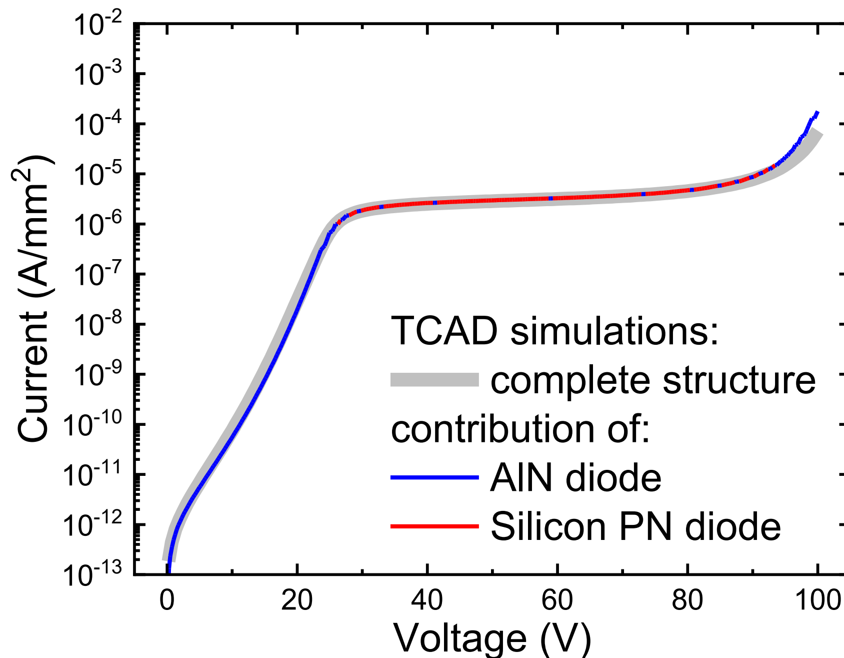


Figure 3.18 – Simulated I-V characteristic of the complete AlN/p-Si junction (light gray line). (red/blue line) combination of the simulated current of the two diodes composing the equivalent model. The combination of the two separate simulations closely represents the I-V characteristic of the full simulation.

3.2.3 Temperature and Si-doping dependences

In order to further validate the presented model, the analysis was extended to higher temperatures, as shown in Figure 3.19 (a). As the temperature increases, the current related to the tunneling injection through the potential barrier (0 V – 20 V) increases, while the slope decreases due to the lower dependence of the injection on the field (as observed in [58]). In the previous discussion, we showed that the current within the plateau region is limited by the reverse leakage of the equivalent p/n junction; the temperature, by increasing the generation rate in the space charge region, causes the increasing of the current level of the plateau. Finally, it can also be noticed that the plateau length increases with the increasing temperature. This can be ascribed to the higher electric field needed for the impact ionization to start generating at higher temperatures. The impact of the ambient temperature predicted by the proposed two

diodes model, is also qualitatively in agreement with the experimental results obtained characterizing a full GaN-on-Si vertical stack (Figure 3.4).

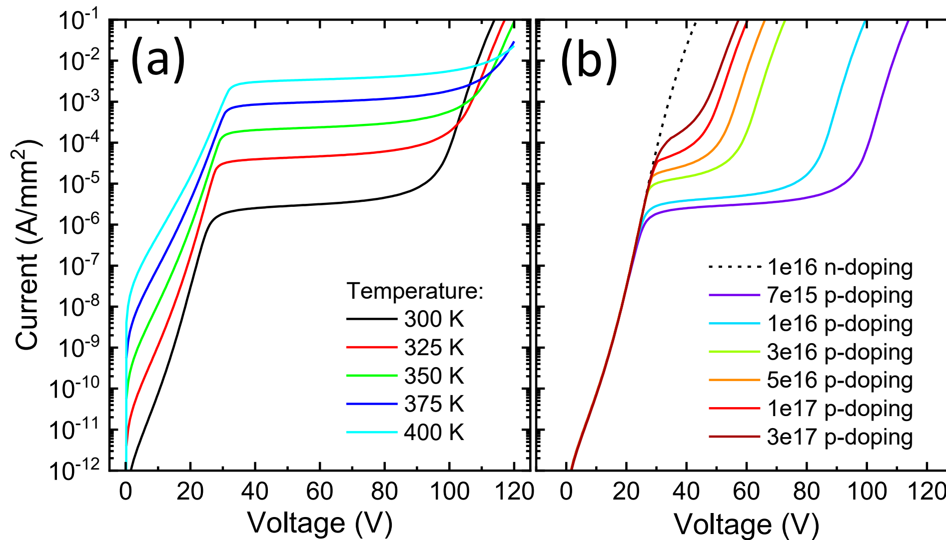


Figure 3.19 – Figure 6: (a) Simulated IV characteristic of the complete AlN/p-Si junction at different temperatures. (b) Simulated IV characteristics of the complete AlN/Si junction with an n-doped silicon substrate (dashed line), and differently p-doped silicon substrate (solid lines).

The presented model is also compatible with the results shown in literature on the impact of the substrate resistivity on the current of a AlN/ Silicon junction ([57], [58]).

In p-doped silicon substrates, as the doping density increases, the avalanche generation takes place at lower voltages, due to the intrinsically higher electric field within the silicon. This limits the length of the plateau region (solid line – Figure 3.19 (b)), because the avalanche generation prevents the equivalent n+/p diode from limiting the current through the whole structure.

In the case of an n-doped silicon substrate, there is no inversion layer at the interface but an accumulation layer; this causes the absence of an equivalent p/n junction on the substrate that limits the current through the structure. This results in the absence of the plateau region if an n-doped substrate is used, as shown by the dashed line in Figure 3.19 (b).

3.2.4 Extension to a full GaN-on-Silicon stack

In order to demonstrate that the presented model, which ascribes the plateau region to the depletion of the substrate and describes the origin of the substrate depletion, is valid also in a GaN-on-silicon stack, a TCAD simulation on a complex

structure shown in the inset of Figure 3.20 has been carried out. The simulated structure is based on the very same Si/AlN junction previously studied. Over the AlN layer, a 500 nm thick $Al_{25}Ga_{75}N$ layer, a 3 μm thick carbon doped (10^{15} cm^{-3}) GaN layer and a 300 nm thick u.i.d GaN layer are placed. Figure 3.20 shows the current-voltage characteristic of the simulated vertical stack. It is worth noticing that the current shows a plateau region even if a complex stack is grown over the Si/AlN junction. The role of the thick epitaxial stack is to limit the voltage drop in the Si/AlN junction, thus bringing the onset of the plateau region toward higher voltages. Nevertheless, once the substrate depletes and limits the current thorough the structure, the onset of the impact ionization is needed in order to allow the current to start increasing again. The substrate depletion within the plateau region is also demonstrated by the inset in Figure 3.20 showing the conduction band of the structure. At voltages lower than the plateau onset, all the applied potential drops on the epitaxial layers. For voltages higher than the plateau (dark-orange and red symbols in the IV shown in Figure 3.20), the conduction band of the silicon bends, as highlighted by the black arrow, thus indicating the substrate depletion.

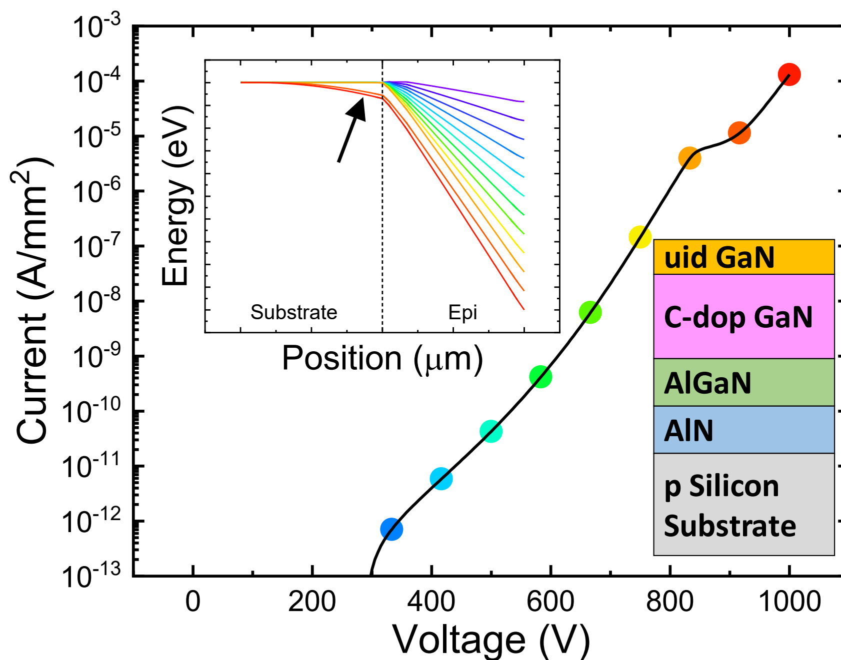


Figure 3.20 – Simulated IV characteristic of a complex epitaxial stack grown on a lowly p-type doped silicon substrate. The schematic representation of the simulated structure is shown in the inset on the bottom-right side of the figure. The inset on the top-left side shows the behavior of the conduction band as a function of the applied voltage; as highlighted by the black arrow, it is worth noticing that the substrate depletes in the last two bias conditions, which are above the onset voltage of the plateau (dark-orange and red dots in the IV curve).

3.3 Conclusions

In this chapter the impact of the substrate resistivity on the vertical leakage and on the stability of lateral AlGaN/GaN HEMTs grown on silicon was evaluated.

We demonstrate that – thanks to the presence of a plateau region in the vertical I-V curves – the wafers with higher silicon resistivity show the highest breakdown voltage. The existence of the plateau is ascribed to the build-up of a depleted region in the silicon substrate, where a part of the drain-source voltage drops thus limiting the voltage dropping on the GaN buffer stack.

Furthermore, we demonstrate that the wafers with high substrate resistivity suffer from additional trapping effects with respect to those with low resistivity. A significant threshold voltage shift is observed when the devices are stressed in the plateau region. Such shift is ascribed to the fact that – at high drain voltages – a considerable voltage-drop (in the range 150-200 V) falls on the depleted Si substrate. Once the stress bias is removed, such voltage-drop leads to positive backgating effects which, in turn, results in the injection of electrons towards the buffer. By monitoring the drain current recovery after a positive backgating bias is applied on the substrate, we demonstrated that the origin of the Vth shift observed during step-stress is the same as in positive backgating, and we provided information on the properties of the related traps. As a general conclusion, we can state that the use of highly resistive substrate can improve the breakdown robustness; however, this happens at the expense of Vth stability. A trade-off must be considered, if resistive substrates are used for fabricating GaN power transistors.

Within the second part of the chapter, we presented a novel 2-diode model that describes the behavior of the current through a junction composed of an AlN layer and a lightly p-doped silicon substrate. Modelling the inversion layer that is placed at the material interface as a highly n-doped silicon layer, we were able to split the structure in two sub-junctions: (i) a Schottky-like n+-Si/AlN diode and (ii) a p/n^+ silicon diode.

The current through the whole structure is driven by the tunneling injection from the inversion layer into the AlN, which intensifies as the voltage drop on the AlN increases. This process lasts until the depletion of the substrate occurs: this limits the

current through the whole structure and generates a plateau region. As soon as the voltage drop on the substrate is sufficiently high, an avalanche generation process increases the conductivity of the substrate, causing the total current to be limited again by the tunneling process.

Chapter 4:

GaN-based trench gate MOS devices

4.1 Devices description

In this chapter an extensive analysis on the trench gate of (semi-) vertical transistors will be presented. As discussed in the introduction, vertical GaN-based devices aim to high voltage application, overcoming issues related to the area consumption and to the surface effects which affect lateral devices. Since the development of vertical GaN devices is on its early stages, there is a lot of room for improvement and optimization of the devices, as well as for the understanding of the electrical behavior and for the definition of new experimental approaches.

There are several architectures of vertical transistors proposed in literature, the tested devices can be introduced describing the following four features:

- **GaN-on-Silicon**: the GaN-based active layers which are involved in the normal operation of the devices are grown over a silicon substrate and several AlGaN-based transition layers, which allow the strain/relief stress management and ensure a good material quality in the active layers.
- **Semi-vertical**: due to the GaN-on-Silicon growth, a fully vertical architecture is impossible to be developed. For this reason, a semi-vertical architecture is preferred. A highly doped n^+ layer, which represents the bottom of the active region of the device, was integrated in the epitaxial stack; a deep-via routes back to the surface the current that flows the n^+ layer. This solution allows the fabrication of low-voltage vertical devices (due to the limited epi thickness, which can be easily improved by using thicker homo-grown GaN) in a large area wafers, thus reducing the costs of the development of this new technology.
- **MIS**: the gate module is based on a Metal-Insulator-Semiconductor system. The channel of the transistors is formed by biasing the gate metal up to the inversion of the p-doped semiconductor. The OFF-state condition is obtained by depleting the semiconductor close to the gate contact.
- **Trench gate**: in a vertical transistor the current flows in a vertical path from the top toward the bottom of the semiconductor stack. This imply that the

channel must lie in a vertical plane, and so the gate MIS structure. This condition is achieved by etching a trench in the semiconductor and by depositing sequentially the gate insulator and the gate metallization over the trench.

A schematic cross section of the epitaxial stack is depicted in Figure 4.1. Over a 200 mm silicon substrate, a nucleation layer and a complex (Al)GaN-based transition layers are grown. The aim of the transition layers is to accommodate the mechanical stress that originates during the growth-process (especially during the cooling-down phase) due to the thermal mismatch between the materials. These layers improve the performance of the final devices, by limiting the dislocation density on the GaN active region, which is composed by a n^+ layer, a lowly-doped n layer, a 400 nm p-doped layer and a 250 nm n^+ layer.

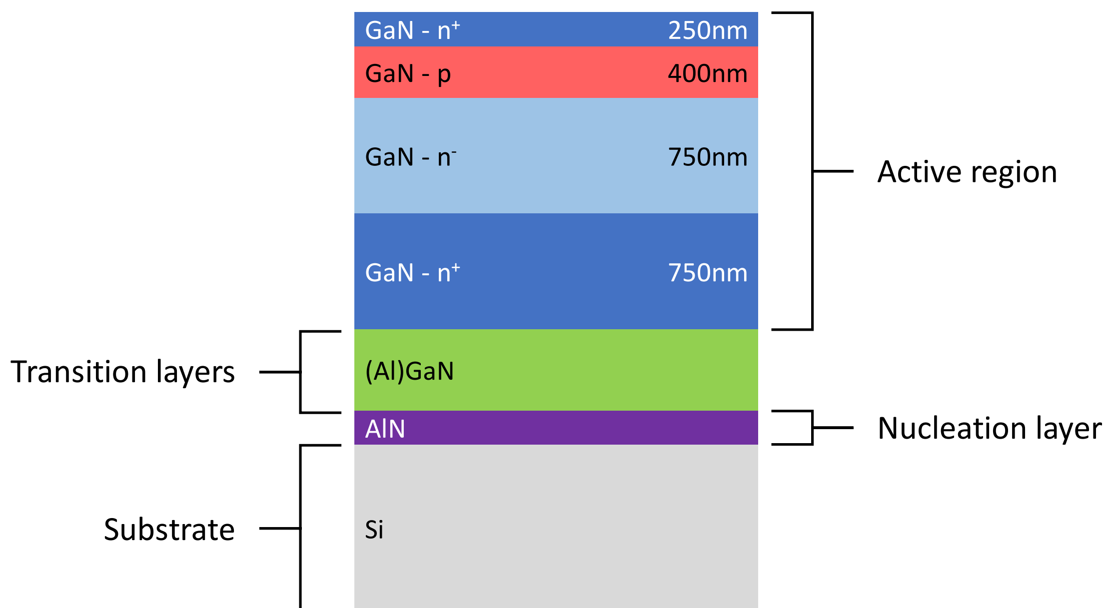


Figure 4.1 – schematic representation of the epitaxial stack. The specified thicknesses are the reference for the tested devices; nevertheless, some variations on these parameters might be discussed in the following.

Each layer of the active region plays a role during the normal operations of the final device, thus further insight on these four layers will follow.

The 750 nm-thick n^+ GaN layer grown over the stress-compensation layers, is crucial to achieve a functioning semi-vertical configuration; in fact, this layer is responsible to route laterally the carriers from the bottom of the drift region toward the actual location of the drain ohmic contact (deep-via). In this layer the GaN is doped with

a concentration of Silicon shallow donor atoms higher than $3 \cdot 10^{18}$ cm^{-3}, essential to guarantee both a high conductivity and a good ohmic drain contact.

On the other hand, the 750 nm lowly n-doped GaN, will be the drift region of the final device. This latter deeply depletes during the OFF-state condition, allowing the electric field to spread uniformly within a wide bulky region of semiconductor. The doping level of this layer is crucial for the OFF-state robustness of the final device, and it needs to be as low as possible; the samples studied in the following analysis have a silicon doped drift region, with a doping density in the order of 10^{16} cm^{-3}.

The p-doped layer is the body of the final device. This means that the inversion region, i.e. the channel of the MOS, is formed within this layer. The doping level strongly affects either the threshold voltage and the carrier's mobility within the channel; the higher the doping level, the higher the threshold but the lower the carrier mobility. The tested devices have a Mg-doped GaN, with a density about 10^{19} cm^{-3}. The thickness of the p-doped layer corresponds to the transistor channel length. It is worth noticing that this latter does not depend on the processing mask set but it only depends on the epitaxial structure; this means that all the devices processed in the same wafer have the same channel length.

The top n^+ layer is highly Si-doped (density between $3 \cdot 10^{18}$ cm^{-3} and $5 \cdot 10^{18}$ cm^{-3}), and it is the source access region of the devices. The high doping level is needed for ensuring a lowly resistive path between the source contact and the channel.

Basing on the described epitaxial stack the semi-vertical trench-gate MOS transistors are fabricated. Figure 4.2 shows either the schematic cross section of the active layers and the top view of the tested devices. The typical values of the geometrical parameter of the tested devices are summarized in the Table 4.1. The active area of the device is enclosed by an isolation. The drain module consists of a deep-via filled by a metal which forms an ohmic contact with the highly doped n^+ buried layer; the current, after flowing through the drift region, and laterally through the n^+ layer, is routed back to the surface by means of the drain deep-via metal. The source metallization lies between two gate trenches in the middle of the active region, and it is electrically connected with both the n^+ layer (source contact) and to the p-layer. It is processed by

etching the surface down to the p-layer, ensuring a stable body potential (grounded) during the normal operation of the device.

The gate module is the more complex, and it is fabricated by etching the gate trench until penetrating the drift region. Over the trenched area the gate dielectric is deposited. Even though the reference dielectric material is a 2.5 nm Al_2O_3 / 35 nm SiO_2 bilayer, different dielectric materials are evaluated and compared, including the aluminum oxide Al_2O_3. The Gate metal deposited over the dielectric allows the control of the gate potential, thus changing the condition of the semiconductor close to the dielectric (accumulation / depletion / inversion). It is worth noticing that the trench sidewalls are not exactly vertical (as depicted in Figure 4.2), but they form an angle of ~ 20° with the vertical plane (measured by XSEM inspection after the etching).

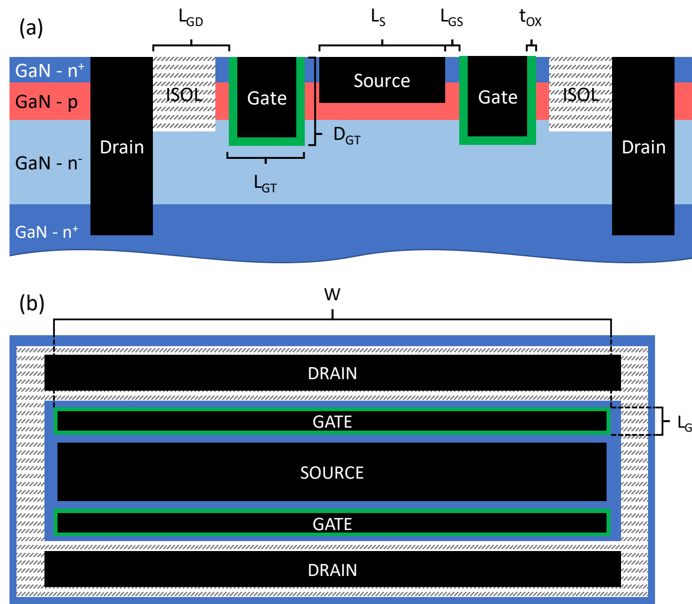


Figure 4.2 – schematic representation of both the (a) cross section and the (b) top view of the tested devices.

Label	Description	Typical value
W	Gate width	100 µm / 500 µm
L_{GD}	Gate-Drain length	16 µm
L_{GS}	Gate-Source length	1 µm
L_S	Source Length	10 µm
L_{GT}	Gate trench length	4 µm
D_{GT}	Gate trench depth	950 nm
t_{OX}	Dielectric thickness	35 nm / 2.5 nm+35 nm

Table 4.1 – Description of the dimensions specified in Figure 4.2 and summary of the typical values.

4.2 Gate transport mechanisms

The characterization of the gate leakage is useful to evaluate both the losses of the devices and the stability and reliability of the gate dielectric. Moreover, some insight on the device operation can be obtained.

In this section the gate leakage behavior as a function of the gate voltage will be discussed. Different measurement configurations will be presented, and the experimental results will be deeply analyzed in order to understand the transport mechanisms behind the observed behavior. Moreover, the gate leakage is characterized on several devices processed with four different gate dielectrics, and the failure electric field is evaluated for each technology.

4.2.1 Gate-Source, Gate-Drain and OFF-state characterization

The gate leakage current as a function of the gate voltage was measured by means of a Keysight B1505 equipped with a High-Power Source-Measurement Unit (HP-SMU) and a High-Voltage SMU (HV-SMU). The gate voltage was swept from 0 V up to the failure of the gate stack in both forward and reverse polarization, and in two different configurations (Figure 4.3), which are source grounded and drain floating (GS), and source floating and drain grounded (GD). The test was carried out on 8 samples for each connection and bias condition.

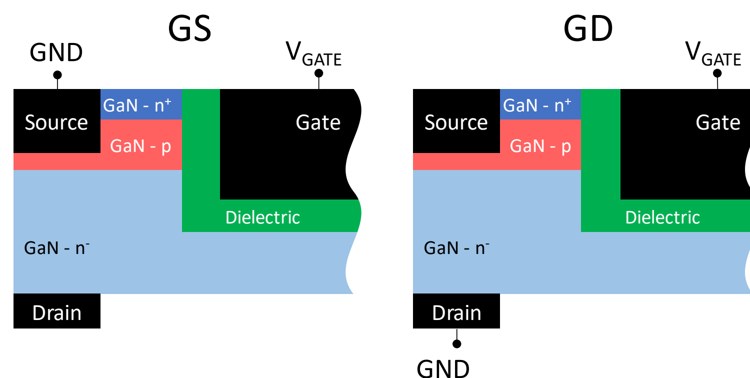


Figure 4.3 – connection configurations tested for the investigation of the gate leakage. On the left the GS configuration, where the gate leakage toward the source contact is probed; on the right the GD configuration, where the gate to drain leakage is measured.

By biasing the gate terminal, the condition of the semiconductor close to the dielectric changes according to the bias polarity. If the gate bias tends to attract the

majority charge carriers, an accumulation layer is formed at the GaN-dielectric interface; on the other hand, if the gate potential repels the majority charge carriers, the semiconductor depletes and, for an increasing bias, an inversion channel is formed.

When the gate is forward biased, in both n^+ and n^- GaN regions an accumulation layer is formed close to the dielectric, while the p-GaN layer is instead brought into depletion regime, as shown in Figure 4.4.

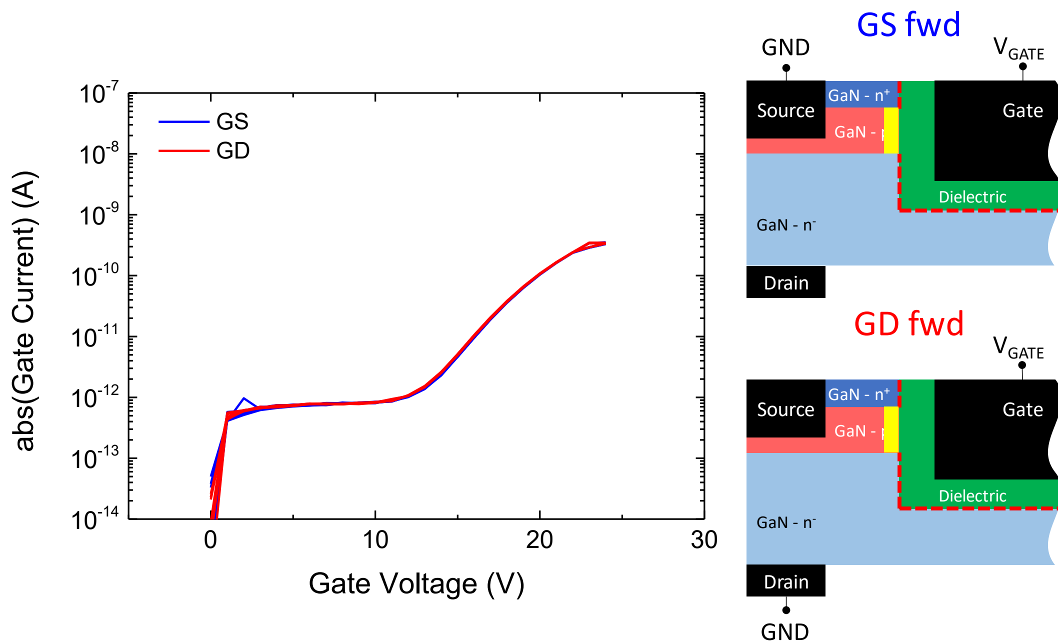


Figure 4.4 – (left) Gate-Source (blue line) and Gate-Drain (red line) behavior with the applied gate voltage. (right) schematic representation of the device biased in forward gate condition: the n-type GaN is in accumulation close to the dielectric (red dashed line), while the p-doped GaN is in depletion regime (yellow).

It is worth noticing that the behavior of the gate current is the same in the GS and GD configuration. Qualitatively, this can be ascribed to the presence of a n-type semiconductor in accumulation regime which routes the carriers toward the grounded contact. Once the accumulation channel is formed (weak potential needed, especially in the n^+ layer), all the applied potential drops on the dielectric, which is thus included between the gate metal and a sheet of electrons and starts leaking due to the increasing electric field. Even if the injection mechanisms from the gate into the semiconductor will be object of future studies, two conduction regimes can be identified: at relatively low gate voltages the leakage current weakly increases with the temperature, whereas a second conduction mechanism appears around 15 V and causes the current to increase with the applied voltage up to the failure of the devices.

Concerning the current levels measured in the GS and GD configurations, it can be observed that the curves are exactly overlapped, even if the areas of the n^+ and n^- interfaces with the dielectric are considerably different. This behavior is still under investigation, and a possible explanation is discussed in the following. When the gate bias increases above the threshold voltage of the device, the whole gate dielectric is included between the gate metal and a highly conductive sheet of electrons. This latter originates from the accumulation channel in the n-doped regions (both n^+ and n^-) and from the inversion channel in the p-doped region. Consequently, independently on the measurement configuration, at gate biases higher than the threshold voltage, the carriers are injected from the gate metal into the sheet of electrons that surrounds the trench; this latter routes the current toward the semiconductor region connected to the ground, i.e. n^+ and n^- respectively in the GS and GD configuration, as depicted in Figure 4.5.

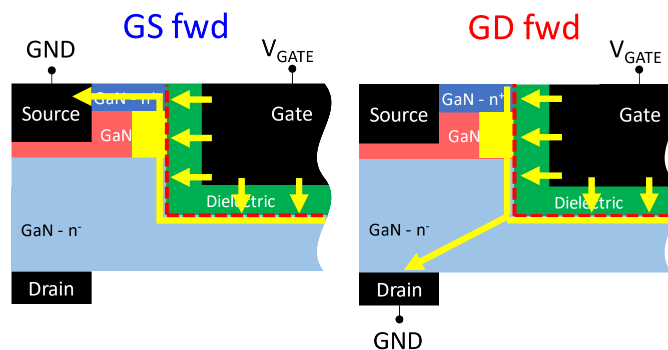


Figure 4.5 – schematic representation of the gate leakage current path in both GS and GD configurations under forward gate bias.

A similar analysis on the gate leakage current is carried out on both GS and GD configurations at reverse gate bias. Negative voltage on the gate terminal brings the n-doped GaN into depletion regime, while the p-doped GaN goes into accumulation, and a sheet of free holes is created in the region close to the dielectric.

The GS configuration current (Figure 4.6 - blue line) has a similar double-slope behavior than the current in forward bias condition. An accumulation layer is formed in the p-doped GaN at the dielectric interface, and all the applied gate bias drops on the dielectric, which starts leaking up to its failure.

On the other hand, the gate leakage measured in the GD configuration (Figure 4.6 - red line) slowly increases with the applied gate voltage and the dielectric breakdown occurs at about -45 V, without showing a high-slope current region. In order to

understand the process which limits the gate current in the GD configuration, the gate leakage is measured by sweeping the drain voltage toward positive biases while keeping the gate grounded (same condition than gate-drain reverse bias). During the drain voltage sweep the source potential was measured, as well as the drain current.

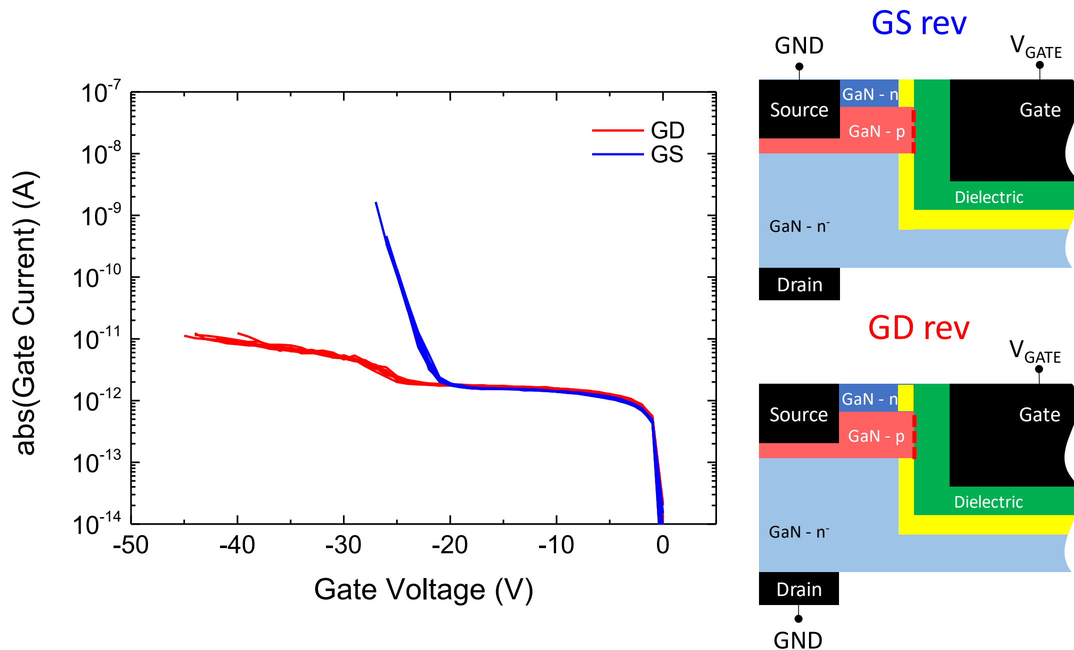


Figure 4.6 – (left) Gate-Source (blue line) and Gate-Drain (red line) behavior with the applied gate voltage. (right) schematic representation of the device biased in reverse gate condition: the p-type GaN is in accumulation close to the dielectric (red dashed line), while the n-doped GaN is in depletion regime (yellow).

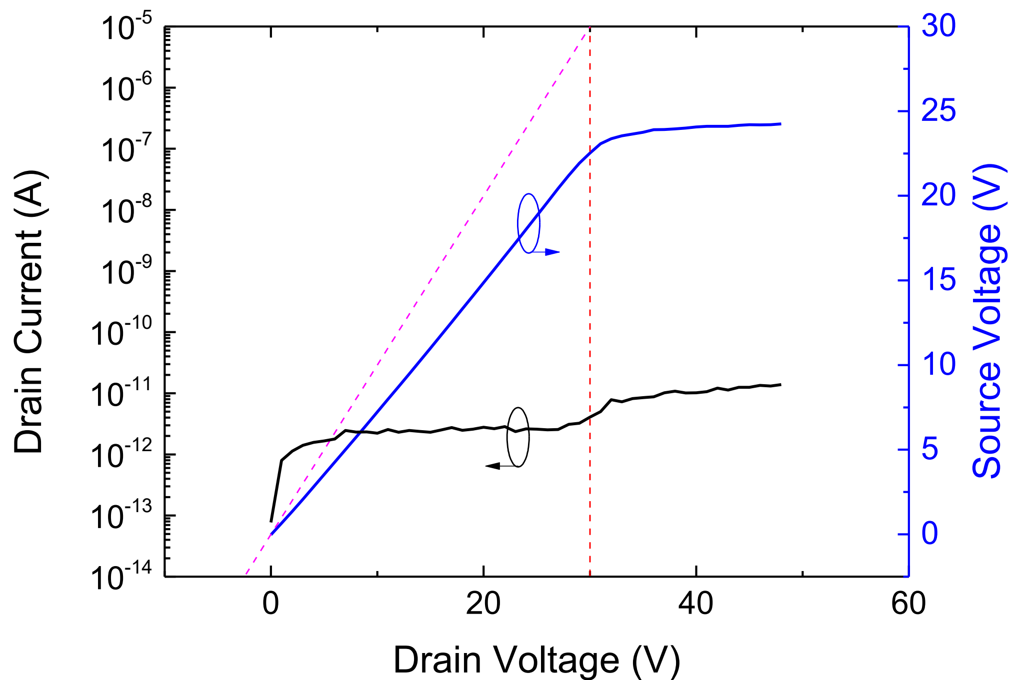


Figure 4.7 – Drain current and Source voltage in a reverse biased Gate-Drain measurement. X-axis represents the increasing positive drain voltage, while the gate was kept to 0 V. Left Y-axis shows the drain current, which shows the same behavior than the GD reverse current in Figure 4.6. Right Y-axis shows the source potential during the drain voltage sweep.

Figure 4.7 shows the drain current and the source voltage during the reverse biased GD measurement. The vertical dashed red line defines two different regimes characterized by a different dependence of both the current and the source voltage on the applied drain voltage. In particular, the drain current shows a hump in the transition between the two regimes. On the lower voltage regime, on the left-side of the red dashed line in Figure 4.7, the drain current slightly increases with the applied drain voltage, and its level is close to the GS current (see Figure 4.6); in this voltage range the source voltage increases with the drain voltage, meaning that almost all the applied voltage drops on the gate dielectric. This suggests that, in this voltage range, the GD current is limited by the leakage through the gate dielectric. For higher drain voltages, the source voltage becomes almost constant regardless the increasing drain bias; this indicates that the applied drain voltage starts dropping on the reversed biased p/n$^-$ junction instead of on the gate dielectric. The drain current in this region weakly increases with the drain bias.

The presented measurement highlights the presence of a series-connection-like conduction. In the lower-voltage regime, the current is limited by the gate dielectric, and

all the applied voltage drops on it. When the gate dielectric becomes leaky and its current becomes higher than the current of the reverse biased p/n⁻ junction, this latter starts depleting, and most of the applied drain voltage drops on it.

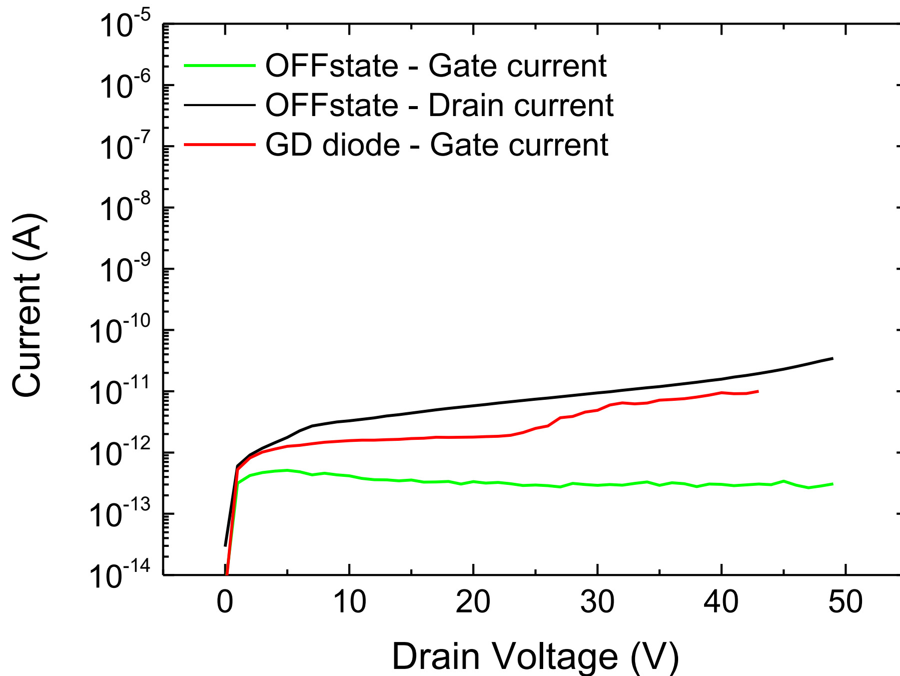


Figure 4.8 – OFF-state drain leakage (black line) and reverse biased GD diode (red line) measured up to the failure of the device. Green line represents the gate leakage during the OFF-state sweep.

The described process can be demonstrated also comparing the drain leakage in the reversed bias GD configuration with the drain leakage in OFF-state condition. When the device is kept in OFF-state condition, both gate and source are biased to 0 V, while the drain bias is higher than 0 V; in this condition the drain leakage current flows through the reverse biased p/n^- junction, while the gate leakage is considerably low, due to the low voltage drop on the dielectric (both gate and source are grounded). Figure 4.8 shows that the drain current of the reverse biased GD diode at $V_D > 30$ V, which was supposed to be limited by the p/n^- junction, is considerably close to the OFF-state drain current, thus proving that the limiting conduction mechanism is the same in the two measurement configurations.

The discussed experimental tests indicate that the reverse biased gate-drain leakage measured with the source floating mainly flows through the side of the gate trench and through the p/n^- junction. To further demonstrate the presented model,

devices with different p/n$^-$ junction area are characterized. The diode area scaling is obtained by measuring device with different gate-source distance L_{GS} (Figure 4.2).

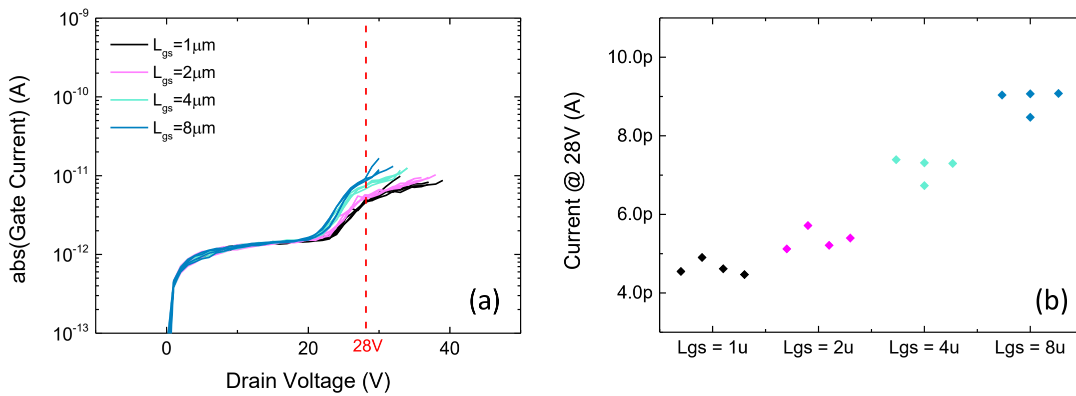


Figure 4.9 – (a) reverse biased GD leakage of devices with different L_{GS} length, thus different p/n$^-$ junction area. (b) reverse biased GD leakage current at 28 V as a function of the gate-source length L_{GS}.

Figure 4.9 shows a clear linear trend of the reverse biased GD current with the increasing p/n$^-$ junction area. This proves that the current flows indeed through the side of the gate trench and successively through the p/n$^-$ junction. On the other hand, for drain voltages lower than 20 V (i.e. gate reverse voltages more negative than -20 V), there is no dependence of the gate-drain current on the diode area, thus indicating that the current in this voltage range is not limited by the p/n$^-$ junction but on the gate dielectric, as previously discussed.

4.2.2 Gate dielectrics comparison

The same gate leakage and robustness analysis performed in the devices with Al_2O_3 / SiO_2 bilayer gate dielectric, is carried out also in devices with different gate dielectric material, which are 35 nm thick aluminum oxide (Al_2O_3), 35 nm thick aluminum oxynitride (ALON), and a 2.5 nm thick ALON / 35 nm thick SiO_2 bilayer.

The gate leakage is measured in the two GS and GD configurations previously described, with both positive gate voltages (forward bias) and negative gate voltages (reverse bias). Several devices are measured for each gate dielectric, so that also the repeatability of the measurement is evaluated. The gate voltage is swept up to the failure of the device, so that also a robustness analysis can be performed.

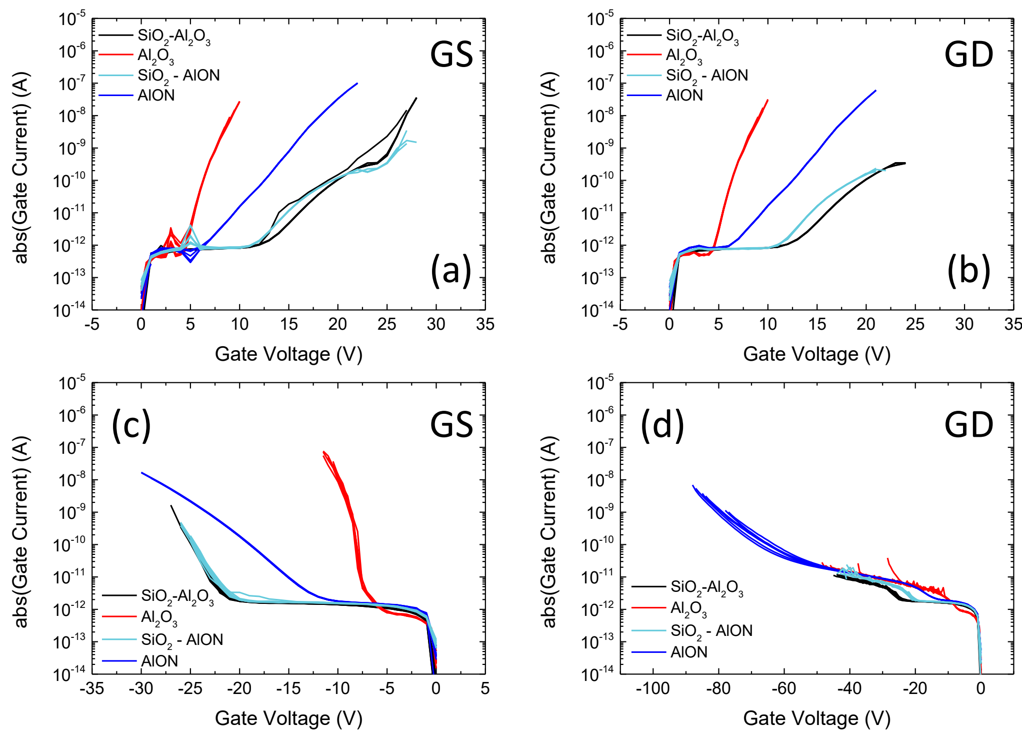


Figure 4.10 – Gate leakage current measured in GS (a, c) and GD configuration (b, d), at both forward (a, b) and reverse (c, d) biases.

The general behavior of the gate leakage current with different dielectrics in the four measurement configurations (shown in Figure 4.10) is in line with the previous analysis performed on the Al_2O_3 / SiO_2 bilayer devices. Nevertheless, focusing on Figure 4.10 (a, b, c), both the onset and the slope of the leakage current and the failure voltage of the gate stack strongly depend on the dielectric material. It is worth noticing that the two set of devices with a 35 nm thick SiO_2 result in a comparable behavior in all the measurement configurations of both the gate leakage current and the gate robustness, independently on the material of the 2.5 nm thick dielectric interface layer (Al_2O_3 or ALON). Moreover, the Al_2O_3 is the dielectric which results in earlier onset of the high-slope current region among the four tested solutions and in a consequent lower robustness.

Focusing on Figure 4.10 (d), which shows the reverse bias leakage measured in the GD configuration, it can be noticed that, independently on the gate dielectric, the current behaves as discussed in the previous paragraph, showing two conduction regimes with a current-hump in between. The current level within the first conduction regime, which occurs in the voltage range between 0 V and the current hump, as well as the gate voltage

where the hump occurs, depends on the gate dielectric used. On the other hand, the current level and behavior in the second conduction regime (at gate voltages more negative than the hump voltage), does not depend on the gate dielectric, thus confirming the previous analysis which ascribed the current after the hump to the p/n^- junction; this latter is indeed almost identical in the four tested devices set.

The presented gate leakage measurements allow also to preliminary evaluate the robustness of the different gate dielectrics, and to compare them. The results are summarized in Figure 4.11. For each gate dielectric, the devices show a similar failure voltage when stressed in GD forward bias, GS reverse bias and GS forward bias configurations. As previously discussed, in these three measurement configurations an accumulation layer is formed either in the p-doped layer or in the n^+-doped layer; consequently, the gate dielectric is included between the gate metal and a free-charge layer, which can be assumed to behave like a conductor. In this condition all the applied voltage drops on the gate dielectric, which catastrophically breaks when its critical electric field is reached. On the other hand, the reverse biased GD configuration results in a higher robustness, which is comparable to the OFF-state robustness of the devices. As discussed in the previous paragraph, in both reverse biased GD and OFF-state measurement, the n^- drift region gets depleted, and the electric field distribution within the device is comparable: recent studies ascribe the OFF-state failure of the trench gate MOS devices to the crowding of the electric field around the trench corners.

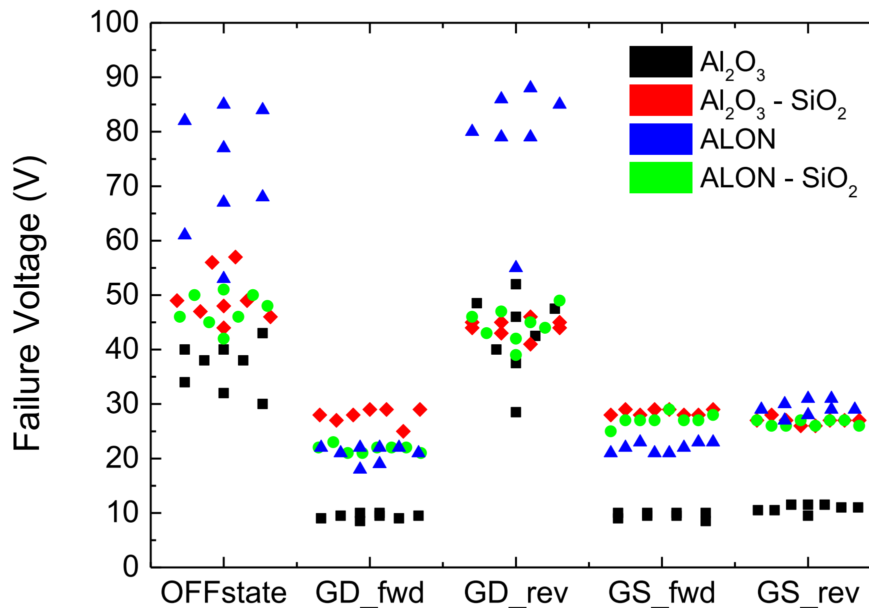


Figure 4.11 – Failure voltage of the devices measured in five different configurations: OFF-state, GD forward bias, GD reverse bias, GS forward bias and GS reverse bias. Several devices are tested for each gate dielectric.

Lastly, it is worth noticing that the devices with ALON gate dielectric have a higher failure voltage in both OFF-state and reverse biased GD configurations with respect to the other tested dielectrics. An OFF-state breakdown measurement carried out in a device with ALON gate dielectric (Figure 4.12) reveals that the gate dielectric does not show an instantaneous catastrophic failure as the electric field reaches a critical value, but a gradual increase of the leakage current occurs; this latter, which possibly flows at the trench corner where the electric filed has a maximum, preserves the dielectric from the abrupt failure by mitigating the electric field within the material. Due to the local nature of the process, which depends on the quality of the dielectric where the electric field peaks, there is a considerably high device-to-device variability in the failure voltage distribution.

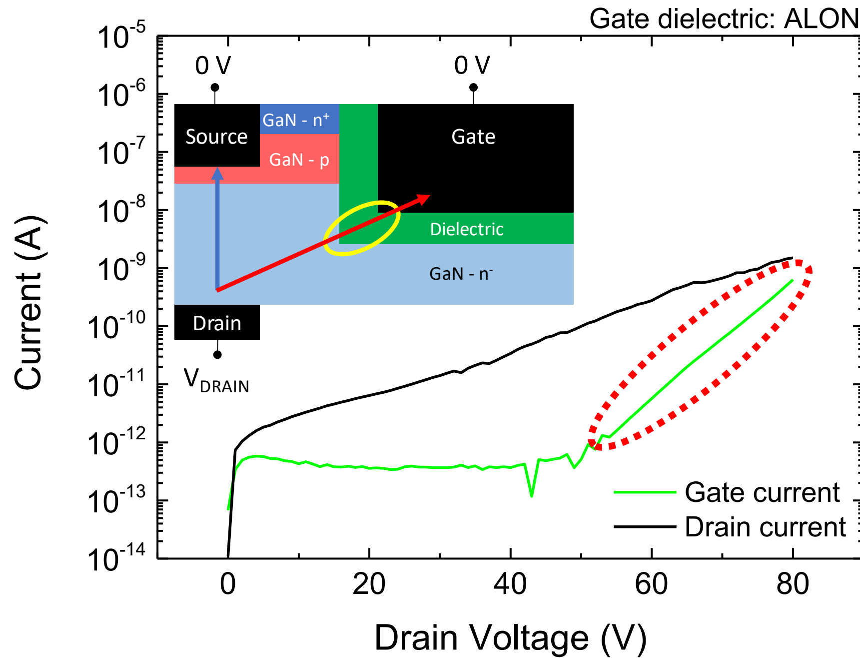


Figure 4.12 – Drain current (black line) and Gate current (green line) during an OFF-state measurement. The inset shows the schematic cross section of the device: the region where the electric field peaks is highlighted by a yellow circle, while the path of the drain-gate leakage current above 50 V (dashed red circle in the plot) is indicated by the red arrow.

Finally, an accurate analysis on the robustness of the different dielectric tested is performed by comparing the results obtained in the GS forward configuration. In this configuration the n^+ layer is in accumulation regime, and a sheet of electrons acts as a metal plate on the semiconductor-side of the dielectric. Moreover, the high doping level of the n^+ layer results in a negligible resistivity of both the semiconductor and the source ohmic contact. As a result, it can be assumed that all the applied gate voltage drops on the dielectric, thus allowing to accurately estimate the dielectrics robustness.

The critical electric field of the four tested material is calculated by dividing the failure voltage by the dielectric thickness, which is 35 nm. In the case of the bilayer, the 2.5 nm thick interface layer is neglected, and the considered dielectric thickness is the sole SiO_2 thickness. This approximation is based on the results obtained in the forward biased GS measurements, which show that a 35 nm thick either Al_2O_3 or ALON dielectric is considerably leakier than the SiO_2-based bilayer, especially in the voltage range close to the failure of the bilayer dielectric (~ 30 V). This means that the equivalent resistance of a 2.5 nm Al_2O_3 or ALON layer is definitively lower than the equivalent resistance of a

35 nm thick SiO_2 layer. Consequently, most of the applied voltage drops on the higher-resistivity material, which is the SiO_2.

Among the different tested gate dielectrics, the Al_2O_3 shows the lower electric field at the breakdown, which results 2.79 MV/cm. On the other hand, ALON has a breakdown field of 6.28 MV/cm, more than double than the Al_2O_3; nevertheless, a high device-to-device variability is observed. Finally, the analysis demonstrates that the devices with the SiO_2-based bilayer, independently on the interfacial material, have the highest robustness among the tested materials, which results about 8 MV/cm. It is worth noticing that the Al_2O_3 interface layer results in a considerably better repeatability of the failure voltage, and all the devices with Al_2O_3/SiO_2 bilayer dielectric show a breakdown filed higher than 8 MV/cm.

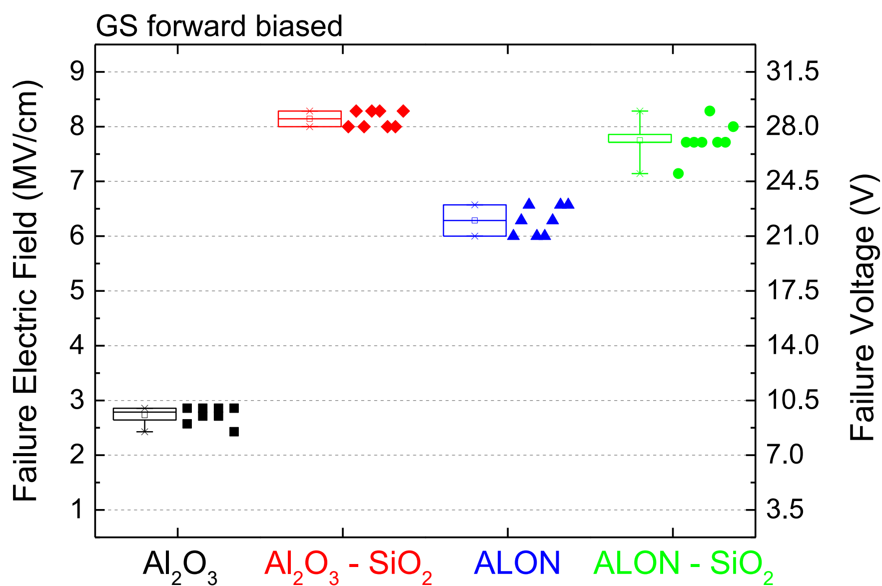


Figure 4.13 – Failure electric field (left Y-axis) and failure voltage (right Y-axis) of devices with different gate dielectric, i.e. Al_2O_3 (black), Al_2O_3 - SiO_2 bilayer (red), ALON (blue), ALON - SiO_2 bilayer (green).

4.3 Gate capacitance

Measuring and characterizing the gate capacitance is useful for understanding the physical phenomena which occur in a device when the gate terminal is submitted to a bias condition. During a Capacitance-Voltage (CV) measurement the impedance of the device under test is measured by means of a low-amplitude AC signal as a function of the applied DC bias. In a MOS structure the gate DC bias impacts the equilibrium of the semiconductor by changing its electrostatic condition, thus leading the material into three different conditions, which are accumulation, depletion and inversion, which can be identified by measuring the AC capacitance.

In this paragraph a deep analysis on the gate capacitance will be presented. First the gate capacitance behavior as a function of the applied gate voltage will be discussed and modeled, then a preliminary analysis on the dielectric traps and their characterization by means of gate CV measurements will be presented.

4.3.1 Gate capacitance calculations

When a MOS structure is biased in either accumulation or inversion condition, a sheet of free charges exposes in the semiconductor at the dielectric/semiconductor interface. As this condition is reached, the measured capacitance between the gate metal and the semiconductor approaches the dielectric capacitance; the dielectric is included between the gate metal and the high-density sheet of free charges and can thus be modeled as a planar capacitor. Basing on this, the first step of the analysis is the analytical calculation of the gate capacitance:

$$C = \varepsilon_0 \varepsilon_r \frac{A}{t_{ox}}$$

Where:

- C is the capacitance
- ε_0 is the dielectric constant of the vacuum
- ε_r is the dielectric constant of the dielectric
- A is the area of the planar capacitor
- t_{ox} is the dielectric thickness

The gate dielectric is Aluminum Oxide Al_2O_3, whose dielectric constant is 9.3 [61], while the gate thickness is 35 nm. Basing on these values, the normalized capacitance per unit of area of the studied MOS structure is:

$$C = \varepsilon_0 \varepsilon_r \frac{1}{t_{ox}} = 2.35 \cdot 10^{-7} \ \frac{F}{cm^2}$$

In the trench gate devices under analysis the same gate potential control differently doped semiconductors, which definitively behave differently with the applied gate bias. This leads to the splitting of the gate capacitance into 4 different contributions, as illustrated in Figure 4.14, which are:

- C_{n+}: capacitance between the gate meatal and the highly-doped layer connected to the source.
- C_p: capacitance between the gate and the p-doped layer. As the gate bias increases first the semiconductor depletes and then an electron inversion layer (which is the channel of the transistor) is formed at the interface with the dielectric.
- C_{n-}: this capacitance represents the capacitive contribution of the gate trench which penetrates the drift region.
- C_B: the bottom capacitance takes into account the contribution of the bottom of the trench; despite the other three capacitances which lie on the side of the trench, the area of this capacitance does not depend on the epi structure but only on the mask design.

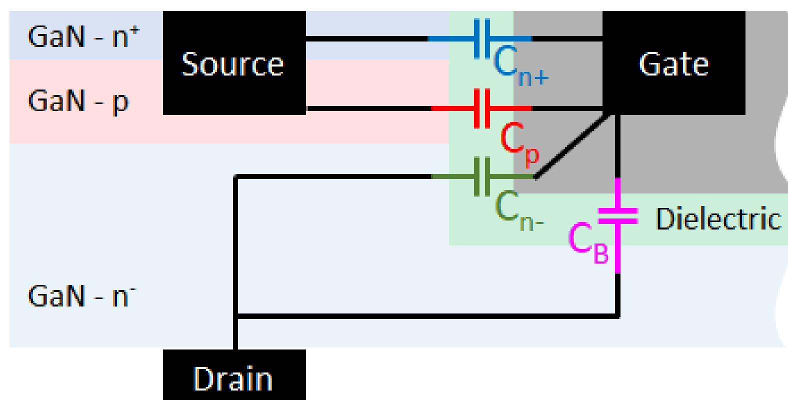


Figure 4.14 – trench gate capacitances contribution and equivalent electrical circuit.

The dielectric constant and the thickness are the same in all the contributions, while the area is different, and it depends on the layer thickness and on the perimeter of the trench, while the bottom capacitance depends on the design layout. For the area calculation is important to consider that the tested devices have two 500 μm gate fingers. The total top-view perimeter of the gate trench(es) results (see Figure 4.2):

$$P = \#fingers \cdot (2 \cdot W + 2 \cdot L_{GT}) = 2 \cdot (2 \cdot 500\mu m + 2 \cdot 4\mu m) = 0.2016\, cm$$

By multiplying the trench total perimeter by the n^+ and p layer thickness, the C_{n+} and the C_p areas are obtained, while the C_{n-} is calculated by multiplying the perimeter by the trench penetration depth into the n^- drift layer. The total area of each equivalent capacitance is corrected by the trench angle, which is about 20°. The results are summarized in Table 4.2.

		Total area	Total area corrected by the trench angle
C_{n+}	P · 250 nm	$5.040 \cdot 10^{-6}$ cm^2	$5.36 \cdot 10^{-6}$ cm^2
C_p	P · 400 nm	$8.064 \cdot 10^{-6}$ cm^2	$8.58 \cdot 10^{-6}$ cm^2
C_{n-}	P · 350 nm	$6.048 \cdot 10^{-6}$ cm^2	$6.43 \cdot 10^{-6}$ cm^2

Table 4.2 – area calculations of the equivalent capacitances which lie on the side of the trench.

The area of the planar surface on the bottom of the trench is calculated as:

$$A_B = \#fingers \cdot (L_{GT} \cdot W) = 2 \cdot (500\mu m \cdot 4\mu m) = 4 \cdot 10^{-5}\, cm^2$$

Basing on the calculated areas, each capacitance contribution can be calculated thanks to the equation previously described by multiplying the capacitance per unit of area by the area of each contribution. The analytically calculated capacitance values are summarized in Table 4.3.

	Total area	Total area corrected by the trench angle	Capacitance	Capacitance corrected by the trench angle
C_{n+}	$5.040 \cdot 10^{-6}$ cm^2	$5.36 \cdot 10^{-6}$ cm^2	1.19 pF	1.26 pF
C_p	$8.064 \cdot 10^{-6}$ cm^2	$8.58 \cdot 10^{-6}$ cm^2	1.90 pF	2.02 pF
C_{n-}	$6.048 \cdot 10^{-6}$ cm^2	$6.43 \cdot 10^{-6}$ cm^2	1.42 pF	1.51 pF
C_B	$4 \cdot 10^{-5}$ cm^2		9.4 pF	

Table 4.3 – Analytical values of each capacitive contribution to the total gate capacitance.

The total gate dielectric capacitance of the samples under analysis with two gate fingers each one 500 μm wide (*W*) and 4 μm long (L_{GT}), is:

$$C_{n+} + C_p + C_{n-} + C_B = \begin{matrix} 13.91\ \text{pF} & - \text{trench angle } 0° \\ 14.19\ \text{pF} & - \text{trench angle } 20° \end{matrix}$$

4.3.2 Gate CV measurement and modelling

In this section the experimental results obtained by measuring the gate capacitance of the devices will be discussed. The gate capacitance has been measured by using an LCR-meter Keysight E4980A. Different connection configurations have been tested, which are depicted in Figure 4.15:

- GS: gate-source capacitance, measured by sweeping the gate DC voltage, while keeping the source grounded and the drain floating.
- GD: gate-drain capacitance, measured by sweeping the gate DC voltage, while keeping the drain grounded and the source floating.
- G-SD: gate-source-drain capacitance; in this configuration source and drain are both shorted to the ground, while the gate DC bias sweeps within the chosen voltage range.

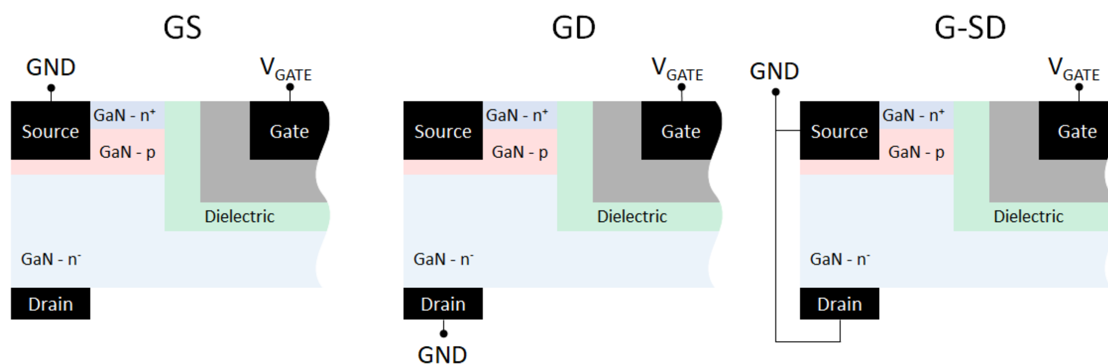


Figure 4.15 – Schematic cross section of the device with the three tested configurations: GS (left), GD (center) and G-SD (right).

GS – gate-source capacitance

When the device gate capacitance is measured with the source grounded and the drain floating, both the n^+ layer and the p layer are grounded. This means that the gate potential directly affects the equilibrium condition of two layers which are doped differently: an increasing gate bias on a MOS structure with a n^+ semiconductor leads to the formation of an electron accumulation layer in the semiconductor at the dielectric

interface; on the other hand, when the MOS structure involves a p-doped semiconductor, a depletion region builds up, and, for increasing gate voltage, an inversion channel forms.

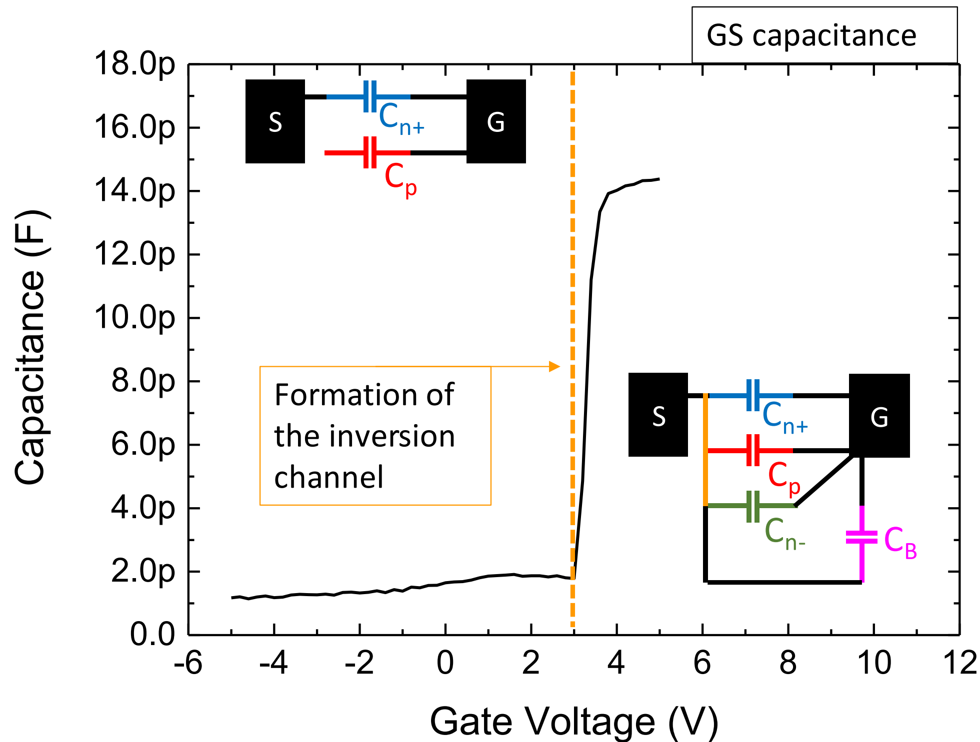


Figure 4.16 – Measured GS capacitance. Top left inset shows the equivalent circuit at gate voltages below the threshold voltage of the device, while the bottom right inset shows the equivalent circuit above the threshold.

Figure 4.16 shows the behavior of the GS capacitance as a function of the applied gate voltage. The capacitance level is less than 2 pF until the gate bias reaches 3 V; after this voltage level, which corresponds to the threshold voltage of the device under analysis, the capacitance sharply increases to more than 14 pF. The strong dependence on the threshold voltage means that the formation of the inversion channel plays a key role on the gate CV. Moreover, it is worth noticing that for gate voltages higher than the threshold voltage, the capacitance level approaches the analytical value of the total gate capacitance, which is 14.19 pF. This indicates that the inversion channel in the p-layer short-circuits the accumulation channel present in the n^+ and in the n^- layers; in this condition the whole gate dielectric is included between the gate metal and an electron sheet of charge in the whole trench area, and the equivalent capacitance is the sum of all the contribution calculated, i.e. C_{n+}, C_p, C_{n-}, C_B (inset bottom right Figure 4.16). For gate voltages below the threshold, the equivalent capacitance between gate and source is

composed by the parallel connection (arithmetical sum) between the C_{n+} and the C_p reduced by the depletion capacitance of the p layer; this means that the measured capacitance should be included between C_{n+} and $C_{n+} + C_p$, which results 1.19 pF < $C_{sub\text{-}th}$ < 3.09 pF. These values are compatible with the experimental results.

GD – gate-drain capacitance

By measuring the gate-drain capacitance with the drain grounded, the applied bias directly affects the n^- drift region and the dielectric in the bottom of the trench. In principle at low (or negative) gate bias the semiconductor is depleted, while it evolves to an accumulation regime as soon as the gate potential increases and attracts electrons from the bulky semiconductor toward the semiconductor-dielectric interface.

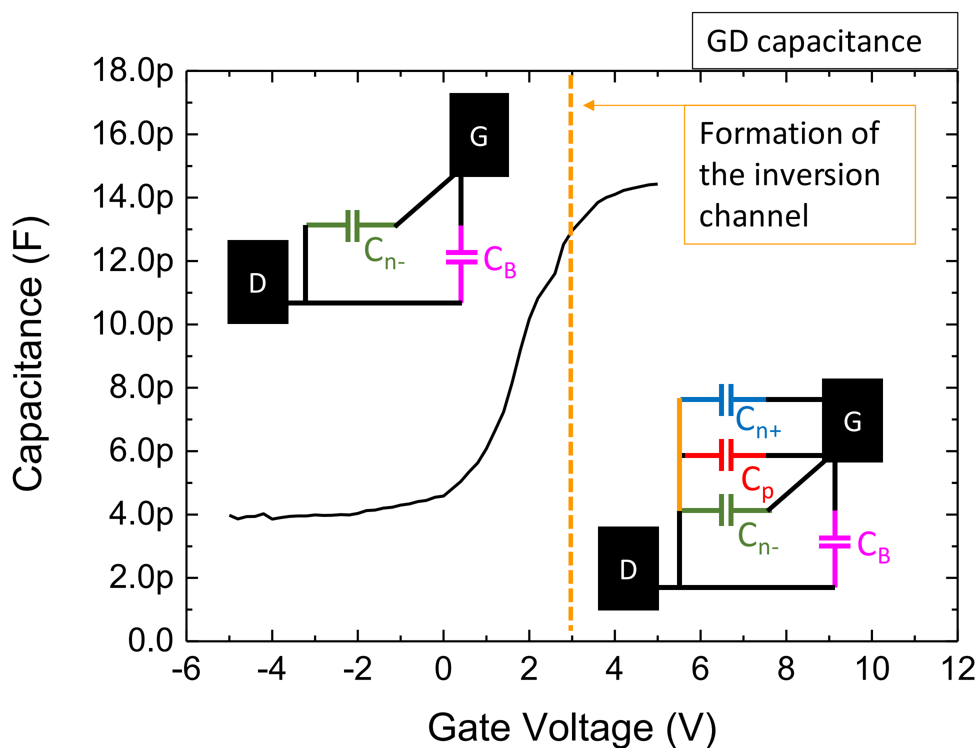


Figure 4.17 – Measured GD capacitance. Top left inset shows the equivalent circuit at gate voltages below the threshold voltage of the device, while the bottom right inset shows the equivalent circuit above the threshold.

Figure 4.17 shows the behavior of the measured gate-drain capacitance as a function of the applied gate voltage. The capacitance level is about 4 pF for negative voltages, and it shows a hump from 0 V to 2 V increasing up to more than 11 pF. Around the threshold voltage of the device the capacitance shows a second hump, and it increases up to roughly 14 pF. As previously discussed, as the inversion channel forms

in the p-doped layer, the gate dielectric becomes included, along the whole trench area, between a sheet of electrons and the gate metal; this results in a total gate capacitance of 14 pF, as previously calculated.

The GD capacitance-voltage characterization (Figure 4.17) shows a hump that occurs between 0 V and 2 V; in this voltage range the inversion channel is not formed yet, meaning that the capacitance variation is caused by the n^- drift region. In particular, as the gate voltage increases, the n^- doped semiconductor goes from a depletion regime to an accumulation regime, and an accumulation electron layer forms at the GaN-dielectric interface. In order to verify this hypothesis, the GD capacitance was measured in devices with different bottom areas. This test was carried out in single finger devices with SiO_2 gate dielectric (ε_r = 3.9), gate width W of 100 µm, and a gate trench length L_{GT} of 2 µm, 4 µm, and 8 µm; as a consequence, the gate capacitance is considerably lower than the analytical calculations shown in 4.3.1.

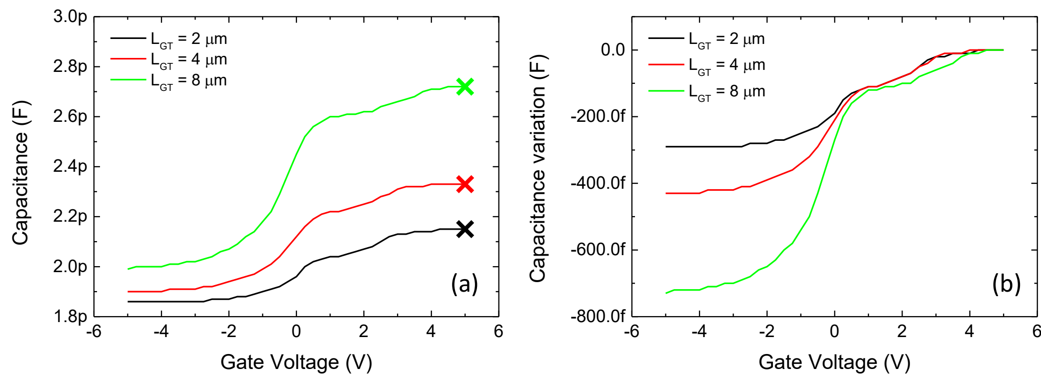


Figure 4.18 – (a): Gate-drain capacitance C_{GD} (source floating) measured on devices with different gate trench length. (b): C_{GD} normalized by the capacitance value at V_G = 5 V; the variation of the bottom area only affects the capacitance variation that occurs before 0 V.

The variation of the bottom area of the devices clearly impacts the amplitude of the first hump Figure 4.18 (a), which occurs at gate voltages lower than 0 V in the devices measured in this test. As the gate bottom area, and thus the bottom capacitance, increases, the capacitance variation within the first hump increases. This dependence is even clearer in Figure 4.18 (b), where the total trench capacitance, which is different on the three tested devices, is taken as reference (0 pF). Moreover, it is worth noticing that the second hump, which occurs near the threshold voltage of the device, has the same amplitude in the three tested devices, confirming that it is related to the formation of the inversion channel.

Figure 4.18 (b) demonstrates that the variation of the trench-bottom area affects the amplitude of the first hump, while Figure 4.18 (a) shows that the variation of the bottom area results in an increased total gate capacitance. Considering the measured total trench capacitances and focusing on the bottom-area scaling, the correctness of the analysis can be proved by monitoring the dependence of the trench capacitance on the bottom area, which must be linear.

First the bottom capacitance theoretical values need to be calculated. Using the formula of the planar capacitor, the theoretical bottom capacitances C_B of the tested structure results:

$$C_B = \varepsilon_0 \varepsilon_r \frac{A_B}{t_{ox}} = \varepsilon_0 \varepsilon_r \frac{W \cdot L_{GT}}{t_{ox}} = \begin{matrix} 0.197\ \text{pF} & - L_{GT} = 2\ \mu\text{m} \\ 0.394\ \text{pF} & - L_{GT} = 4\ \mu\text{m} \\ 0.789\ \text{pF} & - L_{GT} = 8\ \mu\text{m} \end{matrix}$$

These capacitance values refer to the dielectric capacitance measured when the electrons accumulation layer is formed, which means for gate voltages sufficiently high. In order to compare the experimental data with the analytical results, in Figure 4.19 the gate-drain capacitances measured at $V_G = 5$ V (crosses in Figure 4.18 (a)) are plotted as a function of the gate trench length L_{GT}.

The total gate capacitance as the whole trench is included between the gate metal and the electron sheet of charge (accumulation/inversion) is:

$$C_{GD} = C_{offset} + C_B$$

where C_{offset} includes all the gate capacitance contributions except for the bottom capacitance. Replacing C_B with the planar capacitance formula, the total gate-drain capacitance can be calculated as:

$$C_{GD} = C_{offset} + C_B = C_{offset} + \varepsilon_0 \varepsilon_r \frac{W \cdot L_{GT}}{t_{ox}} = C_{offset} + \frac{\varepsilon_0 \varepsilon_r W}{t_{ox}} \cdot L_{GT}$$

The gate-drain capacitance linearly depends on the gate trench length, where:

- Intercept: C_{offset}
- Slope: $(\varepsilon_0 \cdot \varepsilon_r \cdot W) / t_{ox} = 9.2 \cdot 10^{-10}$ F/cm

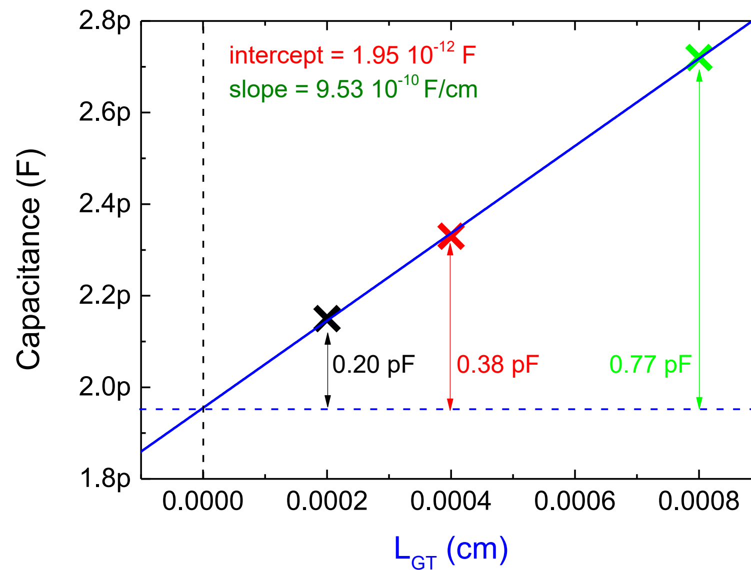


Figure 4.19 – gate-drain capacitance measured at V_G = 5 V versus the gate trench length. The blue line is the linear fit thought the obtained experimental data.

As can be noticed in Figure 4.19, the total trench capacitance measured in the devices with different bottom area lies on a line, which intercept and slope are respectively $1.95 \cdot 10^{-12}$ F and $9.53 \cdot 10^{-10}$ F/cm; this latter completely agrees with the analytical value previously calculated. Moreover, by subtracting the intercept value from the measured C_{GD}, the bottom capacitance C_B can be indirectly obtained from the experimental data (arrows in Figure 4.19).

The following table summarizes the analytical values and the experimental results of the capacitance of the trench bottom and of the slope of the C_{GD} vs L_{GT} plot. The experimental results closely fit the analytical prediction.

		Analytically calculated	Experimental result
	$(\varepsilon_0 \cdot \varepsilon_r \cdot W) / t_{ox}$	$9.2 \cdot 10^{-10}$ F/cm	$9.53 \cdot 10^{-10}$ F/cm
L_{GT} = 2 μm	C_B	0.197 pF	0.20 pF
L_{GT} = 4 μm		0.394 pF	0.38 pF
L_{GT} = 8 μm		0.789 pF	0.77 pF

Table 4.4 – comparison between the calculated values and the experimental results concerning the bottom capacitance and the slope of the C_{GD} versus L_{GT}.

G-SD – gate to drain-source capacitance

The last configuration tested has both drain and source shorted to the ground, while the gate terminal is biased. In this configuration all the capacitance contributions described in Figure 4.14 are measured.

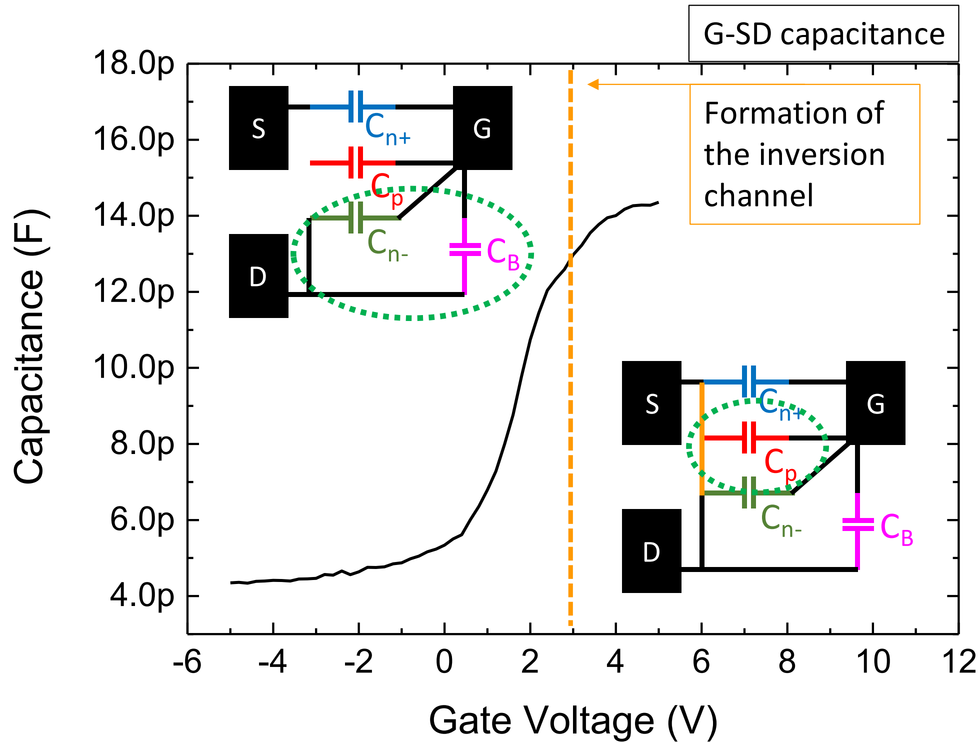


Figure 4.20 – Measured G-SD capacitance. Top left inset shows the equivalent circuit at gate voltages below the threshold voltage of the device, while the bottom right inset shows the equivalent circuit above the threshold.

At negative gate bias, only the n^+ layer/dielectric interface might be in accumulation regime, while p-layer and n^- layer are in a depletion condition. This means that the measured capacitance is the depletion capacitance of the semiconductor around the trench except for the n^+ layer related gate area. As the gate voltage increases toward 0 V, the depletion region within the n^- region starts reducing, thus resulting in an increasing capacitance as described for C_{GD}. Finally, as the gate voltage approaches the threshold voltage of the device, the capacitance shows a second hump related to the formation of the inversion channel in the p-layer. At gate bias above the threshold the whole gate trench area is included between the gate metal and a sheet of electron; the resulting $C_{G\text{-}SD}$ capacitance results slightly higher than 14 pF, which again agrees with the total trench capacitance analytically calculated.

Comparison between GS, GD and G-SD capacitances

The behaviors of the capacitance-voltage measurements in the three tested configurations are summarized and compared in Figure 4.21.

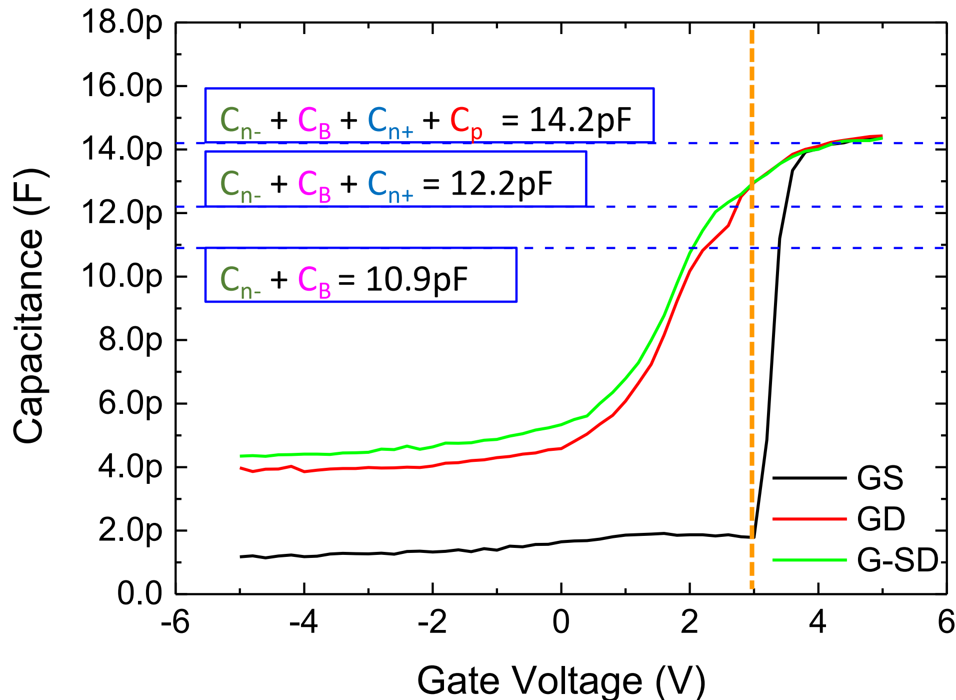


Figure 4.21 – comparison between C_{GS}, C_{GD}, and $C_{G\text{-}SD}$. Blue dashed lines are the analytically calculated capacitance level. Orange dashed line indicates the threshold voltage of the device.

As previously pointed out, at gate biases higher than the threshold voltage the measured capacitance approaches the total gate trench capacitance, independently on the measurement configuration. Moreover, it is worth noticing that, for gate voltages lower than the threshold voltage, there is an offset between the gate-drain C_{GD} capacitance and the gate-drain-source $C_{G\text{-}SD}$ capacitance; this offset is related to the C_{n+} capacitance, whose contribution is always measured in the $C_{G\text{-}SD}$ configuration, whereas it is only measured at gate biases higher than Vth in the C_{GD} configuration.

The blue dashed lines indicate the calculated analytical values of the capacitances. In C_{GD} as the accumulation layer is formed in the bottom of the trench (first hump), the probed capacitance is C_{n-}+C_B, whose theoretical value is 10.9 pF. At the same gate bias the $C_{G\text{-}SD}$ capacitance is about 1.3 pF higher than C_{GD}, due to the contribution of C_{n+}. Lastly it is worth noticing that, in the $C_{G\text{-}SD}$ configuration, the amplitude of the second capacitance hump that occurs around 3 V (threshold voltage of the transistor), is close to

the analytical value of the C_P, meaning that the capacitance variation is actually related to the formation of the inversion channel.

An important outcome of this analysis is the evaluation of the optimal measurement configuration to characterize the dielectric performances in term of stability and reliability of the final device. Since the channel of the trench gate transistors lies in the p-layer at the semiconductor/dielectric interface, the characterization of the dielectric by means of CV measurements (study of either dielectric and interface traps), must be performed by measuring only the C_P contribution (and the capacitance variation related to the depletion of the p-doped GaN layer). The optimal solution is to measure the gate capacitance with the source and the drain shorted to ground ($C_{G\text{-}SD}$ configuration); the contribution of C_{n+}, C_{n-} and C_B are constant in the voltage interval around the threshold voltage, in which the p-doped semiconductor depletes and the channel forms.

4.3.3 Dielectric trap density evaluation and comparison

In this section the standard PBI experimental method is described and applied for the evaluation of the dielectric bulk traps, mainly aimed to the comparison between two different dielectrics, which are Al_2O_3 and Al_2O_3/SiO_2 bilayer. Due to either the complex structure of the gate module and the complex gate capacitance behavior discussed in 4.3.2, the presented analysis is a preliminary study carried out on the available structures; a more accurate study will be performed on *ad hoc* designed test structures.

The measurement technique consists on the monitoring the variation of the gate CV hysteresis with the increasing gate bias (i.e. increasing electric field within the dielectric). During the upward sweep, as the inversion channel is formed, all the applied voltage drops on the dielectric, thus bending its bands and enhancing charge trapping within deep energy states. The trapped charges cause a shift of the CV behavior during the backward sweep. From the measured hysteresis induced by a defined electric field, the amount of trapped charges can be estimated. Moreover, by evaluating the dependence of the trapped charges density on the electric field, an estimation of the energy distribution of the trap states within the dielectric energy gap can be obtained.

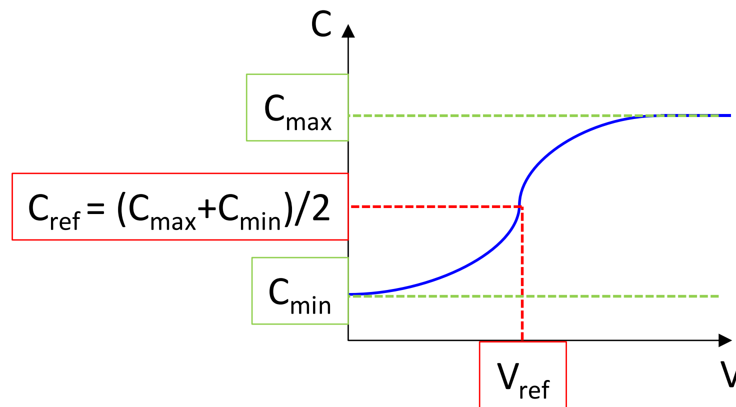


Figure 4.22 – schematic representation of the behavior of a CV characteristic. V_{ref} and C_{ref}, which are important parameters for the presented analysis, are highlighted.

Basing on the typical behavior of a gate capacitance-voltage characteristic of a MOS device, which is shown in Figure 4.22, it is defined:

- C_{max}: the maximum capacitance value measured when the inversion channel is formed. This value corresponds to the dielectric capacitance.
- C_{min}: the capacitance level measured before the formation of the inversion channel, when the gate capacitance is the series connection of the dielectric capacitance and the semiconductor depletion capacitance.
- C_{ref}: in this work the "reference capacitance" is defined as the average capacitance between the C_{min} and the C_{max}.
- V_{ref}: the reference voltage is the gate voltage at which the gate capacitance is equal to the reference capacitance C_{ref}.

In the following analysis the reference voltage is an important parameter, since it defines different electrostatic condition of the MOS structure. For gate voltages lower than the V_{ref}, the applied bias depletes the semiconductor up to the formation of the inversion channel, which forms at V_G approximately equal to V_{ref}. All the gate potential which exceeds V_{ref} drops on the dielectric, causing the electric field within the insulator to increase. It is important to define the overdrive voltage V_{OV}, which indicates the amount of potential that drops on the dielectric with a defined gate voltage V_G:

$$V_{OV} = V_G - V_{ref}$$

The experimental technique consists on characterizing the gate capacitance with a double sweep measurement (upward and backward) reaching increasing overdrive voltages. The amount of charge in a capacitor *C* biased at a voltage *V* is:

$$Q = C \cdot V$$

During the double sweep measurement on a capacitance *C* with area *A*, the voltage variation ΔV (hysteresis) can be ascribed to an effective amount of trap N_{eff} per unit of area which captures an electron (which charge is *q*). Please notice that this calculation gives not the net amount of trap states, but the equivalent (effective) trap density in the hypothesis that all the traps are located in the dielectric border close to the channel.

$$N_{eff} = \frac{C}{A} \cdot \frac{1}{q} \cdot \Delta V$$

Concerning the devices under test, the gate capacitance and its dependence on the gate voltage are widely described in 4.3.2. For the hysteresis measurement it is important to test the gate/p layer capacitance C_P, so the gate to source-drain $C_{G\text{-}SD}$ configuration is used. The starting voltage is chosen so that the accumulation layer is formed in both the n^+- and n^--layer and so C_{n+} and C_{n-} give a constant contribution to the measured capacitance. The voltage sweeps from the starting voltage up to a stop voltage which is higher than V_{ref}, so that the dielectric is submitted to an electric field E_{OX} defined as:

$$E_{ox} = \frac{V_{OV}}{t_{ox}}$$

The measurement is repeated for increasing overdrive voltages on different devices belonging to the same set in the maskset, in order to guarantee a good reproducibility avoiding memory effect.

To define the starting voltage of the measurements it has been considered that the total gate capacitance of the tested devices is 14.5 pF, and, subtracting half of the analytical C_P value, the C_{ref} results 13.5 pF at V_G equal to 3 V, which has been defined as V_{ref}. The tested overdrive voltages span from 0.5 V to 2.5 V, step 0.25 V.

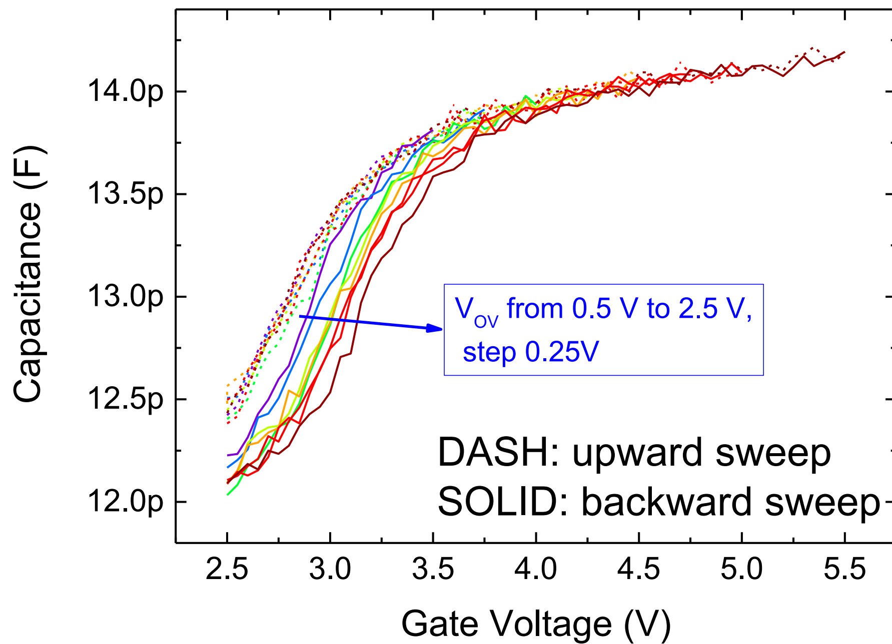


Figure 4.23 – Capacitance hysteresis measurements carried out on a trench gate Al_2O_3 MOS devices with increasing overdrive voltages.

The experimental results obtained on trench gate Al_2O_3 MOS devices are shown in Figure 4.23. It is worth noting that as the overdrive voltage increases (rainbow color scale respectively from purple to brown) the hysteresis increases, thus indicating that charges are trapped within the dielectric.

The very same analysis has been performed on trench gate GaN MOS devices with 35 nm SiO_2 / Al_2O_3 bilayer dielectric (Figure 4.24). In these samples also a 2.5 nm thick Al_2O_3 interfacial layer is present between the SiO_2 and the GaN. In this case the C_P value is lower than the Al_2O_3 devices, because of the reduced dielectric constant of SiO_2; this results in a lower resolution of the measurement, and a noisy behavior of the curves. For the measurement the extrapolated C_{ref} is 7.45 pF, and the respective reference voltage V_{ref} is 1.5 V. In the devices with SiO_2 gate dielectric the CV measurements show a hysteresis due to the trapping of fixed charges, as discussed in the Al_2O_3 gate dielectric devices. Moreover, the trapping phenomena increase with the increasing overdrive voltage.

Assuming that the trapping phenomena only occurs in the SiO_2 layer, the calculation of the dielectric (SiO_2) electric field at different overdrives in the case of the bilayer results:

$$E_{SiO} = V_{OV} \cdot \frac{\varepsilon_{Al2O3}}{\varepsilon_{Al2O3} \cdot t_{SiO} + \varepsilon_{SiO} \cdot t_{Al2O3}}$$

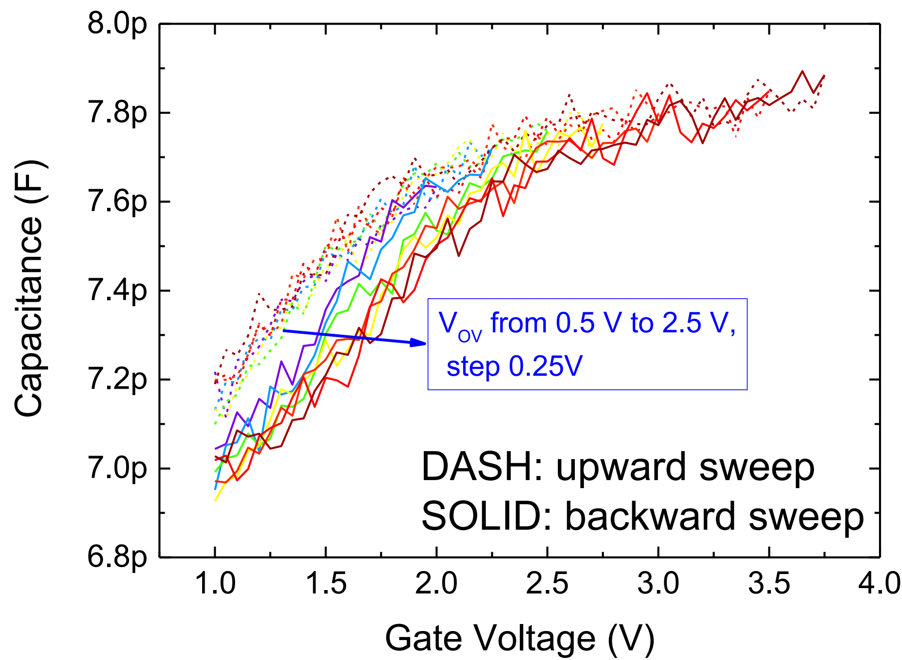


Figure 4.24 – Capacitance hysteresis measurements carried out on a trench gate SiO_2 MOS devices with increasing overdrive voltages.

The effective trap density extraction performed in Al_2O_3 and SiO_2 gate dielectrics allows the comparison between the two different solutions, as shown in Figure 4.25.

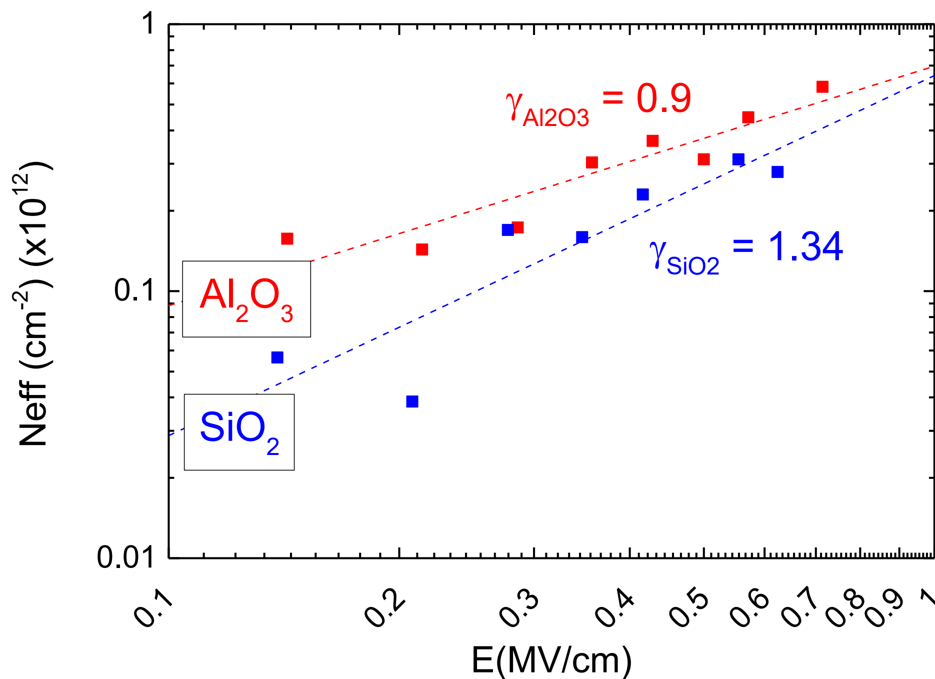


Figure 4.25 – Effective trap density versus the dielectric electric field for Al_2O_3 (red) and SiO_2 (blue) dielectrics.

The density of traps in the two gate dielectric stacks are similar, and, for Al_2O_3 devices, in agreement with some results presented in the literature for dielectrics on III-

V materials [62]. Moreover, the slopes γ of the fitting lines in Figure 4.25 give an indication on the energy distribution of the traps involved in the measured hysteresis. A high slope means that the traps are narrowly distributed within the energy gap of the dielectric, and once all the states are filled, the variation of the Fermi level does not cause any variation on the trapping condition of the material; on the other hand a reduced slope indicates that the traps are widely energetically distributed, and a variation of the Fermi level within the bandgap of the insulator results in an improved trapping. A slope around 1-1.5 agrees with previous papers reported in literature, and it is typical of dielectric deposited on III-V semiconductor, as shown in [63].

4.4 Conclusions

Vertical architecture is a promising solution to push Gallium Nitride based devices over the 1000 V limit, thus expanding the applications range where GaN can have an impact on the performance of power converters.

In this chapter, the gate of (semi-)vertical GaN based was deeply studied and characterized. Particularly, gate leakage and gate capacitances were experimentally measured and modeled.

The first part of the chapter is focused on the study of the gate leakage mechanisms as a function of both different biases and different measurement configurations. The experiments allow to locate the different leakage paths depending on the bias condition (forward or reverse gate voltage) and on the connection configurations (GD and GS). Moreover, the OFF-state leakage was investigated, showing that it is limited by the p/n$^-$ junction until the failure of the gate dielectric due to the high electric field which possibly peaks at the trench bottom corner. Lastly, a comparison between different gate dielectrics was presented; the breakdown electric field of each material was estimated and the capability on limiting the gate losses was compared.

The second part of the chapter proposes a model able to explain the gate capacitance behavior of a vertical trench-gate MOS device. The gate capacitance was split in four capacitive elements that contribute to the total gate capacitance, depending on the condition of the GaN at the dielectric/semiconductor interface. These contributions were analytically calculated, and they result to be comparable with the experimental results. Finally, a set of hysteresis capacitance measurements allows to estimate the bulk trap concentration of the gate dielectric, and to compare two different dielectric materials.

Chapter 5:

Analysis of the gate instabilities

5.1 Vth transient experimental setup

One of the main parameters of GaN based power devices is the threshold voltage. Several approaches have been developed in order to obtain the normally-off condition in HEMT devices, which is a fundamental requirement for safety operations of power converters. The investigation of the physical mechanisms that cause gate related issues is important in order to improve the stability and the reliability of the devices. Moreover, since most of vertical GaN devices are based on a Metal-Insulator-Semiconductor gate module, the gate dielectric trapping behavior needs to be deeply investigated.

Independently on the device architecture, the study of the gate instabilities shown an increasing interest for the gate module optimization, thus an *ad hoc* setup able to monitor the threshold voltage behavior in a wide time range has been developed. The so-called threshold voltage transient setup is mainly used for characterizing on-wafer devices, but the testing of packaged devices can be performed as well.

The measurement is based on the characterization of the IdVg curve of the device under test as a function of the time and of the bias condition. The time duration of the IdVg characterization is crucial, and it must be as short as possible in order not to affect the trapping condition of the device. All the conventional semiconductor parameter analyzers take several seconds in order to measure the IdVg characteristic of a transistor, and this is not acceptable for the described purposes. Reisinger et al. [64] proposed a setup which uses a complex feedback loop to determine the threshold voltage of the DUT by forcing a defined drain current. The mentioned setup is able to monitor the Vth after 1μs after the stress voltage is removed. Nevertheless, several runs are needed in order to characterize the Vth behavior in a wide time range. Moreover, the recovery (relaxation) transient is measured by keeping a constant current (and drain voltage) through the device. This might result in an inaccurate transient estimation, due to the well-known accelerating effect of the electric field in the detrapping kinetic.

In the presented setup an arbitrary waveform generator (AWG) provides a voltage ramp and a square pulse to two amplifiers, whose outputs are respectively connected to the gate terminal and to the drain terminal of the device under test. The current flowing

through the drain of the transistor is measured thanks to a current probe, which is connected to an oscilloscope which measures also the gate voltage. The oscilloscope external trigger is connected to the sync output of the AWG. A schematic representation of the connections is shown in Figure 5.1.

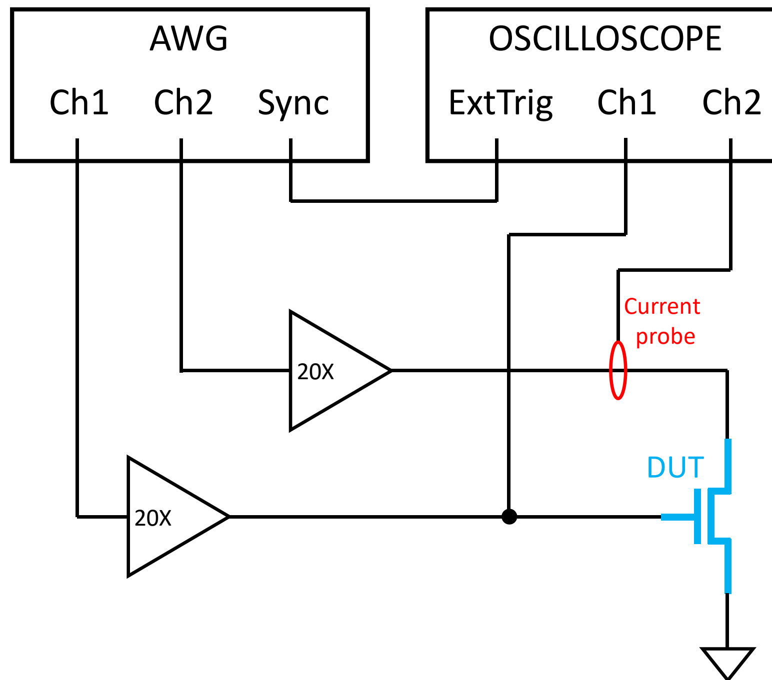


Figure 5.1 – Schematic representation of the connections of the Vth transient setup.

The measurement sequence is split into two phases, as shown in Figure 5.2:

- Constant bias phase – within this time period, which can last from 1 second to hundreds of seconds depending on the user settings, the device is submitted to a constant bias. The aim of this phase is to induce the filling of the traps by means of a constant electric field; depending on the bias condition, traps located in different regions within the device structure can be studied. Since the Vth transient setup is aimed to monitor the threshold voltage variation, it is common to apply a constant gate bias, either forward or reverse. The maximum voltage range, limited by the 20x amplifiers, goes from -200 V up to 200 V.
- Vth monitoring phase – during this phase, a constant bias condition defined as "quiescent bias" is systematically interrupted in order to perform a fast IdVg characterization. The quiescent bias level is a user-defined parameter, whose limits are ± 200 V. The IdVg characterization has

a fixed duration of 10 μs, while all the voltage parameters of the IdVg curve can be defined from the user interface of the program. The monitoring phase, which extends in a time range from 10 μs to 100 s, is interrupted for 10 μs 3 times per decade (i.e. 10 μs, 30 μs, 50 μs, 100 μs…30 s, 50 s, 100 s).

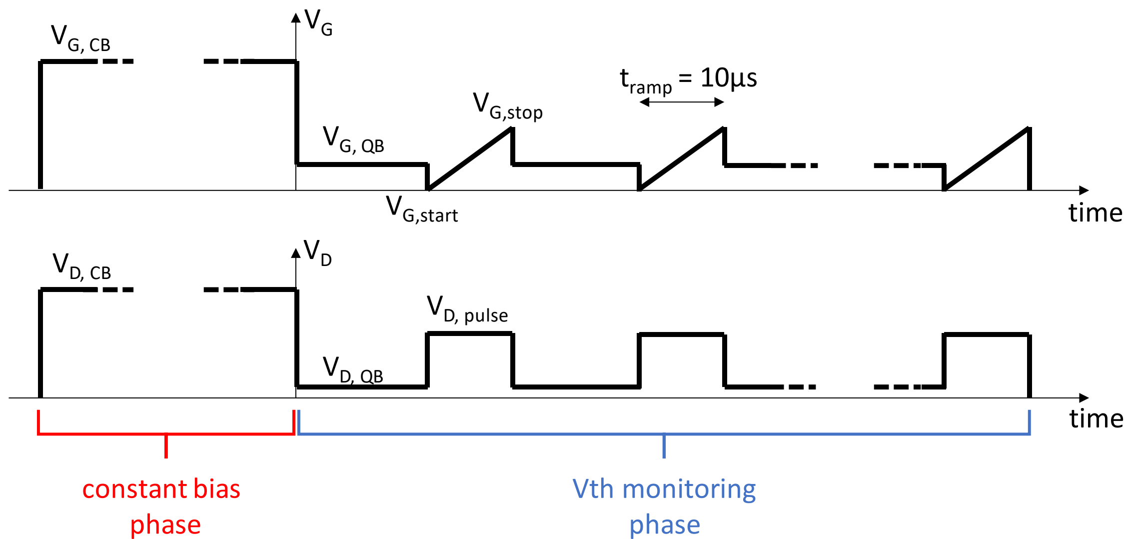


Figure 5.2 – Gate voltage (top) and drain voltage (bottom) during the Vth transient measurement. Both constant bias and Vth monitoring phases are highlighted.

The fast measurement of the IdVg characteristic of the transistor deserves a detailed description. As anticipated, the characterization of the device must be as fast as possible, so that its period can be considered negligible with respect to the recovery process timing. The timing of the IdVg characterization, which is fixed to 10 μs, is limited by the performances of the two amplifiers used for increasing the AWG output current and voltage. The limited bandwidth of the amplifier requires hundreds of nanoseconds before the drain voltage become constant, which is a fundamental condition for the IdVg characterization. For this reason, an adjustable delay time is interposed between the raise edge of the drain voltage and the starting time of the gate voltage ramp (highlighted with a red line in Figure 5.3).

Concerning the voltage limits of the setup, both the gate and the drain voltages can range between - 200 V and + 200 V. Depending on the bias condition needed, the operator must choose the appropriate bias condition. In particular, for the IdVg measurement, the following parameters must be specified:

- $V_{G, QB}$ – gate quiescent bias, which is the gate voltage at which the device must be kept during the Vth monitoring phase

- $V_{D,\,QB}$ – drain quiescent bias, which is the gate voltage at which the device must be kept during the Vth monitoring phase
- $V_{G,\,start}$ – Gate ramp starting voltage, which is the minimum voltage of the IdVg characterization
- $V_{G,\,stop}$ – Gate ramp stop voltage, which is the maximum voltage of the IdVg characterization
- $V_{D,\,pulse}$ – Drain pulse voltage, which is the drain voltage to be kept constant during the IdVg characterization

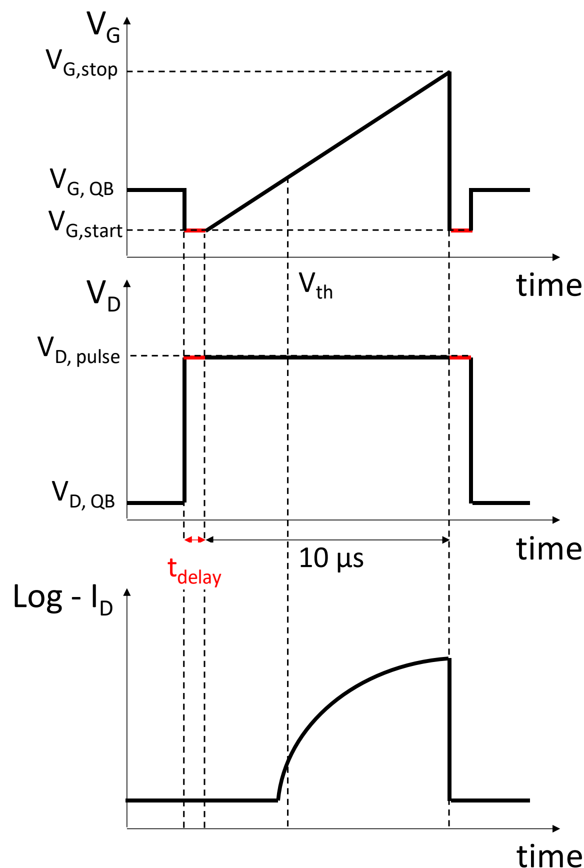


Figure 5.3 – Schematic behavior of the gate and the drain voltage during the characterization of the IdVg of the device under test. On the bottom a sketch of the measured drain current.

The result of the presented measurement is the behavior of the threshold voltage over 100 seconds in a defined bias condition, and after a defined period with a constant bias condition, as shown in Figure 5.4 – MEAS 2. The main purpose of this setup is to monitor the evolution of the threshold in a zero-bias condition after a constant bias has been applied in the first measurement phase. This allows to extract a threshold transient over the time, which has a time constant strictly related to the emission time of the traps

filled during the constant bias phase. Performing the measurement at different temperatures, it is possible to fully characterize the traps involved in the detrapping process, determining their activation energy.

Nevertheless, the same setup can be used to characterize also the trapping kinetic. By setting a negligible constant bias phase (1 s, zero bias) and a non-zero quiescent bias point during the Vth monitoring phase, the variation of the threshold voltage of the device over the time can be monitored. Moreover, by repeating on the same device the Vth transient measurement twice, one for the trapping kinetic and one for the zero-bias recovery, it is possible to fully characterize the traps which cause the threshold voltage instability, as shown in Figure 5.4.

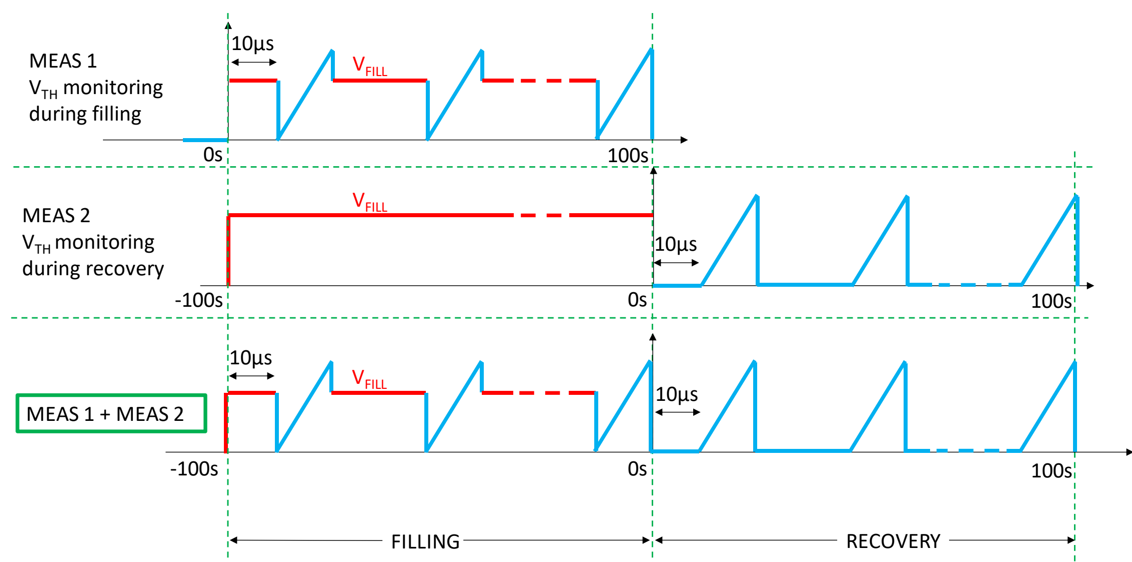


Figure 5.4 – Gate voltage behavior during the two measurements needed (MEAS 1, MEAS 2) in order to obtain a full characterization of the trapping and detrapping kinetics which cause the threshold voltage instability. During MEAS 1 the threshold voltage is measured with a non-zero quiescent bias (V_{FILL}), while during MEAS 2, the threshold voltage recovery at zero-bias is characterized after a constant bias (V_{FILL}).

A further improvement of the presented Vth transient setup allows to investigate the impact of monochromatic light on the detrapping kinetics. As a photon reaches a trapped carrier, it can easily transfer its energy, promoting, if the latter is higher than the energy level of the trap state, the detrapping process. By studying the behavior of the threshold recovery transient as a function of the wavelength of the light which shines on the sample, an estimation of the energy level involved in the Vth variation can be obtained.

The core structure of both the program and the setup is the same described previously, but an additional AWG, which is synchronized with the gate-drain signal

generators, is needed for driving the light source. The latter is a Light Emitting Diode (LED), which must be biased at a controlled and user-defined current. The LED is kept off during the constant bias phase of the measurement, and it turns on sharply at the beginning of the monitoring phase. A simple electronic circuit based on a Si-based MOSFET driven by an operational amplifier, shown in Figure 5.5, acts as a controller for the LED, ensuring a fast turn-on and a constant user-defined current flowing through the LED. Thanks to the negative feedback loop, the current through the LED is equal to the output voltage of the AWG over the value of the resistor, which was set equal to 10 Ω.

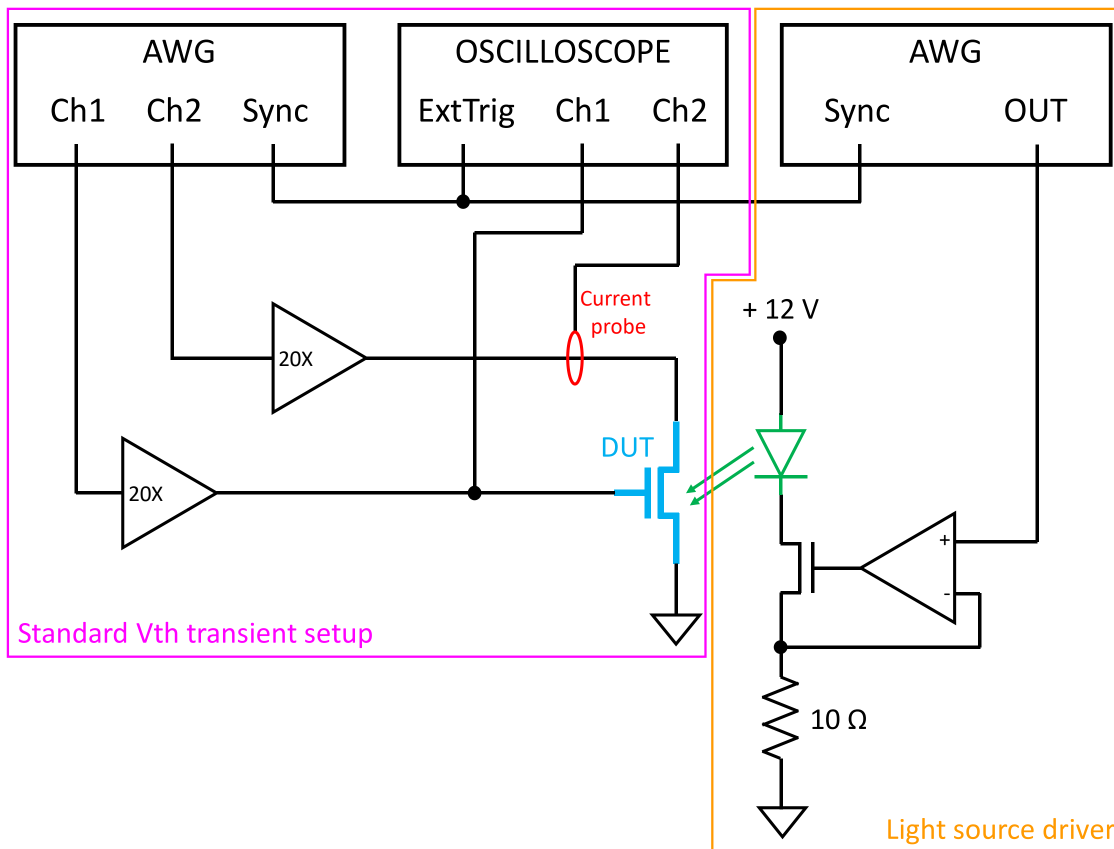


Figure 5.5 – Schematic representation of the Vth transient setup used for the monitoring of the light-assisted recovery of the threshold voltage.

5.2 Application of the Vth transient setup

In this paragraph two examples of application of the Vth transient setup discussed in paragraph 5.1 are presented; the data, the figures and the discussion that will follow are published in [65] and [66]. The two analysis were carried out on remarkably different device, respectively a p-GaN gate HEMT and a trench gate MOS; nonetheless, in both the cases, the evaluation of the threshold voltage variation over the time contributes to deeply understand the gate instabilities.

5.2.1 µs-Range Evaluation of Threshold Voltage Instabilities of GaN-on-Si HEMTs with p-GaN Gate [65]

This work is focused on the analysis of the gate stability of lateral HEMT devices, which are based on an AlGaN/GaN heterojunction. In order to achieve the normally-off condition, the studied devices have a p-GaN doped gate which locally depletes the 2DEG. The impact of the p-GaN gate on the dynamic performance of the devices was widely discussed in literature [67]–[71], and three mechanisms responsible for the threshold voltage instability in forward gate bias regime were identified:

Mechanism 1: injection of electrons from the 2DEG in donor-like states in the AlGaN barrier, causing a positive Vth shift at low gate biases

Mechanism 2: accumulation of holes at the p-GaN/AlGaN interface and subsequent hole trapping in the AlGaN barrier, causing a negative Vth shift at low stress time at higher gate biases

Mechanism 3: depletion of holes within the p-GaN layer, causing a positive Vth shift at high gate biases for longer stress time

Two set of samples are available, namely Etch A devices and Etch B devices; these samples differ for the p-GaN etch process used for the fabrication of the gate module, which results to be improved in the Etch B devices. On Etch A samples, a forward gate double pulse characterization is performed, by using the setup shown in [72]. The Vth variation as a function of the gate baseline voltage obtained by means of the double pulse measurements is shown in Figure 5.6. It is worth noticing the non-monotonic behavior of the Vth variation with the increasing gate baseline: below $V_G = 3$ V the Vth weakly increases due to the electrons injection (mechanism 1) whereas, for higher gate voltages,

the Vth considerably decreases, due to the hole accumulation at the p-GaN/AlN interface (mechanisms 2).

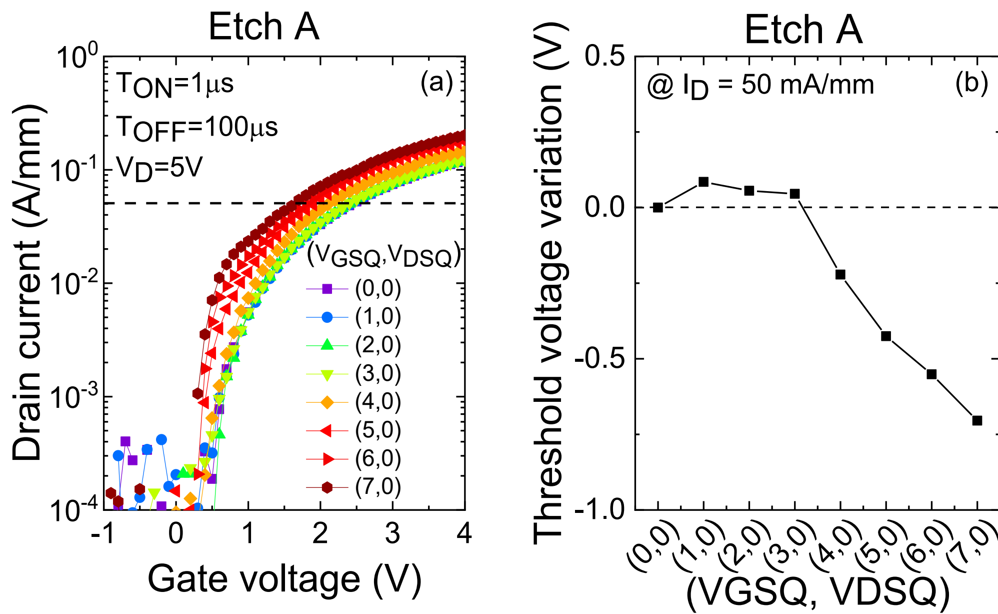


Figure 5.6 –Pulsed IdVg characterization of an Etch A sample (a) and corresponding Vth variation as a function of the applied baseline (b).

The results obtained from the double pulse analysis give insight into the trapping mechanisms occurring in the device, but no information on the time dependence of the trapping process can be acquired. The threshold evolution over the time is analyzed by means of a set of Vth transient measurements performed at different gate bias and different temperatures, as shown in Figure 5.7. The drain quiescent bias is 0 V, while the drain pulses are 5 V. The source is kept grounded during the whole measurement. The gate ramp, whose length is 10 μs, starts from 0 V up to 2.5 V.

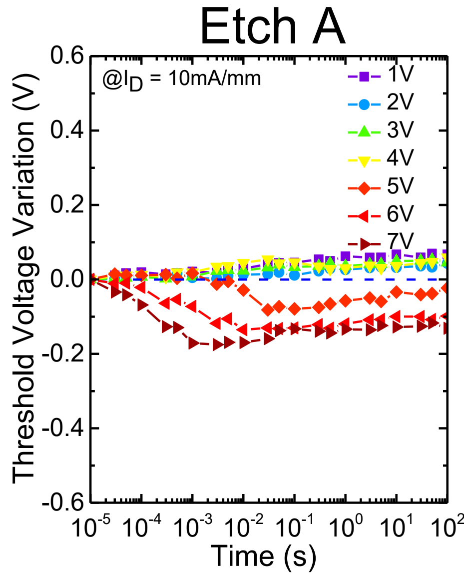


Figure 5.7 – Vth transient performed at different forward gate biases.

The threshold transient as a function of the gate bias clearly confirms the presence of the first two mechanisms previously discussed: for gate biases up to 4 V, the Vth tends to slightly increase due to the trapping of electrons within the AlGaN barrier layer, whereas, for higher gate biases, the hole injection causes the threshold voltage to decrease. The impact of the temperature on the trapping kinetic is evaluated by measuring the Vth transient in two bias conditions, respectively below and above the hole injection onset, for temperatures ranging from 30 °C to 150 °C. The results are shown in Figure 5.8.

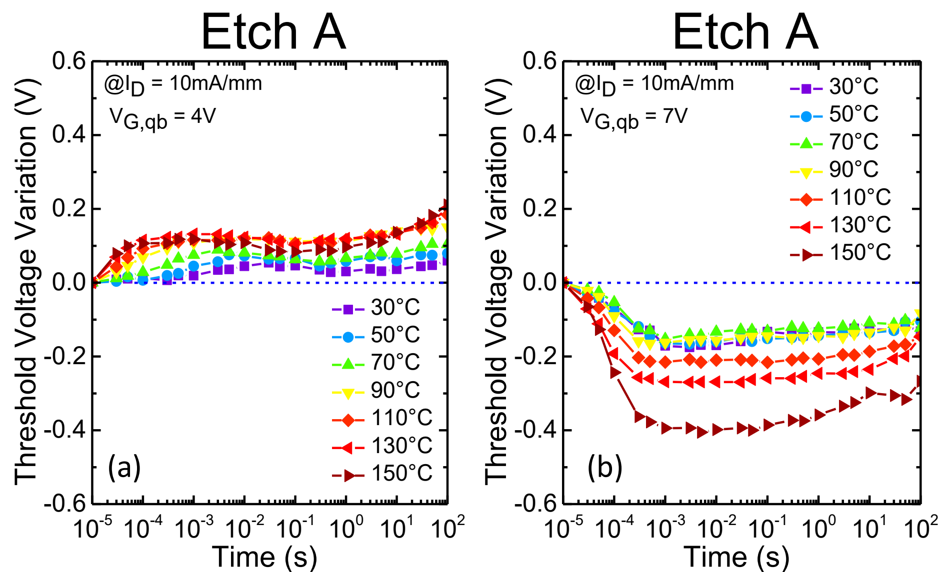


Figure 5.8 – Vth transient performed at different ambient temperatures ranging from 30 °C and 150 °C at gate bias of (a) 4 V and (b) 7 V.

The measurements demonstrate that both mechanisms 1 and mechanism 2 are thermally activated; moreover, in Figure 5.8 (a), the Vth positive shift which occurs after 1 s of stress, can be ascribe to mechanism 3. By fitting the Vth variation caused by the charge trapping with a linear function, the activation energy of the trapping process is estimated, and it results equal to 0.17 eV. This suggests that the electrons are trapped into an energy level located in the AlGaN approximatively 170 meV above the level of the 2DEG. A similar analysis (but fitting with an exponential function) is performed for the Vth transient measured at $V_G = 7$ V, and an activation energy for the trapping kinetics of 70 meV is obtained.

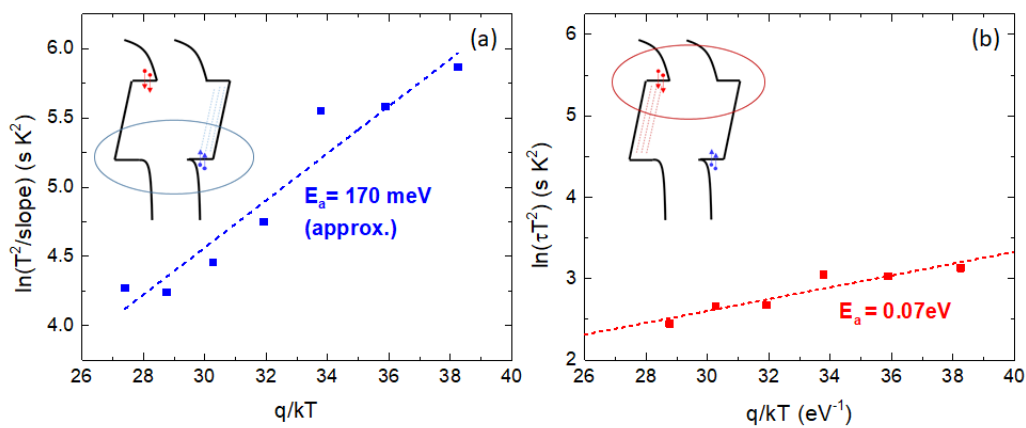


Figure 5.9 – Arrhenius plot of the trapping kinetics measured at (a) 4 V, where electrons are trapped and the threshold voltage increases, and at (b) 7 V, where the hole injection causes a negative Vth shift.

The hypothesis of the hole injection is also confirmed by comparing the temperature dependence of the Vth transient maximum amplitude, which is proportional to the amount of trapped charges, with the gate current. This correlation is clearly shown in Figure 5.10.

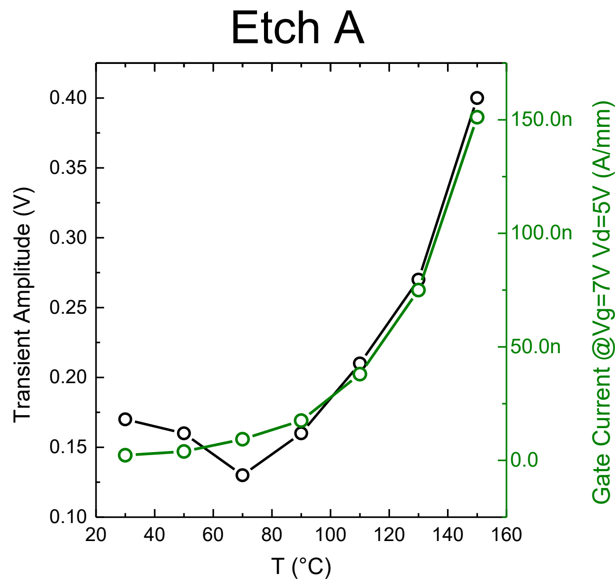


Figure 5.10 – transient amplitude at V_G = 7 V and gate leakage current at V_G = 7 V as a function of the temperature.

Finally, a comparison between two p-GaN etching processes for the gate module realization is carried out. The threshold voltage behavior over the time of a device fabricated with the Etch B process is characterized as a function of the forward gate bias baseline and compared with the same measurement performed on a device fabricated with the Etch A process. The comparison is shown in Figure 5.11, where the improvement obtained from Etch B process is clear. This suggests that the hole injection which causes the Vth instability occurs in the sidewalls of the p-gate layer, where the material is more defective.

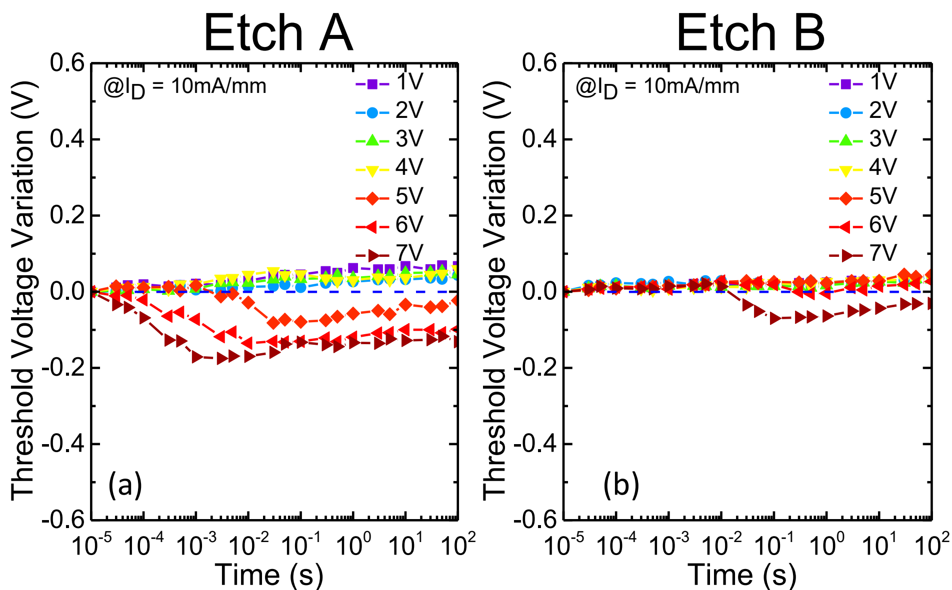


Figure 5.11 – Vth transient performed at different forward gate biases on a device processed with (a) Etch A and (b) Etch B.

5.2.2 Gate Stability and Robustness of In-Situ Oxide GaN Interlayer Based Vertical Trench MOSFETs (OG-FETs) [66]

The aim of the following analysis is to characterize the gate stability of vertical GaN-on-GaN trench gate MOS devices (Figure 5.12 (a)). The channel region of these devices lies on a regrown n-doped GaN layer, designed for limiting the impact of the trench etching process on the device performance. The gate dielectric is a 50 nm thick Al_2O_3 layer.

A preliminary pulsed analysis is carried out on a device in order to understand the dynamic behavior of the threshold voltage, thus evaluating the Vth stability. The setup used for this measurement is presented in [72]. The pulsed IdVg characteristic is measured for increasing forward gate biases from 0 V up to 12 V. The resulted curves, which are shown in Figure 5.12 (b), point out a shift of the Vth toward higher positive voltages, thus indicating that a trapping mechanism occurs when the device is biased in forward gate condition. Particularly, by analyzing the Vth behavior as a function of the gate quiescent bias point (Figure 5.12 (c)), it can be observed that the threshold voltage is remarkably stable for gate baselines lower than 5 V, while it starts to increase significantly for gate quiescent bias points higher than 6 V.

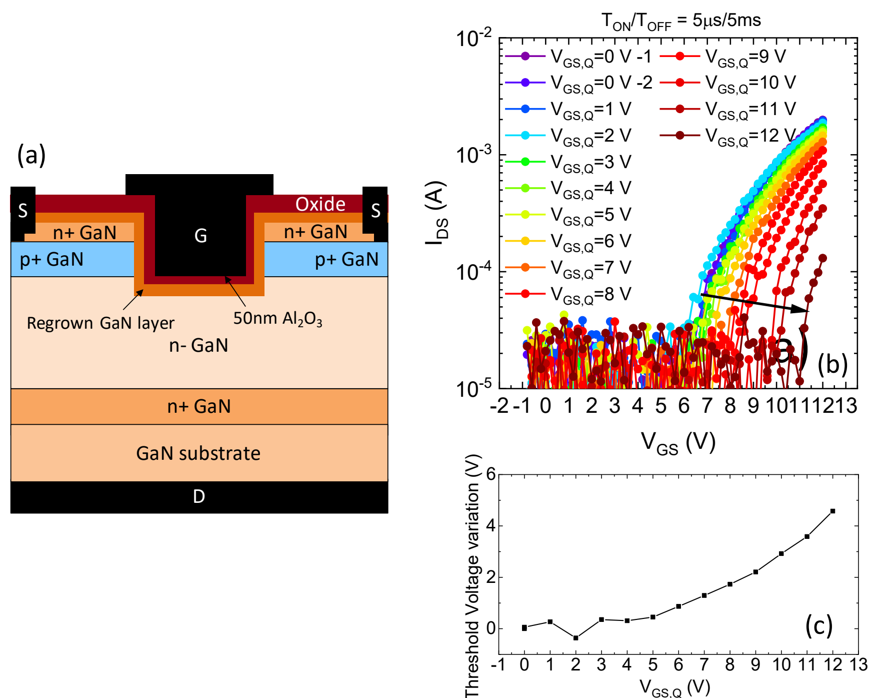


Figure 5.12 – (a) schematic representation of the tested devices; (b) pulsed IdVg measured at different forward gate quiescent bias points; (c) threshold voltage variation extracted from the pulsed IdVg carried out at different forward gate biases.

Further investigations on the trapping kinetic are carried out by means of the Vth transient setup, which was presented in the first paragraph of this chapter. The gate quiescent biases span from 5 V up to 12 V, while the drain quiescent bias is always zero. The Drain pulse voltage applied during the 10 μs-long IdVg characterization is 4 V. The IdVg characteristic is measured by sweeping the gate terminal from 4 V up to 12 V.

The threshold voltage transients are shown in Figure 5.13 (a) for increasing gate baselines. By analyzing the Vth transients, it is worth noticing that the Vth of the device under test linearly increases in a semi-log plot, meaning that the trapping process has a logarithmic time dependence. Moreover, the slope of the Vth transients increases with the increasing gate quiescent bias; by plotting the slope of the Vth-time curves as a function of the gate voltage which induces the threshold variation (Figure 5.13 (b)), a linear dependence is pointed out. The observed behavior was previously reported by Wolters and Verweij [73] and is caused by the injection of charges into a dielectric: once a charge is injected and trapped inside a material, its repulsive electrostatic effect prevents more charge to be injected, thus resulting in a reduced trapping probability and in a slower trapping process. This leads to a linear dependence of the Vth versus the log(time), as observed.

The threshold voltage transients are monitored also at higher temperatures, as shown in Figure 5.13 (c). The measurements are carried out with a gate quiescent bias of 8 V, for temperature ranging from 35 °C to 95 °C. The experimental results suggest a considerably low temperature dependence, thus confirming the field-related character of the injection process.

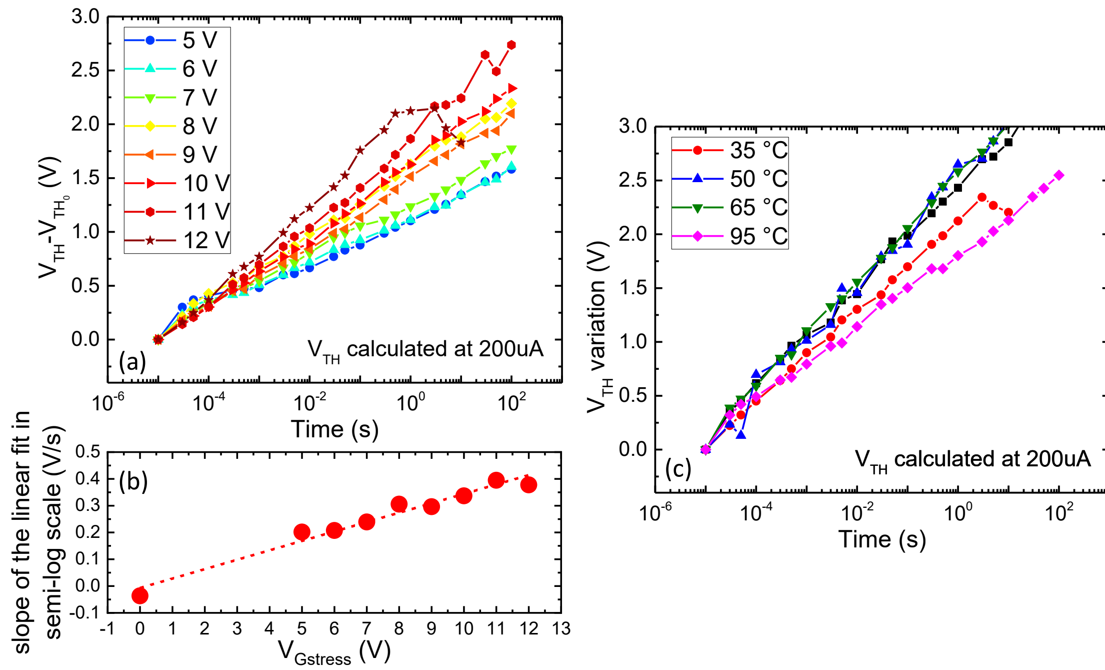


Figure 5.13 – (a) Vth transient carried out at different forward gate biases, and (b) respective Vth variation as a function of the V_G of stress. (c) Vth transient characterization performed at different temperatures.

Conclusions

This thesis discusses different aspects on the stability and reliability of Gallium Nitride based transistors grown on Silicon substrates, either High Electrons Mobility Transistors (HEMTs) and (semi-)vertical trench gate Metal Oxide Semiconductor (MOS) devices.

The vertical stack of lateral devices was widely characterized and studied. The "buffer decomposition experiment" allowed to investigate the role of the different layers that compose the vertical stack on the drain to substrate leakage current. It was shown that both the thickness and the composition of the epitaxial stack, beside enhancing the breakdown voltage, improve the material quality by limiting the propagation of defects and dislocations. The critical electric field of an AlN layer grown on silicon was measured to be 3.2 MV/cm at room temperature, and it was demonstrated that its failure is current driven and ascribable to a percolation process. The reliability analysis was also extended to a full GaN-on-Si stack, showing that the time to failure is (i) Weibull distributed, (ii) weakly temperature dependent and (iii) strongly impacted by the electric field. Moreover, the electroluminescence analysis showed that the failure might occur in a random position under the drain pad.

Beyond the reliability aspects of the vertical GaN-on-Si stack, the impact of the silicon substrate resistivity on the performance of the devices was investigated. It was demonstrated that the increasing substrate resistivity results in an improved robustness of the vertical stack thanks to a plateau region (i.e. a voltage range where the current stays nearly constant despite the increasing applied bias), which only occurs if a highly resistive substrate is used. It was also pointed out that within the plateau region is the threshold voltage of the devices considerably shifts. The latter is ascribed to the fact that – at high drain voltages – a considerable voltage-drop (in the range 150-200 V) falls on

the depleted Si substrate. Once the stress bias is removed, such voltage-drop leads to positive backgating effects which, in turn, results in the injection of electrons towards the buffer. Furthermore, it was demonstrated that the threshold variation is caused by a positive backgating bias resulting from the capacitive coupling of the depleted substrate (which only occurs if highly resistive substrates are used). The use of highly resistive substrate can improve the breakdown robustness; however, a trade-off between the vertical robustness and the threshold stability must be considered.

An additional topic analyzed within this thesis was the gate leakage and the gate capacitance behaviors of trench-gate (semi-) vertical MOS devices. The experiments allowed to locate the different leakage paths depending on the bias condition (forward or reverse gate voltage) and on the connection configurations (GD and GS). Moreover, the OFF-state leakage was investigated, showing that it is limited by the p/n^- junction until the failure of the gate dielectric due to the high electric field which possibly peaks at the trench bottom corner. Lastly, a comparison between different gate dielectrics was presented; the breakdown electric field of each material was estimated and the capability on limiting the gate losses was compared. Furthermore, it was proposed a model able to explain the gate capacitance behavior of a vertical trench-gate MOS device. The gate capacitance was split in four capacitive elements that contribute to the total trench capacitance, depending on the condition of the GaN at the dielectric/semiconductor interface. These contributions were analytically calculated, and they resulted to be comparable with the experimental results. Finally, a set of hysteresis capacitance measurements allows to estimate the bulk trap concentration of the gate dielectric, and to compare two different dielectric materials.

Within the final part of the thesis a novel custom setup was presented. The developed measurement setup allows to monitor the threshold voltage variations of a device in a wide time interval, ranging from 10 μs to 100 s, allowing the analysis of the trapping and detrapping kinetics as a function of the gate bias and of the temperature. This allows the full characterization of the traps involved in the threshold voltage shift.

List of publications

Journals

M. Borga, M. Meneghini, I. Rossetto, S. Stoffels, N. Posthuma, M. Van Hove, D. Marcon, S. Decoutere, G. Meneghesso, and E. Zanoni, "*Evidence of Time-Dependent Vertical Breakdown in GaN-on-Si HEMTs*", IEEE Trans. Electron Devices, vol. 64, no. 9, pp. 3616–3621, Sep. 2017, DOI:10.1109/TED.2017.2726440.

H. Amano et al., "*The 2018 GaN power electronics roadmap*" J. Phys. D. Appl. Phys., vol. 51, no. 16, p. 163001, Apr. 2018, DOI:10.1088/1361-6463/aaaf9d.

M. Borga, M. Meneghini, S. Stoffels, X. Li, N. Posthuma, M. Van Hove, S. Decoutere, G. Meneghesso, and E. Zanoni, "*Impact of Substrate Resistivity on the Vertical Leakage, Breakdown, and Trapping in GaN-on-Si E-Mode HEMTs*" IEEE Trans. Electron Devices, pp. 1–6, 2018, DOI:10.1109/TED.2018.2830107.

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