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Control of Grid-Tied Inverters for Nano-Grids

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List of Acronyms

ac Alternate Current

ADC Analog to Digital Converter

BIBCI Bidirectional Isolated Boost with Coupled Inductors

DB Dead Beat

dc Direct Current

DCCI Direct-Current-Controlled Inverter

DER Distributed Energy Resource

DFT Discrete Fourier Transform

DG Distributed Generation

DSO Distribution System Operator

DSP Digital Signal Processor

ESR Equivalent Series Resistance

FPGA Field Programmable Gate Array

GCF Grid Current Feedback

HCC Hysteresis Current Control

HMI Human Machine Interface

ICCI Indirect-Current-Controlled Inverter

ICF Inductor Current Feedback

IDE Integrated Design Environment

L-C-L Inductor-Capacitor-Inductor

LCO Limit Cycle Oscillation

LVRT Low-Voltage Ride Through

MAF Moving Average Filter

NLL Non-Linear Load

P Proportional

PCC Point of Common Coupling

PI Proportional Integral

PID Proportional Integral Derivative

PLL Phase-Locked Loop

PR Proportional Resonant

PV photovoltaic

R Resonant

rms Root Mean Square

SCR Short-Circuit Ratio

SM Synchronous Machine

SOGI Second-Order Generalized Integrator

SPC Synchronous Power Controller

SPWM Sine Pulse Width Modulation

THD Total Harmonic Distortion

UPS Uninterruptible Power Supply

VI Virtual Instrument

VSG Virtual Synchronous Generator

VSI Voltage Source Inverter

VSM Virtual Synchronous Machine

ZOH Zero-Order Hold

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Abstract

The traditional, centralized, top-down power distribution networks have been dominating worldwide over the past decades, as they represent an effective solution for the electrification of populated regions from a limited number of energy production sites. However, their rigid organization brings in some disadvantages, among which the unavoidable transmission losses, the need for expensive maintenance to ensure adequate reliability, the heavy reliance on fossil sources of energy are the main concerns. In recent times, with the development of renewables, the concept of micro-grid emerged, representing a novel bottom-up power distribution organization. The micro-grid can integrate the nearby distributed, and mostly renewable, energy sources, the storage devices and the loads into the grid, with increased efficiency, flexibility and reliability, showing significant economical and environmental benefits. An enormous interest has therefore been attracted in the field of micro-grids, testified by copious contributions to the technical literature and the definition of several related standards.

The micro-grid concept can be further scaled down to the range of a single house or small building, and differentiated by a new terminology, namely that of nano-grid. However, there is not much theoretical difference between nano-grids and micro-grids. The proposal of the nano-grid concept is aimed at simplifying the application scenarios, so that a hierarchical bottom-up power distribution network can be established, where the nano-grid plays the lowest-end role. It can not only operate autonomously, feeding the typical household appliances from the available renewable sources; thanks to the modular smart grid architecture, it can also be conveniently interconnected to other similar units, operating in parallel and harmoniously energizing a larger region in a city, a small-island or a village. In addition, the nano-grid also has the possibility of self-integrating into the util-

ity grid, exchanging power with the mains when needed, thanks to a specifically designed grid interface converter. Referring to the latter, a variety of requirements are defined by applicable standards, in terms of load power quality, grid support functionalities, abnormal condition ride-through and protection means, just to cite the most important ones.

The realization of the above functionalities is heavily dependent on the control of the grid interfacing inverter hosted within the nano-grid, about which numerous solutions have been proposed in the existing literature. However, few of them can realize all the functionalities simultaneously in a single controller. The target of this dissertation is therefore *proposing, analyzing and testing a high-quality, multi-functional control scheme for grid-tied inverters.* The intended application is in the above described nano-grid scenario, that simplifies the experimental validation significantly. However, most of the developed solutions can be easily adapted to higher power levels and different smart-grid architectures. The proposed inverter controller is capable to concurrently realize all the key functionalities required to operate as a grid interface converter, as well as to guarantee high stability margins and a flexible management of different operating modes.

This goal is reached in three steps: *i*) a deep literature review, *ii*) the identification, study and realization of the multi-functional inverter controller, and *iii*) the implementation of further, higher level functionalities, like the grid-supporting and parallel operation capabilities.

Accordingly, the study is initiated from step *i*), with an overview of existing control strategies and key functionalities of grid-tied inverters. The comprehensive review of a research topic is, in any case, very advantageous to define the state of the art solutions and to evaluate the margins for improvement in the existing technology. In this research case, it allowed to understand that a triple-loop controller structure is the most suitable to achieve high-performance control of the nano-grid electrical system and the most promising as to the capability of implementing multiple interface and protection functionalities jointly.

However, a great challenge for its implementation is how to reduce the control delays, so as to widen as much as possible the controller bandwidth. To solve this issue, in the second step *ii*), a large-bandwidth triple-loop controller is proposed, whose implementation is the first contribution of this dissertation. The peculiarity of the proposed controller is the

large-bandwidth control of the injected grid current, which brings in many beneficial features. Leveraging on this controller organization, multiple functionalities are later implemented by means of a superimposed, flexible mode-transition manager and an auto-tuner, altogether forming a high quality, multi-functional control scheme for grid-tied inverters. This represents the second contribution delivered by this dissertation. Finally, in step *iii*), the extended scenario of multiple parallel-connected grid-tied inverters is discussed, targeting the realization of distributed grid-supporting functionalities in grid-tied mode and the automatic balanced power sharing in parallel-islanded mode. The final implemented control scheme provides a feasible solution for the forthcoming smart nano-grids and represents the third contribution delivered by the Ph.D. research program.

To evaluate the proposed control schemes and solutions, a $3\,\mathrm{kVA}$ single-phase, hybrid nano-grid laboratory prototype has been installed. The prototype incorporates dc and ac sources, dc and ac loads, and a single voltage source inverter that interfaces the inner dc bus with the local ac bus and, ultimately, both of them with the utility grid. All comes quite naturally from the inverter topology, where an inductor-capacitor-inductor (*L-C-L*) output filter is exploited to generate a de-coupled, local ac bus.

At the control level, both digital signal processor (DSP) and field programmable gate array (FPGA) devices are used, so as to set-up a highly reconfigurable and flexible control platform. Control tasks are hierarchically distributed, based on their target bandwidth, among the different devices. As a general rule, sampling and low-level state variable controllers are implemented on programmable digital hardware, higher level control tasks, supervisory and monitoring functions are instead assigned to software programmable devices.

Extensive tests have been performed on this prototype, and the effectiveness of the proposed control scheme has been verified experimentally in a wide set of conditions, corroborating the theoretical analysis and, hopefully, supporting the research claims convincingly.

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Chapter 1

Introduction

1.1 Scenario of interest

Renewable energy resources, such as photovoltaic (PV) and wind farms, are nowadays more and more integrated in electrical power systems, contributing to the limitation of fossil fuel consumption. The integration process involves the electrical infrastructure at all levels, from high-voltage, three-phase to low-voltage, single-phase grids. Small-scale PV sources and batteries, especially, are typically being integrated directly into the latter, often at the consumer's premises [1–5], and coordinated by local dispatchers or controllers [6–8]. Fig. 1-1 displays a representative scenario, where electronic power converters are diffusely applied as interfaces among different electrical domains. In particular, grid-tied dc-ac converters, namely, inverters, are used to interface with the ac grid simple dc sources or more complex aggregations of energy resources and loads that may compose, by themselves, what we define as nano-grids. Nano-grids, indeed, indicate smaller scale, actively controlled aggregations of renewable energy sources, storage devices and loads [9] like, for example, those applicable to single houses or buildings, as shown in Fig. 1-1.

A peculiarity of smart nano-grids is to be fully controllable, dispatchable, and flexible power systems, that can operate in, at least, three different modes, depending on the state of the two switches SW_1 and SW_2, shown in Fig. 1-1. The former switch SW_1 is assumed to be controlled locally, i.e. by the inverter itself, while the latter SW_2 is supposed to be controlled remotely by, for example, the distribution system operator (DSO). In this thesis,

the three operation modes are defined as grid-tied (G), islanded (I), and autonomous (A), and present the following characteristics:

1. Grid-tied mode: SW_1 and SW_2 are both closed. Nano-grids are interfaced with the utility grid. The utility grid imposes the voltage, while the nano-grid behaves as a current source or, possibly, as a power source.

2. Islanded mode: in the event of faults of the utility grid, the disconnection of the nano-grids from the mains may be issued by upstream automation apparatuses as a safety measure. In this case, SW_2 is opened while SW_1 is closed. In response to this situation, the nano-grids can operate islanded, in which case they are typically controlled as voltage sources, feeding ac loads connected to the PCC and maintaining the voltage of the islanded system within suitable amplitude and frequency ranges.

3. Autonomous mode: nano-grids may intentionally disconnect from the PCC, by opening SW_1, and operate autonomously. In this case, the interface converter operates as a controlled voltage source for the local loads only.

In the application case of Fig. 1-1, grid-tied inverters play a key role. These devices are referred to in the literature by different names, intended to particularly emphasize one of the different possible converter tasks: *i*) *utility interface converters*, coupling ac nano-grids with an upper level ac power system [10–12]; *ii*) *grid interface converters*, coupling dc nano-grids with the main ac grid [13–16]; *iii*) *interlinking converters*, coupling dc with ac nano-grids [17–21]. In the following discussion, no such distinction is made, as the solutions presented in this dissertation are generally applicable to all the above mentioned cases.

In order to provide all the desirable functionalities, grid-tied inverters need to simultaneously achieve different control goals, the main ones, but not the only ones, being the following: 1) grid-tied, islanded and autonomous operation and seamless transitions among different modes; 2) resilience to main grid perturbations, like grid amplitude and frequency variations, voltage sags, low-order harmonics; 3) high grid-forming performance when utility grid is unavailable; 4) active harmonic filtering capability; 5) power flow control and 6) suitable damping of resonances.

Different control strategies for grid-tied inverters have been proposed, but, typically, only specific functionalities are considered, while the challenging development of a truly multi-functional system, comprising all the features 1) to 6) is not yet documented.

1.2 Investigated aspects and contributions

As shown in Fig. 1-1, the control of grid-tied inverters is complicated and hierarchical, including various aspects and control layers. In this thesis, the crucial aspects of the control hierarchy are investigated in a systematic way, which can be summarized as follows:

1. the study begins with an extensive *literature review*, focused on the existing control strategies and critical functionalities of grid-tied inverters;

2. based on the review work, a high-performance *triple-loop controller* structure is proposed, which shows superior performance in many respects;

3. on top of the triple-loop controller structure, a flexible *mode transition manager* is devised, which allows multi-mode operation and almost seamless mode transitions;

4. afterwards, robust, high-performance operation under weak grid conditions is enabled by implementing a novel *auto-tuning technique;*

5. eventually, the study is extended to multiple inverters and focused on the realization of *grid-supporting functionalities and parallel operation capabilities.*

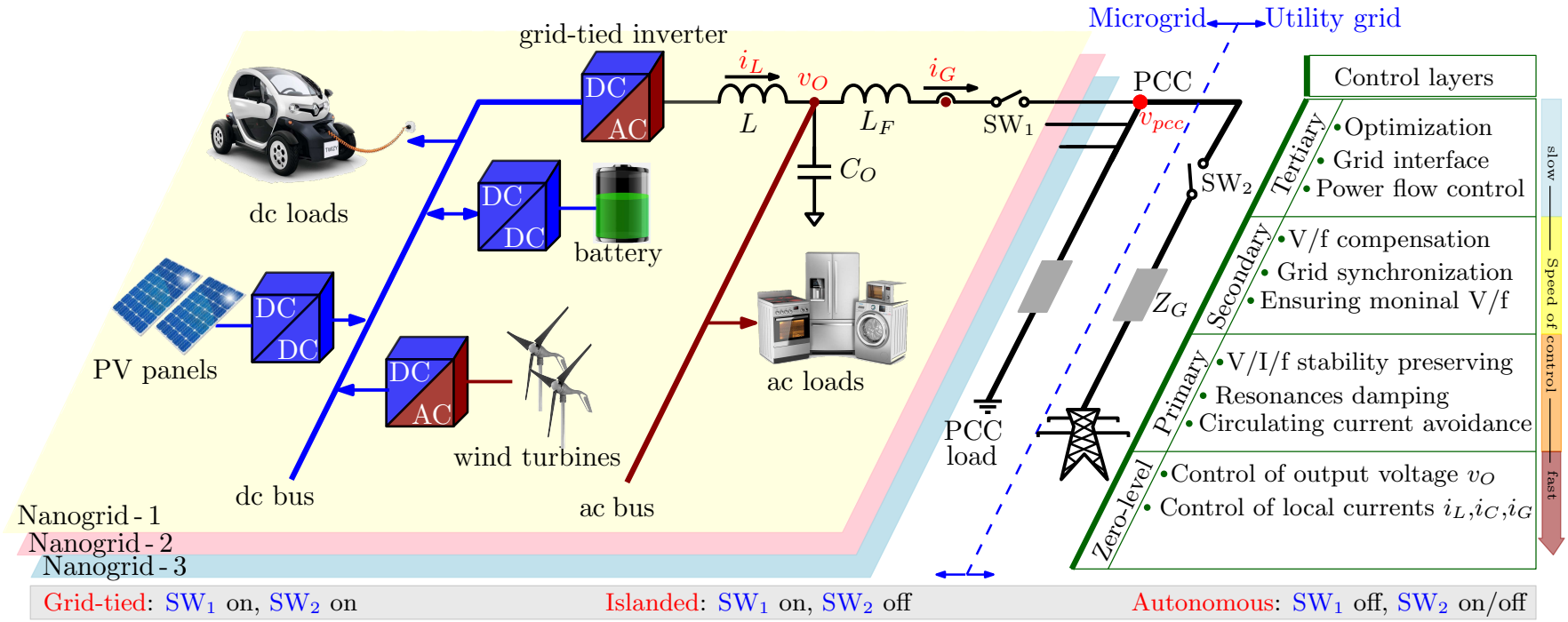


Figure 1-1: Nano-grid representation. Renewable sources, storage systems, loads, or combinations of them are interfaced to the ac distribution system by means of grid-tied inverters. Distributed inverters in nano-grids can be coordinated by hierarchically organized, higher-level control layers [22–26].

1.2.1 Review of control strategies and functionalities for grid-tied inverters

The grid-tied inverters in the scenario of Fig. 1-1 play an important role: they are involved in coupling dc and ac distribution buses, in contributing to feeding the local ac loads, in delivering the energy generated by the local resources to the grid, while complying with all the applicable regulation standards (e.g., IEEE standard 1547 [27]). To allow safe operation in the different modes and seamless transitions [28], accurate control design and good performance are crucial, especially when the upstream grid is weak.

The identification of robust, flexible, and high performance control solutions for grid-tied inverters in the outlined scenario has attracted a significant interest from the research community, as proven by the copious literature on the topic. Depending on the specific control strategy, different control features and performance can be achieved, requiring a proper selection of the most suitable strategies to satisfy the targeted control goals. The control solutions documented in the literature can be divided into the following groups: 1) ad-hoc solutions, tailored for particular problems, such as harmonic attenuation, active damping, smooth mode transitions; 2) multi-functional control, which aims at providing multiple crucial functionalities simultaneously; and 3) hierarchical control (see Fig. 1-1) for the overall system operation [23–26].

Review papers exist that are focused on nano-grid control concepts, development trends, and expected features from a system-level perspective [6,29–42], few of them deal with the small-scale applications that can be found in the low-voltage nano-grids scenario, considering the inverter-level control solutions [43–46].

Chapter 3 of this thesis aims at reviewing the possibilities and features of the different solutions, considering the main contributions in the field and providing information that support a proper selection of the control architecture. The contributions brought by Ch. 3 can be summarized as: 1) a survey of the control strategies for grid-tied inverters operating in the nano- and micro-grid scenario; 2) the identification of the main functionalities that have to be supported by the grid-tied inverters in the different operating modes; 3) the analysis of the applicability and effectiveness of the possible control strategies in implementing

the identified functionalities.

1.2.2 Large-bandwidth triple-loop controller

Based on the review work of Ch. 3, control strategies for grid-tied, *L-C-L*-filtered inverters can be categorized in: single-loop, double-loop, and triple-loop. Compared with single-loop and double-loop solutions, triple-loop control strategies offer superior overall performance. From this standpoint, the triple-loop controller is a promising solution, especially for the implementation of the so called multifunctional converters. As an example, in [47], the grid current, output voltage and capacitor current are fed back respectively from outer to inner, forming a triple-loop control structure. That makes the converter capable of providing continuous power to critical local loads and transferring seamlessly between grid-tied and islanded operation modes. However, the dynamic performance of the grid current loop and the harmonic rejection ability of the converter are negatively affected by the long response delay of inner loops, as these are regulated by proportional-integral (PI) controllers with relatively low bandwidth. Beside that, as the converter current is not directly controlled, serious overloading can be expected if, e.g., voltage sags occur. That is an important reason why, in [48], the control target of the innermost loop is replaced by converter current, forming another possible triple-loop organization. However, as both grid current and output voltage loops are regulated by proportional resonant (PR) controllers, the system is potentially sensitive to weak grids, where voltage sags and frequency perturbations can be frequently encountered. Additionally, the harmonic attenuation and power control performance does not seem to be competitive, again because of the long settling times associated to resonant controllers. In conclusion, large bandwidth grid current control is the key to improve the overall performance of grid-tied inverters, especially when nano-grid interfacing is concerned.

A large-bandwidth triple-loop control strategy is therefore proposed in Ch. 4, whose purpose is exactly to enable the implementation of a large-bandwidth controller for the grid current. The converter current is controlled, in the inner loop, by a dead-beat (DB) regulator achieving ideal system damping and fast inverter over-current protection. The

intermediate, output voltage loop is also introduced and controlled by a DB-type regulator, to guarantee seamless mode transitions as well as to provide uninterrupted high-quality voltage for critical local loads. Thanks to the adoption of two nested DB type regulators, sufficient flexibility is gained to design a relatively fast PI controller ($1\,\mathrm{kHz}$ bandwidth, equal to $1/20$ of the switching frequency) for the outer, grid current control loop. The proposed control strategy shows overall high-performance and brings in simultaneously many favorable features, all of which will be discussed and experimentally verified in Ch. 4.

1.2.3 Multi-mode operation and seamless mode transitions

Grid-tied inverters interface nano-grids with the ac main grid and are expected to operate grid-tied, islanded and autonomously, as introduced in Sec. 1.1. The capability of transitioning among different modes of operation is therefore an important functionality. However, due to a variety of reasons, significant current and voltage spikes can easily occur across the transitions, which makes the mode transition control a challenging task.

Transitions between different operation modes should be performed autonomously and seamlessly, in order to avoid unwanted voltage and current transients [49]. Being this a fundamental functionality, extensive research on mode transition techniques has been reported in the literature. The proposed solutions can be generally divided into three categories according to the implemented controllers: i) droop-control based approach [50–52], ii) current control based approach [47, 53–59] and iii) hybrid approach [60].

In case i), the grid-tied inverter is controlled as a voltage source both in grid-tied and islanded operation modes. However, the harmonic behavior in grid-tied mode depends on the particular power network configuration and, in particular, on the harmonic content of the main grid voltage [61]. In addition, as the grid current is not directly controlled, even a small mismatch between local and grid voltage can result in significant inrush current during the mode-transition [51].

In case ii), when grid-tied, the inverter is controlled as a current source while, in islanded mode, it is controlled as a voltage source. The controller's architecture thus changes with the mode of operation. If managed properly, an uninterrupted output voltage (i.e., ca-

pacitor voltage) can be maintained, which is crucial for critical local loads [59]. However, in grid-tied mode, controllers with multi-loop structures usually present a narrow bandwidth of the outer current loop, due to inner loop delays [47]. In this case, high quality control of the injected grid-current cannot be guaranteed, especially under heavily distorting local loads or in weak grid conditions.

An alternative option for mode-transition control can be the combination of droop and current control, as indicated in case iii). For instance, in [60], the output voltage reference is defined together by the grid current regulator and droop controller, whose contributing proportions are adjusted based on inverter operation modes. This may be a suitable solution in smart grids applications, where multiple inverters are parallel connected. However, the disadvantages of this method are also the combination of case i) and ii).

In Ch. 5, a flexible *mode-transition manager* is proposed, based on the large-bandwidth triple-loop controller organization of Ch. 4. It simultaneously achieves: 1) all the favorable features brought by the triple-loop controller; 2) seamless and autonomous mode transitions between any two different operation modes; 3) low-voltage ride-through capability.

1.2.4 Weak grid operation

Typically, low-voltage single-phase grids are characterized by limited power capability and mainly resistive connection impedances, which, due to the varying power absorption from loads and the intermittent power generation from renewables, bring to grid parameters that are variable both from point to point and over time. The IEEE standard 1204 [62] describes the behavior of an ac power system by stiffness measures that refer to both static and dynamic performance indexes. The short-circuit ratio (SCR) is an index referring to the static grid behavior, being defined as the ratio between the short circuit power and the power of the installed generator. On the other hand, the dynamic grid characteristics are evaluated in terms of inertia, that is, by the capability of the ac power system to keep the grid frequency constant in the presence of variations in the power flow. Stiff grids, namely, grids whose voltage is negligibly affected by power flow and load characteristics, show high SCR and inertia; *vice-versa*, grids whose voltage is significantly affected by power

flow variations are said to be weak and typically show both low SCR and low inertia. It has been shown that low grid stiffness significantly impairs power quality [63], limits the effectiveness of active damping [64], affects control performance of inverters [65], and degrades the stability of converter/grid connections [66]. These non-ideal characteristics make the control of the inverters tied to weak grids particularly challenging.

In these conditions, the typical stability assessment methods, like those based on the Middlebrook criterion [67], are complicated by the uncertain and typically time-varying characteristics of the grid impedance. Indeed, although a series resistive-inductive structure is always maintained [66], both the magnitude and the X/R ratio of the grid impedance are subject to significant variations among the different inverter connection sites and over time. Several papers have shown how suitably shaping the converter output impedance by control design effectively enhances the converter-grid connection stability. From this standpoint, control bandwidth maximization and control delay minimization [68], active damping techniques [69, 70], proper feed-forwarding strategies [71] are all effective provisions. Grid synchronization methods [72] may also be source of relevant stability issues. Grid synchronization is often performed by a phase-locked loop (PLL), whose performance affects the low-frequency behavior of the converter, especially under weak-grid conditions [73]. While this instability may be conveniently exploited in some situations [74], it is, in general, an issue that requires dedicated provisions, like, for example, the tuning of the PLL regulator based on grid impedance estimations [75].

Besides maintaining stability, a grid-tied inverter should be capable of tolerating or, better, rejecting different kinds of exogenous perturbations often encountered in weak grids. These range from voltage frequency or amplitude variations to voltage harmonics that, if not dealt with properly, lead to more detrimental effects, like increased distribution losses, wearing of components (e.g., transformers windings), circulating harmonic currents. A satisfactory performance is therefore as important as stability.

Solutions documented in the literature that aim at complying with power quality standards [27] include repetitive controllers [76], resonant controllers [63, 77], feed-forward of the point of common coupling (PCC) voltage [78], feedback of capacitor voltage [79]. Unfortunately, achieving robust stability and performance at the same time is difficult, because

provisions that give stronger benefits in stability tend to penalize the inverter performance and the other way round.

The solution proposed in Ch. 6 aims at overcoming this undesirable trade-off. It is based, once more, on the triple-loop controller structure proposed in Ch. 4. An *auto-tuning technique* is then developed that adapts the controller to the actual grid characteristics, yielding a much wider stability region and robust performance. The proposed auto-tuning technique *i*) requires minimal *a-priori* knowledge of the grid impedance at the point of connection, *ii*) shows little sensitivity to grid voltage harmonics and other perturbations (i.e., ensures robust performance), and *iii*) can be adapted and applied to any digital PI controller.

1.2.5 Grid-supporting functionalities and parallel operation

From the perspective of primary control, the autonomous power sharing between inverters in both grid-tied and islanded modes has been extensively studied, typically taking inspiration from the operation of synchronous machines. Droop controls [80], virtual synchronous machines (VSMs) [81], and virtual oscillators [82] are some important examples. In this domain, the droop control is a ubiquitous strategy, as it allows automatic synchronization and power sharing between inverters without the need of mutual communication [80], also while operating in an islanded system. Basic droop control replicates the *static* behavior of synchronous machines (SM), linking the control of output voltages with the active and reactive powers without including the effect of rotor inertia, which, however, helps in smoothing grid frequency variations across transients [83–85]. Lately, more sophisticated methods are gaining ground, that aim at a more accurate emulation of the synchronous machine behavior. VSM approaches mimic more accurately the behavior of synchronous machines, also in dynamical terms; examples can be found in [86–88]. Different flavors of VSM emulation can be found in the literature [83]; prominent examples include the virtual synchronous generator (VSG) [86], the power-synchronization control [89], the synchronous power controller (SPC) [88] and the synchroconverters [87]. The virtual oscillators ensure system stability, but present inherent non-linear features [90] making modeling and

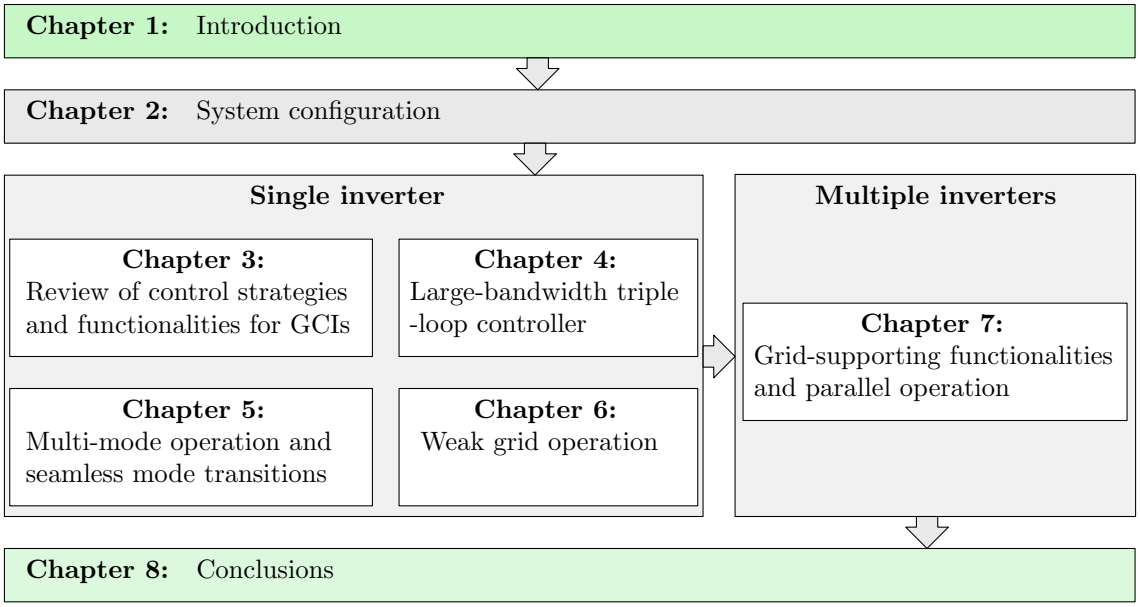


Figure 1-2: Structure of the thesis.

analysis more complex.

Similarly to droop controllers, VSMs employ inverters controlled as voltage sources, which not only enables steady-state grid-support at voltage or frequency changes, but also allows inherent automatic and balanced power sharing in islanded mode. In addition, VSMs, thanks to the emulation of machine inertia [91], dynamically support the grid during voltage or frequency transients, which eases power system regulation [92]. On the other hand, grid current control allows lower circulating harmonics, which is beneficial in terms of power quality, protection effectiveness, and, in a broad sense, system stability. That is why it is interesting and challenging to achieve simultaneously the favourable features brought by droop/VSM and grid current control.

An harmonious combination of various local power quality control functionalities can be effectively obtained by the high performance, triple-loop inverter controller organization proposed in Ch. 4, based on which, Ch. 7 investigates and shows the possibility of implementing *i*) grid supporting capabilities, and *ii*) the parallel operation of more converters, also when islanded from the utility grid.

1.3 Structure of the thesis

The content of this thesis is distributed in 8 chapters, as displayed in Fig. 1-2. Ch. 1 provides a general introduction of the research topic, by describing the scenario of interest, summarizing main research aspects and providing a whole picture of the thesis. A single-phase hybrid nano-grid testbench is presented in Ch. 2; being a highly reconfigurable, flexible, scalable and reliable testing system, it offers the possibility and convenience of studying and verifying different control strategies.

Given its complexity and hierarchical characteristics, the discussion of the grid-tied inverter control is split in two cases: *i*) single converter, and *ii*) multiple converters. Case *i*) is the main focus of this thesis, supported by 4 chapters: from Ch. 3 to Ch. 6. In Ch. 3, from the perspective of a single inverter, an extensive review and comparison of existing control strategies and crucial functionalities is offered. With the panoramic view, it is very convenient to find that multi-loop control strategies are superior in concurrently realizing multiple functionalities, that are equally important for nano-grids. In light of this, a large-bandwidth triple-loop controller organization is proposed in Ch. 4, which brings in many favorable features. To make the interface converter ready for the forthcoming scenario of nano-grids, a flexible mode controller is proposed in Ch. 5, aiming at realizing multi-mode operation and seamless mode transitions of the grid-tied inverter. In Ch. 6, a critical working condition, the weak grid, is considered. To deal with this issue, an auto-tuning technique is proposed, which allows automatic and rapid adjustments of the downstream triple-loop controller, on the basis of online estimation of control loop bandwidth and phase margin.

In Ch. 7, the study is extended to the case of multiple paralleled converters. A power flow control strategy is proposed for the purpose of 1) implementing grid-supporting functionalities, 2) allowing automatic power dispatching among multiple converters in islanded mode, and 3) keeping all the high-performance achieved in Ch.4, Ch.5, Ch.6. Eventually, Ch.8 concludes the dissertation.

Chapter 2

System configuration

This dissertation deals with the development of a flexible and high-performance multi-functional control scheme for grid-tied inverters, mainly intended to be used in nano-grids. In the interpretation adopted in this dissertation, a nano-grid corresponds to the electrical power system of a single house/building. In order to enable the required experimental verification of the different control solutions, a laboratory single-phase nano-grid testbench has been designed and is currently being implemented, that will be briefly described in the following sections.

2.1 Nano-grid architecture

Being a small-scale power entity, the nano-grid shows inherent modular nature, which makes it convenient to create larger power networks by means of interconnecting multiple nano-grids, forming a micro-grid structure. So doing, and following a bottom-up approach, a hierarchical power distribution system can be established, from nano-grids to micro-grids, then to the national utility grid, as shown in Fig. 2-1. To realize the aforementioned hierarchy of power distribution, a variety of nano-grid architectures has been proposed. Simplifying to some extent the plethora of different proposals, nano-grids can be roughly categorized into three types, as presented in Fig. 2-2: dc nano-grids, ac nano-grids and hybrid nano-grids.

Given the dc nature of the majority of renewable sources and the abundance of elec-

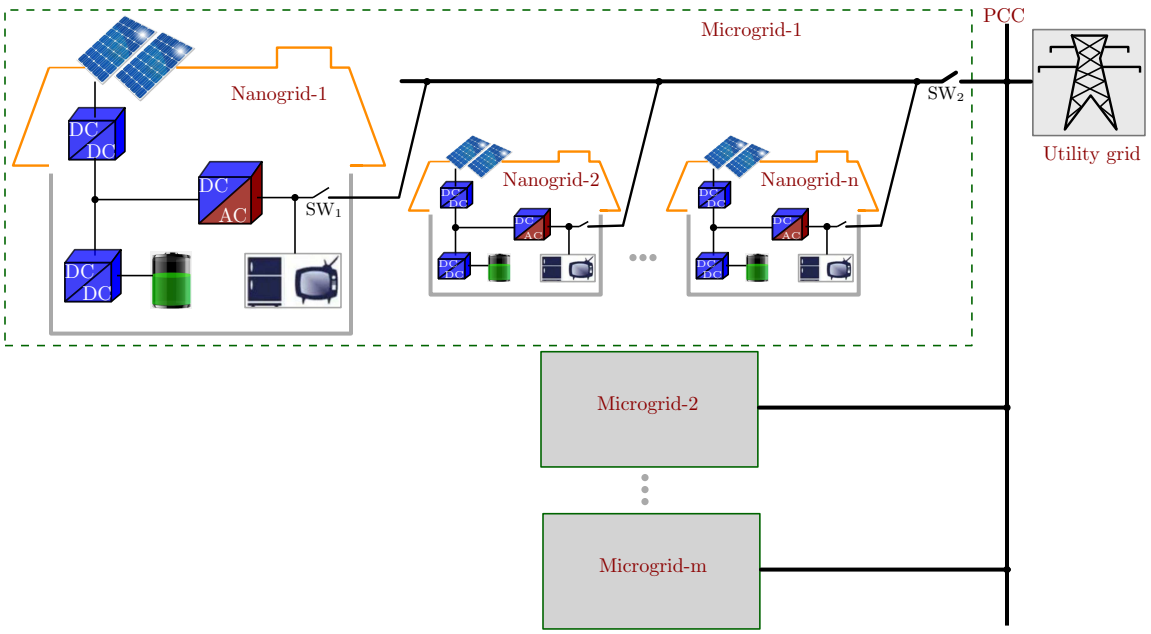
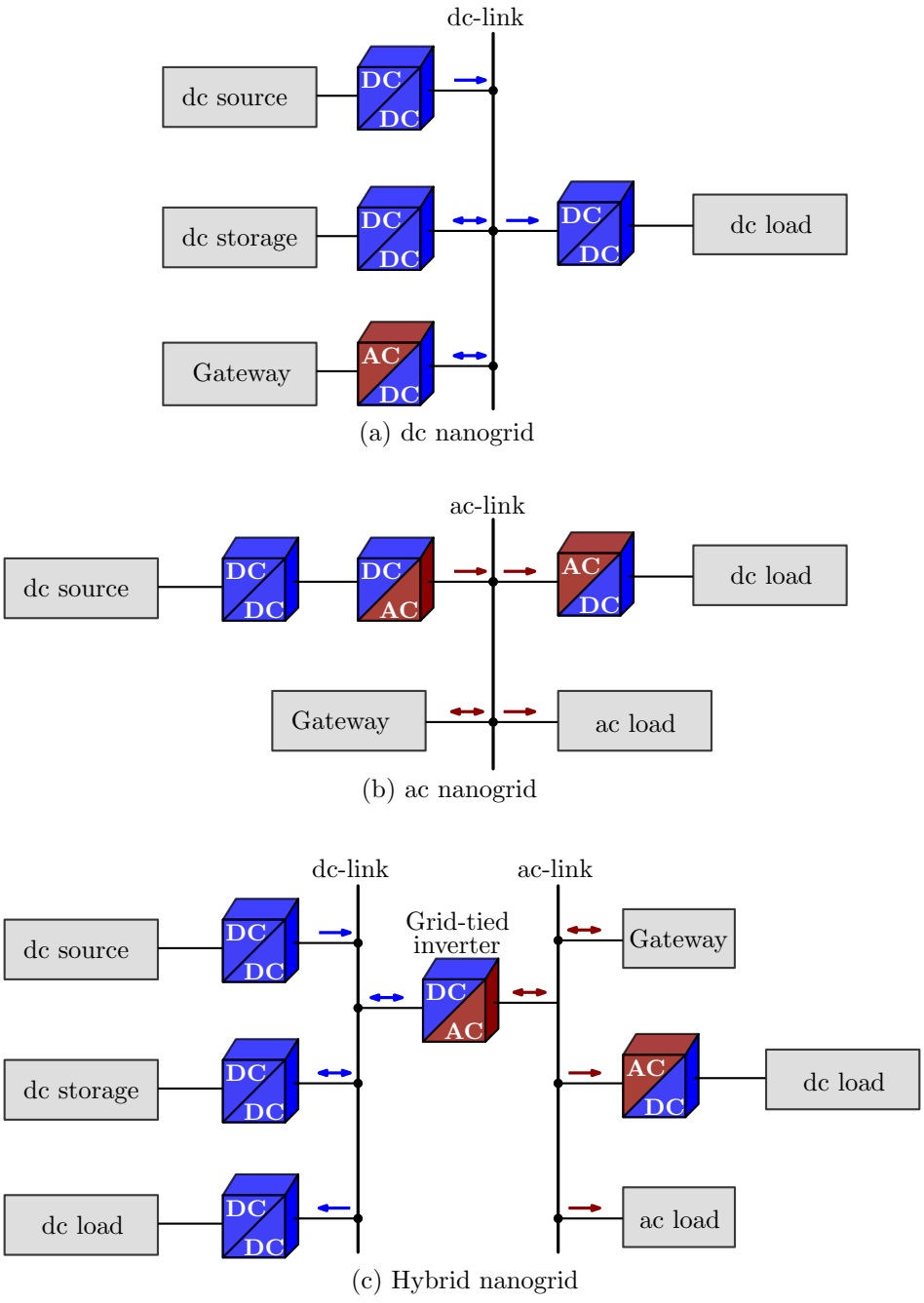


Figure 2-1: Hierarchical power distribution: utility grid → microgrid → nano-grid.

tronic loads in the low-voltage domain, dc nano-grids (Fig. 2-2 (a)) are recently attracting significant interest as a promising means to improve the overall efficiency of electrical energy utilization. These can be directly interfaced with the ac power systems and (virtually) operate as bidirectional power sources, offering power flow control at their point of connection [13–16].

In ac nano-grids, as shown in Fig. 2-2 (b), loads and sources located relatively close to each other are clustered in organized electrical systems. These systems typically interface with the ac distribution grid at PCC, through which they can provide enhanced power quality (e.g., compensation of reactive and harmonic currents, voltage support) and power flow control (e.g., dispatchability, demand-response) by exploiting local generation, storage and control flexibility [10, 11]. Thanks to the integration of Distributed Energy Resources (DERs), loads, and control, ac nano-grids can operate also islanded, namely, isolated from the mains, offering extended operating ranges for the hosted loads and isolation from exceptional conditions, anomalous phenomena or faults affecting the utility grid.

The synergistic and concurrent operation of ac and dc nano-grids is also possible by interlinking the corresponding ac and dc buses, as shown in Fig. 2-2 (c). This allows to form the so called hybrid nano-grids [17–21], which are expected to combine the advantages of



(a) dc nanogrid

(b) ac nanogrid

(c) Hybrid nanogrid

Figure 2-2: Possible nano-grid architectures.

the two realms and obtain even wider flexibility.

2.2 Nano-grid testbench installation

A laboratory nano-grid testbench is currently being implemented as shown in Fig. 2-3 for in depth study and control strategy verification. The goal of the testbench is powering a variety of loads, facilitating the study of grid-tied inverter control, including power flow control, load sharing, system stability, protection, etc..

The structure of the implemented nano-grid is of hybrid type, and is configured as follows:

- the dc side integrates a PV source, a battery stack and an ultra-capacitor by means of appropriate dc-dc converters ($1.5\,\mathrm{kVA}$ of each), which convert low dc source voltages to the nominal high dc-link voltage (V_{DC});
- a single-phase dc-ac converter ($3\,\mathrm{kVA}$) is used as the grid-tied inverter to connect the dc and ac sides;
- an *L-C-L* type filter is employed for harmonics filtering and to decouple to local ac bus from the utility grid;
- a controllable switch SW_1 is used to connect the nano-grid to the utility.

The main parameters of the nano-grid are listed in Tab. 2.1.

Table 2.1: Parameters of the implemented nano-grid testbench in Fig. 2-3.

Parameter	**Symbol**	**Value**	
Nominal voltage of dc link	V_{DC}	450	V
Nominal voltage of ac link	V_N	230	V
Nominal current of ac link	I_N	13	A
Nominal frequency of ac link	f_0	50	Hz

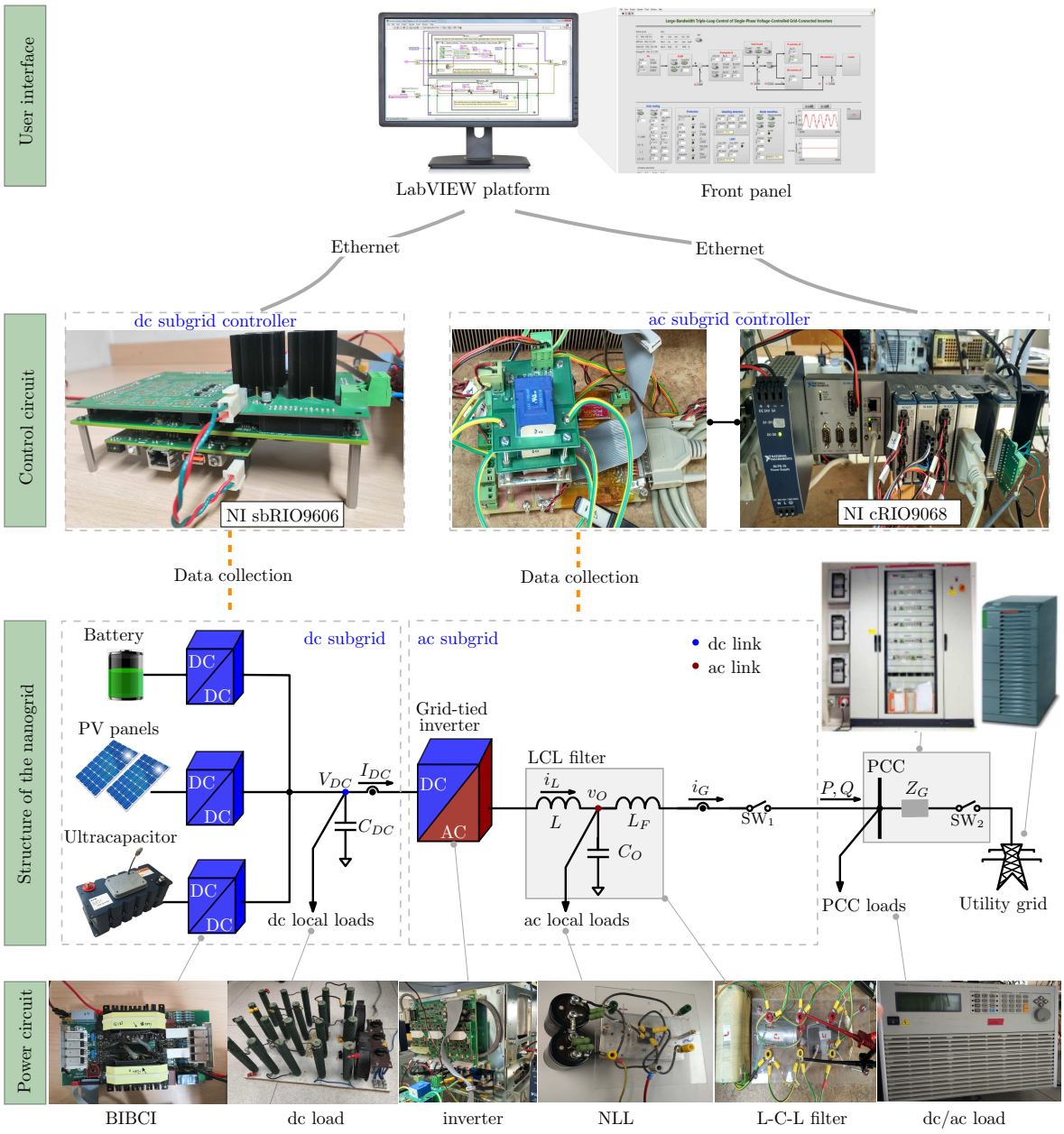


Figure 2-3: Structure of the implemented nano-grid testbench.

2.2.1 Implementation of power circuits

From the perspective of power circuits, converters of dc-dc, dc-ac and ac-dc types are used within the nano-grid, to manipulate the electrical energy generated or stored in the system and to meet specific requirements (see Tab. 2.1) in supplying the different loads.

2.2.1.1 Battery/ultra-capacitor-interfacing converter

Battery/ultra-capacitor-interfacing converters are required in the nano-grid architecture to connect the battery and ultra-capacitor, whose nominal voltage is 48 V, with the inverter dc link, whose nominal voltage is 450 V. Significant efforts have been devoted to realize the required high step-up converters, as discussed in [93, 94].

For safety reasons, galvanic isolation has been considered mandatory from the start, making the numerous non-isolated dc-dc converters documented in the literature, such as [95, 96], not applicable. What's more, to support the charge and discharge processes, the converters have to allow bi-directional power flow. As a result, a high step-up, bidirectional and isolated boost topology has been designed to serve as the battery/ultra-capacitor-interfacing converter. It is indicated as the Bidirectional Isolated Boost with Coupled Inductors (BIBCI) [97] converter, whose topology is shown in Fig. 2-4. The main circuit parameters are instead listed in Tab. 2.2.

The working principle and control strategies of the BIBCI can be found in [97], that illustrates how the converter can satisfy all the functional requirements of an ultra-capacitor/battery manager. The BIBCI is selected also for the following reasons: *i*) the degree of freedom associated with the coupled inductor turns ratio allows to achieve high step-up ratios, while keeping the switch stress at a reasonable level; *ii*) the low voltage side current is inherently filtered and naturally presents low high frequency ripple *iii*) the coupled inductor leakage inductance is exploited to transfer energy between the two sides of the converter; *iv*) zero voltage turn-on of all switches is achieved in a wide load range. All of these favourable features make the BIBCI an almost ideal choice for the bi-directional coupling of very asymmetrical dc sources/sinks.

Finally, it is worth noting that, at the time of writing, the battery is not yet installed in

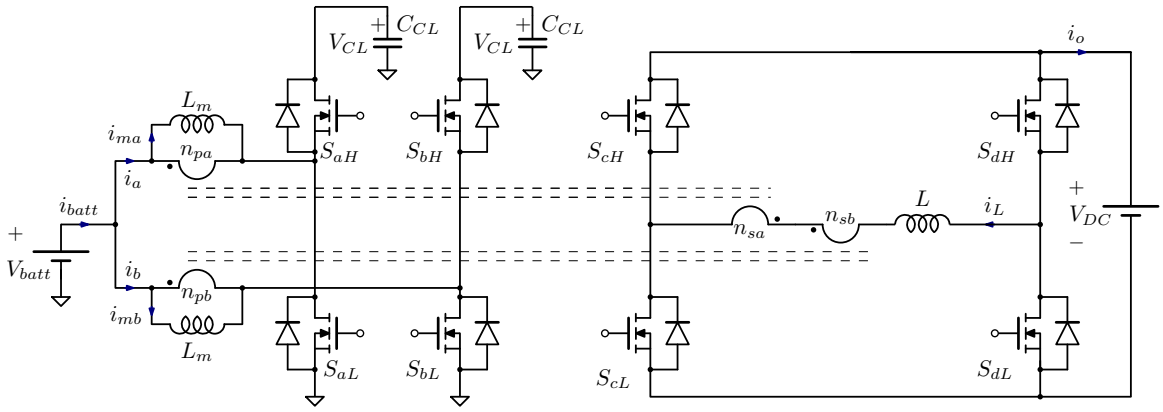


Figure 2-4: Topology of the BIBCI converter, that is used as the PV source, ultra-cap and battery interfacing converter in the nano-grid testbench.

the testbench. Instead, the $83\,\mathrm{F}$ ultra-capacitor, produced by Maxwell, is currently being tested, interfacing it to the dc link via a couple of parallel connected BIBCI units. When the set-up will be completed, hopefully in a few months from now, the battery will be likewise connected to the dc-link and its controller suitably integrated in the dc-subgrid control system, which is described in the following.

Table 2.2: Parameters of the BIBCI converters in Fig. 2-3.

Parameter	**Symbol**	**Value**	
Nominal power of PV-interfacing converter	S_{pv}	1.5	kVA
Nominal power of battery-interfacing converter	S_{batt}	1.5	kVA
Nominal battery voltage	V_{batt}	48	V
Nominal dc link voltage	V_{DC}	450	V
Switching frequency	$f_{sw_{DC}}$	60	kHz
Magnetizing current relative ripple	r_{im}	0.6	pk-pk
Clamp capacitor relative voltage ripple	r_{CL}	0.25	pk-pk
Maximum siwtch voltage stress	$V_{sw_{max}}$	100	V

2.2.1.2 PV-interfacing converter

The PV-interfacing converter, similarly to the battery/ultra-capacitor-interfacing converter, requires a step-up, isolated boost topology. However, due to the unidirectionality of the PV source, both unidirectional and bidirectional converters are applicable. For simplicity,

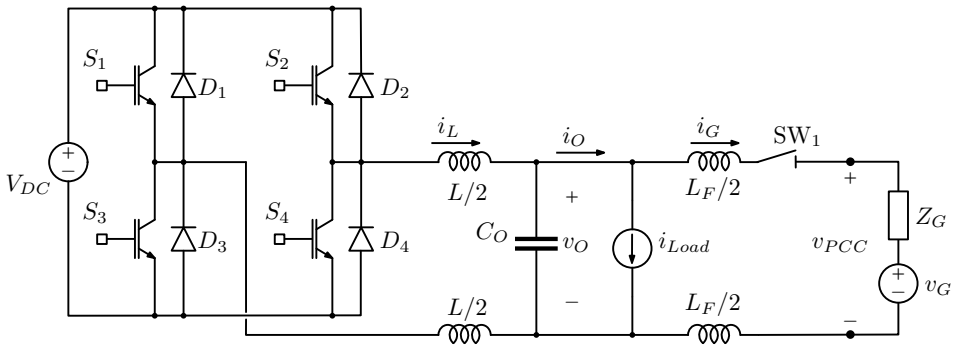


Figure 2-5: Topology of the grid-tied inverter and *L-C-L* filter.

modularity and because costs are not relevant at this stage of the research activity, the same topology, BIBCI, has been selected also for the PV-interfacing converter.

2.2.1.3 Grid-tied inverter

In connecting the nano-grid to the mains, bi-directionality is mandatory, as it allows, on the one hand, free power exchange between the dc and ac buses within the nano-grid itself, while, on the other hand, it enables the nano-grid to interact with the mains, e.g. to deliver and draw electrical power from the external distribution system when needed.

The classical full bridge topology is selected to implement the grid-tied inverter, as presented in Fig. 2-5. For simplicity, the grid-tied inverter is implemented by exploiting a SEMIKRON commercial converter (IGD-1-424-P1N4-DL-FA) which is available in our lab. The converter integrates voltage, current and temperature sensors, making it very convenient for control and protection. In addition, the embedded IGBT driver board integrates SKYPER 32PRO driver cores, sensing circuitry for dc-link voltage, currents, heat-sink temperature. Thus, significant hardware-developing time is saved and a high-reliability is guaranteed as well. The main parameters of the grid-tied inverter are reported in Tab. 2.3. As can be noticed from the IGBT characteristics, a significant over-rating is applied, so as to minimize the impact of unintentional current transients and operate safely even in faulty conditions. Given the target of the study and the already mentioned irrelevance of cost issues at this stage of the research, this oversizing has been considered a valuable safety measure.

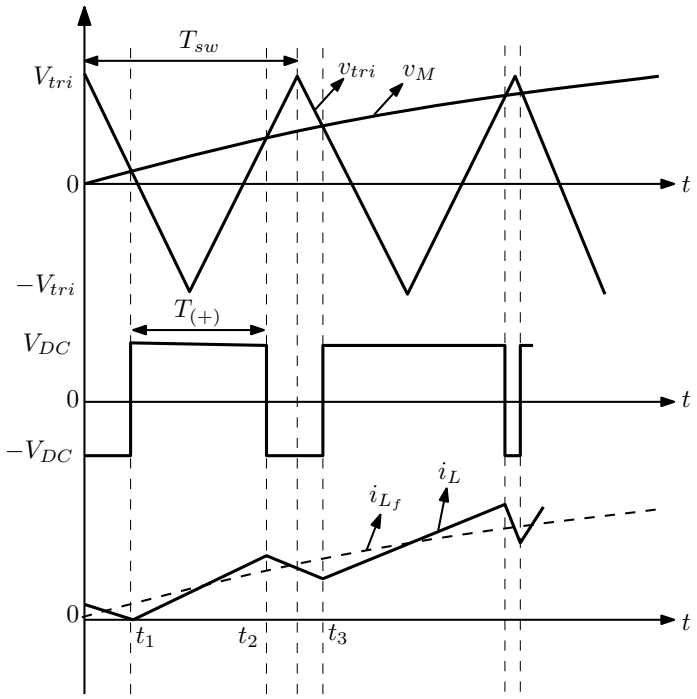


Figure 2-6: The converter-side current under bi-polar SPWM control.

2.2.1.4 *L-C-L* filter

The *L-C-L* filter is used for the purpose of reducing high-frequency harmonics generated by the grid-tied inverter, but also to establish a local ac bus, whose terminals are the filter capacitor's ones, that will be closed loop controlled. Likewise, the presence of an inductor between the local ac bus and the grid will enable the closed loop control of the current injected into the mains. Clearly, compared with conventional L filter, the *L-C-L* filter significantly enhances the attenuation performance of switching harmonics, with a reduced overall size, weight as well as, if properly designed, cost [98]. The *L-C-L* filter has a significant impact on the overall performance of grid-tied inverter control system, so that extensive studies have been conducted on its design methodology in previous works, like [99, 100]. For convenience, the design procedure of the implemented *L-C-L* filter is now summarized.

(a) *Design of the converter-side inductance L*

Fig. 2-6 shows the converter-side current of the full bridge under bi-polar SPWM control, indicating as i_{L_f} the fundamental component of converter-side inductor cur-

rent (i_L). In addition, T_{sw} is the carrier period ($T_{sw} = 1/f_{sw}$), v_M and v_{tri} are respectively the modulation and carrier signals.

- When $v_M > v_{tri}$, $v_{inv} = V_{DC}$, it is easy to derive

$$L\frac{di_L}{dt} = V_{DC} - v_O \tag{2.1}$$

where v_O is the capacitor voltage.

The capacitor voltage v_O changes slowly during a modulation period, so that the converter-side inductance current is assumed to increase linearly, namely,

$$\Delta i_{L(+)} = \frac{V_{DC} - v_O}{L} T_{(+)} \tag{2.2}$$

where, $T_{(+)} = t_{12}$.

- When $v_M < v_{tri}$, $v_{inv} = -V_{DC}$,

$$L\frac{di_L}{dt} = -V_{DC} - v_O. \tag{2.3}$$

In this case, the inverter-side inductance current is assumed to decrease linearly,

$$\Delta i_{L(-)} = \frac{V_{DC} + v_O}{L} T_{(-)} \tag{2.4}$$

where $T_{(-)} = t_{23}$.

The slow variation of v_O along the line cycle makes $T_{(+)}$ and $T_{(-)}$ time varying. Considering the grid voltage source to be ideal, the capacitor voltage can be assumed equal to the grid voltage at any time, since the voltage drop on the grid side filter inductor is typically negligible at line frequency. As a result, the fundamental component of converter output voltage can be written as

$$v_O(t) \approx v_G(t) = M_r V_{DC} \sin 2\pi f_0 t, \tag{2.5}$$

where f_0 is the fundamental line frequency, yielding

$$\begin{aligned} T_{(+)}(t) &= \frac{v_M(t) + V_{tri}}{2V_{tri}} T_{sw} = \frac{1}{2} T_{sw}(M_r \sin 2\pi f_0 t + 1) \\ T_{(-)}(t) &= T_{sw} - T_{(+)}(t) = \frac{1}{2} T_{sw}(1 - M_r \sin 2\pi f_0 t) \end{aligned} \tag{2.6}$$

where M_r is the inverter modulation index, which needs to be always lower than 1, at least in the steady-state.

Substituting (2.5) and (2.6) into (2.2) and (2.4), after simple calculations, we get

$$\Delta i_{L(+)} \cong \Delta i_{L(-)} = \frac{V_{DC} T_{sw}}{2L}(1 - M_r^2 \sin^2 2\pi f_0 t) \tag{2.7}$$

Then, the maximum ripple amplitude of the converter-side current can be expressed as

$$\Delta i_{L(max)} = \frac{V_{DC} T_{sw}}{2L}. \tag{2.8}$$

Accordingly, the minimum value of the converter-side inductance can be defined by

$$L_{(min)} = \frac{V_{DC} T_{sw}}{2\Delta i_{L(max)}}. \tag{2.9}$$

In the considered system, the maximum allowable ripple of converter side inductor current $\Delta i_{L(max)}$ is designed as $8\,\mathrm{A}$, so that the calculated inductance value is $1.41\,\mathrm{mH}$. In practice, a slightly reduced value of $1.40\,\mathrm{mH}$ has been manufactured and used in the prototype converter.

(b) Design of the capacitance C_O

In the *L-C-L* filtered full bridge inverter, the filter capacitor may need a substantial reactive power supply, which increases the overall conduction losses in the inverter. So, it is necessary to take reactive power into consideration in the design of the capacitor and to size it properly. Assuming that λ_c is the ratio of the absorbed reactive

power Q_{C_O} with respect to rated active power P_N, that is

$$\lambda_c = \frac{Q_{C_O}}{P_N}, \tag{2.10}$$

it is possible to write the following design equation:

$$\begin{aligned} Z_{C_O} &= \frac{V_O^2}{Q_{C_O}} = \frac{1}{jw_o C_O}, \\ V_{O_{max}} &= V_G. \end{aligned} \tag{2.11}$$

where $V_G = V_N$ is the nominal grid rms voltage. Accordingly, the maximum value of the capacitance, the one that keeps the reactive power below the specified limit, can be calculated as follows

$$C_{O_{max}} = \lambda_c \frac{P_N}{2\pi f_0 V_N^2}. \tag{2.12}$$

Considering a relatively large reactive power ratio, namely, $\lambda_c = 0.15$, the calculated capacitance is $27\ \mu\text{F}$. In practice, a $30\ \mu\text{F}$ capacitor is selected.

(c) Design of the grid-side inductance L_F

The grid side inductor can be sized by evaluating the residual high-frequency current ripple the inverter is going to inject into the grid and imposing a suitable upper limit. The limit can be conveniently expressed in relative terms, assuming as the reference the expected rms grid current I_N, that is measured, e.g., when the inverter is delivering or absorbing the nominal active power. To this purpose, it is convenient to derive the relation between the voltage v_{inv}, generated by the converter, the grid current i_G and the grid voltage v_G. It can be expressed as:

$$v_{inv}(s) = (LL_F C_0 s^3 + Ls + L_F s) i_G(s) + (LCs^2 + 1) v_G(s), \tag{2.13}$$

based on which, it is immediate to get

$$G_{LCL}(s) = \frac{i_G(s)}{v_{inv}(s)} = \frac{1}{L\,L_F C_0 s^3 + (L + L_F)s} = \frac{1}{(L + L_F)s} \cdot \frac{w_r^2}{w_r^2 + s^2} \tag{2.14}$$

Table 2.3: Parameters of the grid-tied inverter and *L-C-L* filter in Fig. 2-3.

Parameter	Symbol	Value	
Nominal power of grid-tied inverter	S_N	3	kVA
Switching frequency	f_{sw}	20	kHz
Filter inductance	L	1.40	mH
Inductor equivalent resistance	ESR_L	60	mΩ
Output capacitance	C_O	30	μF
Line inductance	L_F	0.55	mH
Inductor equivalent resistance	ESR_{L_F}	75	mΩ
L-C-L filter resonant frequency	w_r	9188	rad/s
ac grid frequency	$f_o = f_{v_{pcc}}$	50	Hz

where $w_r = \sqrt{\frac{L+L_F}{LL_FC_0}}$, is the resonance frequency of the *L-C-L* filter.

Because for the bi-polar SPWM controlled full bridge inverter the most significant injected switching noise is located at $f_{sw} = 20\,\mathrm{kHz}$, it makes sense to assume the resonant frequency of the *L-C-L* filter is such that $2\pi f_{sw} >> w_r$. As a result, the filter attenuation of the switching frequency noise can be approximated as

$$\frac{|i_G(j2\pi f_{sw})|}{|v_{inv}(j2\pi f_{sw})|} = \frac{1}{|LL_FC_0(j2\pi f_{sw})^3 + j2\pi f_{sw}(L+L_F)|}. \tag{2.15}$$

By defining $\lambda_f = |I_G(j2\pi f_{sw})|/|I_N|$, the minimum grid-interfacing inductance can be derived as

$$L_{F(min)} = \frac{1}{LC_0(2\pi f_{sw})^2 - 1}\left(L + \frac{|V_{inv}(j2\pi f_{sw})|}{2\pi f_{sw}\lambda_f I_N}\right), \tag{2.16}$$

where $I_G(j2\pi f_{sw})$ and $V_{inv}(j2\pi f_{sw})$ indicate, once again, the rms value. Setting $\lambda_f = 0.05\,\%$ according to the grid interfacing requirements for injected currents[27], from (2.16) $L_F = 0.58\,\mathrm{mH}$ is found. In practice, the inductance of L_F is implemented as $0.55\,\mathrm{mH}$.

Eventually, the designed parameters of *L-C-L* filter are reported in Tab. 2.3 and tested performance under ideal grid condition is provided in Fig. 2-7.

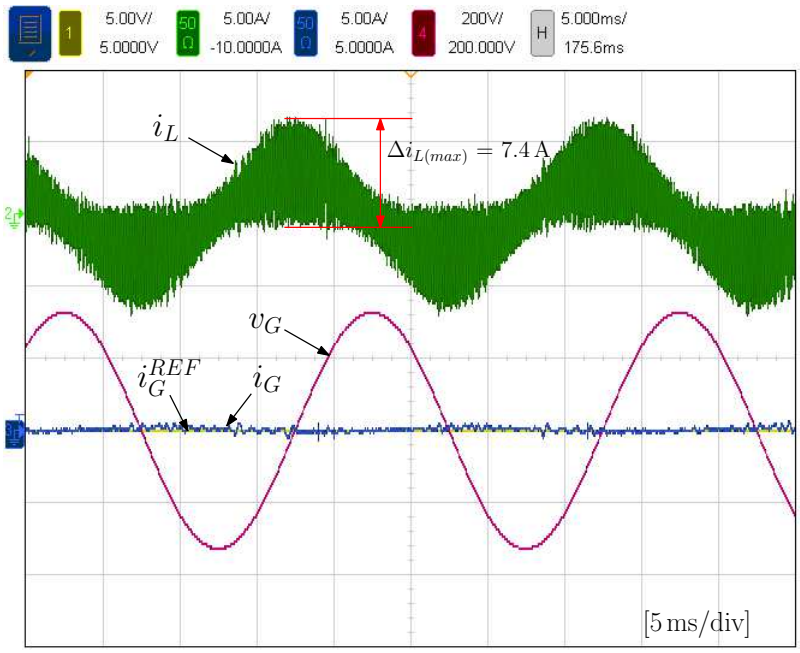


Figure 2-7: Tested performance of the designed *L-C-L* filter under ideal grid condition.

2.2.1.5 Loads

As shown in Fig. 2-3, loads of both dc and ac type are integrated in the hybrid nano-grid testbench. A reconfigurable resistor array (4×5, each one is $27\,\Omega$) is connected at dc link (indicated by the blue dot), playing the role of a local dc load. On the ac link (indicated by the red dot in the figure and corresponding to voltage v_O), a non-linear load (NLL) is connected, which is implemented by means of a diode rectifier. Topology of the non-linear load is shown in Fig. 2-8. Additionally, an electronic load (Chroma programmable ac/dc load 63804) can be adopted, acting as a PCC load or an additional ac/dc load. The configuration is not fixed, rearrangement of the loads, like adding, removing and swapping positions, is allowed for different testing scenarios. A summary of the load characteristics is given by Tab. 2.4.

2.2.1.6 Utility grid

The utility grid is implemented by means of an $80\,\mathrm{kVA}$ electronic ac source, that is used as a grid emulator. This allows the convenient customizing of different grid conditions, guarantees galvanic isolation from the mains and offers a high degree of protection for the

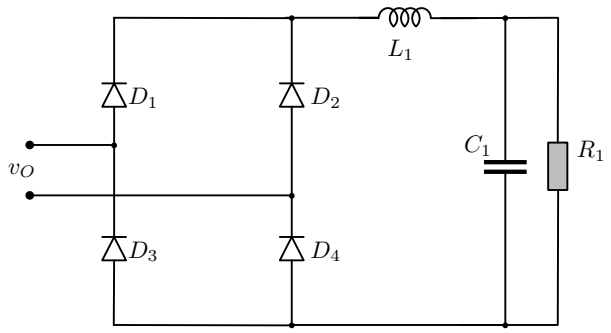


Figure 2-8: Topology of the non-linear load.

Table 2.4: Summary of implemented loads in Fig. 2-3.

Load	Connecting point	Parameter	Value	
Reconfigurable resistor array	dc link	R_{DC}	$4 \times 5 \times 27$	Ω
Non-linear load	ac link	L_1	3	mH
		C_1	2000	μF
		R_1	180	Ω
		Crest factor	2.6	
Electronic load	PCC	Chroma 63804		

nano-grid testbench. The safety of the operators during experiments is also significantly enhanced. Being its rating very large with respect to the nano-grid interface dc-ac converter, the grid emulator, by default, represents a practically ideal grid.

However, inside the cabinet of the nano-grid switch-gear, the length of the cables that link the grid emulator and the nano-grid can be adjusted, making it easy to modify the equivalent grid impedance. Likewise, all the useful sections (battery/ultra-capacitor input, PV source input) can be interconnected by adjustable distribution cables, allowing the emulation of different nano-grid layouts.

What has been described so far represents the 'body' of the hybrid nano-grid testbench. However, to run the system properly, a smart 'brain' is also needed, that is represented by the control system, introduced in the following section.

2.2.2 Implementation of the control system

As briefly mentioned in Sec.1.2, control of a hybrid nano-grid can be fairly complicated, as it presents a multi-layer hierarchical organization, covering a series of functions that have been briefly outlined before. In order to guarantee high-performance of the control system, some key requirements and features need to be taken into account at the early stage of control platform development, the main ones being: reliability, scalability, configurability and flexibility. More specifically:

- reliability refers to the controller capability of operating properly in the experimental testbench, for a given amount of time, presenting adequate robustness and tolerance with respect to the typically encountered conditions, including electro-magnetic noise, thermal stress, electrical transients. It is considered the essential characteristic for the task at hand;

- scalability is the property of the controller to handle a growing amount of tasks by adding resources to the system. For example, under some circumstances, adding more ADC or DAC channels, implementing new control algorithms, or integrating third-party instruments;

- configurability corresponds to the possibility for the operators to tailor, to some extent, the controller to their needs by adjusting the main regulator parameters or selecting predefined options like, for instance, modifying over-current protection thresholds;

- flexibility implies the capability for the operators to change conveniently the controller organization, e.g. excluding some parts of it in response to different scenarios, like different operation modes, facilitating the experimental tests.

In the above list the first two items constrain mostly the hardware of the control platform, while the last two are more related to the quality of the integrated design environment (IDE) that supervises the configuration and programming of the control platform.

Generally, in the field of nano-grids, the control system can be implemented either on a DSP or on a FPGA platform. The DSP is a specialized microprocessor, typically pro-

grammed in C language. It is suited to complex math-intensive tasks but, on the other hand, is limited in performance by its clock frequency and the sequential execution of its program. In contrast, an FPGA is programmed in a hardware description language (e.g., VHSIC Hardware Description Language or Verilog). The programming phase defines the physical connections of the available logic gates so as to realize a large set of sequential and combinational logic functions, from basic ones, e.g. multipliers, registers ..., to more complex ones, like computational engines, encoders/decoders ... Thanks to its parallel operation capability, the device is superior in performing ultra-fast tasks, but is limited by the available gates, whose number is finite, and by other chip non-idealities, like, e.g. the clock distribution lines or the number of I/O pins.

As far as the memory is concerned, both DSP and FPGA typically have a limited amount of internal storage; but a DSP is typically optimized for use of external memory. Because both DSPs and FPGAs have pros and cons and excel in different aspects, an optimal control solution could be represented by the integration of the two devices in a single control system, which will allow the programmer to intelligently split the control tasks between the DSP and the FPGA domains.

This is an ideal solution for a complicated control system like that of nano-grids and perfectly suits its hierarchical organization, where very different computational speeds are required. Indeed, the fast and time-critical tasks can be allocated onto the FPGA chip, while relatively slow and memory-hungry functions are more effectively allocated on the DSP.

In addition, a common programming environment, allowing the user to easily set-up reconfigurable human machine interfaces (HMIs), together with monitoring and data logging functions is considered essential, to minimize the development time of the control system and the achievement of the above mentioned key features.

In light of these considerations, the control system of the nano-grid testbench utilized in this study is implemented as follows:

- *Dc subgrid control platform:* a NI sbRIO 9606 is exploited for the purpose of dc-subgrid control. The single-board compactRIO 9606 is an embedded controller that integrates a real-time processor, a reconfigurable FPGA, and I/Os on a single printed

circuit board. Some characteristics of sbRIO 9606 are reported in Tab. 2.5. A custom-designed interfacing board is used to connect the control circuit, i.e. the single-board compactRIO 9606, with the three target power circuits, the PV-/battery- and ultra-capacitor-interfacing converters. Important signals in dc-subgrid are measured by current and voltage sensors that are mounted on the PV-/battery- and ultra-capacitor-interfacing converters, then filtered and amplified to desired ranges by the interfacing board, and eventually sent to the sbRIO 9606 for manipulation. The sbRIO 9606 generated gate signals directly drive the PV-/battery- and ultra-capacitor-interfacing converters, forming a feedback controlled system.

Although the detailed discussion of the dc-subgrid control system and its performance is not within the scope of this dissertation, it is worth adding a few details, as these are essential for the correct interpretation of the results presented in this thesis. The most important feature of the dc subgrid controller is its capability to achieve a relatively large bandwidth, above $1\,\mathrm{kHz}$, in the dc link voltage controller. This allows the dc subgrid to appear, from the grid-tied inverter's standpoint, as a stiff dc voltage source, almost as stiff as a laboratory dc power supply.

As a result, the ripple on the dc link voltage at twice the line frequency is kept to very low levels, in the order of $1-2\%$ of its nominal voltage. The power pulsation is indeed absorbed by the ultra-capacitor current, passing through the BIBCI converter connected to the dc link.

This set-up makes the inverter controller capable of its maximum performance. In addition, the ultra-cap provides an energy storage with enough power density to allow an almost complete de-coupling of the battery from any fast power transient. The battery, in other words, will only feed the dc link with the average requested power, while all the fast fluctuations and transients will be absorbed by the ultra-cap. Once again, cost is not considered an issue at this stage, whereas maximum performance is what is mostly sought for.

Other important dc-subgrid control functions are needed to operate the nano-grid system properly, such as the supervisory control of the dc link voltage, including, e.g.

Table 2.5: Characteristics of NI sb-RIO 9606.

Component	Specifications
FPGA type	Xilinx Spartan-6 LX45
Real-time processor	1-core, 400 MHz
Nonvolatile memory	512 MB
DRAM	256 MB
USB	1 port
CAN	1 port
RS-232 Serial Ports	1 port
Network interface	Ethernet, 1 port

Table 2.6: Specifications of NI c-RIO 9068.

Component	Specifications
FPGA type	Xilinx Zynq 7020
Real-time processor	2-core, 667 MHz
Nonvolatile memory	1 GB
DRAM	512 MB
USB	1 port
RS-232 Serial Ports	2 ports
RS-485 Serial Ports	1 port
Network interface	Ethernet, 2 ports
Slots for C series modules	8
Adopted C series modules	NI9223, NI9263, NI9401

the capability to curtail the power flowing from the PV source and the battery/ultra-capacitor management logic. None of these will be discussed in this thesis, however, as they represent the object of another Ph.D. student's research.

- *Grid-tied inverter control platform:* similarly, a NI cRIO 9068 is exploited for the purpose of grid-tied inverter control. The device is a powerful embedded system, which combines a dual processor-core, a reconfigurable FPGA and eight slots for modules of the series C in a chassis. Important parameters of NI cRIO 9068 are given by Tab. 2.6. In the ac-subgrid, signals sampling is performed by means of various C series modules, which are flexibly assembled in the chassis, as shown in Fig. 2-3. The availability of surplus slots allows flexible modification and convenient extension of the developing testbench. In addition, it also facilitates system tests

by outputting simultaneously multiple control variables, which can be visualized directly on an oscilloscope. Once again, a custom-designed interfacing board is used to bridge the grid-tied inverter with the control platform cRIO 9068, with the functionalities of isolation, signal conditioning and hardware protection. At a later stage, the inverter controller will be migrated to a second sbRIO board, for better modularity and compactness.

- *User interface:* as far as the software development of DSP and FPGA is concerned, it often requires a long-time training of specialized programming languages and time-consuming debugging processes, especially for the case of the FPGA chip. Instead, both sbRIO 9606 and cRIO 9068 are programmed in the LabVIEW© based IDE. The IDE brings in many advantages, for example 1) the extremely straightforward graphical programming language allows complex programming tasks to be accomplished in a fraction of the time if other programming languages were used; 2) the LabVIEW programming is uniform across all targets; 3) it provides a series of add-ons and plug-ins to help speed up the program development; 4) it automatizes a lot of details of FPGA programming (at the expense of non-optimal gate usage and memory occupation), so that the users can focus just on their control algorithms; 5) it provides different running modes, allowing, for example, the user to interact at run-time with the VIs (the basic program modules in the LabVIEW language) deployed on the FPGA through a PC front panel.

  By taking advantage of LabVIEW, an user interface can be developed easily, from where operators can send commands and receive feedback signals at run-time. An example is given in Fig. 2-9, where the cRIO 9068 is considered. As can be seen in Fig. 2-10, its program can be divided into three parts: the user interface VI, real-time VI and FPGA VI. In the implemented system, the user interface VI operates in the host PC, while the other two run on the board processor and FPGA respectively. Communication between the host PC and the device is accomplished by Ethernet, while signal transmission within the device is allowed by the PCI bus available on-board.

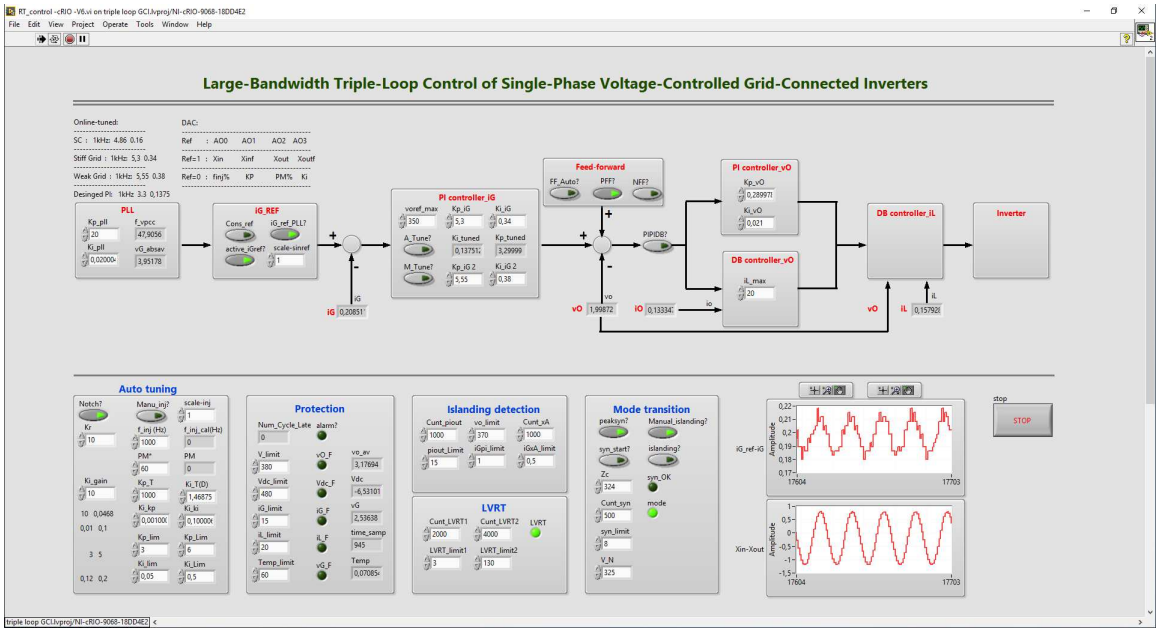


Figure 2-9: The implemented user interface.

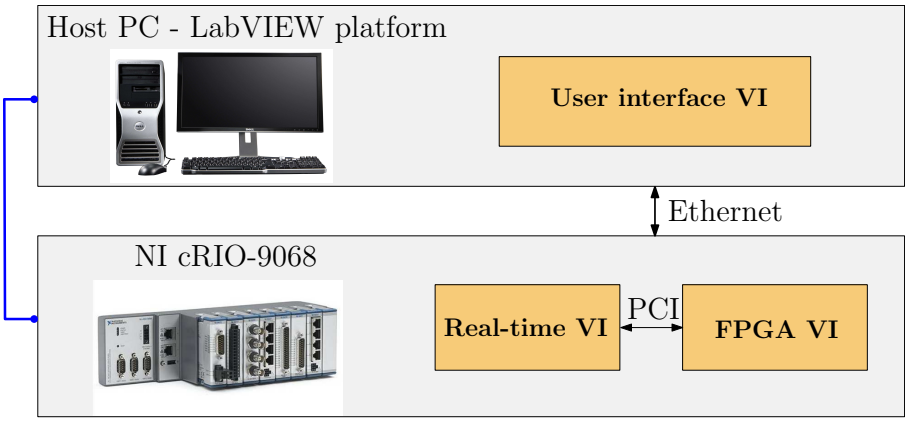


Figure 2-10: Structure of the LabVIEW-FPGA program.

In summary, the nano-grid control system is formed by a sbRIO 9606 based dc-subgrid control platform plus a cRIO 9068 based grid-tied inverter control platform. These two parts are eventually linked to the same host PC through Ethernet cables and controlled on the same LabVIEW-based user interface. This configuration integrates the merits of both DSP and FPGA, rich in peripherals and fast in signal transmission, in an industrial-environment-proof package, which, altogether, guarantees sufficient reliability, scalability, configurability and flexibility of the implemented control system.

2.3 Summary

This chapter describes the configuration of the nano-grid testbench that has been set-up to support the experimental activity documented in this thesis. Different nano-grid architectures have been firstly introduced, including the dc nano-grids, the ac nano-grids and the hybrid nano-grids. Among these, the hybrid nano-grids are considered superior in accommodating both dc and ac loads, and thus adopted as the structure of the nano-grid testbench used throughout the research activity.

There are two main concerns in implementing the considered testbench, the *i*) power circuit, and *ii*) the control system. From the power circuit point of view, high step-up, bidirectional isolated boost topology is required for both the PV-/battery- and ultra-capacitor interfacing converters. To this purpose, the BIBCI is considered to be an ideal solution. A full bridge voltage source inverter (VSI) topology is instead selected as the grid-tied converter, which, thanks to the *L-C-L* filter configuration is used not only to link the dc and ac sides of the nano-grid, but also to set-up a local ac bus that can be, to some extent, dynamically decoupled from the mains.

From the control system perspective, a DSP and FPGA combined platform is considered the optimal choice. The complicated and hierarchical control of the multiple nano-grid converters can be shared in an efficient way between DSP and FPGA chips, provided that these are integrated onto a common control platform and can efficiently exchange data. The final implemented control system incorporates a NI sbRIO 9606 based dc-subgrid control platform and a NI cRIO 9068 based grid-tied inverter control platform, showing high relia-

bility, scalability, configurability and flexibility. Altogether, the developed hybrid nano-grid testbench fulfills almost all the study aims and testing requirements.

The entire system configuration is introduced here for completeness. However, as mentioned above, the main focus of this thesis is in the development and testing of the control functions required by the grid-tied inverter of the nano-grid. Therefore, in the following sections, while referring to the general framework represented by the power circuit and control system configuration here described, the discussion will be restricted mainly to the ac side of the nano-grid and, specifically, to the grid-tied inverter control functions.

A very important note is needed at this point. In order to limit the complexity of the experimental set-up (both of power and control systems), as far as the material presented in this thesis is concerned, *the inverter dc link will be fed by a laboratory dc power supply.* This physically decouples the dc and ac domains within the nano-grid, but, thanks to the performance of the dc subgrid controller (as per Sec. 2.2.2), this replacement does not change significantly the operating conditions of the inverter controller.

Chapter 3

Review of control strategies and functionalities for grid-tied inverters

Grid-tied inverters are widely used for interfacing renewable energy sources and/or storage systems to low-voltage electrical power distribution systems. Lately, a number of different control techniques have been proposed to address the emerging requirements of the smart power systems scenario in terms of both functionalities and performance. This chapter reviews the techniques proposed for the implementation of current-controlled or voltage-controlled inverters in smart micro-grids and/or nano-grids. By referring to a voltage source inverter with *L-C-L* output filter, the different control architectures are classified as single-, double-, and triple-loop. Then, the functionalities that are needed or recommended in the grid-tied, islanded, and autonomous operating modes of the grid-tied inverter are identified and their implementation in the different control structures is evaluated. Based on that, the ideal controller configuration is identified, whose development and experimental validation will be described in Ch. 4.

3.1 Control strategies classification

Considering the single-phase *L-C-L*-filtered inverter shown in Fig. 1-1, six electrical variables can be identified for control: inductor current i_L, inverter-side inductor voltage v_L, capacitor current i_C, output voltage v_O, grid current i_G, and grid-side inductor voltage v_{L_F}.

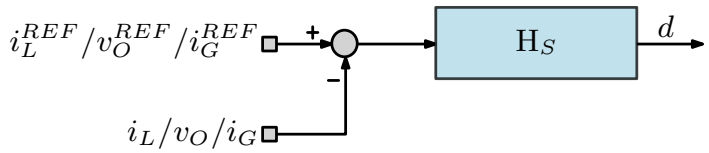


Figure 3-1: Single-loop controller structure. H_S is the regulator.

These variables can be divided into two groups: *i*) *state variables*, namely, i_L, v_O, and i_G, which can be fed-back and closed-loop controlled, so as to guarantee a specified reference tracking performance; *ii*) *auxiliary* variables, including v_L, i_C and v_{L_F}, which can also be fed-back, mainly in complementary loops, for the purpose of improving control performance. Among the latter, v_L and v_{L_F} are the least frequently employed in control loops. They are only briefly considered in [45] and used mainly to facilitate the implementation of proportional-integral-derivative (PID) regulators of the respective state variables. Therefore, v_L and v_{L_F} will not be further considered in the following discussion.

With the remaining four variables, that is, i_L, i_C, v_O and i_G, it is theoretically possible to set-up 13 different cascaded controller structures. These can be further classified into three arrangements: single-loop, double-loop, and triple-loop. The classification is done without counting the feedforward of a variable as a *loop*. These controller structures are described in details in the following.

3.1.1 Single-loop control

A single-loop control is implemented when only one variable is measured and regulated. In the case of the *L-C-L* filter, the applicable variables are i_L, v_O, and i_G. Fig. 3-1 shows the single-loop controller structure, where H_S indicates the applied regulator.

3.1.1.1 i_L controller (ICF)

Inductor current i_L feedback control (ICF) is quite commonly used in the cost-sensitive industrial applications. It requires a single current sensor, which is a standard part of the inverter hardware, built-in to provide overcurrent protection [63, 78]. It is proven in [101] that ICF has an inherent damping effect, which helps to neutralize the resonance introduced by the reactive *L-C-L*-filters' components.

In the past decades, various regulators were proposed for this type of structure, such as proportional (P) [102], proportional-integral (PI) [101], proportional-resonant (PR) [103–107], dead-beat (DB) [108], among which, the PR regulator is prevalent.

With this type of controller, it is not so easy to achieve sufficient grid harmonic current attenuation, even using high-quality regulators, because the grid current is not directly controlled. However, the harmonic attenuation ability can be enhanced through different methods, such as: *i)* a proper definition of the inverter current reference [109], *ii)* grid voltage [78,110] feedforward, or *iii)* capacitor voltage [78,111] feedforward. The principle behind the latter provisions is that harmonic components of the grid current can be damped as much as the inverter output voltage replicates the grid voltage harmonics.

3.1.1.2 v_O controller

Single-loop control of the output voltage v_O is mostly used in some applications of $L-C$-filtered uninterruptible power supply (UPS) systems [102, 112, 113], especially with low pulse-ratios (i.e. the ratio between the switching frequency and the grid fundamental frequency $f_{sw}/f_{v_{PCC}}$) [114–117]. A typical example is given by airplane ground power supplies, whose fundamental frequency is as high as 400 Hz. Single-loop voltage control is equally applicable to *L-C-L*-filtered inverters, as those used in nano-grids. In this case, since v_O is closed-loop controlled, an uninterrupted, high-quality local ac voltage can be guaranteed, which is needed for critical local loads [102, 112, 113]. Besides, an accurate control of the output voltage allows convenient power sharing among parallel inverters, especially in islanded operation mode, by integrating an external droop regulator [50–52].

Different regulators are compatible with this controller structure: P [102, 114], resonant (R) [113, 114], PR[114, 117], Discrete Fourier Transform (DFT) based ones [112] are possible solutions. Regardless of the adopted regulator, this controller structure does not have inherent resonance damping nor short-circuit protection capabilities; therefore, additional provisions need to be implemented to improve the system stability margin [114] and reliability.

3.1.1.3 i_G controller (GCF)

Grid current i_G feedback (GCF) control is used mainly in grid-tied inverters. GCF is considered superior to other solutions in both harmonic attenuation and power flow regulation [78], as the grid current is directly controlled. However, similarly to v_O control, additional damping methods need to be implemented in GCF controller. To this purpose, numerous passive and active damping methods were proposed. The passive methods rely on a proper design of the *L-C-L*-filter [118], also possibly considering the insertion of damping components [101, 119], which, on the other hand, increase volume, cost, and power losses. Active methods, instead, consist in control provisions like 1) the addition of a further control loop involving, for example, the capacitor current [120, 121] or the output voltage [122, 123], as described in Sec. 3.1.2, 2) the use of filter-based feedforward, with notch [124], lead-lag [125], or all-pass filters [126]; and 3) the use of a model-based reduced-order current control method, by splitting the filter capacitor [127] or by using weighted average current control [128].

Despite the variety of the possible improvements, single-loop controllers are structurally unable to concurrently provide multiple functionalities for grid-tied inverters. Such a limitation is overcome by multi-loop controllers, described next.

3.1.2 Double-loop control

When more than one variable is fed-back, the controller design gains more flexibility. In the case of power converters, multi-variable control is almost always set-up in a cascaded arrangement, where the loop hierarchy typically matches the energy density of the output filter reactive components, so that the inner loop regulates the fastest responding electrical variable. A double-loop cascaded controller structure is established when two control variables are fed back as shown in Fig. 3-2. In this case, seven types of double-loop controller structures can be distinguished, namely, by reporting the controlled variables from the inner to the outer loops, 1) i_L-i_C, 2) i_L-v_O, 3) i_L-i_G, 4) i_C-v_O, 5) i_C-i_G, 6) v_O-i_G and 7) i_G-v_O.

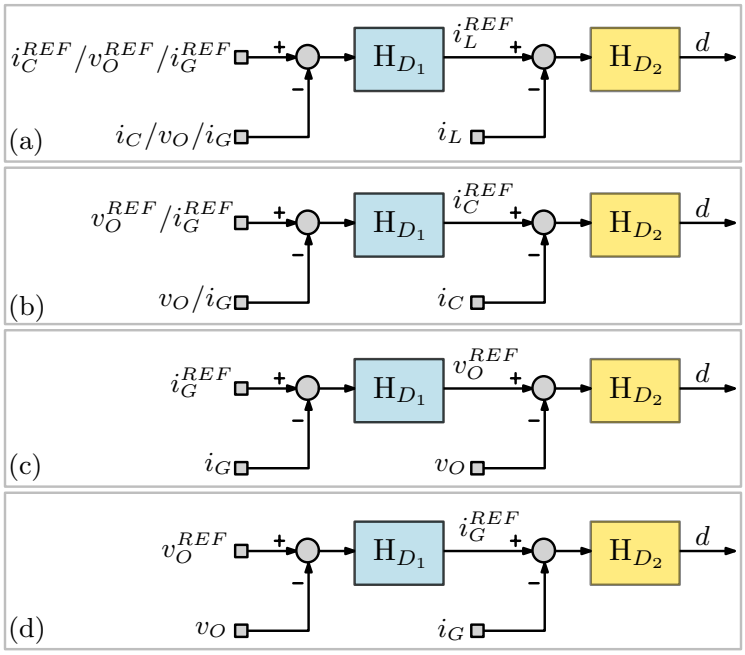


Figure 3-2: Double-loop controller structures. H_{D1} and H_{D2} are regulators.

3.1.2.1 i_L-i_C controller

As mentioned in Sec. 3.1.1.1, ICF is not good at attenuating grid voltage harmonics, which can freely flow through the filter capacitor C_O. The capacitor current i_C, being the derivative of the voltage v_O, brings information about the grid voltage harmonic spectrum and it is exploited in the i_L-i_C double-loop controller. The outer i_C loop acts as a harmonic compensator (i.e., with reference set to zero for the harmonics), while the inner i_L loop contributes to damp resonances [63, 129]. In some case, like in [63], the capacitor current signal i_C is obtained by time-differentiating v_O.

3.1.2.2 i_L-v_O controller

The i_L-v_O controller is widely used in UPS systems with *L-C* filter [102, 130], but it is also applicable to grid-tied inverters with *L-C-L* filters [131–133]. The controller structure is organized in a cascaded way, where the output voltage v_O and the inductor current i_L are controlled as outer and inner loops, respectively, making the inverter operate as a controlled voltage source. Various regulators (i.e., H_{D_2}-H_{D_1}) have been employed in this type of controller; the most representative ones are the P-P [102], P-PI [117], P-PR [131, 132, 134],

PI-PR [133], PR-PR [135], DB-DB [130]. Among these, the P-PR is a very common solution.

3.1.2.3 i_L-i_G controller

The double-loop control of i_L and i_G is an effective solution to simultaneously damp resonances and reduce grid current harmonics. Specifically, the grid-current i_G is configured as the outer loop and provides the reference for the inner, inductor current i_L loop. So doing, the inverter is current-controlled.

Different implementations of the regulators H_{D_2} and H_{D_1} can be found in the literature, such as, the P-PI [136, 137], P-H$^\infty$ [138], P-PR [45, 103], DB-PI [139], PR-R [140], hysteresis current control (HCC)-PR [141]. In summary, the purpose of these regulators is to achieve a sufficiently fast response for the inner i_L loop and a high-gain in the lower frequency region for the outer loop.

3.1.2.4 i_C-v_O controller

From Fig. 1-1, it is evident that the capacitor current i_C can be derived directly from the output voltage v_O, meaning that these two variables are not independent. For this reason, in practice, it is not recommendable to control i_C and v_O concurrently [45]. This type of controller is only briefly presented in [117], where v_O is the outer loop, controlled by a PR compensator, while i_C is the inner loop, regulated by a simple P compensator. It is worth remarking that, in this controller structure, the inner i_C loop is not a reference tracking loop, but it simply adds to the voltage-loop output a signal that is proportional to i_C, which is just a convenient way to implement a derivative (D) control of v_O. As a result, the double-loop controller is functionally equivalent to a single-loop control of v_O with a PR+D regulator.

3.1.2.5 i_C-i_G controller

As shown in [142], proportional feedback of the capacitor current i_C is equivalent to a virtual inductance connected in parallel with the converter output capacitor C_O. Similarly to i_L-i_G controllers, the inner capacitor current loop is exploited for system stabilization,

while the outer loop is responsible for harmonic attenuation and power flow regulation. In some applications, it is possible to control the inner loop with a simple proportional regulator for the sole purpose of increasing the high-frequency loop gain, while steady-state errors in the grid-current control are handled by the outer grid current loop [143]. The outer loop regulator varies from application to application; the literature reports the use of the simple PI control [143, 144], the PR [103, 106, 142, 145], or, at the opposite end of the spectrum, the exotic quasi-proportional-resonant-fuzzy control [146] .

3.1.2.6 v_O-i_G controller and i_G-v_O controller

In nano-grids, inverters are often expected to be capable of operating both connected and islanded. From this perspective, the v_O-i_G controller is advantageous because the outer i_G loop allows the regulation of the exchanged power and the attenuation of the injected harmonics in grid-tied mode, while the inner v_O loop allows the islanded or autonomous operation; examples of application can be found in [147, 148]. To further enhance the system performance, an H^∞ synthesized regulator combined with a repetitive controller is adopted in both the loops in [147]. With this solution, the quality in steady-state of the inverter local voltage and the injected grid current are improved simultaneously.

However, the performance of v_O-i_G controller can be significantly affected by the resonances induced by the *L-C-L*-filter, making it necessary to apply additional damping provisions. An interesting solution is proposed in [149], where the control loops are swapped, making v_O the outer loop regulated by a virtual admittance to provide reference for the inner i_G loop, using a PR + D regulator. While improving the damping, this arrangement makes the realization of seamless mode transitions more complicated.

3.1.3 Triple-loop control

Triple-loop control is the latest controller structure proposed in the literature. It is considered more difficult to implement than double- or single-loop solutions, because each loop bandwidth is limited by the inner loop response delay. For the typical inverter switching frequencies ($< 20\,\mathrm{kHz}$), with three cascaded loops, it is therefore difficult to achieve a

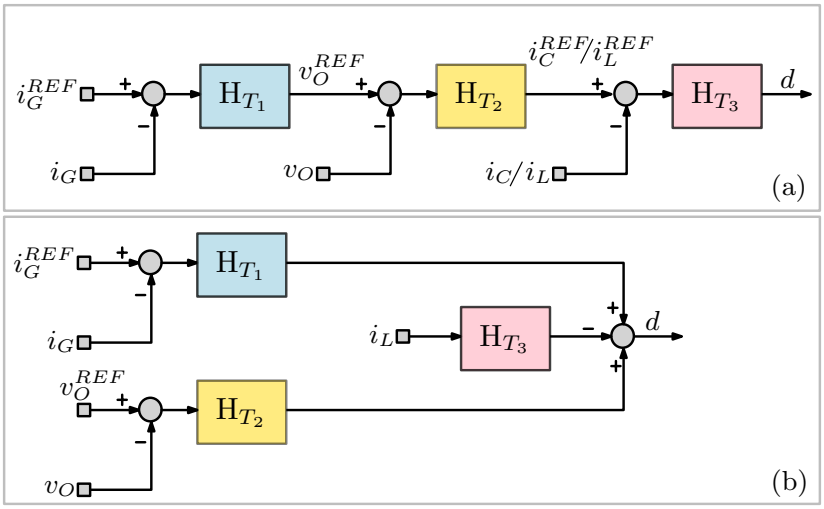


Figure 3-3: Triple-loop controller structures. H_{Tx} are regulators, where $x = 1,\ 2,\ 3$.

reasonable bandwidth on the outer one.

Although, in principle, there might be other structures, only two triple-loop control structures are discussed in the literature, namely, the i_L-v_O-i_G, and the i_C-v_O-i_G, which are discussed in the following.

3.1.3.1 i_L-v_O-i_G controller

This controller structure is similar to the v_O-i_G double-loop controller, but has an inherent damping effect, thanks to the insertion of the innermost i_L loop. The controller can be configured in two different ways, namely, *i*) i_L-v_O-i_G controller, where i_L, v_O, and i_G loops are connected in a cascaded pattern [11, 48, 54, 150, 151] [see Fig. 3-3 (a)]; *ii*) alternatively, i_L+v_O+i_G controller, where the three loops are arranged in a parallel [77, 152, 153] [see Fig. 3-3 (b)].

As far as the i_L-v_O-i_G controller is concerned, different regulators were presented in previous papers (from inner to outer loops), DB-DB-PI [150] (this type of control strategy will be the object of Ch. 4), PR-PR-PR [151], hysteresis/DB-PI-repetitive filter [11], hysteresis control-PI-P [54], P-PR-PR [48]. For i_L+v_O+i_G controller, instead, i_G is controlled by a PR regulator, i_L is controlled by a simple P regulator, while v_O can be controlled either by an R [152, 153] or PR regulator [77].

3.1.3.2 i_C-v_O-i_G controller

Instead of controlling i_L, it is possible to control i_C in the innermost loop, as it is the case in [47, 154]. Only one type of regulator combination is found, which is organized in a cascaded way: the innermost i_C loop (P regulator), intermediate v_O loop (PI regulator) and outer i_G loop (PI regulator). Similar to the double-loop i_C-v_O controller, the i_C loop in this controller is implemented for the purpose of enhancing control performance of the intermediate v_O loop, instead of playing as a tracking loop. So doing, it is functionally equivalent to a double-loop v_O-i_G controller with PID-PI regulators.

Compared with the single- and double-loop controllers, the triple-loop controller provides the highest control flexibility, which can be beneficial to a safer and higher performance operation of grid-tied inverters. However, measures must be taken in the triple-loop controllers to reduce control delays, to maximize performance. To this purpose, [108, 155, 156] propose the use of predictive control, while [142, 157, 158] suggest means to minimize the sampling delays. A panoramic view of the existing controllers for grid-tied inverters is provided in Tab. 3.1.

3.2 Controller functionalities

With the development of nano-grids, more and more control functionalities have been proposed and requirements identified for grid-tied inverters, which made standardization an imperative. Different countries (e.g., USA, Germany) and international organizations [e.g., Institute of Electrical and Electronics Engineers (IEEE), the International Electrotechnical Commission (IET)] have participated in this process and released important standards [43]. Standards like IEEE 1547[27], IEC 61727[162], IEEE 2030.7 [7], and IEEE 929[163], together with national standards like RULE 21 [164] and VDE-AR-4105[165] specifically refer to low-voltage nano-grids and represent the basis of the following discussion.

Table 3.1: Classification of controllers for grid-tied inverters

Pattern	Loop	Inverter type	Structure (inner-outer)	Regulators (inner-outer)	Reference
cascaded	single	current-controlled	i_L	Proportional (P)	[102]
				Proportional-Integral (PI)	[78, 101, 107]
				Robust inverter current feedback resonance supression (ICFRS) + PI	[159]
				Proportional-Resonant (PR)	[103–107]
				Deadbeat (DB)	[108]
			i_G	PR + high pass filter(HPF)	[160]
				Grid current feedback resonance supression (GCFRS) + quasi-proportional resonant (QPR) regulator	[68]
		voltage-controlled	v_O	P	[102, 114]
				Resonant (R)	[113, 114]
				PR	[114, 117]
				Discrete Fourier Transform (DFT)	[112]
	double	current-controlled	i_L - i_C	PR - P	[63]
				(D-Σ) - P	[129]
			i_L - i_G	P - PI	[136, 137]
				P - H^∞	[138]
				P - PR	[45, 103]
				DB - PI	[139]
				PR - R	[140]
				Hysteresis current control (HCC) - PR	[141]
			i_C - i_G	P - PI	[143, 144, 161]
				P - PR	[45, 103, 106, 142, 161]
				P - (PR+ odd harmonic repetitive control (OHRC))	[145]
				P - QPR fuzzy control	[146]
			v_O - i_G	D - PR	[148]
				H^∞ repetitive - PR	[147]
				H^∞ repetitive - H^∞ repetitive	[147]
		voltage-controlled	i_L - v_O	P - P	[102, 115]
				P - PI	[117]
				P - PR	[131, 132, 134]
				PI - PR	[133]
				PR - PR	[135]
				DB - DB	[130]
			i_C - v_O	P - PI	[117]
				P - PR	[45]
			i_G - v_O	(PR + D) - Virtual admittance	[149]
	triple	current-controlled	i_L - v_O - i_G	P - PR - PR	[48]
				PR - PR - PR	[151]
				DB - DB - PI	[150]
				DB - PID - Repetitive	[11]
				HCC - PI - P	[54]
			i_C - v_O - i_G	P - PI - PI	[47, 154]
parallel	3 branches		i_L + v_O + i_G	P + R + PR	[152, 153]
				P + PR + PR	[77]

3.2.1 Functionalities overview

According to the indications provided by the standards, nano-grids are expected to present specific features concerning stability, flexibility, scalability and grid supporting capabilities [30, 166–168]. In particular, nano-grids should *i*) present adequate stability margins in both steady-state and transient conditions; *ii*) be able to automatically react to faults to allow prompt restoration of normal operating conditions for loads and sources; *iii*) extend the nano-grid operation, possibly by passing to the islanded autonomous mode; *iv*) offer the possibility to seamlessly add or remove loads and sources; and *iv*) provide ancillary services, such as active and reactive power regulation, dispatchability, data-logging, remote diagnostic.

Depending on the chosen grid-tied inverter control strategy, the above features can be implemented to some degree, or be altogether impossible to achieve, which results in limited nano-grid performance. From the converter control perspective, it is therefore worth considering *i*) what are the most critical functionalities and *ii*) what are the most suitable control strategies for their implementation.

As mentioned above, standards like [27, 62, 162–165] define a set of versatile functionalities to be implemented by grid-tied inverters. Others have been identified and proposed in the literature, like [32, 167–171]. Altogether, the set of functionalities can be categorized by separately referring to four different circumstances of operation, denoted in Fig. 3-4 as grid-tied (G), islanded (I), autonomous (A), transition from G to I or A, and transition from A to G or I. In addition, *normal* and *abnormal* working conditions are distinguished.

3.2.1.1 Grid-tied mode (G)

Under normal conditions, power flow control [43, 169, 172, 173] and harmonic current attenuation [174] are the most important functionalities of a grid-tied inverter. Power flow control is typically performed by means of *droop control*, which allows to regulate active and reactive power based on grid frequency and amplitude, respectively, in predominantly inductive grids [25,33]. However, low-voltage networks may also show significant resistive components. Without accurate estimation of the grid impedance, the effectiveness of droop

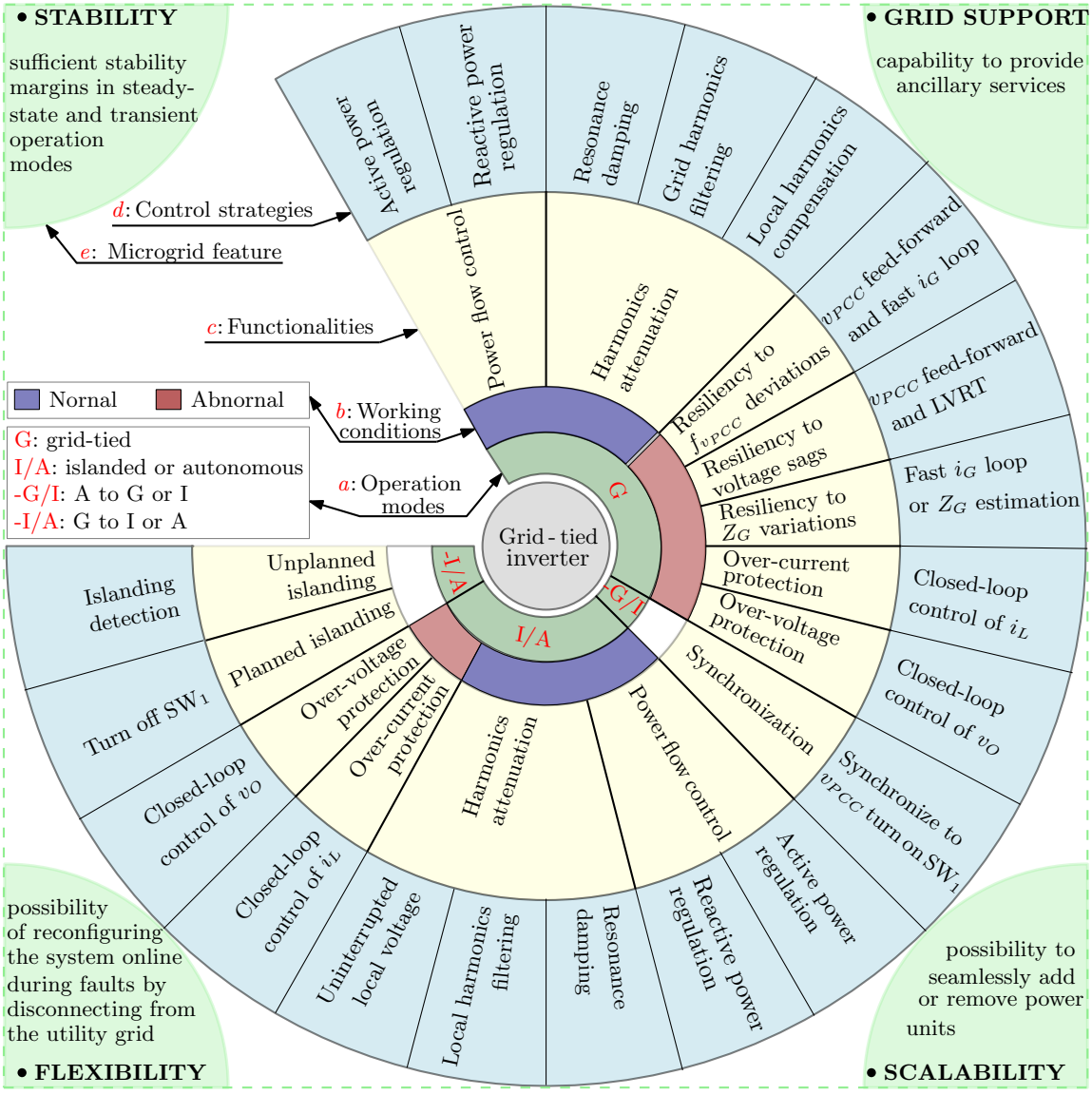


Figure 3-4: Overview of nano-grid features, functions and operating modes. From the perspective of a single grid-tied inverter (at the center), the required operation modes (*a*), the different working conditions (*b*) and functionalities (*c*) are illustrated together with the associated control techniques (*d*). The corners describe the four fundamental features of nano-grids (*e*).

control can be significantly degraded [25]. To cope with this issue, the adoption of *virtual impedance* has been proposed, which allows to keep the impedance seen by the droop controller of a specific kind (e.g., inductive), facilitating the decoupling of active and reactive power regulation [135,175,176]. On the other hand, the function of harmonic attenuation is mostly realized by damping the resonances caused by the *L-C-L*-filter reactive components [98, 99, 177, 178], by filtering the grid-side harmonics [30, 167, 170, 174, 179–181], and by actively compensating the pollution possibly caused by local-distorting loads [182].

As far as the abnormal condition is concerned, perturbations like frequency variations [43, 170], voltage sags [183–186], and impedance changes [187–189] are commonly encountered, especially in weak grids. To minimize the perturbations to the system across grid voltage sags, low-voltage ride through capabilities are often requested [185, 186]. In general, an improvement of system resiliency to grid voltage disturbances—in frequency $f_{v_{PCC}}$ as well as in amplitude $|v_{PCC}|$—is obtained by feed-frowarding the grid voltage [190, 191] to the voltage loop or directly to the modulator. However, the effectiveness of grid voltage feed-forward can be significantly affected when the grid-impedance increases, in which case it may actually become a feedback loop. Apart from that, a higher than expected grid impedance tends to narrow the grid current control loop bandwidth and easily leads to instability.

In order to enhance the system's resiliency to grid impedance variations, possible solutions are *i*) to maximize the control loop bandwidths [150] by design, *ii*) to use adaptive control techniques [192] based on grid-impedance estimation, or *iii*) to adopt on-line autotuning techniques that adjust the control loop gains [65].

Finally, because over-current and over-voltage conditions can trigger faults and damage the inverter, various types of hardware and software protections are mandatory for any grid-tied inverter [8, 193].

3.2.1.2 Islanded or autonomous mode (I/A)

In islanded or autonomous mode, the functionalities required for the grid-tied inverters are pretty much the same than in the previous case and include, in normal conditions, power flow control and harmonic attenuation, and, in abnormal conditions, over-current

and over-voltage protection. Performance levels [6] largely depend on the inverter control organization. As an example, voltage-controlled inverters are capable of providing high-quality uninterrupted local voltage, which is important for critical local loads [5]. On the other hand, current-controlled inverters are superior in power regulation, but less easy to use as local voltage power supplies, as they normally lack the voltage forming capability.

In islanded mode, parallel operation of multiple units is sometimes required and should take place without impairing the system stability. From this standpoint, the inverter output impedance characteristics brought by the different controller organizations are of paramount importance, an aspect that will be discussed in Ch. 4.

3.2.1.3 Transition from grid-tied to islanded / autonomous mode (-I/A)

The transition to the islanded or the autonomous modes can be performed in either an unintentional or intentional way. The former type of transition is defined as a sudden disconnection of an electrical subsystem from the utility grid without any prior notification to the subsystem undergoing the transition. Intentional islanding refers to the opposite situation in which the transition to the islanded operation is initiated by the subsystem itself [5]. As previously mentioned, the nano-grid experimental set-up here considered allows to test both unintentional and intentional transitions, thanks to the presence of two controlled switches, SW_2 and SW_1, as is shown in Fig. 1-1.

At the occurrence of an unintentional islanding event, if no provisions are taken, the grid-tied inverter may experience severe current and voltage transients or even incur into instability [49], while still energizing the islanded network. Therefore, for safety reasons, the implementation of some anti-islanding-detection functionality is mandatory in many countries.

		Normal condition			Abnormal condition		
	Controller structures (inner-outer)	**Power flow control**	**Quality of injected current**	**Smooth mode transitions**	**Resiliency to grid changes** ($f_{v_{pcc}}, \lvert v_{pcc}\rvert$)	**Resiliency to** Z_G **variations**	**Protection** (over voltage or over current)
Single loop	i_L	×	×	×	×	×	×
	v_O	×	×	×	×	×	×
	i_G	√	√	×	√	√	×
Double loop	i_L - i_C	×	×	×	×	×	×
	i_L - v_O	×	×	×	×	×	√
	i_L - i_G	√	√	×	√	√	×
	i_C - v_O	×	×	×	×	×	×
	i_C - i_G	√	√	×	√	√	×
	v_O - i_G	√	√	√	√	√	×
Tri. loop	i_L - v_O - i_G	√	√	√	√	√	√
	i_C - v_O - i_G	√	√	√	√	√	×

Figure 3-5: Controller performance (√: practical implementation, ×: implementation not straightforward).

3.2.1.4 Transition from autonomous to grid-tied / islanded mode (-G/I)

For the interconnection of two systems that initially operate independently, synchronization is of paramount importance to prevent undesirable transients. This is the case, for example, of the closure of SW_1 for the connection of an inverter autonomously sustaining its local loads with a regularly operating islanded system (if SW_2 is open) or with the grid (if SW_2 is closed). The synchronization functionality is normally realized by means of a PLL and, for voltage controlled converters, it may be assisted by soft-start techniques, like virtual output impedance control.

3.2.2 Feasibility of control strategies

Let us now consider the feasibility of the above described functionalities to be implemented on top of the controller structures discussed in Sec. 3.1. A view of the available options is proposed in Fig. 3-5, where, for better readability, only the most commonly used controller structures of cascaded type are presented, separately considering normal and abnormal grid conditions.

3.2.2.1 Normal operation

Under normal conditions, commonly required functionalities are power flow control, harmonic attenuation, and smooth mode transitions.

Regulation of active and reactive power can be conveniently realized by droop control (see Fig. 4 in [6]). In voltage controlled inverters, the frequency and amplitude of the output voltage reference v_O^{REF} is adjusted slowly by an outer droop controller to regulate output active and reactive powers. In current controlled inverters, instead, the inductor current reference i_L^{REF} or grid current reference i_G^{REF} is slowly modified by droop controller. From the standpoint of power regulation, there is no practical difference between voltage-controlled and current-controlled inverters.

As far as the harmonics attenuation ability is concerned, closed-loop control of grid current i_G is the most effective in limiting harmonics from propagating from the inverters to utility grid or vice-versa.

Guaranteeing uninterrupted local voltage is important in both islanded and autonomous mode, especially when critical local-loads are connected. On account of that, closed-loop control of output voltage v_O becomes necessary.

In islanded conditions, furthermore, the capability to maintain the PCC voltage within pre-defined frequency and amplitude boundaries results from the upper level control layer organization, which will not be discussed in this thesis. In general terms, all the control organizations discussed so far are compatible with an upper level droop-based controller, but the final effectiveness and performance can be different depending, once again, on the controller output impedance characteristics.

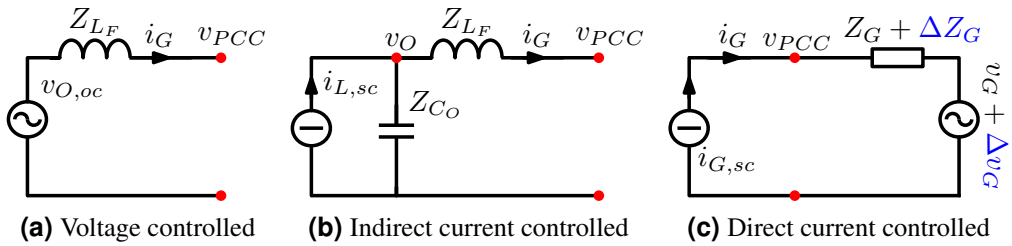
Smoothness of mode transitions guarantees that both the local voltage v_O and the injected grid current i_G do not experience large transients switching among grid-tied, islanded, and autonomous modes. This relies on: 1) precise voltage synchronization, 2) fast control of grid current i_G to damp transients and guarantee high-quality power injection in grid-tied mode, and 3) high-performance control of output voltage v_O, to guarantee uninterrupted local voltage in islanded or autonomous mode. Accordingly, controllers that integrate both grid current and output voltage loops are preferable for the implementation of smooth mode transitions.

3.2.2.2 Abnormal condition

Equivalent circuits of voltage-controlled inverter (VCI), indirect-current-controlled inverter (ICCI), direct-current-controlled inverter (DCCI), operating in grid-tied mode, are illustrated in Fig. 3-6. For simplicity, the inverters are assumed to be controlled as ideal voltage or current sources. According to Fig. 3-6, the variations in the grid voltage Δv_G and the grid impedance ΔZ_G can be written for the case of VCI, ICCI, and DCCI as (3.1), (3.2) and (3.3) respectively,

$$\Delta i_G = -\frac{\Delta v_G}{Z_{L_F} + Z_G} + \frac{v_G \cdot \Delta Z_G}{(Z_{L_F} + Z_G)^2} \tag{3.1}$$

$$\Delta i_G = -\frac{\Delta v_G}{Z_{L_F} + Z_G + Z_{C_O}} + \frac{v_G \cdot \Delta Z_G}{(Z_{L_F} + Z_G + Z_{C_O})^2} \tag{3.2}$$



(a) Voltage controlled **(b)** Indirect current controlled **(c)** Direct current controlled

Figure 3-6: Inverter equivalent circuits.

$$\Delta i_G = 0. \tag{3.3}$$

Equations (3.1)-(3.3) show that larger grid current perturbations will appear in VCI than ICCI (the denominator is larger in the latter case) for given voltage or impedance variations. At the same time, one clearly sees that, ideally, DCCI offers maximum resiliency to both the grid perturbations. In this case, large-bandwidth control of grid current i_G, which implies higher inverter output impedance and almost ideal current source behavior, is more suitable for improving system resiliency to grid perturbations.

Over-current and over-voltage protections can be easily realized when closed-loop control of both the inductor current i_L and output voltage v_O are implemented. To this purpose, fast sampling helps to rapidly identify the over-current and/or over-voltage conditions and a large control bandwidth guarantees voltage and current within reasonable levels even under severe transients. Accordingly, controllers that include both v_O and i_L loops are the most suitable to implement over-current and over-voltage protections.

3.3 Stability considerations

The stability of any interconnection of multiple systems that are stable when considered singularly can be studied considering to their output impedances and applying methods like [66, 194]. The Middlebrook criterion [67] gives a sufficient condition for the stability of an inverter with output impedance Z_{out} connected to a grid of impedance Z_g, namely, $|Z_g|/|Z_{out}| < 1$. Considering the implemented control structures, Fig. 3-7 shows the measured impedance magnitudes. Qualitatively, among the current controlled structures, the

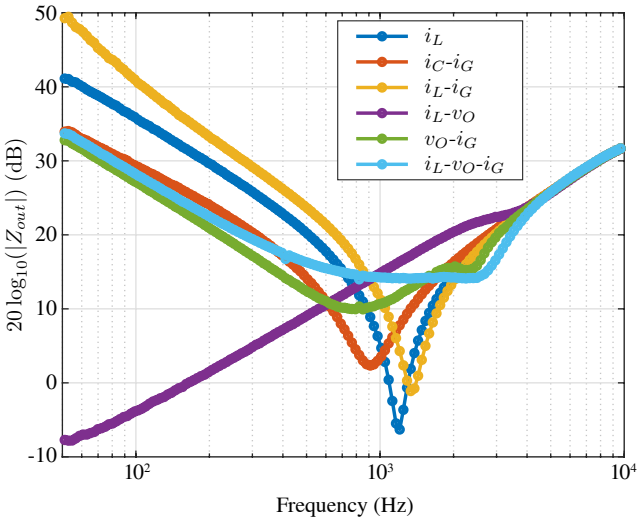


Figure 3-7: Measured output impedance.

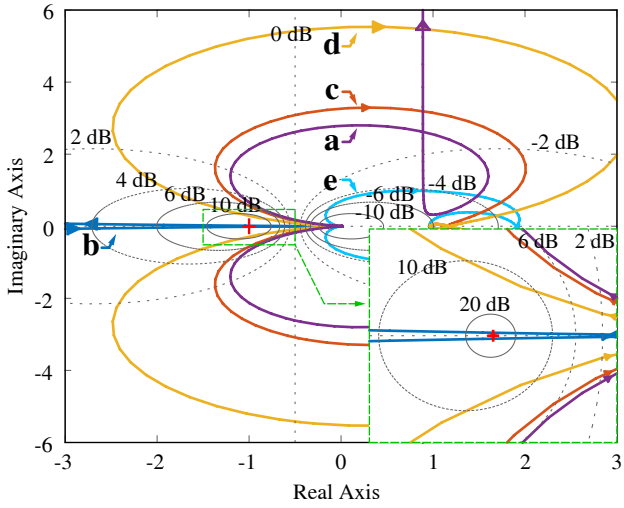


Figure 3-8: Nyquist plot of: a) inverter with i_C-i_G control grid-tied with $Z_{pcc} = Z_g = 0.1\,\Omega + 0.5\,\text{mH}$, b) islanded inverter with i_C-i_G control and $Z_g = 300\,\text{mH}$, c) islanded parallel connection of inverter with i_C-i_G and inverter with i_L-v_O control, d) islanded parallel connection of inverter with i_L and inverter with i_L-v_O control, e) islanded parallel connection of inverter with i_L-v_O-i_G and inverter with i_L-v_O control.

i_L control shows the lowest impedance around resonance, while double and triple loop solutions allow better conditions referring to the impedance ratio Z_g/Z_{out}. An exact assessment can be performed by Nyquist plot analysis of the impedance ratio. Five conditions are reported in Fig. 3-8 to show the potential unstable interactions relevant to the zero-level control (see Fig. 1-1) when multiple converters are interconnected. In particular: a) is the case of a grid-feeding [6] inverter with i_C-i_G control connected to a real grid, b) represents the same converter in islanded conditions, while connected to an inductive impedance Z_g of high magnitude (the considered value is the one measured at the output of a transformer with compatible ratings while open circuited at the primary side due to protection tripping), c) is the basic case of the master-slave microgrid architecture, in which a grid-forming [6] inverter implemented with i_L-v_O control supplies a grid-feeding converter with i_C-i_G control, d) is the same as the previous case but with grid-feeding converter with i_L control, e) is the same as the previous case but with grid-feeding converter with i_L-v_O-i_G control. As expected while referring to Fig. 3-7, i_C-i_G shows better stability margins than the i_L control while connected to a voltage source, being it the grid or a voltage-controlled inverter with i_L-v_O control. Better performance are shown by the i_L-v_O-i_G control.

3.4 Summary

This chapter provides an overview of existing control strategies for grid-tied inverters applicable to nano-grids and describes the crucial functionalities that these converters should offer. In addition, the chapter discusses feasibility of realizing such functionalities on each type of controller organization. In summary, the analysis suggests that: *i*) the closed-loop control of i_L is effective in damping *L-C-L* filter resonances and allows the implementation of inverter overcurrent protection; *ii*) a voltage control loop, like in the i_L-v_O controller, is certainly needed to provide high-quality local voltage, smooth transitions between different operating modes and inverter overvoltage protection; *iii*) closed-loop control of i_G is, in all cases, very effective in attenuating grid current harmonics and beneficial for the regulation of injected active and reactive power.

Accordingly, it is possible to conclude that a triple-loop control strategy of the i_L-v_O-

i_G type is the one that shows better potential in providing simultaneously the multiple critical functionalities required by nano-girds. Therefore, in the following chapter, a large-bandwidth triple-loop controller of that type will be introduced, designed and extensively tested in the different operating conditions that have been considered so far.

Chapter 4

Large-bandwidth triple-loop controller

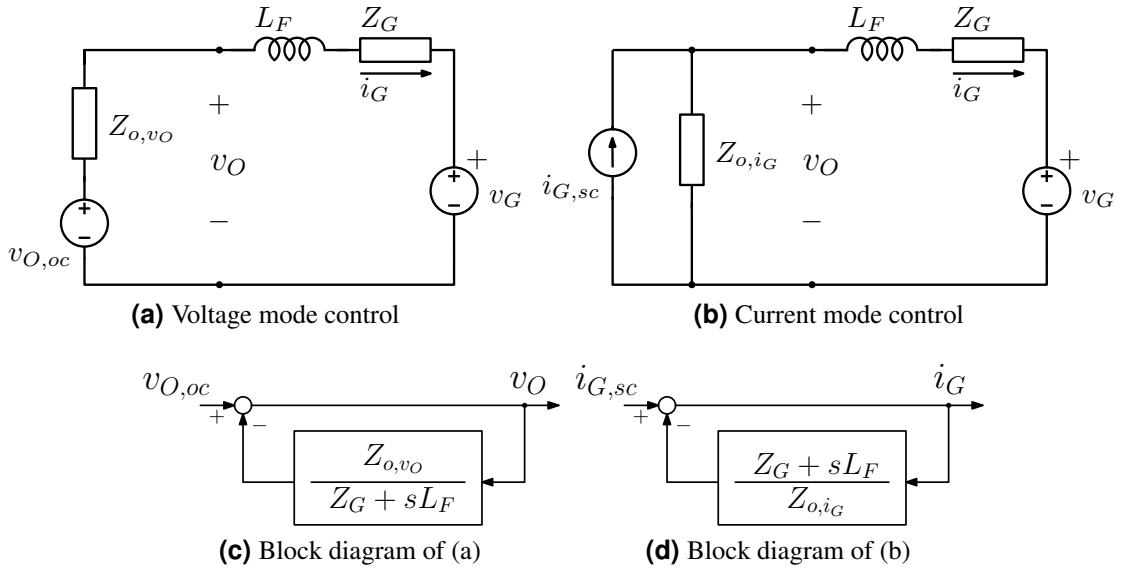
Following the discussion presented in Ch.3, this chapter analyzes a large-bandwidth, triple-loop controller designed for single-phase, voltage-source grid-tied inverters with *L-C-L* output filter. The inner control loops regulate the inverter output current and the filter capacitor voltage respectively, while the third, outer one regulates the current injected into the grid. The inner loops employ dead-beat type regulators, whose minimum response delay allows the third loop to achieve a relatively large regulation bandwidth. This organization provides several benefits, showing very good potential for application to nano-grids.

4.1 Analysis of converter/grid connection

The stability of the connection between a grid-tied VSI and the utility grid can be discussed deriving some simple relations between the inverter output impedance and the series impedance of the grid source, $Z_G(\omega) = R_G + j\omega L_G$. The latter is, in general, only partially known and can vary significantly, which complicates the discussion to some extent. Nevertheless, stability conditions of general validity can be determined, that can be used to steer the design of the VSI control system. To this purpose, in the following, we will derive different output impedance expressions referring to the topology shown in Fig. 2-5, whose main parameters are listed in Tab. 2.3.

Let us consider, in the first place, the case where the VSI is controlled as a voltage source. In this case, it is possible to model its small-signal behavior, as seen from the output

terminals where the voltage v_O can be measured, with the series connection of an equivalent voltage source $v_{O,oc}$, generating the inverter open circuit voltage, and an equivalent output impedance Z_{o,v_O}. This is the situation described by Fig. 4-1 (a).



(a) Voltage mode control **(b)** Current mode control

(c) Block diagram of (a) **(d)** Block diagram of (b)

Figure 4-1: Small-signal modeling of the inverter/grid connection.

The transfer function between the actual output voltage v_O and the open circuit voltage $v_{O,oc}$ can be easily determined and is given by:

$$\frac{v_O(s)}{v_{O,oc}(s)} = \left[1 + \frac{Z_{o,v_O}}{Z_G + sL_F}\right]^{-1} . \tag{4.1}$$

This expression can be interpreted as the input-output, closed loop transfer function of a feedback system, as shown in Fig. 4-1 (c). From this standpoint, according to the Middlebrook's stability criterion [67, 195], the connection of the inverter with the grid is unconditionally stable if:

$$|Z_{o,v_O}| < |Z_G + sL_F| . \tag{4.2}$$

Similarly, when the VSI is controlled as a current source, its small-signal behaviour can be modeled by the parallel connection of an equivalent current source $i_{s,sc}$, generating the inverter short-circuit current, and an equivalent output impedance Z_{o,i_G}. The transfer

function between the grid current i_G and the short-circuit current $i_{s,sc}$ is:

$$\frac{i_G(s)}{i_{s,sc}(s)} = \left[1 + \frac{Z_G + sL_F}{Z_{o,i_G}}\right]^{-1} . \tag{4.3}$$

The corresponding feedback system representation is displayed in Fig. 4-1 (d). In this case, the connection is unconditionally stable if:

$$|Z_{o,i_G}| > |Z_G + sL_F|. \tag{4.4}$$

In practice, (4.2) and (4.4) are often too conservative to be matched unconditionally and in a wide frequency range. Particularly critical cases are represented by possible resonances (or anti-resonances) between sL_F + Z_G and Z_{o,v_O} or Z_{o,i_G}. At the resonant frequencies, to satisfy the stability conditions can be very difficult and, as a result, undesired, lightly damped modes can manifest themselves during transients or even in the steady-state. Nevertheless, (4.2) and (4.4) clearly show that the design of a grid-tied inverter control system should always aim at properly shaping the converter output impedance. Indeed, the inverter/grid connection is expected to be robustly stable, even in the presence of uncertainty in Z_G, if the magnitude of the inverter output impedance is *i*) minimized, in case of voltage-controlled VSIs, or *ii*) maximized, in case of current-controlled VSIs. In the following, these criteria will be applied in designing each controller of the proposed triple-loop organization. The resulting converter output impedance will be analytically derived in the frequency domain and experimentally measured. The impedance spectroscopy will allow to *i*) quantify the controller's performance in a relatively simple and repeatable manner; *ii*) quantitatively compare different control options, allowing to choose the highest performing regulator for each loop.

4.2 Large-bandwidth triple-loop controller

The organization of the proposed controller is shown in Fig. 4-2. As mentioned in Ch. 3, this architecture has several advantages: *i*) it guarantees high voltage quality to the local loads, thanks to the v_O voltage control loop, *ii*) it employs a simple *L-C-L* output filter,

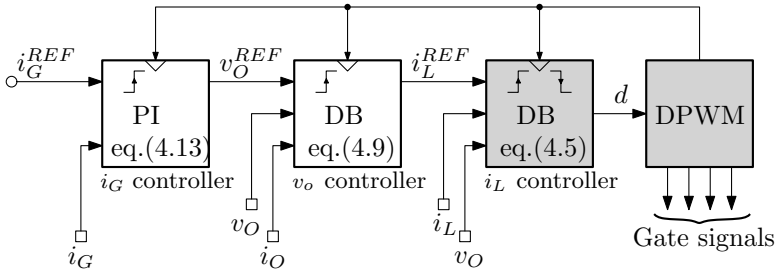


Figure 4-2: Proposed triple-loop controller architecture.

commonly adopted in grid-tied converters [196], *iii*) it enables the seamless transition between grid-tied and islanded operations, thanks to the grid current i_G controller. The down side is represented by the need for three current sensors and a voltage sensor. However, only the sensor of inductor current i_L needs to be of high quality, in terms of bandwidth and accuracy. The output current i_O and grid current i_G sensors, instead, operate on naturally filtered signals, which makes their bandwidth requirements much less demanding (a few kHz can perfectly do).

In principle, a variety of regulators can be adopted for each control loop. Choosing among the various options is often a matter of designer's experience and preference. To make the design process somewhat less arbitrary, the above discussed impedance optimization criterion will be used, aimed at deriving a solidly built, robustly performing solution.

4.2.1 Inductor current controller

The inductor current controller and modulator organizations considered here (indicated by the shaded boxes in Fig. 4-2) replicate those presented in [108], as they offer excellent dynamic performance, in both small-signal and large-signal terms. As will be shown in Section 4.4, they also guarantee the converter output impedance is maximized in a wide frequency range. The controller is designed to be realized in hardware form, on an FPGA chip (see Sec. 2.2.2), so that the computation time is reduced to a negligible fraction of the switching period ($34\ \mathrm{ns}$, in our specific implementation) and the duty-cycle can be adjusted *twice per modulation period*. At each control iteration, the following *duty-cycle update* equation is computed :

$$d(k) = \frac{\tilde{L} f_{sw}}{V_{DC}} \cdot \left[i_L^{REF}(k) - i_L(k) \right] + \frac{v_O(k)}{2V_{DC}} + \frac{1}{2}. \tag{4.5}$$

Please notice that the symbols with ˜ indicate estimated variables.

To tolerate possible perturbations that may be present in the dc link voltage, the V_{DC} can be sampled for the purpose of updating on-line the coefficients of (4.5). By doing so, there will be no significant differences in inverter performance, whether the dc link is supported by a dc power supply or by a dc subgrid with a relatively large bandwidth regulation of the dc link voltage.

The discrete-time, closed-loop transfer function W_{i_L} between the current reference i_L^{REF} and the inductor current i_L can be determined from (4.5) and the zero-order-hold (ZOH) discretization of inductor L dynamic equation (please see also Sec. 4.3.1), yielding:

$$W_{i_L}(z) = \frac{I_L(z)}{I_L^{REF}(z)} = z^{-1}. \tag{4.6}$$

The result is exactly equal to a one-sampling-period delay, where the sampling period equals *one half of the modulation period* [i.e., $T_{sw}/2 = 1/\left(2f_{sw}\right)$]. Therefore, this current controller guarantees deadbeat type dynamics with minimum response delay ($T = T_{sw}/2$). For clarity, the experimental measurement of the inductor current loop small-signal step response is shown in Fig. 4-3. The sampling instants are indicated to show that the error correction takes only one sampling period ($T = T_{sw}/2$), measured from the first sample after the step.

4.2.2 Output voltage controller

A deadbeat type controller is adopted to regulate v_O as well, aiming at achieving a large regulation bandwidth and a limited response delay. For the current controller, the synchronization between the symmetrical modulation carrier and the sampling process allows the average inductor current value to be exactly acquired at the beginning and at the middle of each modulation period, independently from the particular duty-cycle value or load condition, as is shown in Fig. 4-4, where the white squares indicate the ideal sampling instants

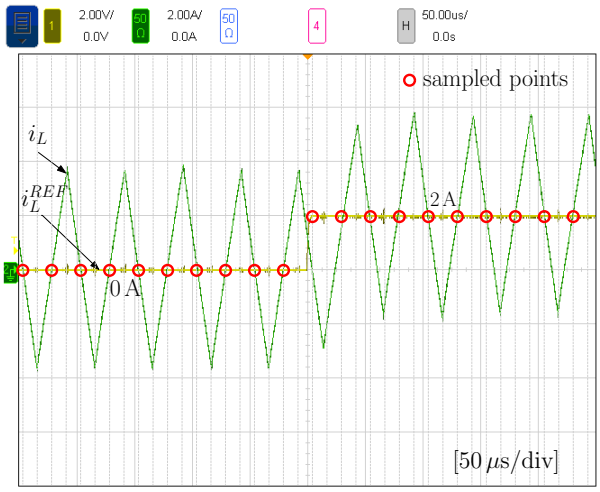


Figure 4-3: Small-signal step response of the inductor current controller.

of i_L, diamonds indicate the v_O samples.

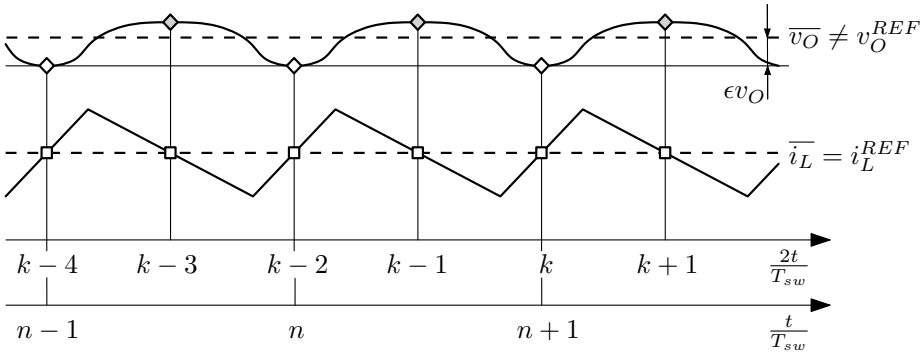


Figure 4-4: Voltage and current sampling processes.

Unfortunately, the exact value of the average output voltage cannot be acquired as easily, since there is not a fixed position within the sampling period where this can be found at all times and in any condition. Because it is not practical to track its ideal sampling instant, the output voltage is sampled synchronously with the converter current, even if that generates a (small) error, indicated as ϵv_O in Fig. 4-4. It is worth recalling that the output voltage ripple at the switching frequency is typically very small (0.55 V in the considered set-up), so that ϵv_O is almost undetectable.

More importantly, the iteration period of the voltage controller cannot be equal to that of the current controller. Indeed, if two equally spaced voltage samples were taken in each modulation period, as is done for the current signal, the regulation error would unavoid-

ably turn into a sequence of alternating positive and negative values, even in the steady state. Even if the inner loop maintained a stable operation, this would result in continuous adjustments of the current reference i_L^{REF} and a persistent limit cycle oscillation (LCO) would be generated. To prevent that, only a single sample per period can be taken. In the implementation considered in this paper, only those samples indicated by white diamonds in Fig. 4-4 are actually acquired.

The voltage controller equation is now derived, assuming the inner current loop to be accurately described by (4.6) and neglecting again the calculation delay. That is possible because the voltage controller is realized on the same FPGA chip that executes the current control algorithm, which allows their concurrent calculation. Let us consider the discrete-time, ZOH approximation of the output voltage dynamic equation, calculated along two consecutive sampling periods of $T_{sw}/2$ duration:

$$\begin{aligned} v_O(k+1) = v_O(k-1) + \frac{1}{2C_O f_{sw}} \cdot \left[\overline{i_L(k)} + \overline{i_L(k-1)}\right] + \\ - \frac{1}{2C_O f_{sw}} \cdot \left[i_O(k) + i_O(k-1)\right] . \end{aligned} \tag{4.7}$$

Being the average inductor current equal to its one-step-delayed reference, as per (4.6), and assuming the output current i_O not to vary significantly in, at least, two consecutive sampling periods, (4.7) can be simplified and re-written yielding:

$$v_O(n+1) = v_O(n) + \frac{1}{C_O f_{sw}} \cdot \left[i_L^{REF}(n) - i_O(n)\right], \tag{4.8}$$

where the index n is updated *just once* per modulation period. Thus written, (4.8) represents the down-sampled (by a factor 2) dynamic equation of the inverter output voltage, from which the following control equation can be derived:

$$i_L^{REF}(n) = \tilde{C_O} f_{sw} \cdot \left[v_O^{REF}(n) - v_O(n)\right] + i_O(n), \tag{4.9}$$

assuming that $v_O(n+1) = v_O^{REF}(n)$. The down-sampling applied to (4.7) means that, from the standpoint of the inner current control algorithm, i_L^{REF} is invariant in two consecutive

sampling periods of $T_{sw}/2$ duration, resulting in the following identity:

$$\overline{i_L(k)} = \overline{i_L(k-1)} = i_L^{REF}(k-2), \tag{4.10}$$

which was implicitly used in the derivation of (4.8). Please note that (4.8) is obtained integrating the output capacitor current during any two consecutive time intervals when the *average inductor current is stationary.*

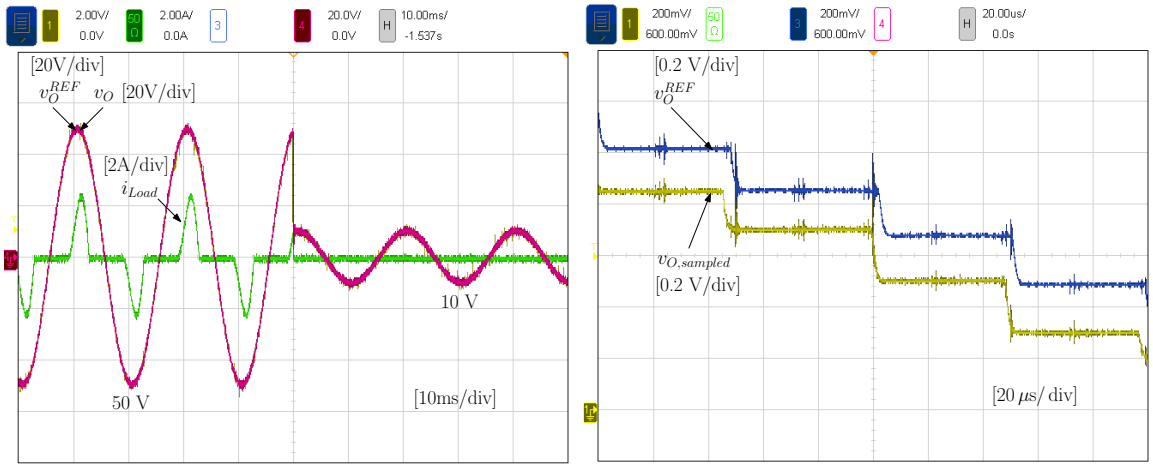
Based on (4.7), it is possible to determine the closed loop transfer function between the output voltage and its reference. As can be inferred from the above derivation, the procedure requires some tricky re-arrangement of the control equations, due to the different sampling rates of the inner current loop and the outer voltage loop. An approximate solution can be found re-sampling (4.9) and integrating the output capacitor current during any two successive sampling periods where the *current reference* i_L^{REF} *is stationary*. The dynamic equation for the output voltage then becomes:

$$\begin{aligned} v_O(k+2) = v_O(k) &+ \frac{1}{2}\left[v_O^{REF}(k) + v_O^{REF}(k-1)\right] \\ &- \frac{1}{2}\left[v_O(k) + v_O(k-1)\right] \\ &+ \frac{1}{2C_O f_{sw}}\left[i_O(k-1) - i_O(k+1)\right]. \end{aligned} \tag{4.11}$$

By $\mathcal{Z}$-transforming (4.11), after few mathematical manipulations, the small-signal transfer function is found to be equal to

$$W_{v_O}(z) = \frac{V_O(z)}{V_O^{REF}(z)} = \frac{1}{2z^2 - 2z + 1}. \tag{4.12}$$

It is worth noting that, differently from (4.6), the function $W_{v_O}(z)$ is not the pure z^{-2} delay one would expect. This is due to the dynamic interaction between the inner current control loop and the outer voltage control loop operating at different sampling rates. Because of that, the prediction of the output voltage trajectory that is used to derive the control law (4.9) is only approximated and the closed loop transfer function cannot be exactly deadbeat. Nevertheless, the practical consequence is very limited, as it is possible to see in Fig. 4-5. The figure shows the controller's response to a step reference variation from $50\,\mathrm{V}$



(a) Large-signal step **(b)** Small-signal step

Figure 4-5: Step response of output voltage controller.

to 10 V (peak), when the converter is operating with just the two inner control loops closed and with a distorting load (i.e., non-linear load) applied in parallel with the filter capacitor. As can be seen in Fig. 4-5(a), voltage v_O tracks the reference almost ideally, reaching the new set-point very rapidly and with no undesired transients. The steady-state tracking delay is shown in detail in Fig. 4-5(b), where it is possible to verify that it matches the expected single period duration ($T = T_{sw}$). This result is important because a small response delay allows the maximization of the third loop bandwidth and, as will be shown in Sect. 4.4, a significant output impedance reduction in a wide frequency range.

4.2.3 Grid current controller

The grid current i_G is sampled once per switching period, synchronized with the output voltage v_O. Considering the expected uncertainty in the grid impedance parameters, a simple PI controller is adopted for the grid current loop. Indeed, the PI structure ensures a reasonably robust stability, once the loop phase margin is adequately oversized. The complete small-signal block-diagram of the controller is shown in Fig. 4-6. Based on that, the control equation can be written as

$$v_O^{REF}(z) = H_{i_G}^{PI}(z)(i_G^{REF}(z) - i_G(z))\,. \tag{4.13}$$

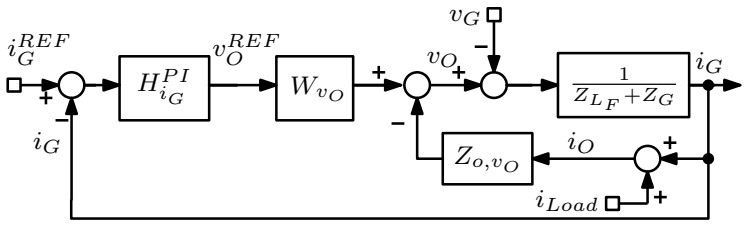


Figure 4-6: Small-signal block-diagram of the proposed triple-loop controller.

where $H_{i_G}^{PI}(z) = Kp_{i_G} + Ki_{i_G} \cdot \dfrac{z}{z-1}$ is the PI controller's discrete-time transfer function. Accordingly, the open loop gain is given by

$$T_{i_G}(z) = H_{i_G}^{PI}(z) W_{v_O}(z) \frac{1}{Z_{o,v_O}(z) + \tilde{Z}_G(z) + Z_{L_F}(z)}\,, \tag{4.14}$$

where Z_{o,v_O} is the inverter output impedance when inductor current and output voltage loops are both closed, while Z_{L_F} and $\tilde{Z_G}$ are the grid interfacing inductor impedance and the estimated grid impedance, respectively. All impedances are specified in the discrete time domain, as will be explained in Sect. 4.4. In particular, the analytical derivation of Z_{o,v_O} will be presented in Sect. 4.4-B. Based on that and on the knowledge of the grid interfacing inductor L_F, the PI controller can be designed to meet specified bandwidth and phase margin values. The grid impedance Z_G is considered negligible in this design, assuming the converter is connected to an ideal grid. As will be shown in Sect. 4.4.3, the PI controller ensures a satisfactory robustness against Z_G parameters variations. Besides, the performance of the system in a weak grid case will be adequately dealt with in Ch.6.

4.3 Stability analysis

This section discusses the sensitivity of inductor current and output voltage loop stability to the uncertainty affecting the regulator parameters. All equations assume steady-state operation and consider electrical variables averaged over the sampling period. As mentioned above, the stability analysis of grid current loop, which is related closely to the grid impedance, will be presented in Sec. 6.1.

4.3.1 Stability of the inductor current control loop

Considering symmetrical PWM and averaging the voltage applied to the inductor in any half of a modulation period, the following average-current equation can be written:

$$\overline{i_L}(k+1) = \overline{i_L}(k) + [2d(k) - 1] \cdot \frac{V_{DC}}{2Lf_{sw}} - \frac{\overline{v_O}(k)}{2Lf_{sw}}\,, \tag{4.15}$$

where L is the actual filter inductance. From (4.5) and (4.15), the closed-loop transfer function between the inductor current and its reference is found to be given by:

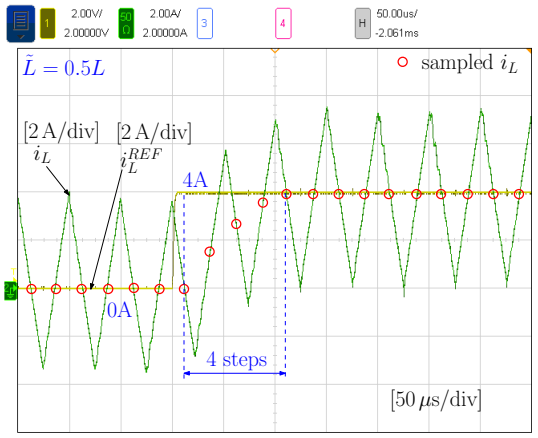
$$W_{i_L}(z) = \frac{i_L(z)}{i_L^{REF}(z)} = \frac{\frac{\tilde{L}}{L}}{z - 1 + \frac{\tilde{L}}{L}}\,. \tag{4.16}$$

To maintain stability, the pole of this discrete-time transfer function must lie within the unity circle. Simple calculations show that if $|(\tilde{L} - L)/L| < 1$, namely, if the relative error of the modeled inductance value is less than $\pm 100\%$, the stability of the inductor current loop is guaranteed. It is worth remarking that, in deriving (4.15), the parasitic resistance of the inductor is neglected, under the assumption that its L/R time constant is in any case *orders of magnitude longer* than the averaging period.

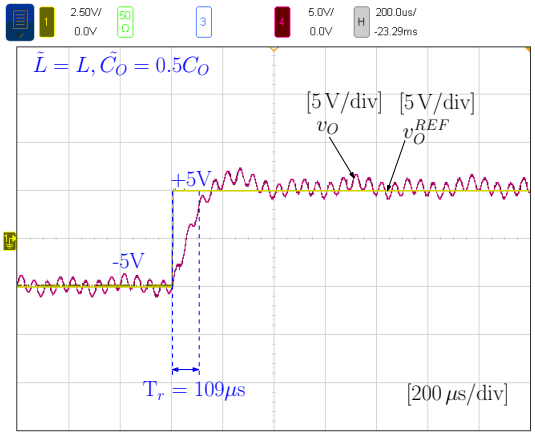
Fig. 4-7(a), (c), (e) show the small-signal step responses of the inductor current loop considering: *(a)* an underestimation of the filter inductance by 50% (i.e., $\tilde{L} = 0.5L$), *(c)* the exact value of the filter inductance (i.e., $\tilde{L} = L$), *(e)* an overestimation of the filter inductance by 50% (i.e., $\tilde{L} = 1.5L$). Fig. 4-7(a) and 4-7(e) highlight a detrimental effect on the inductor current regulation, which, however, keeps stable in both cases. Compared with Fig. 4-7(c), the inductor current in Fig. 4-7(a) shows slower dynamics (i.e., 4 steps) in tracking the current reference.

4.3.2 Stability of the output voltage control loop

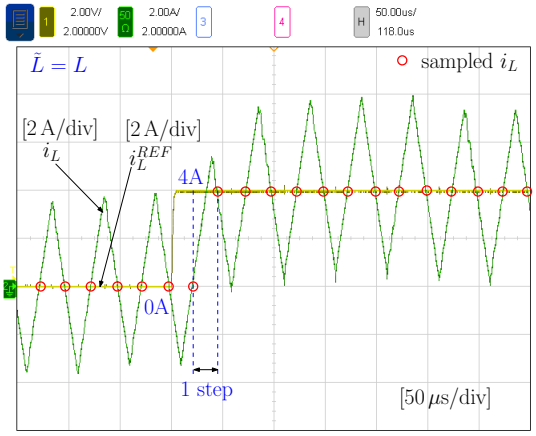
Because the voltage controller updates i_L^{REF} every period T_{sw}, while the current controller operates with time step equal to $T_{sw}/2$, the current reference samples in (4.5) are actually



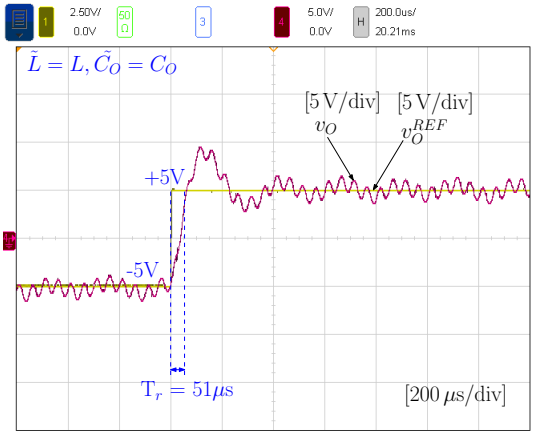
(a) Underestimation of L



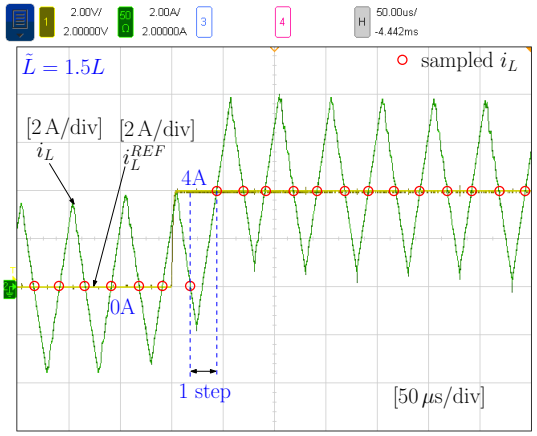
(b) Underestimation of C_O



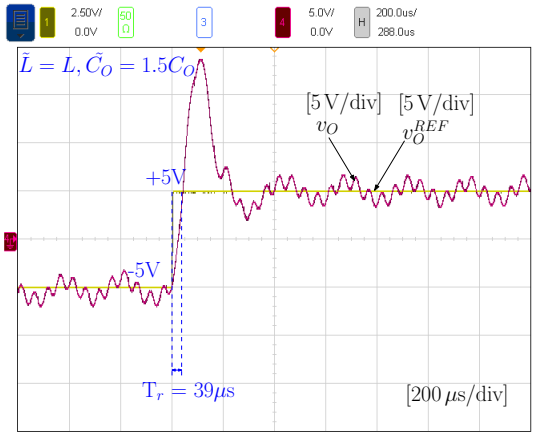
(c) Precise estimation of L



(d) Precise estimation of C_O



(e) Overestimation of L



(f) Overestimation of C_O

Figure 4-7: Behavior of the inner loops if errors are introduced in the parameters of the control laws (4.5) and (4.9).

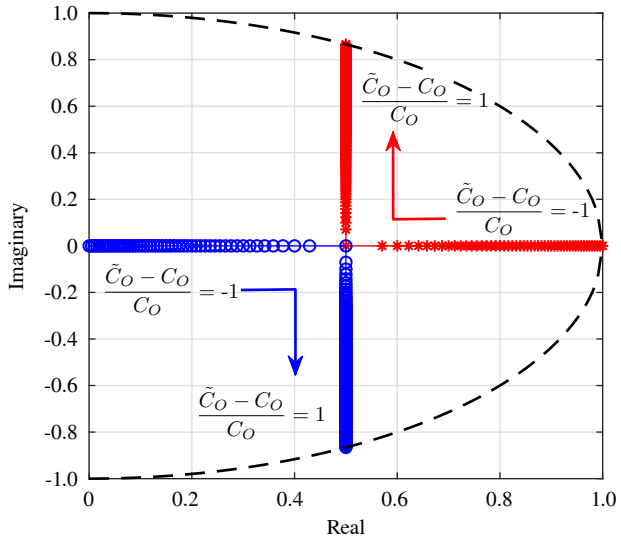


Figure 4-8: Root locus of (4.19) with respect to variations of output capacitance C_O.

constrained by the following relation:

$$i_L^{REF}(k+1) = i_L^{REF}(k) = i_L^{REF}(n). \tag{4.17}$$

Now, by $\mathcal{Z}$-transforming (4.7) and using (4.9) and (4.17), after some algebraic manipulations [150], the reference to output voltage transfer function can be derived as:

$$W_{v_O}(z) = \frac{\frac{\tilde{L}\tilde{C}_O}{LC_O}}{2z^2 - 2z(2-\frac{\tilde{L}}{L}) + \frac{\tilde{L}\tilde{C}_O}{LC_O} + 2(1-\frac{\tilde{L}}{L})}. \tag{4.18}$$

Provided that the inductor L is precisely modeled by the inner inductor current loop, namely, $\tilde{L}/L = 1$, (4.18) can be further simplified as:

$$W_{v_O}(z) = \frac{\frac{\tilde{C}_O}{C_O}}{2z^2 - 2z + \frac{\tilde{C}_O}{C_O}}, \tag{4.19}$$

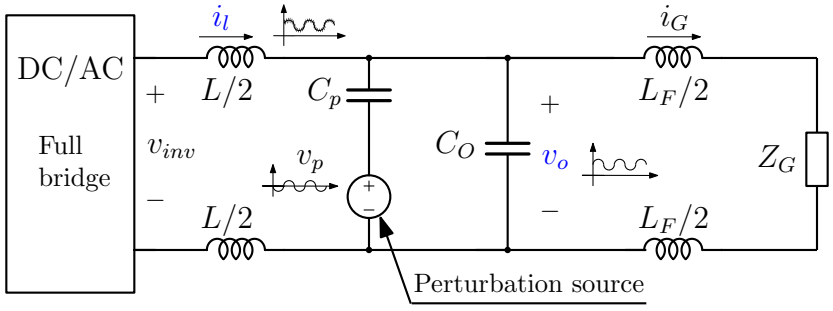
where the uncertainty in the controller parameter C_O is explicitly represented. By sweeping the relative error of the capacitor [i.e., $(\tilde{C}_O - C_O)/C_O$], the poles of the transfer function (4.19) can be determined as shown in Fig. 4-8. Notably, an error lower than 100% for $(\tilde{C}_O - C_O)/C_O$ guarantees stability, being the maximum magnitude of the poles always smaller than unity. Of course, if the inner and/or the outer loop are not properly tuned, the controller

dynamic performance might significantly differ from the nominal one. Nevertheless, both loops can be considered intrinsically robust, as the critical parameter estimation error is much larger than the typical component tolerance.

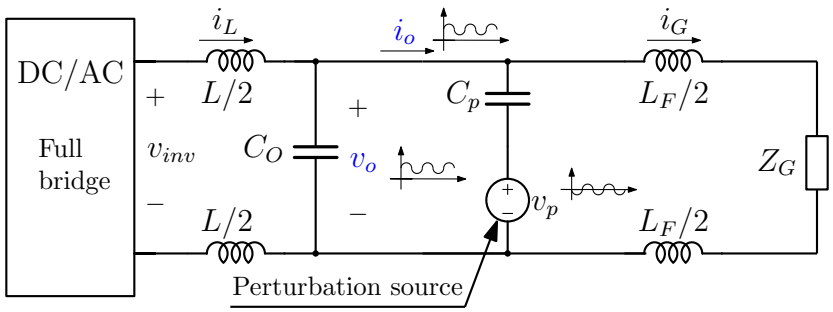
Similar tests are performed and reported in Fig. 4-7(b), (d), (f) for the output voltage loop, varying the value of the modeled output capacitance $\tilde{C}_O$, while not introducing errors in the inductance value (i.e., $\tilde{L} = L$). For a 50% underestimation of C_O [see Fig. 4-7(b)], a rise time T_r = 109 μs is measured, which is almost doubled compared with that of case Fig. 4-7(d), where T_r = 51 μs. In addition, it is also verified that a 50% overestimation of C_O [see Fig. 4-7(f)] does not cause unstable behaviors, neither in the inductor current nor in the output voltage. This result shows the intrinsic robustness of the controller with respect to mismatches in the inner loop parameter values.

4.4 Output impedance analysis

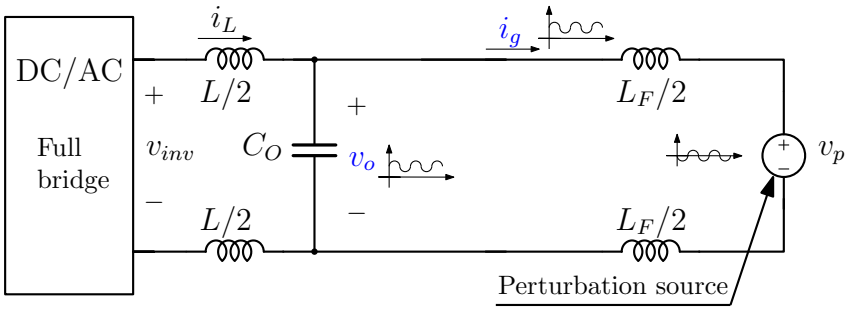
As discussed in Sec. 4.1 and in Sec. 4.2, the optimal shaping of the converter's output impedance in the frequency domain is the criterion adopted to steer the whole control system design. In this section, the analytical expressions of the converter output impedance is derived as determined by the proposed control system in Fig. 4-2. The results are also verified by numerical simulations and direct measurements. Both simulations and measurements are performed as is illustrated in Fig. 4-9, namely, by injecting a perturbation signal and measuring the appropriate voltage and current signals at different frequencies. The frequency of the injected perturbation signal spans the range $[0.1,\ 10]$ kHz. At low frequencies, an ac power supply is used, while the power operational amplifier PA107DP is employed above 1 kHz. It is worth noting that, in the literature, the converter output impedance is most often analyzed in the $\mathcal{S}$-domain, that is, using the Laplace transform [197–201]. This approach is not applicable to digital controllers that have no continuous-time counterpart, like the DB controllers. These can only be approximately described in the continuous time domain, yielding inaccurate results, especially close to the Nyquist frequency. On the contrary, the discrete-time analysis here performed perfectly matches the discrete-time controller nature and, as a consequence, provides more accurate results.



(a) Inductor current (i_L) loop is closed



(b) Output voltage (v_O) loop is closed



(c) Grid current (i_G) loop is closed

Figure 4-9: Measurement of the converter output impedance.

4.4.1 Inductor current loop

Even if the converter of Fig. 2-5 is not going to be controlled just by the single inductor current loop, the study of its output impedance is now presented, both for completeness and to further validate the analysis of the controller's dynamic response. Based on (4.5), the output impedance expression for the current deadbeat controller, Z_{o,i_L}, is easily derived as:

$$Z_{o,i_L}(z) = -\frac{v_O(z)}{i_L(z)} = \frac{4 f_{sw} L}{1 - z^{-1}}. \tag{4.20}$$

The form of (4.20), that corresponds to a discrete time integral function, reveals that the

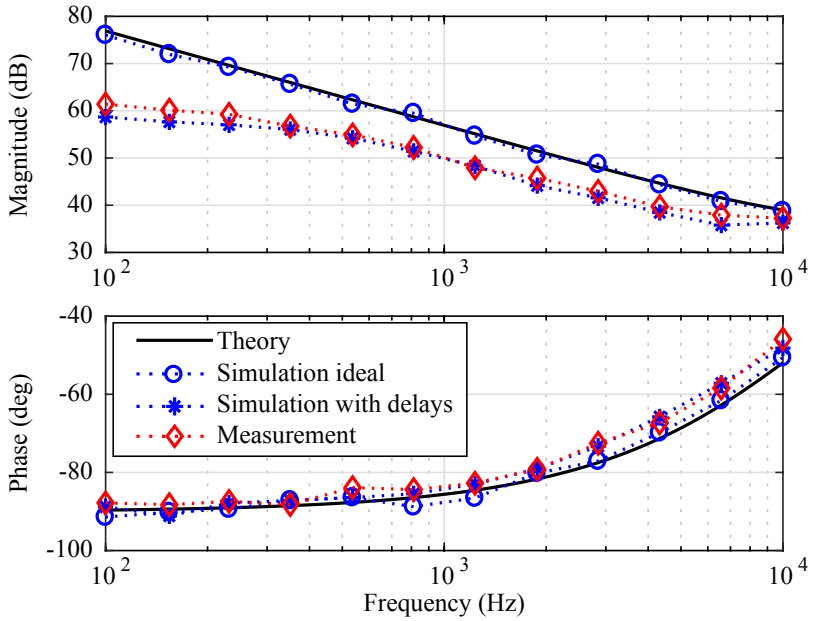


Figure 4-10: Converter output impedance when only inductor current loop is closed.

output impedance is capacitive in nature, at least up to the Nyquist frequency. It is easy to determine the equivalent capacitor corresponding to the same impedance. That turns to be very small, being equal to $C_{i_{Leq}} = 1/(8 f_{sw}^2 L) \cong 224\,\text{nF}$ in the considered set-up. Fig. 4-10 compares the results given by (4.20), the results from an accurate simulation model, and the measurements from the experimental implementation of the system in Fig. 2-5, performed as shown in Fig. 4-9a.

It is worth noting that, according to (4.20), Z_{o,i_L} is extremely high, which makes its measurement very sensitive to the effects of all possible non-idealities of the converter implementation. For this reason, the validity of (4.20) is here proven by showing both the results marked as "simulation ideal", that refer to a simulation model where the controller is fed with the *exact* values of i_L and v_O, and the results marked as "simulation with delays", that refer to a slightly more complex model, where the delays due to the analog de-noising filters of i_L and v_O are included, as detailed in Tab. 4.1. Notably, these small delays have a significant effect on the measured output impedance.

Even if lower than in the ideal case, the measured output impedance is still very high. In magnitude, it is higher than the converter physical impedance, ωL, even at the maximum test frequency. This is due to the extremely large bandwidth of the current controller.

Table 4.1: Bandwidths of signal sensing circuits

Signals	Filter cutoff frequency	Unit
Inductor current, i_L	50	kHz
Output current, i_O	10	kHz
Grid current, i_G	10	kHz
Output voltage, v_O	8	kHz

4.4.2 Output voltage loop

When also the voltage control loop is closed, the converter can be modeled as in Fig. 4-1 (a). The resulting control structure, featuring two nested dead-beat type controllers, is denoted here as DB-DB. The output impedance resulting from this control structure is now analyzed. It can be determined by $\mathcal{Z}$-transforming (4.11) and extracting the small-signal dynamic relation between the output voltage and the output current. After a few mathematical manipulations, we find:

$$Z_{o,v_O}(z) = -\frac{V_O(z)}{I_O(z)} = \frac{1}{C_O f_{sw}} \cdot \frac{z-1}{2z^2-2z+1}\,. \tag{4.21}$$

It is interesting to determine the low frequency and high frequency asymptotic approximations of Z_{o,v_O} in the *continuous time domain.* As far as the former is concerned, we find that

$$Z^{LF}_{o,v_O} \approx \frac{C_O^{-1} f_{sw}^{-1}\left(1+\frac{T_{sw}}{2}s-1\right)}{2(1+T_{sw}s)-2(1+\frac{T_{sw}}{2}s)+1} \approx \frac{s}{2C_O f_{sw}^2}\,, \tag{4.22}$$

where a first order Taylor series approximation is used, while the latter is found to be

$$Z^{HF}_{o,v_O} \approx \frac{1}{C_O f_{sw}} \cdot \frac{1}{2(z-1)} \approx \frac{1}{C_O s}\,, \tag{4.23}$$

using the backward Euler approximation of the integral function. It is therefore proven that, at low frequencies, the converter output impedance presents an approximately inductive behavior, with equivalent inductance value $L_{v_{oeq}} = 1/(2C_O f_{sw}^2)$. At high frequencies, instead, the converter output impedance is capacitive, with equivalent value $C_{v_{oeq}} = C_O$,

as it could be expected. The intersection frequency f^* of the two asymptotes is:

$$f^* = \frac{1}{2\pi \cdot \sqrt{L_{eq} \cdot C_{eq}}} = \frac{f_{sw}}{\sqrt{2}\pi}\,, \tag{4.24}$$

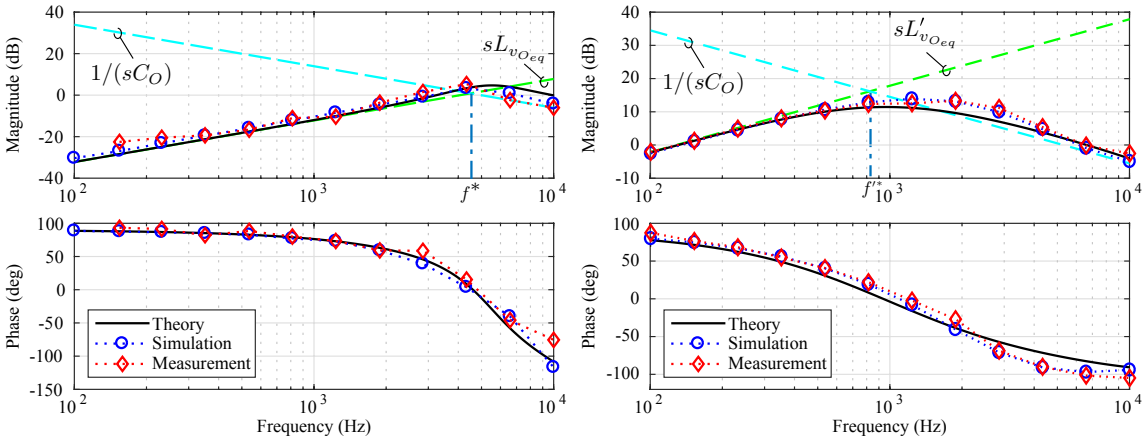
which is equal to $4.50\,\mathrm{kHz}$ in the considered set-up. To better highlight the advantages of the DB-DB controller, this is now compared to a DB-PI controller, that is, a controller that employs the same deadbeat regulator (4.5) for i_L, but a standard PI regulator to control v_O. It is possible to calculate the converter output impedance Z'_{o,v_O} and closed loop transfer function W'_{v_O} determined by the DB-PI controller. These are given by:

$$Z'_{o,v_O}(z) = -\frac{V_O(z)}{I_O(z)} = \frac{\dfrac{1}{2C_O \cdot f_{sw}} \cdot \dfrac{z}{z-1}}{1 + \dfrac{H^{PI}_{v_O}(z)}{2C_O \cdot f_{sw}} \cdot \dfrac{1}{z-1}}\,, \tag{4.25}$$

$$W'_{v_O}(z) = \frac{V_O(z)}{V_O^{REF}(z)} = \frac{\dfrac{H^{PI}_{v_O}(z)}{2C_O \cdot f_{sw}} \cdot \dfrac{1}{z-1}}{1 + \dfrac{H^{PI}_{v_O}(z)}{2C_O \cdot f_{sw}} \cdot \dfrac{1}{z-1}}, \tag{4.26}$$

where $H^{PI}_{v_O}(z) = Kp_{v_O} + Ki_{v_O} \cdot \dfrac{z}{z-1}$ is the discrete-time transfer function of the output voltage PI controller. For a fair comparison, the PI gains are chosen to achieve a relatively large crossover frequency, equal to $1.5\,\mathrm{kHz}$, and a $60°$ phase margin. Actually, with the parameters of Tab. 2.3 and the considered phase margin, $1.5\,\mathrm{kHz}$ represents the largest possible bandwidth. The asymptotes of the converter output impedance are derived in this case too: at low frequency, the output impedance shows again an inductive behavior, corresponding to an equivalent inductance $L'_{v_{oeq}} = 1/Ki_{v_O}$; at high frequency, the output impedance shows the expected capacitive behavior, corresponding to capacitance C_O. The corresponding intersection frequency is now $f'^* = \sqrt{Ki_{v_O} f_{sw}/C_O}/2\pi$, which is equal to $0.82\,\mathrm{kHz}$ with the considered parameter values.

Fig. 4-11 displays the converter output impedance in the DB-DB and the DB-PI cases. The low and high frequency asymptotes, $sL_{v_{O_{eq}}}$, $sL'_{v_{O_{eq}}}$ and $1/(sC_O)$ are indicated by dashed lines. Firstly, the figure shows a close match between the obtained analytical, simulation, and experimental results, which validates the expressions (4.21) and (4.25). More-



(a) DB-DB control system **(b)** DB-PI control system

Figure 4-11: Converter output impedance when inductor current and capacitor voltage loops are both closed.

over, comparing Fig. 4-11a and Fig. 4-11b, one sees that the DB-DB controller allows to significantly decrease the converter output impedance with respect to the DB-PI one in a wide frequency range. As an example, at $1\,\mathrm{kHz}$, the DB-PI impedance magnitude is more than $20\,\mathrm{dB}$ larger than the DB-DB's. This result proves that a DB controller in the voltage loop is, by far, a better choice with respect to a PI controller. This holds also for other types of widely adopted linear voltage controllers, like the PR ones. Indeed, replacing the integrator with a bank of resonant filters boosts the loop gain, reducing the output impedance, only at the resonance frequencies, but everywhere else worsens the gain of the controller. Furthermore, the settling time of the resonant filters is unavoidably traded-off against their selectivity, which makes it impossible to simultaneously achieve high gain and fast response. The proposed solution instead, guarantees a minimum delay response and high gain in the whole low frequency region.

As a further assessment, the bandwidth of the closed loop transfer function W_{v_O} has been determined for the two controllers, finding it equal to $1.5\,\mathrm{kHz}$ for the DB-PI and to $7.9\,\mathrm{kHz}$ for the DB-DB. Clearly, the wider small-signal bandwidth of the DB-DB solution ensures an easier design of the third control loop (i.e., the i_G control loop), as is discussed in the following section.

4.4.3 Grid current loop

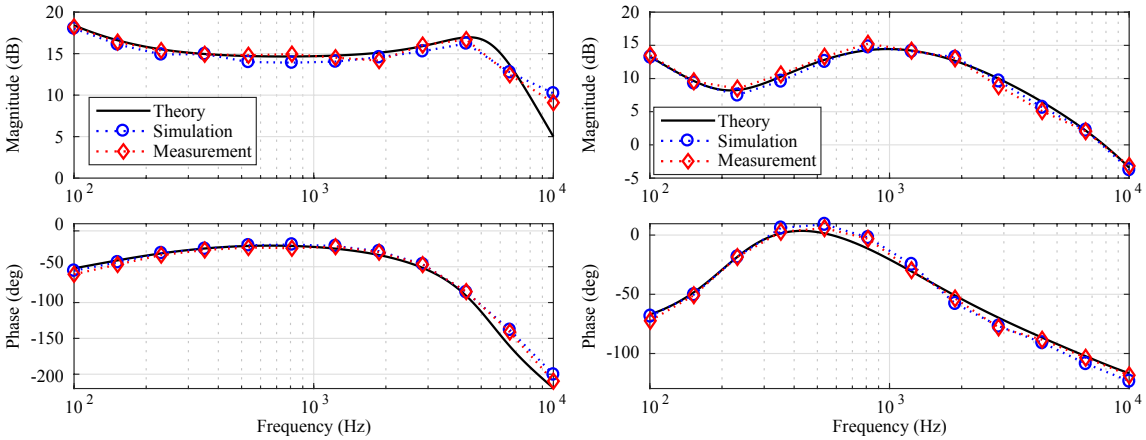
As explained in Sect. 4.2.3, a PI controller is adopted for the outer, grid current i_G control loop. Differently from the inner loops, the external controller's design needs to cope with significant uncertainties in the grid impedance, Z_G. As known, a PI controller is, in principle, capable of ensuring robust stability, provided that the loop phase margin is adequately oversized. The final triple-loop controller is denoted as DB-DB-PI or DB-PI-PI, based on whether the dead-beat or the PI controller is adopted for output voltage control, the latter being considered only as the benchmark of a high performance, conventional design. The third control loop turns the converter again into a controlled current source, that can be represented by the equivalent circuit of Fig. 4-1 (b).

According to (4.4), the equivalent converter output impedance should be as large as possible. The impedance has been derived both for the DB-DB-PI and the DB-PI-PI case, yielding respectively:

$$\begin{aligned} Z_{o,i_G}(z) &= -\frac{V_O(z)}{I_G(z)} = W_{v_O}(z)\cdot H_{i_G}^{PI}(z) + Z_{o,v_O}(z) \\ &= \frac{1}{C_O f_{sw}}\cdot\frac{C_O f_{sw}\cdot H_{i_G}^{PI}(z) + z - 1}{2z^2 - 2z + 1} \end{aligned} \tag{4.27}$$

$$\begin{aligned} Z'_{o,i_G}(z) &= -\frac{V_O(z)}{I_G(z)} = W'_{v_O}(z)\cdot H_{i_G}^{PI}(z) + Z'_{o,v_O}(z) \\ &= \frac{\dfrac{1}{2C_O\cdot f_{sw}}\left[H_{v_O}^{PI}(z)\cdot\dfrac{H_{i_G}^{PI}(z)}{z-1} + \dfrac{z}{z-1}\right]}{1 + \dfrac{1}{2C_O\cdot f_{sw}}\cdot H_{v_O}^{PI}(z)\cdot\dfrac{1}{z-1}} \end{aligned} \tag{4.28}$$

Fig. 4-12 shows the simulation and experimental results for both cases. The maximum achievable bandwidth of the third loop, given a target 60° phase margin, is $1.5\,\mathrm{kHz}$ and $260\,\mathrm{Hz}$ in the DB-DB-PI and in the DB-PI-PI case, respectively. Please note that the design assumed $R_G = 0\,\mathrm{m\Omega}$, $L_G = 0\,\mathrm{mH}$, that is, an ideal connection to the grid. The obtained theoretical, simulation, and experimental results are consistent among each other. By comparing Fig. 4-12a and Fig. 4-12b, it is possible to remark that the output impedance with the DB-DB-PI case is significantly higher than that of the DB-PI-PI case. As a conse-



(a) DB-DB-PI control system **(b)** DB-PI-PI control system

Figure 4-12: Converter output impedance when grid current loop is closed.

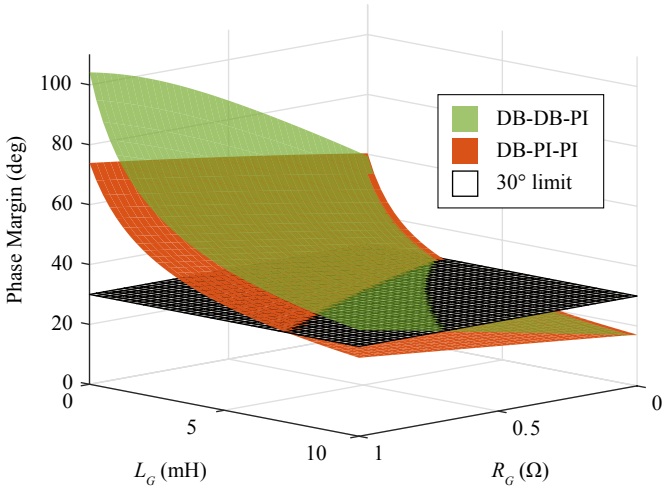


Figure 4-13: Phase margin of the grid current control loop as a function of the grid connection parameters for a constant 260 Hz bandwidth.

quence of (4.4), the former is expected to be capable of higher robustness and performance for any given operating condition.

4.5 Experimental verification

The results presented in Sect. 4.4 show that the DB-DB-PI control structure allows to achieve a large-bandwidth control of the grid current i_G and a high impedance seen at PCC with the grid. These characteristics are now verified experimentally on the nano-grid testbench. Its grid-tied inverter set-up, of course, exactly matches Fig. 2-5, with the pa-

rameters listed in Tab. 2.3. The tests reported in the following refer to the control system configured as in Tab. 4.2.

Table 4.2: Controller parameters

Loop	Type	Parameter	Symbol	Value
i_L	DB	i_L error gain	$L\, f_{sw}/V_{DC}$	0.0622
		v_O gain	$V_{DC}/2$	0.0011
		closed loop gain	W_{i_L}	z^{-1}
v_O	DB	v_O error gain	$C_O \cdot f_{sw}$	0.6
		bandwidth (kHz)	BW_{v_O}	7.94
i_G	PI	proportional gain	Kp_{i_G}	5
		integral gain	Ki_{i_G}	0.43
		bandwidth (kHz)	BW_{i_G}	1
		phase margin (°)	PM_{i_G}	60

4.5.1 Dynamic response of grid current loop

To illustrate the dynamic tracking performance of the injected grid current i_G, the response of the system to step changes of the current reference i_G^{REF} are considered in Fig. 4-14. In this test, the non-linear load is connected in parallel with capacitor C_O.

The current reference is set to apply, at grid voltage peaks, step changes of the power injected into the grid. Specifically, the following sequence of power references is considered: *i*) zero power exchange, *ii*) $1\,\mathrm{kW}$ pure active power injection, *iii*) $1\,\mathrm{kVAr}$ pure reactive power injection, *iv*) zero power exchange. The current quality under the working condition of pure active or reactive power injection is also evaluated by extending the testing time of phases *ii*) and *iii*), respectively. With the non-linear load connected ($\mathrm{THD}_{i_{Load}}$ = 96.4%, rms current is 2.8 A), the proposed triple-loop controller still achieves low-distortion current injection as well as a firm supply to the local loads.

Zoomed-in views of the transitions are shown in Fig. 4-15. As can be seen, grid current i_G reaches its new reference within $450\,\mu\mathrm{s}$ with no significant overshoot. At the same time, the local voltage v_O is almost unaffected by the current step changes; we measured a maximum voltage fluctuation equal to 13.5 % of peak voltage, that is rapidly dampened. In

all cases, i_G shows very little sensitivity to the non-linear load current and so does voltage v_O.

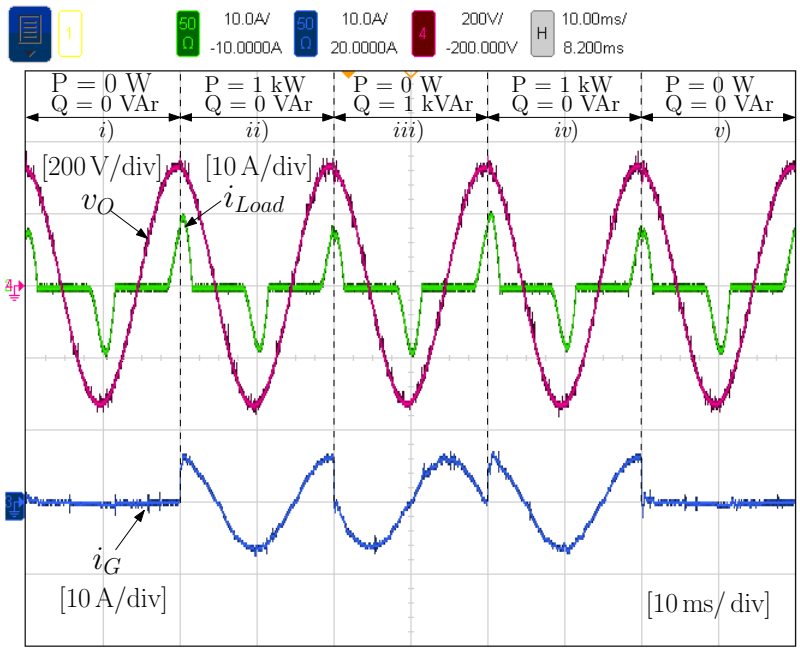
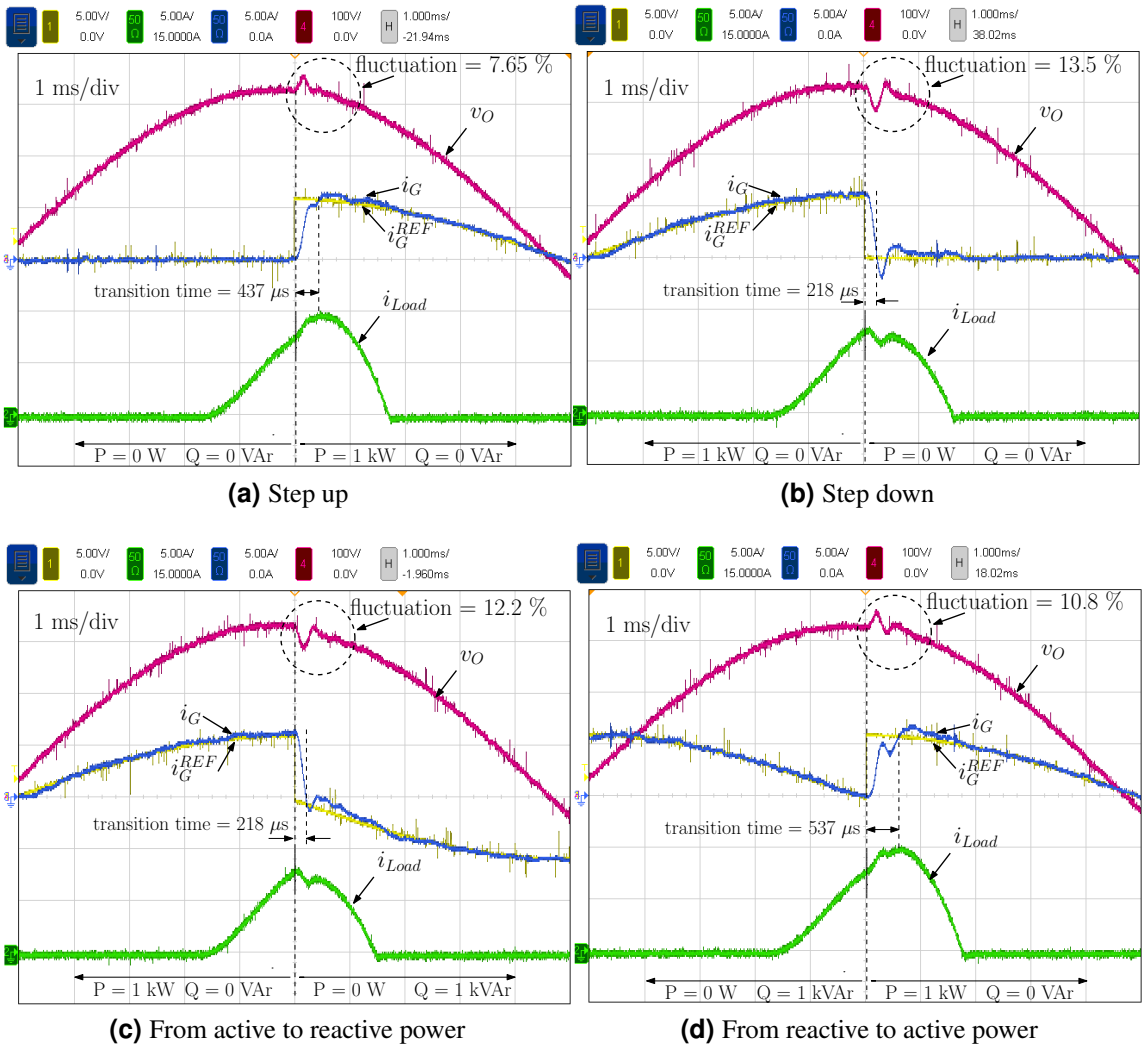


Figure 4-14: Dynamic response : *i*) zero power exchange, *ii*) 1 kW pure active power injection, *iii*) 1 kVAr pure reactive power injection, *iv*) 1 kW pure active power injection, *v*) zero power exchange.

4.5.2 System performance under grid voltage perturbations

Amplitude perturbations and frequency variations are commonly encountered abnormal conditions, especially in weak grids [202]. A grid interface converter should operate reliably even in those cases. Therefore, we tested the performance of the proposed control system in such conditions, obtaining the results discussed in the following.

Fig. 4-16 shows the system behavior when a step change (from 100% to 75% of the nominal voltage) occurs in the amplitude of the grid voltage. As can be seen, despite the severity of the transient, the system remains stable, and recovers normal operation immediately after the step, without measurable performance degradation. Fig. 4-17, instead, shows the converter's response to frequency steps (from 50 Hz to 51 Hz and *vice versa*) of the grid voltage. Notably, the system keeps a stable operation, without causing any visible fluctuation in output voltage v_O or grid current i_G. Only the injected power is slightly affected (less than 5%) during the transients, with negligible practical consequences.



(a) Step up

(b) Step down

(c) From active to reactive power

(d) From reactive to active power

Figure 4-15: Zoomed-in views of the transients in Fig. 4-14.

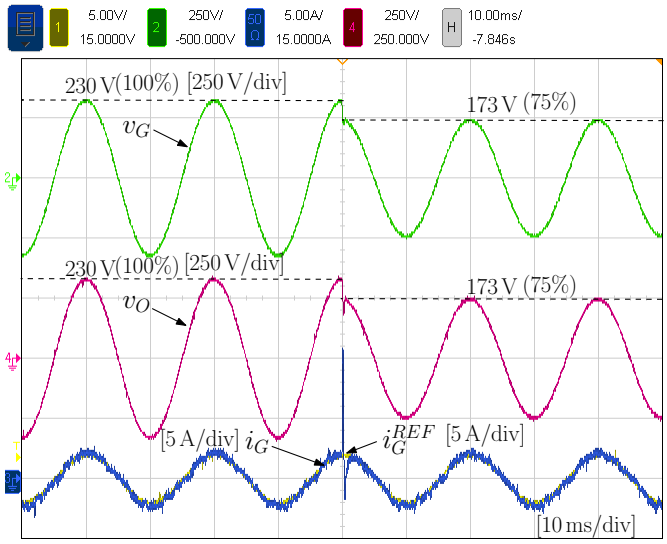


Figure 4-16: Response to a step variation of grid voltage amplitude from 230 V_{rms} (nominal) to 173 V_{rms} (75%).

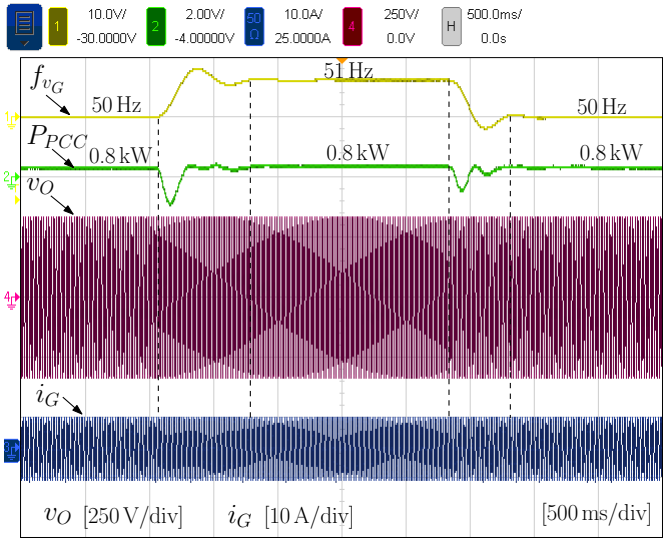


Figure 4-17: Response to a step variation of the grid voltage frequency from 50 Hz to 51 Hz and *vice versa*.

4.5.3 Distortion attenuation ability

The proposed triple-loop control strategy is capable of significantly attenuating grid current harmonics, either injected by the local non-linear loads connected at the converter-side or due to grid voltage distortions.

Recalling the discussion of Ch.3, the most representative controller structures documented in the literature and highlighted in yellow in Fig. 3-5, have been implemented and tested on the same nano-grid test-bench (please see Fig. 2-3), so as to compare them with the proposed controller. To allow a fair comparison, the different controllers structures use the same type of regulator for the same controlled variable. Specifically, *a*) dead-beat regulators are employed in i_L and v_O loops to expand their bandwidths as much as possible; *b*) the i_G loop is designed to achieve the maximum allowable bandwidth; *c*) active damping is implemented when needed to guarantee good stability margins for each controller; *d*) none of the possible steady-state harmonic attenuation provisions (e.g., resonant regulators) is used. Tab. 4.3 summarizes the characteristics of the six controllers implemented, where K_{AD} is the damping gain of i_C loop.

In the following, three test conditions are considered to evaluate the performance of the different solutions: *i*) ideal grid, considered as benchmark, where an ideal grid voltage is considered, provided by an ac laboratory power supply; *ii*) distorted grid, where multiple low-order harmonics (i.e., 5% of 3rd, 5th, and 7th harmonic) are added to consider grid voltage pollution; *iii*) distorted grid with local NLL, where a non-linear load is also added in parallel with the filter capacitor C_O.

Table 4.3: Implemented controllers for the tests of Fig. 4-18, Fig. 4-19 and Fig. 4-20.

Loop	**Controller structure (inner-outer)**	**Schematic**	**Regulators (inner-outer)**		
			Types	**Control equations**	**Control loop parameters**
Single	i_L	Fig.3-1	DB	(4.5)	$[1/(2f_s)]$
Double	i_C-i_G	Fig.3-2 (b)	P-PI	K_{AD} - (4.13)	[Maximum bandwidth]
	i_L-v_O	Fig.3-2 (a)	DB-DB	(4.5)-(4.9)	$[1/(2f_s)]$-$[1/f_s]$
	i_L-i_G	Fig.3-2 (a)	DB-PI	(4.5)-(4.13)	$[1/(2f_s)]$-[Maximum bandwidth]
	v_O - i_G	Fig.3-2 (c)	DB-PI	(4.9)-(4.13)	$[1/f_s]$-[Maximum bandwidth]
Triple	i_L-v_O-i_G	Fig.3-3 (a)	DB-DB-PI	(4.5)-(4.9)-(4.13)	$[1/(2f_s)]$-$[1/f_s]$-[Maximum bandwidth]

Table 4.4: Measured THD values in test condition *i*)

Loop	Controller structure	Distorted grid	
		THD_{v_O}	THD_{i_G}
Single	i_L	0.48 %	0.88 %
Double	i_C-i_G	0.57 %	1.61 %
	i_L-v_O	0.45 %	2.30 %
	i_L-i_G	0.62 %	1.44 %
	v_O-i_G	0.55 %	1.23 %
Triple	i_L-v_O-i_G	0.53 %	0.87 %

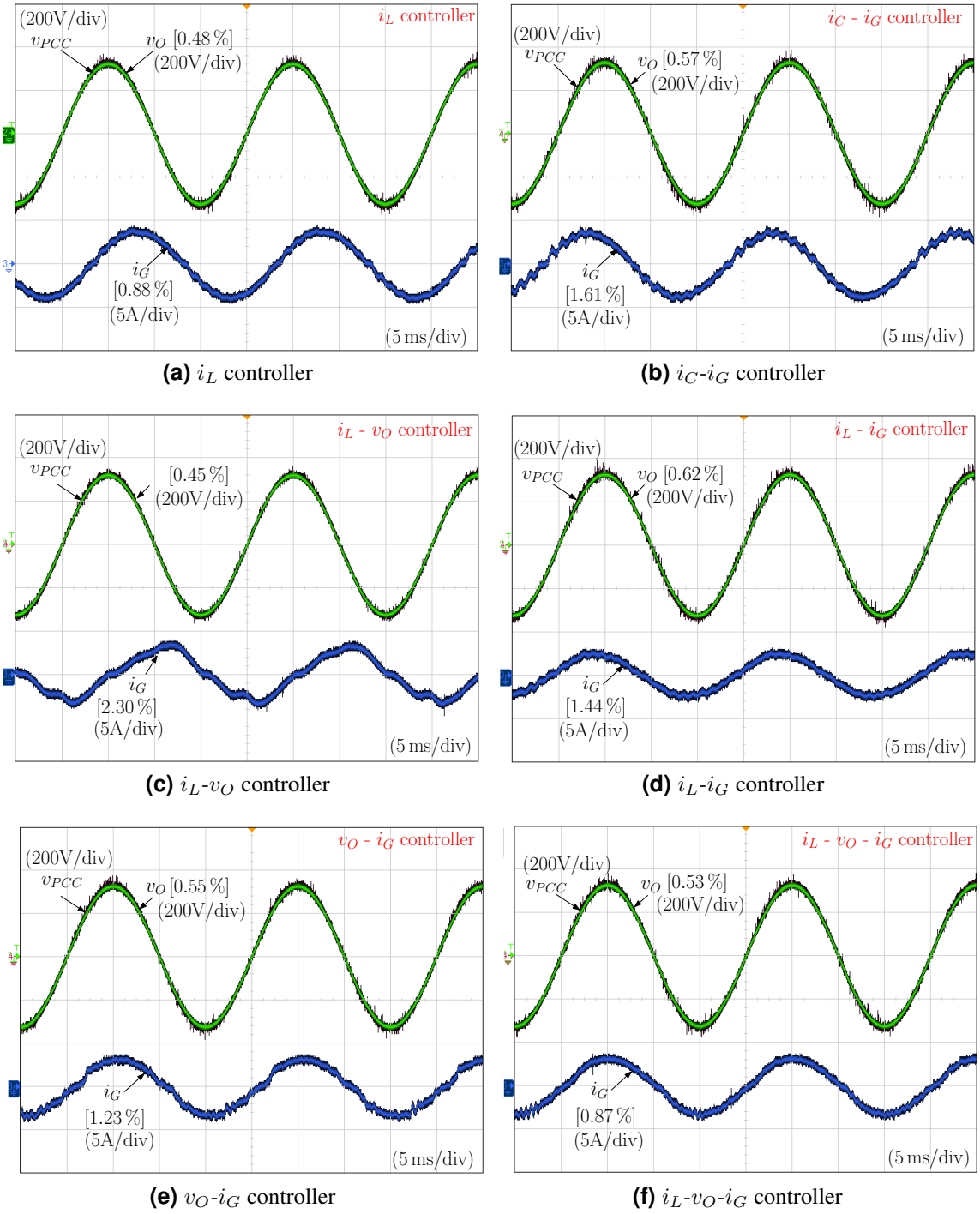
THD_{v_O} and THD_{i_G} are calculated with respect to the nominal voltage V_N and nominal current I_N respectively.

The waveforms from three different tests of six different control strategies are shown in Fig. 4-18, Fig. 4-19 and Fig. 4-20, while the measured THD values are reported in Tab. 4.4, Tab. 4.5 and Tab. 4.6 respectively. On the basis of the obtained results, the following comments can be made.

- The i_L-v_O and the i_L-v_O-i_G controllers have better harmonic attenuation performance for local voltage v_O and injected grid current i_G, respectively, as can be seen in Fig. 4-18 - Fig. 4-20 and confirmed by the THD values in Tab. 4.4 - Tab. 4.6. Without any additional harmonic attenuation provision, THD_{v_O} is as low as 6.29 % with the i_L-v_O controller, while THD_{i_G} is as low as 2.58 % with the i_L-v_O-i_G controller, even under the significantly distorted test conditions *iii*).

- Comparing Fig. 4-20(e) and Fig. 4-20(f), it is possible to appreciate the importance of the i_L loop in damping resonances. This is the reason why the harmonic attenuation performance improves, with THD_{i_G} that reduces from 4.68 % in the case of v_O-i_G to 2.58 % in the case i_L-v_O-i_G.

- Controllers i_C-i_G, i_L-i_G, v_O-i_G and i_L-v_O-i_G show a higher quality of the injected power than the other cases (i.e., i_L and i_L-v_O) where grid current i_G is not controlled. This is consistent with the discussion in Sec. 3.2.1 and agrees with the analysis in Fig. 3-5



(a) i_L controller

(b) i_C-i_G controller

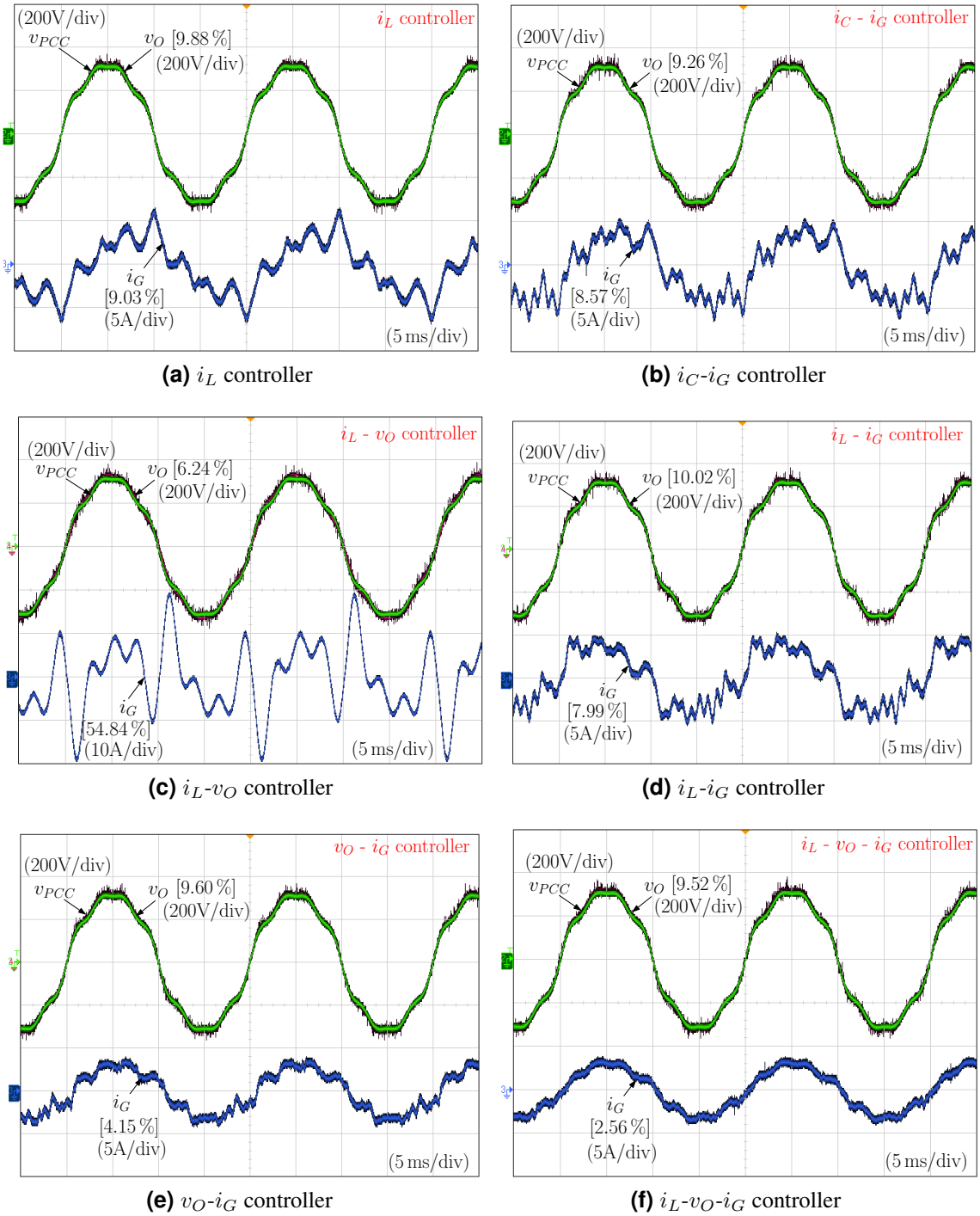
(c) i_L-v_O controller

(d) i_L-i_G controller

(e) v_O-i_G controller

(f) i_L-v_O-i_G controller

Figure 4-18: Inverter performance under *i*) ideal grid voltage.



(a) i_L controller

(b) i_C-i_G controller

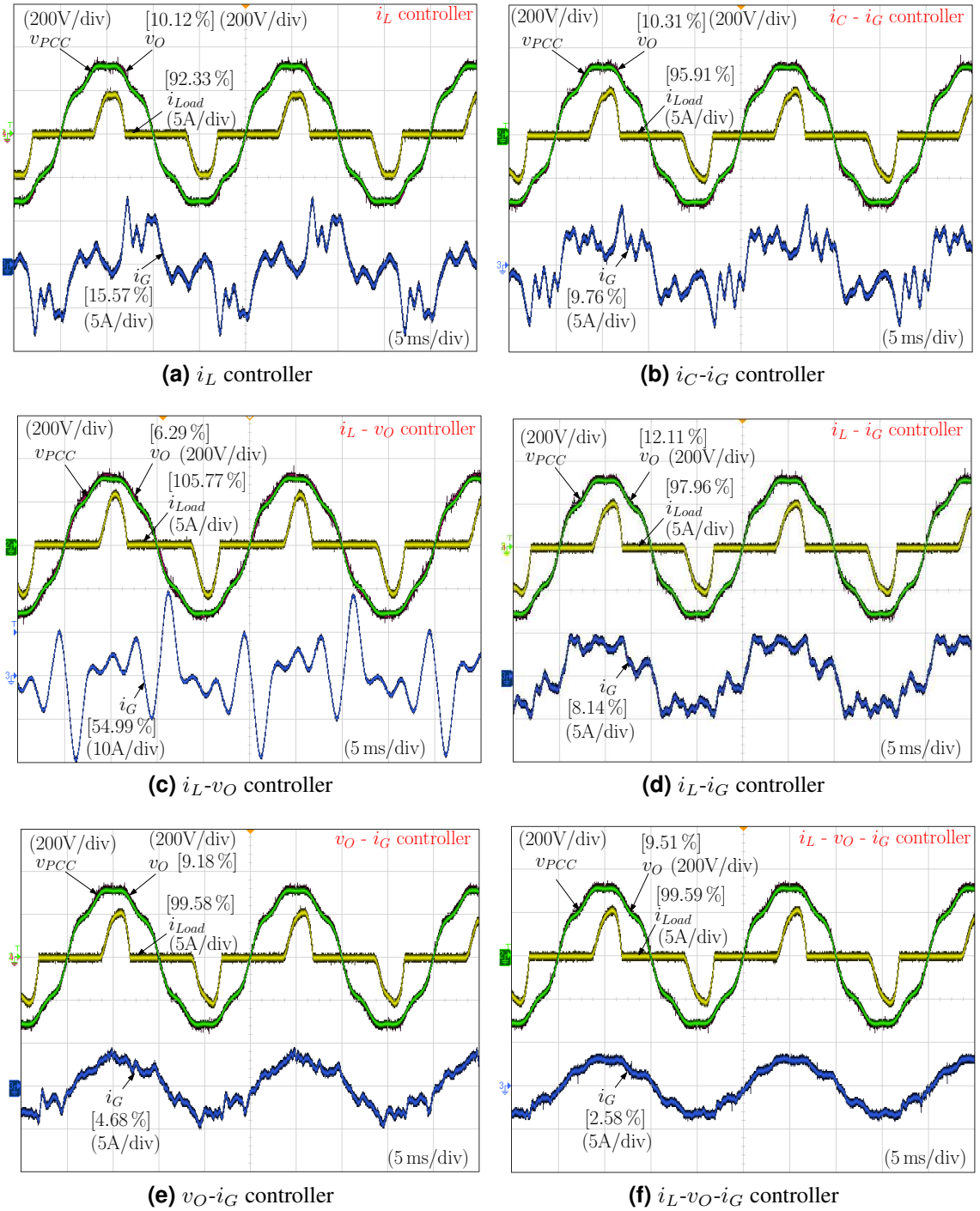
(c) i_L-v_O controller

(d) i_L-i_G controller

(e) v_O-i_G controller

(f) i_L-v_O-i_G controller

Figure 4-19: Inverter performance under *ii*) polluted grid voltage.



(a) i_L controller

(b) i_C-i_G controller

(c) i_L-v_O controller

(d) i_L-i_G controller

(e) v_O-i_G controller

(f) i_L-v_O-i_G controller

Figure 4-20: Inverter performance under *iii*) polluted grid voltage with local distorting load.

Table 4.5: Measured THD values in test condition *ii*)

Loop	Controller structure	Distorted grid	
		THD_{v_O}	THD_{i_G}
Single	i_L	9.88 %	9.03 %
Double	i_C-i_G	9.26 %	8.57 %
	i_L-v_O	6.24 %	54.84 %
	i_L-i_G	10.02 %	7.99 %
	v_O-i_G	9.60 %	4.15 %
Triple	i_L-v_O-i_G	9.52 %	2.56 %

Table 4.6: Measured THD values in test condition *iii*)

Loop	Controller structure	Non-linear load + distorted grid		
		$\text{THD}_{i_{Load}}$	THD_{v_O}	THD_{i_G}
Single	i_L	92.33 %	10.12 %	15.57 %
Double	i_C-i_G	95.91 %	10.31 %	9.76 %
	i_L-v_O	105.77 %	6.29 %	54.99 %
	i_L-i_G	97.96 %	12.11 %	8.14 %
	v_O-i_G	99.58 %	9.18 %	4.68 %
Triple	i_L-v_O-i_G	99.59 %	9.51 %	2.58 %

- The only difference between testing condition *ii*) and *iii*) is the non-linear local load, which can generate multiple harmonics locally. By comparing Tab. 4.5 with Tab. 4.6, it is possible to notice an evident increase of THD_{i_G} values in the case of controllers i_L, i_C-i_G, and i_L-i_G, while only negligible changes for the remaining three cases (i.e., i_L-v_O, v_O-i_G, and i_L-v_O-i_G) where output voltage v_O is directly controlled. The tested results verify the effectiveness of the control of the output voltage v_O in compensating harmonics generated by local loads.

- Referring to Tab. 4.6 and Tab. 4.5, it is clearly shown that the v_O-i_G and i_L-v_O-i_G controllers provide better overall performance. Even without any additional harmonic attenuation provisions, high quality grid current can be guaranteed even under severely distorted condition, easily complying with grid-interface standards (THD_{i_G} < 5 %).

4.6 Summary

This chapter presents a large-bandwidth, triple-loop control strategy for grid-tied single-phase voltage source inverters. The control system is designed hierarchically from inner inductor current, to output voltage and, finally, outer grid current loop. Output impedance optimization criteria are considered to steer the regulators' design, resulting in the adoption of dead-beat type controllers for the two inner loops. A PI controller is chosen for the outer loop as it offers a good trade-off between performance and robustness with respect to grid impedance parameter variations. Thanks to the large-bandwidth control of the injected grid current, the converter achieves *i*) an excellent reference tracking performance, *ii*) a strong attenuation of grid current harmonics, *iii*) robust stability in the presence of grid perturbations and impedance variations. Compared to other organizations, the proposed control strategy shows the highest potential for application to nano-grid utility interface converters.

Based on the proposed triple-loop controller organization, a variety of crucial functionalities can be further implemented, so as to set-up the high quality multi-functional control scheme required by grid-tied inverters operating in nano-grids. These will be the object of the following Chapters.

Chapter 5

Multi-mode operation and seamless mode transitions

This chapter presents a control scheme for multi-mode operation and seamless mode transitions of grid-tied inverters interfacing nano-grids and ac mains. The control system fulfills the requirements reviewed in Sec. 3.2 thanks to the underlying, large-bandwidth, triple-loop control organization introduced in Ch. 4. The target converter is meant to be connected with a local dc sub-grid at the dc side, and with a local ac sub-grid at the ac side (see Fig. 2-3). The controller manages the connection of the ac side sub-grid with the utility grid, ensuring a fast response control of the ac grid current. It therefore allows to interface renewable sources and loads, aggregated in dc and ac nano-grids, with smart power systems, providing enhanced power quality, stability and flexibility of operation.

5.1 Control analysis under different operation modes

As defined in Sec. 1.1 and shown in Fig. 1-1, the grid-tied inverter has three different modes of operation: grid-tied (G), islanded (I) and autonomous (A). It is worth noting that, in this chapter, the islanded mode of operation is considered equivalent to the grid-tied one, assuming the PCC voltage to be controlled by external grid-forming converters. The case where the nano-grid inverter is controlled so as to participate in the PCC voltage control process, therefore operating in parallel with other units as a grid forming converter, will

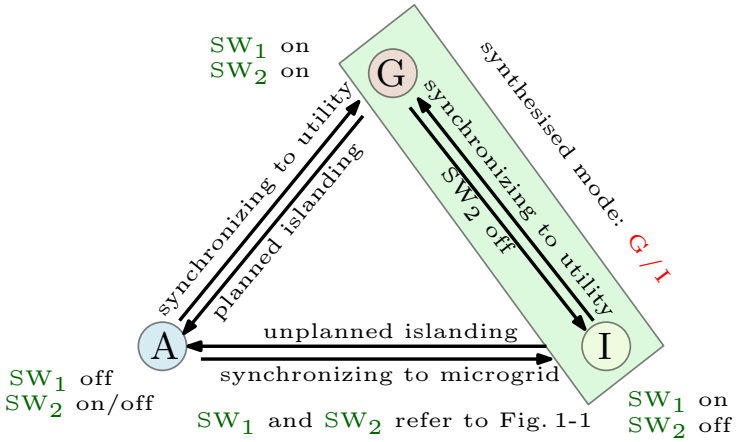


Figure 5-1: Operation modes of grid-tied inverters.

be dealt with in Ch. 7. Accordingly, out of the possible six mode transitions (see Fig. 5-1), namely (1) G to A, (2) G to I, (3) I to A, (4) A to I, (5) A to G and (6) I to G, only 2 will be taken into account: *i*) G/I to A, *ii*) A to G/I, corresponding, respectively, to the action of disconnecting from the PCC (be it planned or not) and to the synchronization and re-connection with the upstream power network (be it the mains or the rest of the micro-grid).

5.1.1 Autonomous mode of operation

When breaker SW_1 in Fig. 2-3 is open, the system operates in autonomous mode and the third control loop is disabled. The converter behaves locally as a grid forming unit, imposing across its output capacitor a sinusoidal reference voltage v_O^{REF}. The performance in this operating mode is determined by the output impedance of the converter, which should be minimized in order to make the voltage v_O independent from the delivered current i_{Load}.

Let's refer back to the small-signal output impedance determined by the adopted deadbeat type voltage controller, that is (4.21), whose plot is shown in Fig. 4-11 (a). The magnitude of (4.21) results very small $(30\,\mathrm{m\Omega}$ at $100\,\mathrm{Hz})$ and lower than $100\,\mathrm{m\Omega}$ up to $400\,\mathrm{Hz}$, a performance hardly obtainable employing standard PI regulators. Remarkably, a low output impedance is beneficial for voltage regulation, to limit voltage distortions induced by possible load harmonic currents.

5.1.2 Grid-tied or islanded mode of operation

When the breaker SW_1 in Fig. 2-3 is closed, the system can operate in either grid-tied (SW_2 is closed) or islanded (SW_2 is open) mode. In both cases, the converter can regulate the current i_G, thanks to its outer control loop. A tight grid current control increases the system's resilience to grid anomalies, such as voltage amplitude variations, voltage distortions and phase shifts in weak grids, and frequency variations in grids with low inertia. Moreover, combined with the inner control loop of v_O, the grid current control loop improves the effectiveness in compensating the harmonic currents generated locally by non-linear loads connected to the ac-link. On the contrary, under the same perturbations, to have the voltage loop driven by an outer droop loop, while allowing a simple power flow control at fundamental frequency, inevitably leads to unwanted harmonic current circulation and to significant inrush currents during severe transients.

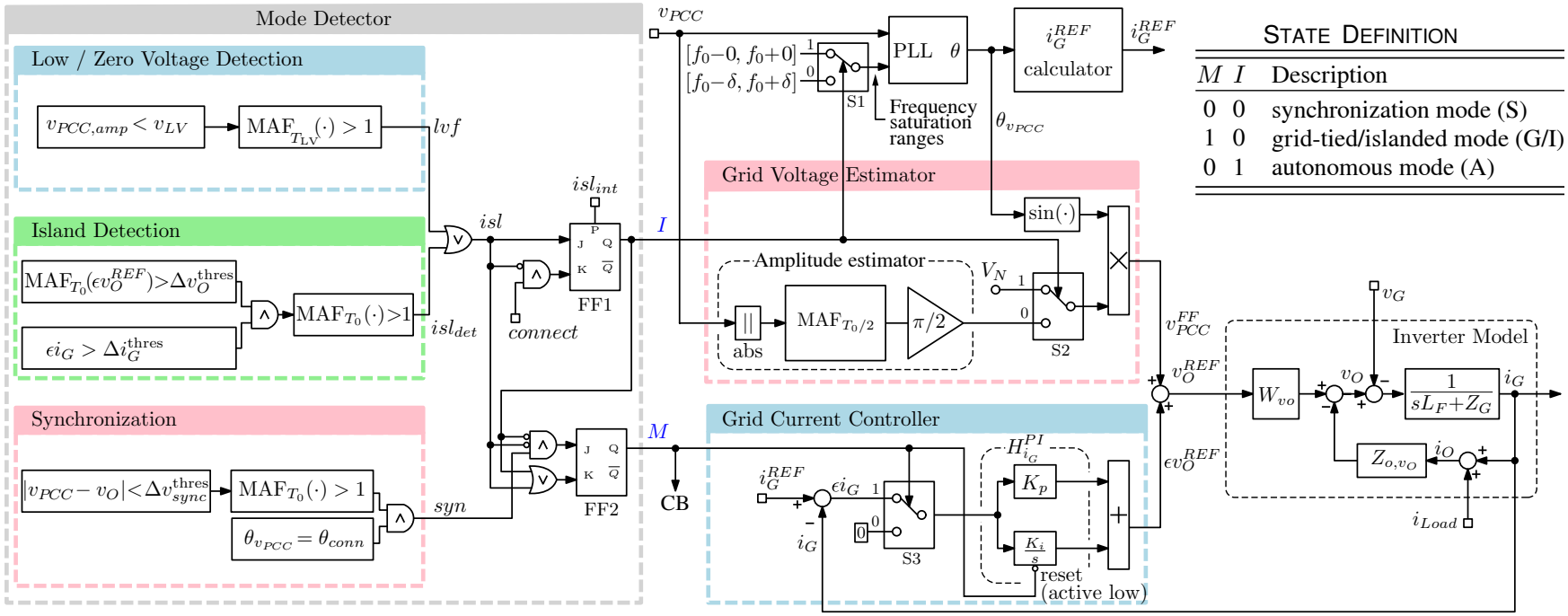
Based on the inverter output impedance Z_{o,i_G} (please see (4.27)), shown in Fig. 4-12 (a), the features described above can be directly quantified by computing the following transfer functions:

$$H_{v_O,i_{Load}}(z) = \frac{v_O(z)}{i_{Load}(z)} = \frac{Z_{o,v_O} \cdot (Z_{L_F} + Z_G)}{Z_{o,i_G} + Z_{L_F} + Z_G}\,, \tag{5.1}$$

$$H_{i_G,i_{Load}}(z) = \frac{i_G(z)}{i_{Load}(z)} = \frac{-Z_{o,v_O}}{Z_{o,i_G} + Z_{L_F} + Z_G}\,, \tag{5.2}$$

$$H_{i_G,v_G}(z) = \frac{i_G(z)}{v_G(z)} = \frac{-1}{Z_{o,i_G} + Z_{L_F} + Z_G}\,. \tag{5.3}$$

In particular, (5.1) and (5.2) quantify the controller's ability to stop the propagation of load perturbations into the ac-link voltage v_O and the grid current i_G, respectively, while (5.3) quantifies its ability of blocking the propagation of grid voltage perturbations into the grid current i_G. Clearly, a better performance is obtained in all cases if the magnitude of these transfer functions is minimized. For (5.1) and (5.2) this is achieved thanks to the very low impedance (4.21) and high impedance (4.27), while for (5.3) the voltage loop does not have any effect, therefore, it is necessary to maximize the bandwidth (and therefore the loop gain) of the current regulator, as discussed in Sec. 4.2.3.



STATE DEFINITION

M	I	Description
0	0	synchronization mode (S)
1	0	grid-tied/islanded mode (G/I)
0	1	autonomous mode (A)

Figure 5-2: Operation principle of the mode transition manager. The main blocks are highlighted in dashed boxes.)

5.1.3 Considerations about mode transitions

In order to realize seamless mode transitions with only one controller (i.e., the triple-loop controller), the following problems need to be taken into consideration:

i) in autonomous mode (A), even if the PCC voltage v_{PCC} is unavailable, the output voltage reference v_O^{REF} should be defined properly, in order to supply critical local loads.

ii) in grid-tied or islanded mode (G/I), the converter output impedance Z_{o,i_G} is expected to be as large as possible, in order to minimize the generation of circulating grid current harmonics due to grid voltage distortion.

iii) in transitions from autonomous to grid-tied or islanded conditions (A-G/I) two issues arise: in order to reduce the transient current and voltage spikes, on the one hand, output voltage v_O needs to be well synchronized with PCC voltage v_{PCC}, on the other hand, the grid current regulator must be properly brought back on-line.

iv) in transitions from grid-tied or islanded to autonomous conditions (G/I-A), the grid current regulator should be disabled and output voltage reference should be kept as smooth as possible.

5.2 Mode transition manager

In this section, we present the flexible control scheme devised to achieve seamless transitions between the grid-tied/islanded and autonomous mode of operation. Its structure and operation principle are illustrated in Fig. 5-2. The control scheme of the mode transition manager comprises:

- The *mode detector* block, where the system control mode is defined by the couple of binary state variables I and M, whose meaning is indicated in the state definition table appearing in the figure. The state transitions are driven by a series of control signals. The communication from autonomous to grid-tied/islanded operation is issued by the signal $connect$ and occurs when the voltages v_{PCC} and v_O are synchronized, which is indicated by the signal syn. The inverse transition is issued by the input isl_{int}. This latter transition can also be triggered by anomalous operating conditions,

namely, the detection of a low-voltage fault (lvf) or the islanded operation (isl_{det}), which are indicated jointly by the signal isl [1]. The following sections describe in detail how these transitions are managed. Tab. 5.1, in particular, shows the state table for M and I corresponding to the sequential circuit in Fig. 5-2.

- The *PCC voltage estimator*, that determines the fundamental component of the PCC voltage v_{PCC}^{FF}, feed-forwarded to the current controller. The phase signal is provided by a PLL, while the amplitude of v_{PCC}^{FF} is estimated, assuming a purely sinusoidal regime, by a discrete-time moving average filter (MAF) over a time interval of length $T_0/2$:

$$\mathrm{MAF}_{T_0/2}(|v_{PCC}|)(nT) = \frac{\sum_{m=0}^{N-1} |v_{PCC}(nT_s - \frac{mT_0}{2N})|}{N} . \tag{5.4}$$

  where T_s is the sampling period of v_{PCC}, n and m are integer numbers, and $T_0 = 1/f_0 = 2NT_s$.

- The *grid current controller*, that regulates the grid current i_G during grid-tied/ islanded operation.

A proper definition of the output voltage reference v_O^{REF} is crucial to attain an effective mode transition control. The reference voltage should be kept as smooth as possible during mode transitions, in order to avoid current and voltage spikes. This is accomplished by the following algorithm:

$$\begin{cases} v_O^{REF} = \epsilon v_O^{REF} + v_{PCC}^{FF} \\ \epsilon v_O^{REF} = M\,(i_G^{REF} - i_G) H_{i_G}^{PI} \\ v_{PCC}^{FF} = \left[\overline{I}\, \underbrace{\frac{\pi}{2} \mathrm{MAF}_{\frac{T_0}{2}}(|v_{PCC}|)}_{v_{PCC,amp}} + I\, V_N \right] \sin(\theta_{v_{PCC}}) \end{cases} , \tag{5.5}$$

where $\overline{I}$ represent the logic negation of the binary state variable I.

[1] Unless the cooperative, grid supporting mode of operation described in Ch. 7 is chosen.

Table 5.1: State Table for M & I variables in Fig. 5-2

Case	Input				State		Next State	
	isl_{int}	$connect$	syn	isl	M	I	$M^\star$	$I^\star$
1	1	X	X	X	X	X	0	1
2	0	X	X	1	X	X	0	1
3	0	1	0	0	0	X	0	0
4	0	1	0	0	1	X	1	0
5	0	1	1	0	X	X	1	0
6	0	0	0	0	0	0	0	0
7	0	0	1	0	X	0	1	0
8	0	0	0	0	1	0	1	0
9	0	0	X	0	X	1	0	1

X indicates that the variable is not relevant for the definition of the next state.

5.2.1 From autonomous to grid-tied/islanded mode

Let us assume to operate in autonomous mode, with state variables set as $MI = 00$. The transition to the grid-tied/islanded operation (i.e., $MI = 10$) is managed as follows.

- Initially, $MI = 00$, therefore SW_1 is open and the grid current controller is disabled. The reference voltage v_O^{REF} is equal to v_{PCC}^{FF}, which gradually aligns in amplitude and phase to the grid voltage by the action of the PLL and the PCC voltage amplitude estimator. The synchronization is considered achieved if $|v_{PCC} - v_O|$ is kept lower than a threshold limit $\Delta v_{sync}^{\text{thres}}$ during a time period of length T_0.

- Once v_O is synchronized with v_{PCC}, the islanded ac-subgrid can be connected to the grid by the circuit breaker SW_1 at the desired angle θ_{conn}. When this occurs, $syn = 1$ and, if $isl = 0$, the state M becomes asserted.

- Being $M = 1$, the SW_1 closes. As $I = 0$, the signal v_{PCC}^{FF} is kept equal to the estimated fundamental component of the PCC voltage. Concurrently, the grid current controller is enabled with the integral part initially set to zero. H_{PI} now regulates current i_G through signal ϵv_O^{REF}.

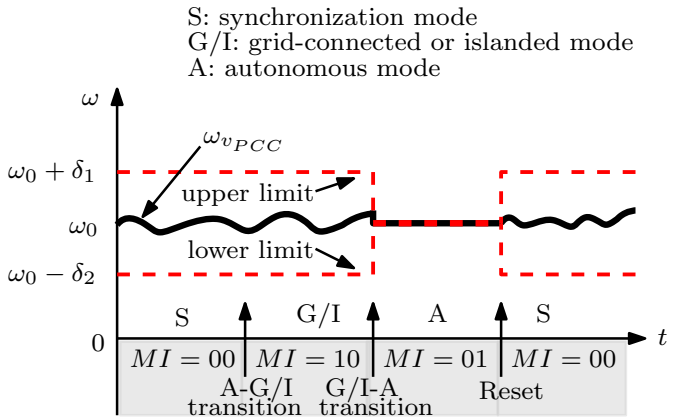


Figure 5-3: The frequency limits for v_{PCC} and v_{PCC}^{FF}.

- With no intentional islanding requests (i.e., $isl_{int} = 0$), the state $MI = 10$ is maintained as long as the PCC voltage amplitude and frequency remain within allowable levels and the SW_2 breaker is kept closed (i.e., $isl = 0$). As an example, the considered frequency limits for v_{PCC} and v_{PCC}^{FF} are shown in Fig. 5-3. Analogous windowing functions are applied to voltage amplitude.

The above procedure smoothly regulates the voltage reference v_O^{REF} to be synchronized with the true PCC voltage v_{PCC}. This limits current and voltage spikes across the transition, which is essential to ensure a seamless operation, as experimentally verified in Sec. 5.3.

5.2.2 From grid-tied/islanded to autonomous mode

Let us assume to operate grid-tied/islanded (i.e., with $MI = 10$); two kinds of transitions towards the autonomous mode can be distinguished, namely, the intentional (or planned) and the unintentional (or unplanned) one. Intentional transitions occur when the isolation from the upstream main grid or micro-grid is determined by the controller, opening the SW_1 breaker. Instead, an unintentional transition is caused by an external event that leads the converter to operate isolated from the PCC without prior notice (e.g., after the opening of SW_2, operated by the DSO, with v_{pcc} exceeding specified frequency and/or amplitude limits).

In the former case, the transition can be managed more easily, because it is driven by the controller itself. Instead, the process that properly manages the unintentional transition

is more complex and comprises two stages: detection of SW_2 opening and intentional transition.

(a) *Intentional transition to the autonomous operation*

Let us consider, at first, an intentional transition. We assume the converter is operating grid-tied/islanded and that the transition to the autonomous operation mode is initiated by asserting the variable I (e.g., by setting the control input isl_{int}).

1. As soon as $I = 1$, FF2 is reset to low (i.e., $M = 0$). As a result, SW_1 is opened and the i_G current regulator is disabled by selecting the input 0 of S3, which ensures zero input error for $H_{i_G}^{PI}$, regardless of any non-ideality of the feedback signal path (e.g., offset errors, noise). The integral part of $H_{i_G}^{PI}$ is reset, to prepare the regulator to future re-connections (as seen in Sec. 5.2.1).
2. The PCC voltage estimator restores the grid frequency (input 1 of S1) and grid voltage amplitude (input 1 of S2) to the nominal levels (please, see Fig. 5-3). The state $MI = 01$ is maintained as long as a grid connection request is issued by acting on the $connection$ command at the K input of FF1, which would bring the system to the state $MI = 00$.

In an implementation perspective, in order to avoid discontinuities in the controllers' state and prevent undesirable transients, the reset to zero of the integral part at step 1) and the return to the nominal frequency and amplitude values at step 2) should be performed gradually. In the nano-grid testbench controller, this is achieved by inserting suitable low pass-filters in the respective loops, so that a smooth transition of the numerical integrators towards the new steady-state condition is obtained.

(b) *Detection of SW_2 opening*

Let us assume that the SW_2 breaker opens during a grid-tied operation (i.e., $MI = 10$). At the occurrence of this condition, if v_{pcc} is not controlled, the converter should, respond by automatically initiating an intentional transition to the autonomous mode. In order to do so, an 'islanding' detection technique must be implemented. It is worth

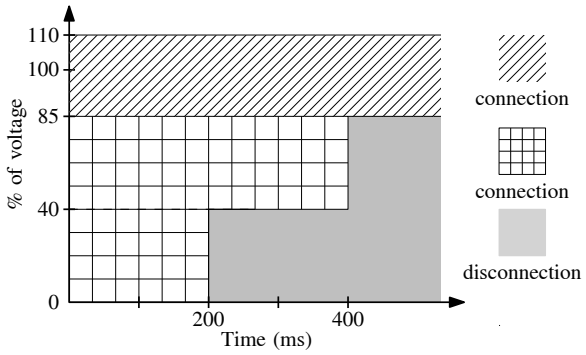


Figure 5-4: Standard CEI 0-21:2012-06 for low voltage ride through.

observing that when SW_2 is opened the i_G control loop is no longer effective, because v_{pcc} is not independent from i_G any more. In these conditions, the PI controller error increases and the output starts diverging.

Accordingly, in the organization shown in Fig. 5-2, the islanded operation condition is detected when, during any period T_0, variable $\mathrm{MAF}_{T_0}(\epsilon v_O^{REF})$ of the 'island' detection block exceeds a predefined threshold $\Delta v_O^{\mathrm{thres}}$, while the measured grid current error ϵi_G diverges. As soon as this occurs, isl_{det} is asserted, $MI = 01$, and the controller starts the procedure described in Sec. 5.2.2. It is worth remarking that the detection technique adopted here is passive, that is, it does not rely on additional injected perturbations to support the islanding detection. Clearly, the specific choice of $\Delta v_O^{\mathrm{thres}}$, $\Delta i_G^{\mathrm{thres}}$, and T_0 determine the effectiveness of the detection technique, with a trade-off between noise rejection and detection responsiveness. Nevertheless, other islanding detection techniques (see, e.g., [203,204]) can also be considered and adapted to be implemented in the corresponding block in Fig. 5-2.

5.2.3 Low-voltage ride through (LVRT) capability

Grid connection standards define how DERs should behave during abnormal grid voltage amplitude reductions (i.e., voltage sags). For example, the Italian grid code CEI 0-21: 2012-06 prescribes the behavior displayed in Fig. 5-4; accordingly, outside the gray area, the energy resource must stay connected, possibly keeping active and reactive power injection. On the other hand, disconnection is permitted within the gray area.

The control scheme proposed herein allows LVRT capabilities, in the sense that the system can go through step variations of the voltage amplitude while keeping normal operation, as experimentally shown in the following section. In this way, requirements similar to those displayed in Fig. 5-4 can be fulfilled.

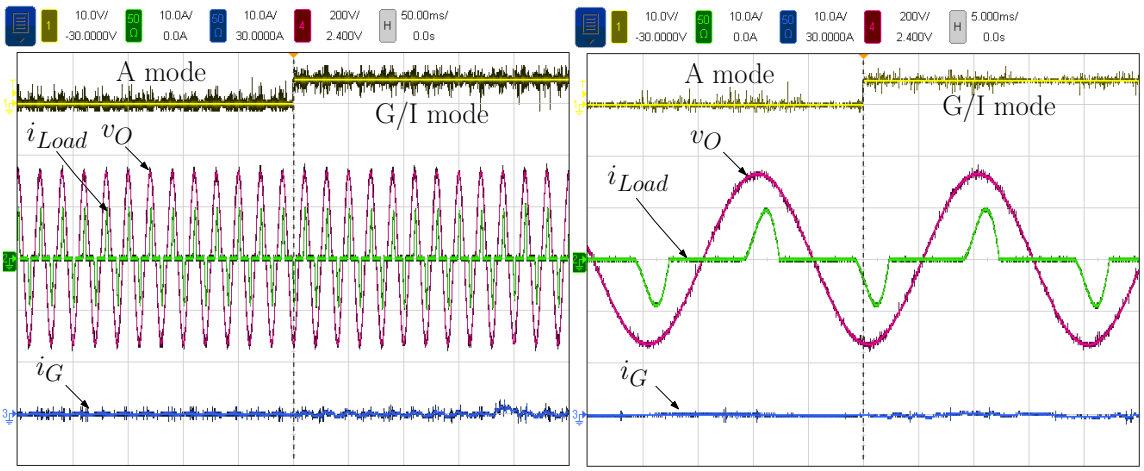
In addition, in case of prolonged voltage sags, the controller in Fig. 5-2 can disconnect and restore—in a controlled fashion—the voltage of the islanded system, which will eventually operate at the nominal voltage amplitude and frequency. In particular, during grid-tied/islanded operation (i.e., $MI = 10$), if the PCC voltage amplitude keeps smaller than a threshold level for more than a time interval T_{LV} (i.e., $v_{PCC,amp}(t^*) < v_{LV}$, $\forall t^* \in [t,\, t + T_{LV}]$), then the flag lvf (low-voltage fault) is asserted, bringing the system to intentionally transition to the autonomous operation (see Sec. 5.2.2).

5.3 Experimental results

The control functions discussed previously are experimentally verified herein. To this purpose, the converter shown in Fig. 2-5 and its triple loop controller are now supervised by the mode transition management system represented in Fig. 5-2. In these experiments, no load is connected to the PCC and v_{pcc} is not controlled in any way.

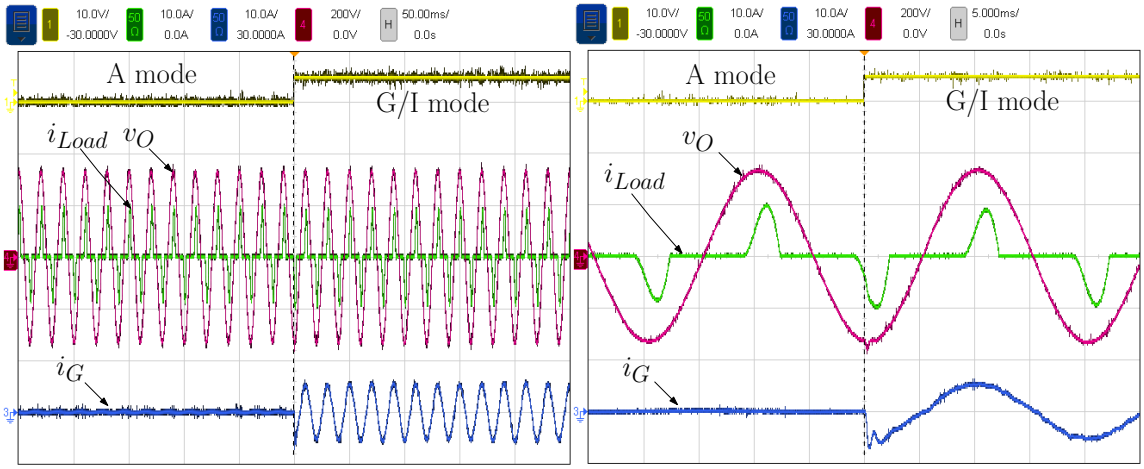
5.3.1 Autonomous to grid-tied/islanded transition

Fig. 5-5(a) shows an autonomous to grid-tied/islanded mode transition with zero injected current (i.e., $i_G^{REF} = 0$), Fig. 5-5(b) shows the related zoomed-in view around the transition instant. A non-linear load absorbing $1\,\mathrm{kW}$ with $CF = 2.6$ is connected to the ac-link, in order to test the sensitivity to possible voltage or current harmonics. Fig. 5-5(c) and the zoomed-in view given in Fig. 5-5(d) refer to the same transition, but with non-zero injected current. In both the considered cases, the transition appears smooth, with no relevant spikes or perturbations in the measured voltages; just a minor settling transient is visible on the grid current, that rapidly reaches the target amplitude. The set values of $\Delta v_{sync}^{\mathrm{thres}}$, T_0, and θ_{conn} are $0.02\,V_N$, $20\,\mathrm{ms}$, and $-\pi/2$ respectively.



(a) Zero injected current ($i_G^{REF} = 0$ A)

(b) Zoomed-in view of (a)



(c) Non-zero injected current ($i_G^{REF} = 5$ A)

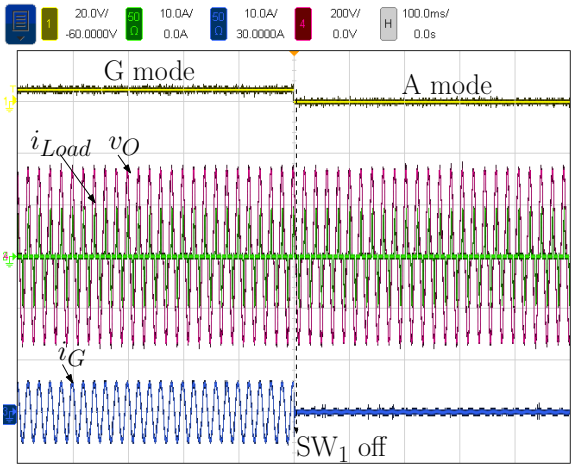
(d) Zoomed-in view of (c)

Figure 5-5: Transitions from autonomous (A) to grid-tied/islanded (G/I) mode.

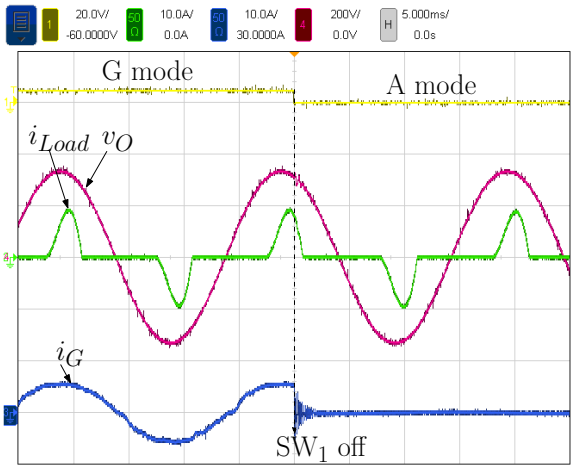
5.3.2 Grid-tied/islanded to autonomous transition

Three different tests were performed, the results are shown in Fig. 5-6. Fig. 5-6(a) shows an intentional transition from grid-tied mode with non-zero injected current (i.e., $i_G^{REF} = 5$), Fig. 5-6(b) shows the related zoomed-in view around the transition instant. Fig. 5-6(c) shows an un-intentional transition with zero injected current (i.e., $i_G^{REF} = 0$), Fig. 5-6(d) is the zoomed-in view around the transition instant. Fig. 5-6(e) and Fig. 5-6(f) show the same un-intentional transition but with non-zero injected current.

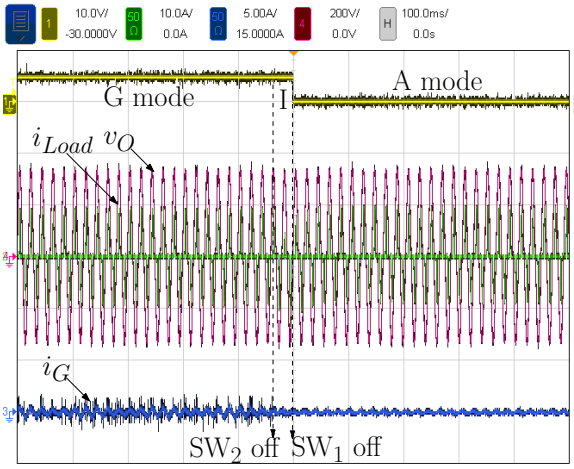
As can be seen, no significant spikes occur during the intentional transition. In particular, the local ac voltage v_O is well controlled and keeps its target waveform almost



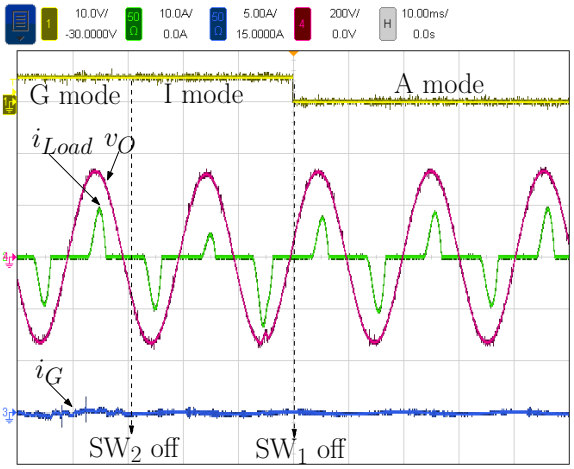
(a) Intentional islanding with $i_G^{REF} = 5$ A



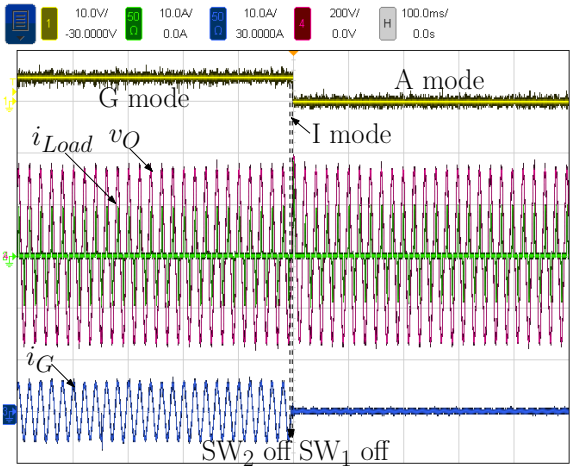
(b) Zoomed-in view of (a)



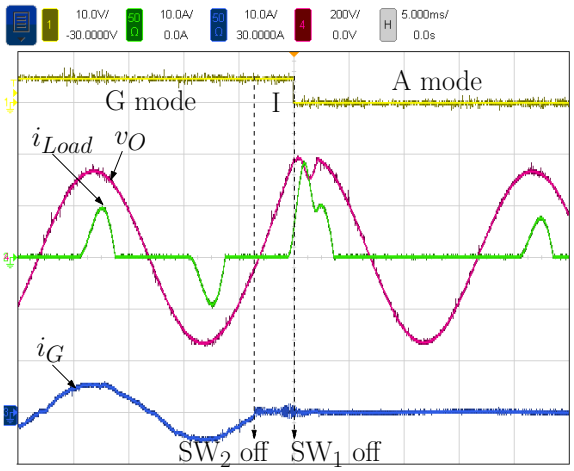
(c) Unintentional islanding with $i_G^{REF} = 0$ A



(d) Zoomed-in view of (c)



(e) unintentional islanding with $i_G^{REF} = 5$ A



(f) Zoomed-in view of (e)

Figure 5-6: Transitions from grid-tied/islanded (G/I) to autonomous (A) mode.

unaffected.

In the unintentional tests, where the SW_2 breaker in Fig. 2-3 is opened without prior notice, the $i_G^{REF} = 0$ case is critical, because it corresponds to an operating point that is compatible with both modes. Indeed, ideally, $i_G = 0$ holds in both conditions, which makes the detection of SW_2 opening more difficult. The $i_G^{REF} \neq 0$ case, on the other hand, involves a hard discontinuity in the system state, which makes the regulation of the voltage v_O to be perfectly sinusoidal across the transition a challenging task.

Despite that, the G/I-A transition is performed promptly [1.5 grid cycles in Fig. 5-6(d) and 0.25 cycles in Fig. 5-6(f)] and again with very limited perturbations on voltage v_O. The set values of $\Delta v_O^{\text{thres}}$ and $\Delta i_G^{\text{thres}}$ are $0.05\,V_N$ and $0.5\,\text{A}$, respectively.

5.3.3 Resilience to grid-voltage amplitude perturbations

Fig. 5-7(a)-(b) show the response to grid perturbations in the form of step amplitude variations with, respectively, zero and non-zero grid current injection. In order to fully test the LVRT capability, the grid voltage amplitude is made to subsequently assume 100%, 50%, and 5% of the nominal value. Each stage lasts more than $3\,\text{s}$ and $T_{LV} = \infty$. On the other hand, Fig. 5-7(c) shows the disconnection of the converter and the transition to autonomous mode of operation during a 50% voltage sag with a duration that exceeds the maximum allowed T_{LV}, now set as described in Fig. 5-4. Fig. 5-7(d) refers to the same scenario, but considering a full voltage sag (i.e., 100%). During all the tests, the system succeeds in safely going through a low-voltage and a zero-voltage fault, while keeping a controlled grid current i_G, as prescribed by the applicable grid connection codes, and preventing protection tripping. Moreover, the specific capability of the proposed scheme to smartly and seamlessly switch to autonomous operation allows to disconnect and promptly restore the local grid voltage v_O, if the low-voltage fault duration exceeds specified limits.

5.4 Summary

In this chapter, the developed flexible mode transition manager for grid-tied inverters is described. It is based on the large-bandwidth, triple-loop VSI controller presented in Ch. 4.

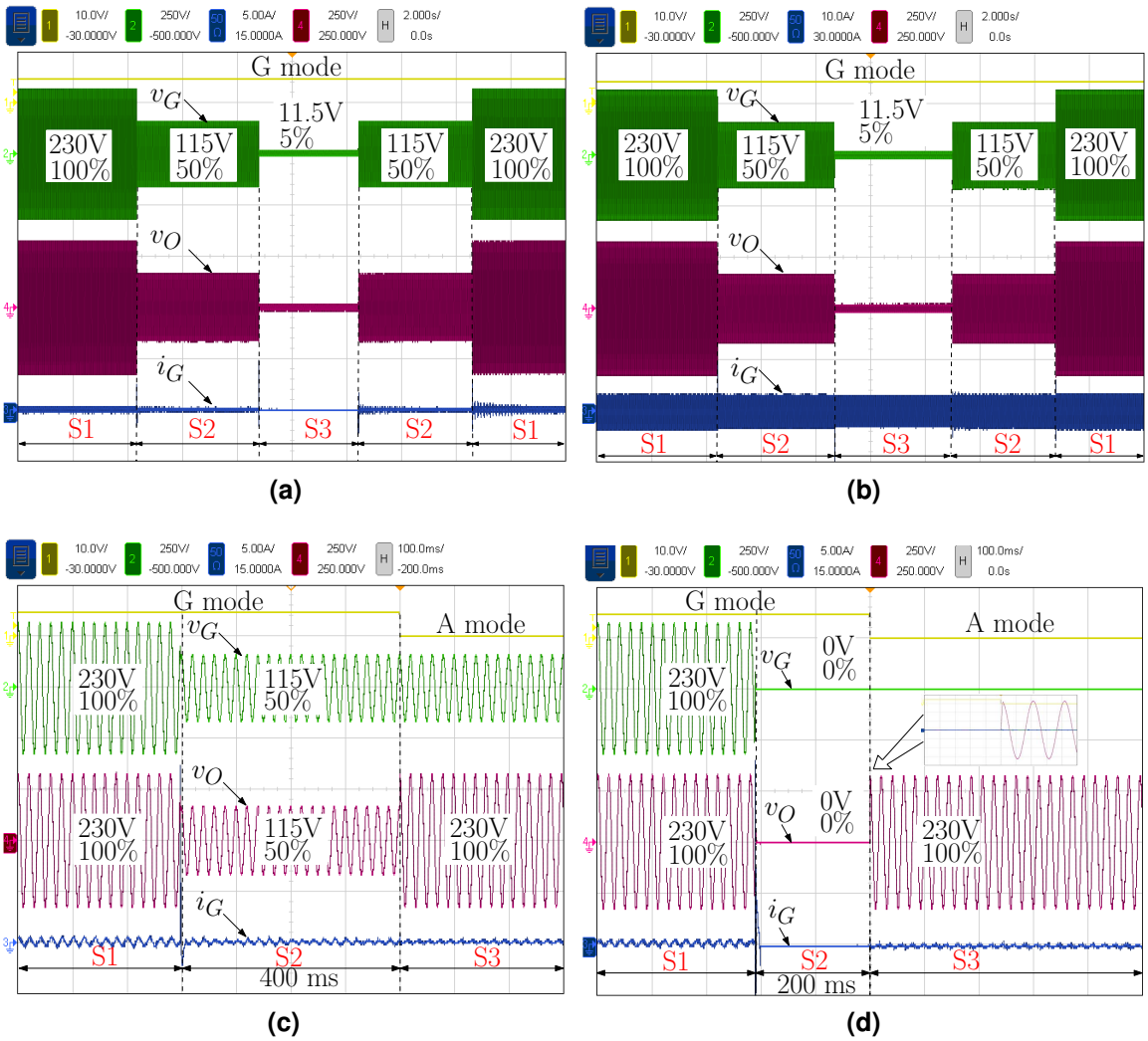


Figure 5-7: Response to voltage sags: (a) Response to voltage sags with $i_G^{REF} = 0\,\text{A}$, operating within the connection area of Fig. 5-4; (b) The same response of (a) but with $i_G^{REF} = 5\,\text{A}$; (c) Response to voltage sags with $i_G^{REF} = 0\,\text{A}$, operating within the disconnection area of Fig. 5-4; (d) The same response of (c) but with a 100% voltage sag.

Several of its interesting functionalities have been analyzed and experimentally verified on the testbench introduced in Ch. 2. Based on the gathered evidence, the proposed solution achieves the following merits: 1) the grid-tied inverters can work in different operation modes, with automatic and smooth transitions; 2) a satisfying, standard compliant, low voltage ride through performance can be guaranteed; 3) the inverter-side non-linear local-load harmonics and the grid-side voltage harmonics can be attenuated significantly, indicating that the local ac-link and the grid are effectively decoupled; 4) excellent UPS-like features can be achieved, guaranteeing high quality power supply to critical local-loads, even when the utility grid is unavailable.

In the next chapter, a critical working condition, the weak grid (frequently encountered in nano-grids) will be considered, aiming at the challenging task of guaranteeing all the aforementioned high-performance even in the presence of large grid-impedance variations.

Chapter 6

Weak grid operation

This chapter discusses how the performance of the grid-tied inverter controller and mode transition management system presented in the previous Ch. 4 and Ch. 5 can be preserved, even when a weak grid connection is available. The proposed solution is based on endowing the high-performance inverter controller with auto-tuning capabilities. Control self-adaptation is particularly useful in the case of weak grids that, due to frequent physical modifications (e.g., network reconfiguration, disconnection of generators/loads) and intrinsic lack of inertia, present strongly time-variant characteristics. It is shown that the applied auto-tuning method can significantly widen the stability region of the grid-tied inverter, covering a broad range of grid impedance values. In addition, within the stable region, the controller maintains the nominal performance.

6.1 Stability analysis of grid current loop

As introduced in Sec.1.2.4, the short-circuit ratio (SCR) is an index referring to the static grid behavior, being defined as the ratio between the short circuit power and the power of the installed generator. In the considered nano-grid scenario, SCR can be conveniently computed by:

$$SCR = \frac{P_{SC}}{S_N} = \frac{V_N^2}{S_N} \cdot \frac{1}{Z_G}\,, \tag{6.1}$$

where, Z_G is the actual grid impedance. As can be seen, the SCR is inversely proportional to the grid impedance Z_G. It means the larger the grid impedance, the lower the SCR, as a result, the weaker the grid. For low-voltage nano-girds, the distributing cables can be modeled as an inductor in series with a resistor, and showing resistive-dominated behavior.

Referring to the triple-loop control structure shown in Fig. 4-2, the stability of the grid-current loop can be analyzed considering its open-loop gain, that is (4.14).

In the absence of any *a-priori* knowledge, $H_{i_G}^{PI}$ can only be designed based on reasonable assumptions on $\tilde{Z}_G$, like its resistive-inductive structure. A possibility is to consider it to be negligible (i.e., like in a strong, ideal grid), to design a stable control loop with desired bandwidth (e.g., $1.0\,\mathrm{kHz}$) and phase margin (e.g., $45°$) and then to verify the stability margins by considering the impedance ratio $Z_G/Z_{o,i_G}^{PCC}$, where Z_{o,i_G}^{PCC} is the converter output impedance, measured at the PCC. The latter is given by:

$$\begin{aligned} Z_{o,i_G}^{PCC}(z) =& -\frac{v_{PCC}(z)}{i_G(z)} = \\ &= \frac{H_{i_G}^{PI}(z)W_{v_O}(z) + Z_{o,v_O}(z) + Z_{L_F}(z)}{1 - H_c(z)W_{v_O}(z)}\,, \end{aligned} \tag{6.2}$$

where H_c is the feedforward gain of v_{PCC}.

In general, any difference between $\tilde{Z}_G$ and Z_G affects the controller's bandwidth and phase margin, making them differ from the design values. To quantify the impact of the uncertainty, we may define the controller performance *acceptable* only when its closed loop bandwidth is larger than $1\,\mathrm{kHz}$ (i.e., 20 times the grid current frequency) and the phase margin is higher than $45°$. It is then possible to derive the map of Fig. 6-1 that shows, in blue, the combinations of resistive (i.e., R_G) and inductive (i.e., L_G) components of Z_G that satisfy the acceptable performance criterion and, in red, combinations causing lower performance.

Noticeably, the performance of the grid current loop is not only related to the SCR (i.e., the magnitude of the grid impedance) but also to the X/R ratio [205]. For example, the $3\,\mathrm{kVA}$ single-phase grid-tied inverter of our testbench, achieves acceptable grid current control performance when SCR > 20 and $X/R < 1/8$. In addition, the performance of the grid current loop degrades more with inductive grids (i.e., $X/R > 1$) than with

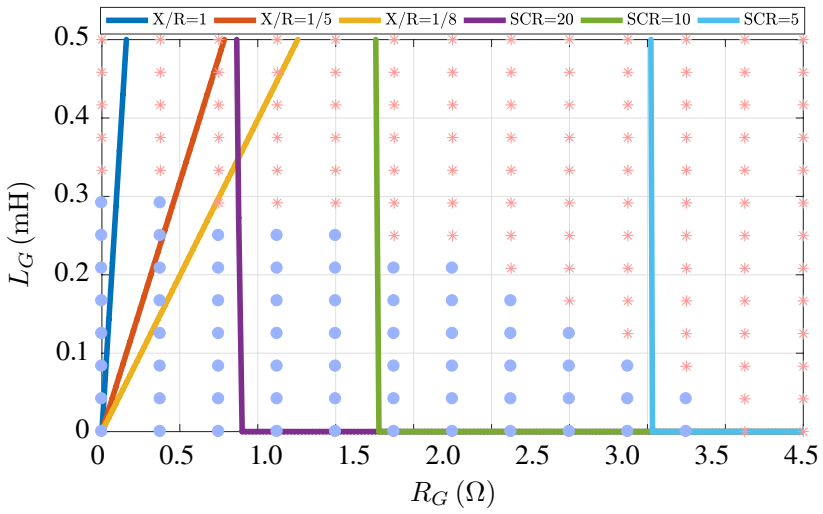


Figure 6-1: Region of acceptable performance (blue dots) of the grid current loop; red crosses indicate points of low performance. Acceptable performance points have bandwidth $\geq 1\,\mathrm{kHz}$ and phase margin $\geq 45°$.

resistive ones. In general, without any provision, grid current control performance degrades remarkably in weak grids. To cope with that, an auto-tuning technique that extends the stability region of the controller is presented in the following section.

6.2 Auto-tuning method

The proposed method can be explained referring to Fig. 6-2. It exploits the estimation method discussed in [206] to automatically adjust the coefficients of the PI regulator H_{iG}^{PI} in the control system in Fig. 4-2. This allows to maintain the desired bandwidth and phase margin for the grid current control loop, guaranteeing optimized performance over a wider range of operating conditions. Please note that, in the following, a continuous-time modeling approach is adopted, although the implementation of the auto-tuner will be, in the end, fully digital. That is only possible because the sampling and algorithm iteration frequencies (i.e., $20\,\mathrm{kHz}$ in the case considered in Sect. 6.3) are orders of magnitude higher than the tuner bandwidth (i.e., $100\,\mathrm{Hz}$ for the fastest loop considered in Sect. 6.3). This allows to neglect the effects of discretization and to design the tuner as if it were a continuous-time system.

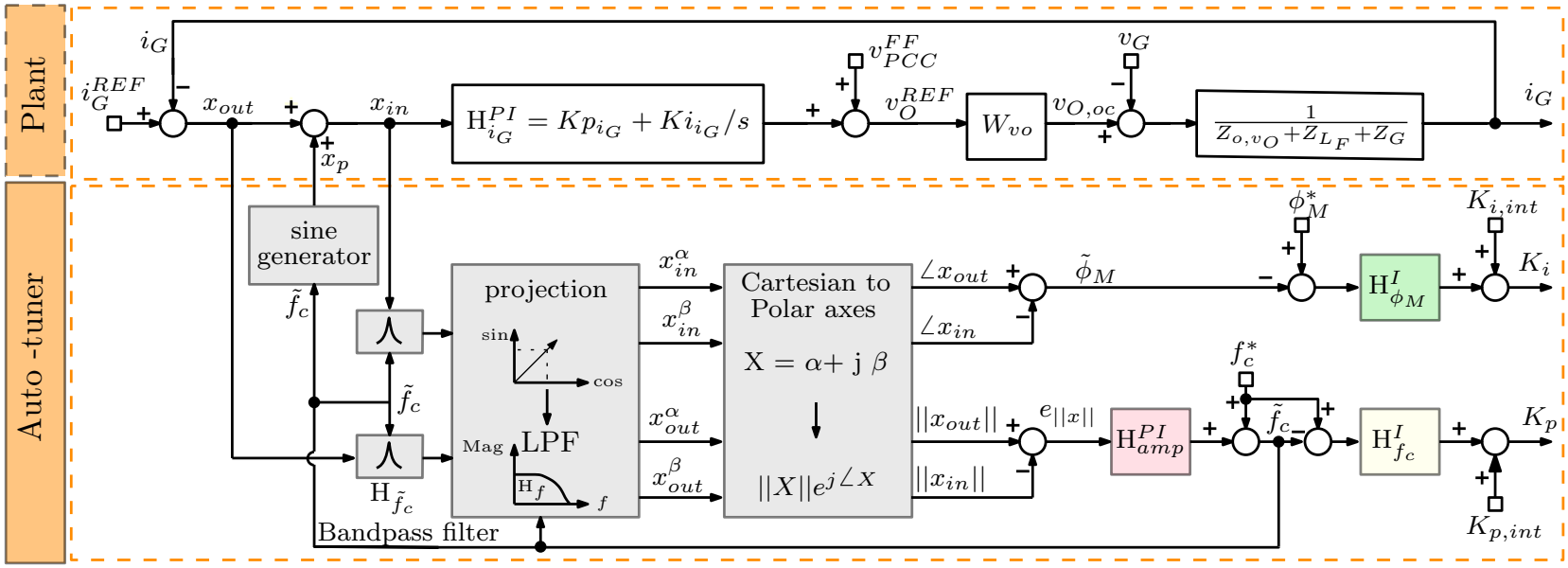


Figure 6-2: Block diagram of the auto-tuning method, based on [206] and used to adjust the PI regulator $H_{i_G}^{PI}$ in the control system in Fig. 4-2.

6.2.1 Estimation of crossover frequency and phase margin

The auto-tuning technique is based on the injection of an adjustable-frequency, small-signal sinusoidal perturbation [i.e., $x_p(t) = |x_p|\sin(\tilde{\omega}_c t)$, $\tilde{\omega}_c{=}2\pi\tilde{f}_c$] that allows to monitor the crossover frequency, f_c, and the phase margin, ϕ_M, of the considered loop. With respect to the injected frequency and based on (4.14), the system block diagram in Fig. 6-2 can be simplified as shown in Fig. 6-3.

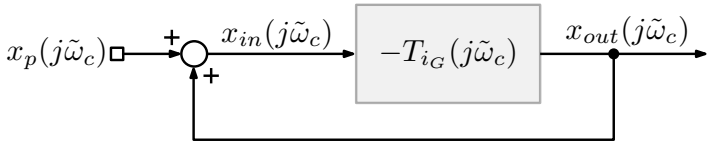


Figure 6-3: Simplified block diagram of Fig. 6-2 considering the injected signal frequency $\tilde{f}_c$.

In the steady-state, the relation between the measured signals x_{in} and x_{out} is:

$$\frac{x_{out}(j\tilde{\omega}_c)}{x_{in}(j\tilde{\omega}_c)} = -T_{i_G}(j\tilde{\omega}_c)\,. \tag{6.3}$$

As shown in Fig. 6-4, only at the true crossover frequency of the loop under test (i.e. when $\tilde{\omega}_c = \omega_c$), the magnitude of the loop gain satisfies:

$$|T_{i_G}(j\tilde{\omega}_c)| = \frac{|x_{out}(j\tilde{\omega}_c)|}{|x_{in}(j\tilde{\omega}_c)|} = 1\,. \tag{6.4}$$

Fig. 6-4 suggests that an accurate estimation of the grid current loop crossover frequency f_c can be obtained by adjusting the perturbation signal frequency $\tilde{f}_c$ so as to make the magnitude difference $|x_{out}| - |x_{in}|$ equal to zero. A PI compensator, H_{amp}^{PI}, can be used to this purpose:

$$\tilde{f}_c = f_c^* + \mathrm{H}_{amp}^{PI}\left(|x_{out}| - |x_{in}|\right)\,, \tag{6.5}$$

where f_c^* is the desired crossover frequency of grid current loop. Similarly, an estimation of ϕ_M is given by:

$$\begin{aligned}\tilde{\phi}_M &= \pi + \angle T_{i_G}(j\tilde{\omega}_c) = \\ &= \angle x_{out}(j\tilde{\omega}_c) - \angle x_{in}(j\tilde{\omega}_c)\,.\end{aligned} \tag{6.6}$$

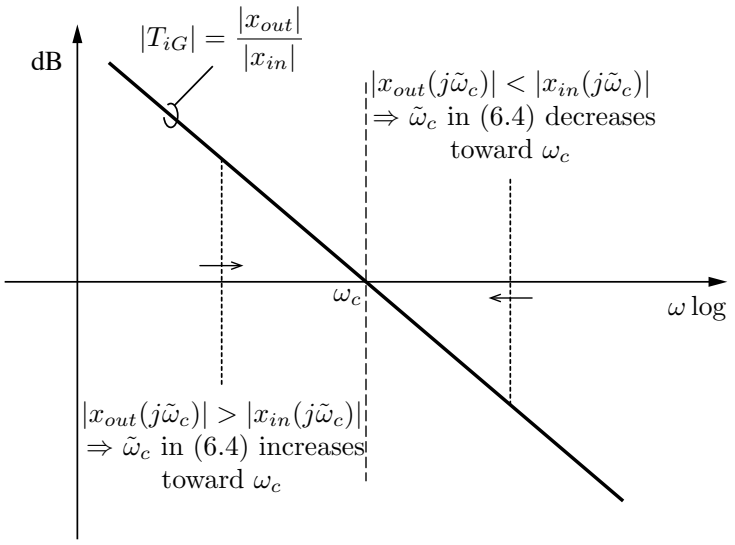


Figure 6-4: Basic principle of crossover frequency identification based on T_{i_G}.

Here, the amplitudes (i.e., $|x_{in}|$ and $|x_{out}|$) as well as the phases (i.e., $\angle x_{in}$ and $\angle x_{out}$) are estimated by performing signal projections onto a rotating frame, synchronized with signal x_p, and a cartesian to polar axes transformation. In order to extract just their components at $\tilde{f}_c$, x_{in} and x_{out} are pre-filtered by a band-pass filter $H_{\tilde{f}_c}$, implemented via a second-order generalized integrator (SOGI) with a peak frequency adaptively tuned to $\tilde{\omega}_c$ and suitably chosen selectivity gain k_f. Its transfer function is [207]:

$$H_{\tilde{f}_c}(s) = \frac{k_f \tilde{\omega}_c^2 s}{s^2 + k_f \tilde{\omega}_c s + \tilde{\omega}_c^2} \,. \tag{6.7}$$

An example of what can be observed considering x_{out} and x_{in} is presented in Fig. 6-9(c), which refers to the case when $|x_{out}| = |x_{in}|$ and, accordingly, $\tilde{f}_c = f_c$ and $\tilde{\phi}_M = \phi_M$.

6.2.2 Analysis of the auto-tuner

First of all, let us consider Fig. 6-5, which shows the open loop gain (4.14) with different choices of $\mathrm{H}_{i_G}^{PI}$. In the figure, T_{i_G} refers to a PI regulator with coefficients giving the desired f_c = 1 kHz and ϕ_M = 60 °, T'_{i_G} with the proportional coefficient doubled, and T''_{i_G} with the integral coefficient doubled. From these plots, it is possible to notice that f_c is mainly linked to the proportional coefficient of $\mathrm{H}_{i_G}^{PI}$, while ϕ_M to the integral one. A more general approach can be based on the numerical calculation of the crossover frequency sensitivity

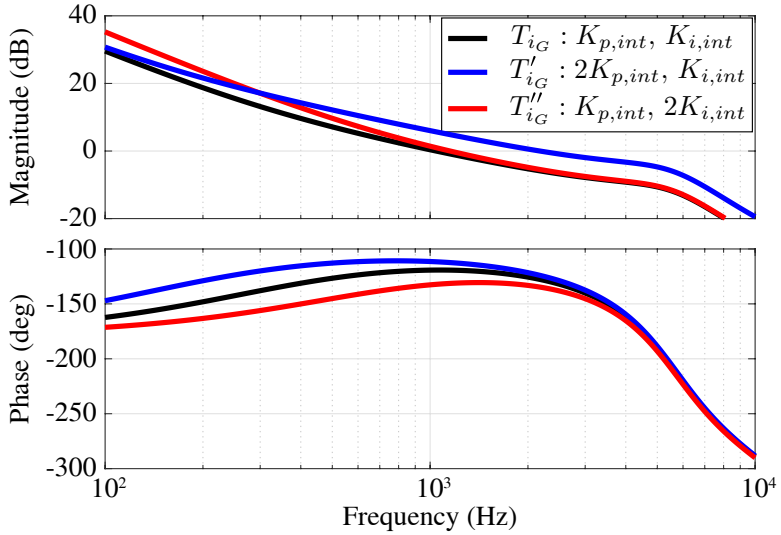


Figure 6-5: Comparison of T_{i_G} with different $\mathrm{H}_{i_G}^{PI}$ coefficients.

to the controller gains. In the case here considered it is easily found that the crossover frequency presents a much higher sensitivity to the proportional gain than to the integral one. Accordingly, the principle of operation of the proposed tuning algorithm is to adjust Kp_{i_G} on the basis of the estimated f_c, and to adjust Ki_{i_G} on the basis of the estimated ϕ_M [208]. Therefore, as can be seen in Fig. 6-2, signals $\tilde{f}_c$ and $\tilde{\phi}_M$ are firstly compared with the respective reference values f_c^* and ϕ_M^*, then the error is closed-loop controlled to zero by the integral controllers $\mathrm{H}_{f_c}^I$ and $\mathrm{H}_{\phi_M}^I$. In particular, Kp_{i_G} is increased to increase $\tilde{f}_c$, while Ki_{i_G} is decreased to increase $\tilde{\phi}_M$.

6.2.3 Design of the auto-tuner

The design procedure for the regulators H_{amp}^{PI}, $\mathrm{H}_{\phi_M}^I$, and $\mathrm{H}_{f_c}^I$ in Fig. 6-2 is presented in the following.

(a) Design of H_{amp}^{PI}

A dynamic model describing how the difference of the estimated amplitudes depends on the frequency of the injected perturbation signal is necessary for the design of H_{amp}^{PI}. To derive that model, namely, the transfer function $e_{\|x\|}(s)/\tilde{f}_c(s)$, recalling

Fig. 6-2 and (6.3), x_{in} and x_{out} can be written in terms of x_p as:

$$\begin{cases} x_{in}(s) = \frac{1}{1+T_{i_G}(s)} x_p(s) \\ x_{out}(s) = -\frac{T_{i_G}(s)}{1+T_{i_G}(s)} x_p(s) \end{cases} . \tag{6.8}$$

These signals are pre-filtered by the filter $\mathrm{H}_{\tilde{f}_c}$ in (6.7), whose response to a signal of the kind $x(t) = A_x \sin(\tilde{\omega}_c t)$ for $t \geq 0$ is the result of the convolution [207]:

$$\begin{aligned} \mathrm{H}_{\tilde{f}_c} * x(t) = & \frac{A_x}{\sqrt{1-\frac{k_f^2}{4}}} \sin\left(\tilde{\omega}_c \sqrt{1-\frac{k_f^2}{4}} t\right) e^{-\frac{k_f \tilde{\omega}_c t}{2}} + \\ & + A_x \sin(\tilde{\omega}_c t) \simeq A_x \left(1 - e^{-\frac{k_f \tilde{\omega}_c t}{2}}\right) \sin(\tilde{\omega}_c t) , \end{aligned} \tag{6.9}$$

where the last approximation holds under the assumption that $\tilde{\omega}_c \gg k_f \tilde{\omega}_c / 2$, that is, the filter dynamics are very slow as compared to the period of the input signal, which is true in the considered application. Fig. 6-6 displays the relation among the amplitude of x and $\mathrm{H}_{\tilde{f}_c} * x$ in case $\tilde{\omega}_c = 2\pi\, 1\,\mathrm{krad/s}$ and $k_f = 1/5$. The transfer function between the amplitude $|x|$ and the estimated amplitude $\|x\|$ is given by the exponential term in (6.9), yielding

$$\frac{\|x\|(s)}{|x|(s)} = H_f(s) \cdot \frac{1}{1 + \frac{2}{k_f \tilde{\omega}_c} s}, \tag{6.10}$$

where H_f is the transfer function of the low-pass filter used to remove the second harmonic oscillations originating from synchronous demodulation in the projection block. It is worth highlighting that the filter $H_{\tilde{f}_c}$ allows to reject background components that may be present in the measured signals and extract just the signal component of interest, at $\omega_{\tilde{f}_c}$. The final relation among amplitude variations of x and the corresponding estimate $\|x\|$ is displayed in Fig. 6-6. As can be seen, the amplitude estimation generated by (6.10) pretty much follows the envelope of the real implementation response. Furthermore, in both cases, the steady-state value is consistent with the amplitude of the input signal. The dynamic model of the amplitude response to frequency variations is therefore validated.

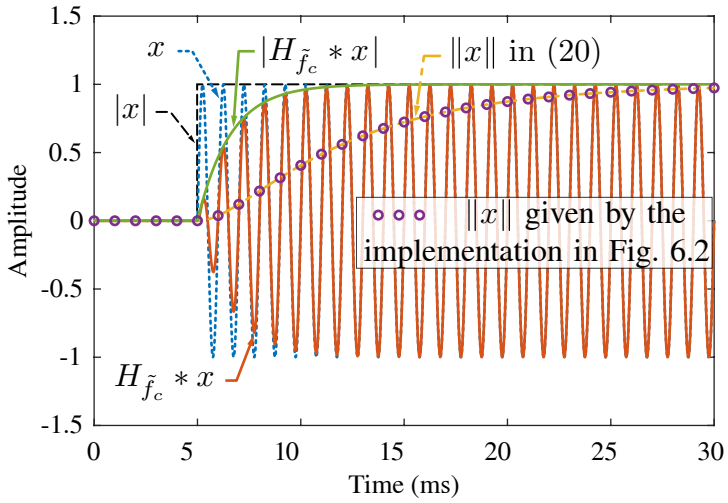


Figure 6-6: Relations between the amplitude of x (i.e., $|x|$) with signal $H_{\tilde{f}_c} * x$ in (6.9) and signal $\|x\|$ in (6.10).

From (6.8) and (6.10), the amplitude error $e_{\|x\|}$ can be written as a function of $|x_p|$, that is:

$$\begin{aligned} e_{\|x\|}(s) &= [\|x_{out}\|(s) - \|x_{in}\|(s)] = \\ &= [|x_{out}|(s) - |x_{in}|(s)] \cdot \frac{H_f(s)}{1 + \frac{2}{k\tilde{\omega}_c}s} = \\ &= \frac{|T_{i_G}(s)| - 1}{|T_{i_G}(s) + 1|} \cdot \frac{H_f(s)}{1 + \frac{2}{k\tilde{\omega}_c}s} \cdot |x_p|(s)\,. \end{aligned} \tag{6.11}$$

In order to find the transfer function $e_{\|x\|}(s)/\tilde{f}_c(s)$ we observe that any small variation of $\tilde{f}_c$ turns into the variation of signals $|x_{in}|$ and $|x_{out}|$. The variations in the amplitudes of $|x_{in}|$ and $|x_{out}|$, will then turn into a variation of the amplitude error $e_{\|x\|}$, whose dynamic is determined by (6.10). If the auto-tuning process is designed to be significantly slower than the system to be tuned (e.g., by one or two orders of magnitude), these two phases of the dynamic process (6.11) can be decoupled and the estimator's one (6.10) can become dominant. This means that the relation between a small-signal variation of $\tilde{f}_c$ and the variations of $|x_{in}|$ and $|x_{out}|$ can be considered instantaneous and its gain can be reasonably approximated by the partial derivative of the steady-state value of (6.11) at frequency $\tilde{f}_c$. The steady-state value of (6.11)

is:

$$e_{\|x\|}\big|_{\mathrm{dc}} = \frac{|T_{i_G}(j2\pi\tilde{f}_c)|-1}{|T_{i_G}(j2\pi\tilde{f}_c)+1|}\cdot|x_p|. \tag{6.12}$$

Its partial derivative, $\partial e_{\|x\|}\big|_{\mathrm{dc}}/\partial\tilde{f}_c$, can be numerically calculated from (4.14) and (6.12). Under the above assumption, we can finally write the following approximated expression of the loop gain to be compensated:

$$\frac{e_{\|x\|}(s)}{\tilde{f}_c(s)} \approx \frac{\partial\, e_{\|x\|}\big|_{dc}}{\partial\tilde{f}_c}\cdot\frac{H_f(s)}{1+\frac{2}{k\tilde{\omega}_c}s}\,, \tag{6.13}$$

The regulator H_{amp}^{PI} can be designed now from (6.13), following any standard procedure. Herein, a bandwidth of $100\,\mathrm{Hz}$ (i.e., approximately a tenth of the system's crossover frequency) and a phase margin of 70° are adopted.

(b) Design of $\mathrm{H}_{f_c}^{I}$

As done for the design of the previous regulator, the design of $\mathrm{H}_{f_c}^{I}$ can be performed on the basis of the dc gain $\partial f_c/\partial K_p|_{\mathrm{dc}}$, which can be numerically evaluated by exploiting (4.14). A purely integral implementation of $\mathrm{H}_{f_c}^{I}$, with a crossover frequency of $0.5\,\mathrm{Hz}$, is adopted for this regulator. Finally, it is worth remarking that mismatches in the estimated transfer function (4.14) can always occur. This aspect has to be taken into account in setting the design specifications of the regulators above (e.g., by setting adequate stability margins and requiring sufficiently slow response times to ensure the validity of the adopted models). So doing, a stable operation of the auto-tuning technique and optimal control performance can be achieved in cases of practical interest.

(c) Design of $\mathrm{H}_{\phi_M}^{I}$

To the purpose of designing the regulator $\mathrm{H}_{\phi_M}^{I}$, a transfer function describing how the estimated phase margin changes with respect to the adjustments of the integral gain Ki_{i_G} is needed. Aiming at a tuning process that should be slow (e.g., with dynamics in the order of 0.1 to 1 s), the dynamics of the previously designed amplitude-difference control loop, having a crossover frequency of about a hundred Hz, can

be neglected. Accordingly, the only relevant parameter in the design of $\mathrm{H}^{I}_{\phi_M}$ is the dc gain $\partial\phi_M/\partial K_i|_{\mathrm{dc}}$, which can be numerically evaluated by exploiting (4.14). A purely integral implementation of $\mathrm{H}^{I}_{\phi_M}$, with a crossover frequency of 2 Hz, is here adopted.

6.2.4 Effectiveness of the auto-tuner

The aim of the auto-tuner is to adapt the controller coefficients in order to keep the control bandwidth and phase margin of the grid current loop constant and, consequently, to get a robust controller performance when impedance characteristics change. The stability and performance of the controller, now equipped with the auto-tuner, are evaluated and reported in Fig. 6-7. As in Fig. 6-1, performance is considered acceptable when the bandwidth is

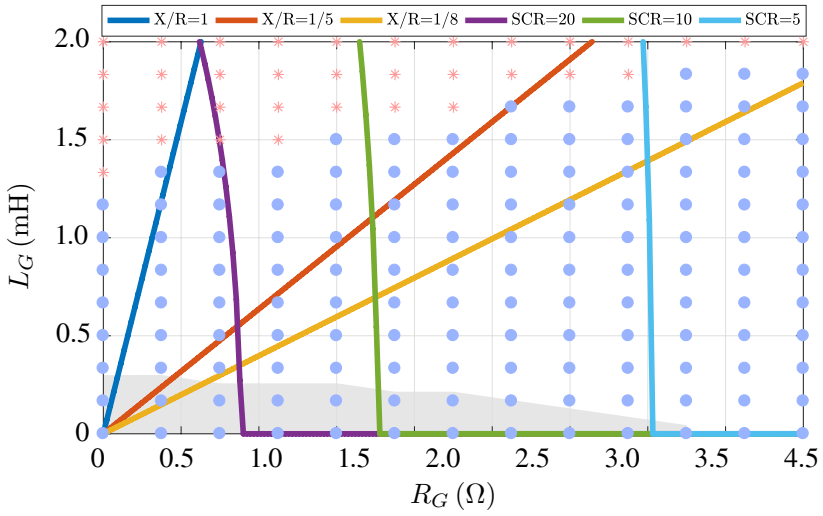


Figure 6-7: Region of acceptable performance (blue dots) of the grid current loop (bandwidth ≥ 1 kHz, phase margin $\geq 45°$); red crosses indicate points of lower performance. For comparison, the shaded area is the acceptable performance region of Fig. 6-1.

$\geq$ 1kHz and the phase margin is $\geq$ 45°. Again, the blue dot area indicates the region of acceptable performance; the red star area indicates lower bandwidth or phase margin. Compared with Fig. 6-1, with the auto-tuner, 1) the stability of the grid-inverter connection as well as an acceptable performance of the triple-loop controller are maintained in a much wider region of grid impedance, 2) the system can provide high performance not only with stiff grids (SCR $>$ 20), but also with weak grids (SCR $<$ 5). All these features are experimentally verified in the following section. Finally, it is also worth remarking that regions of

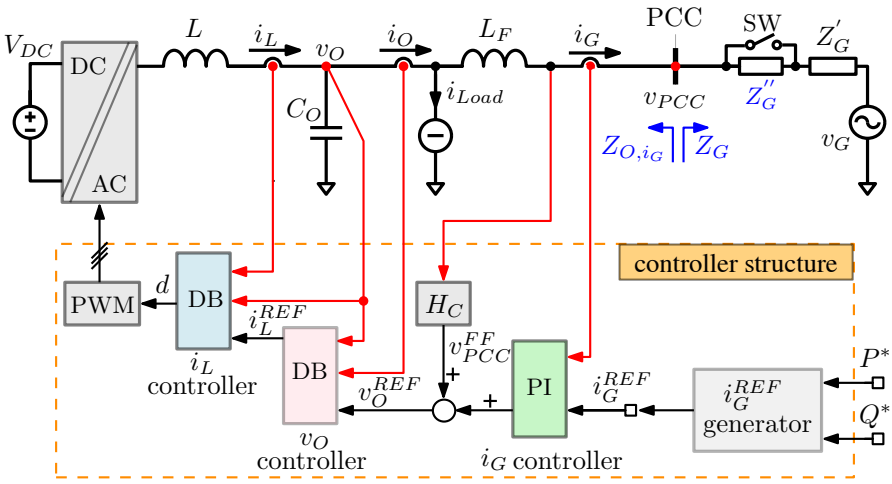


Figure 6-8: Large-bandwidth triple-loop control system. Z_G is the total grid impedance, typically affected by uncertainty and varying over time.

not adequate performance (i.e., red dots in Fig. 6-7) will always exist: they correspond to unfeasible conditions in which, with the given controller and system structure, it is not possible to find any Kp_{i_G} and Ki_{i_G} parameter values that allow to obtain the desired crossover frequency and phase margin.

6.3 Experimental results

The proposed triple-loop controller equipped with the auto-tuning technique in Fig. 6-2 was applied to the grid-tied inverter of the nano-grid testbench, schematically represented in Fig. 6-8 for better clarity.

In the following, the performance of the proposed control system is shown and discussed in terms of *i*) stability, considering parameters uncertainties, *ii*) auto-tuning effectiveness, *iii*) response to grid-impedance variations, *iv*) harmonic rejection capability. In the tests, the magnitude of the injected signal x_p (see Fig. 6-2) is 5% of the rated current. This value is a good trade-off between precision of detection and limitation of harmonic pollution. From experiments, a recommended magnitude range of x_p is found in the range [2%, 10%] of the rated current. In the practical case, to further limit the distortion of the grid current, x_p injection could be performed only intermittently.

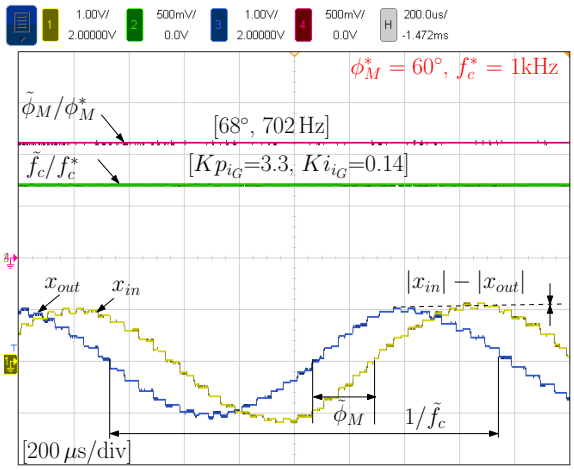
Table 6.1: Testing conditions of Fig. 6-12 under distorted grid voltage v_{PCC} and load current i_{Load}.

	% of rated voltage and current in Tab. 2.1						
Order	**h1**	**h2**	**h3**	**h4**	**h5**	**h6**	**h7**
v_{PCC}	94.8	5.3	1.1	0.7	2.4	0.6	1.1
i_{Load}	18.9	0.7	14.7	0.3	8.3	0.1	2.9
Order	**h8**	**h9**	**h10**	**h11**	**h12**	**h13**	**h14**
v_{PCC}	0.1	0.5	0.1	0.1	0	0.1	0.1
i_{Load}	0.1	2.0	0.1	0.21	0.1	0.11	0.1
Order	**h15**	**h16**	**h17**	**h18**	**h19**	**h20**	
v_{PCC}	0.2	0	0.1	0	0.1	0	
i_{Load}	0.8	0.1	0.9	0.1	0.1	0	

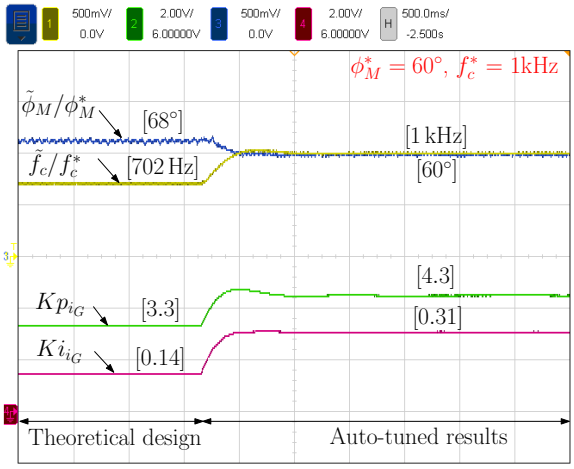
6.3.1 Stability considering parameter uncertainties

The performance of the grid current loop is determined mainly by its bandwidth and phase margin. The PI controller of the grid current loop is designed based on (4.14) targeting $1\,\mathrm{kHz}$ bandwidth and $45°$ phase margin under ideal grid conditions (i.e., $\tilde{Z}_G$ = 0). Its sensitivity to time varying grid characteristics is now tested. A grid impedance variation is actuated by switch SW in Fig. 6-8: when SW is off, the grid impedance Z_G is the series of the impedance $Z_G^{'}$ ($0.45\,\mathrm{mH}$ + $0.15\,\Omega$) and an additional impedance $Z_G^{''}$ that can assume values $\{1\,\mathrm{mH},\ 3.5\,\Omega,\ 1\,\mathrm{mH} + 3.5\,\Omega\}$, when SW is on, Z_G equals $Z_G^{'}$. A significantly distorted grid voltage is considered (THD$_{v_G}$ is 4.86 %) and a non-linear load is connected in parallel with the output capacitor. The harmonic spectra of the grid voltage and the non-linear load current are reported in Tab. 6.1.

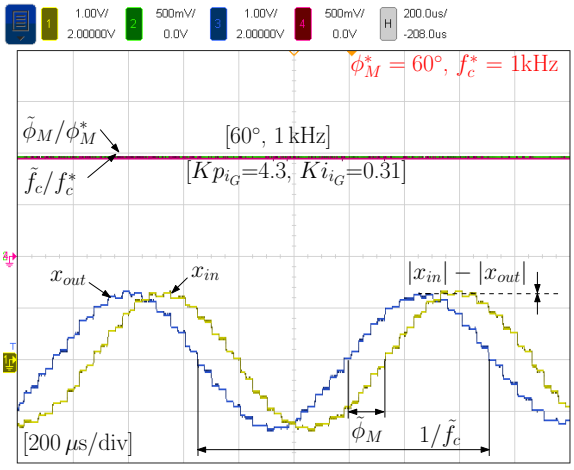
Fig. 6-11(a) shows the controller's performance with the designed PI regulator ($K_{p,int}$ and $K_{i,int}$) under stiff and weak grid conditions in phases S1 and S2, respectively. In the stiff grid case S1 the total grid impedance is set to $0.45\,\mathrm{mH} + 0.15\,\Omega$ (SCR = 85.5). In the weak grid case S2 the total grid impedance is set to $1.45\,\mathrm{mH} + 3.65\,\Omega$ (SCR = 4.8). Due to the effect of the grid impedance, the measured crossover frequency and phase margin are far from the target values (i.e., $f_c^* = 1\,\mathrm{kHz}$ and $\phi_M^* = 45°$): $675\,\mathrm{Hz}$ and $64°$ in S1, $210\,\mathrm{Hz}$



(a)



(b)



(c)

Figure 6-9: Auto-tuning process. (a) Monitored parameters of the i_G control loop before auto-tuning activation; controller's parameters set by design on the basis of T_{i_G} in (4.14) and the measured output impedance Z_G. (b) Dynamics of the auto-tuning when activated. (c) Monitored control loop parameters with auto-tuning active. (a) and (c) refer to the steady-state operation before and after, respectively, the auto-tuning activation shown in (b).

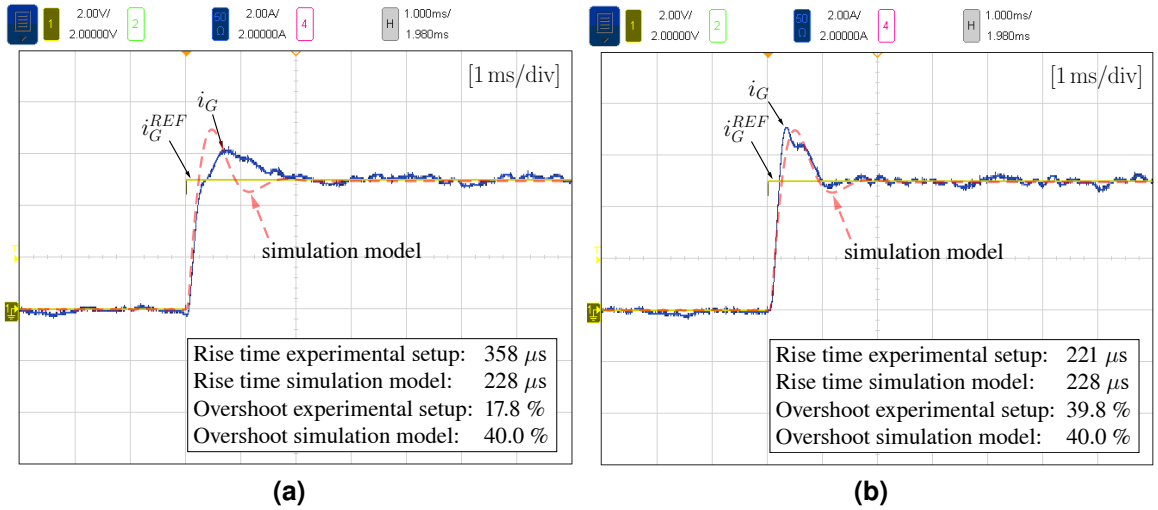


Figure 6-10: Step response of the grid current loop. (a) Before auto-tuning; controller's parameters set by design on the basis of T_{i_G} in (4.14) and the measured output impedance Z_G [conditions as in Fig. 6-9(a)]; (b) after auto-tuning [conditions as in Fig. 6-9(c)].

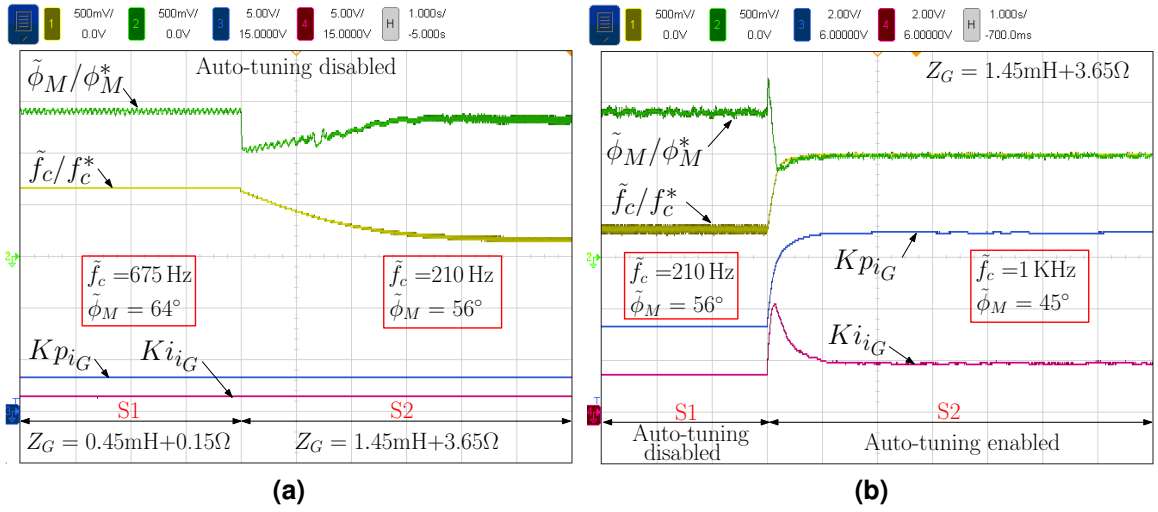


Figure 6-11: Auto-tuning activation. **(a)** Response to grid impedance variations with auto-tuning disabled. **(b)** Auto-tuner from disabled to enabled–initial conditions set as in S2 of (a).

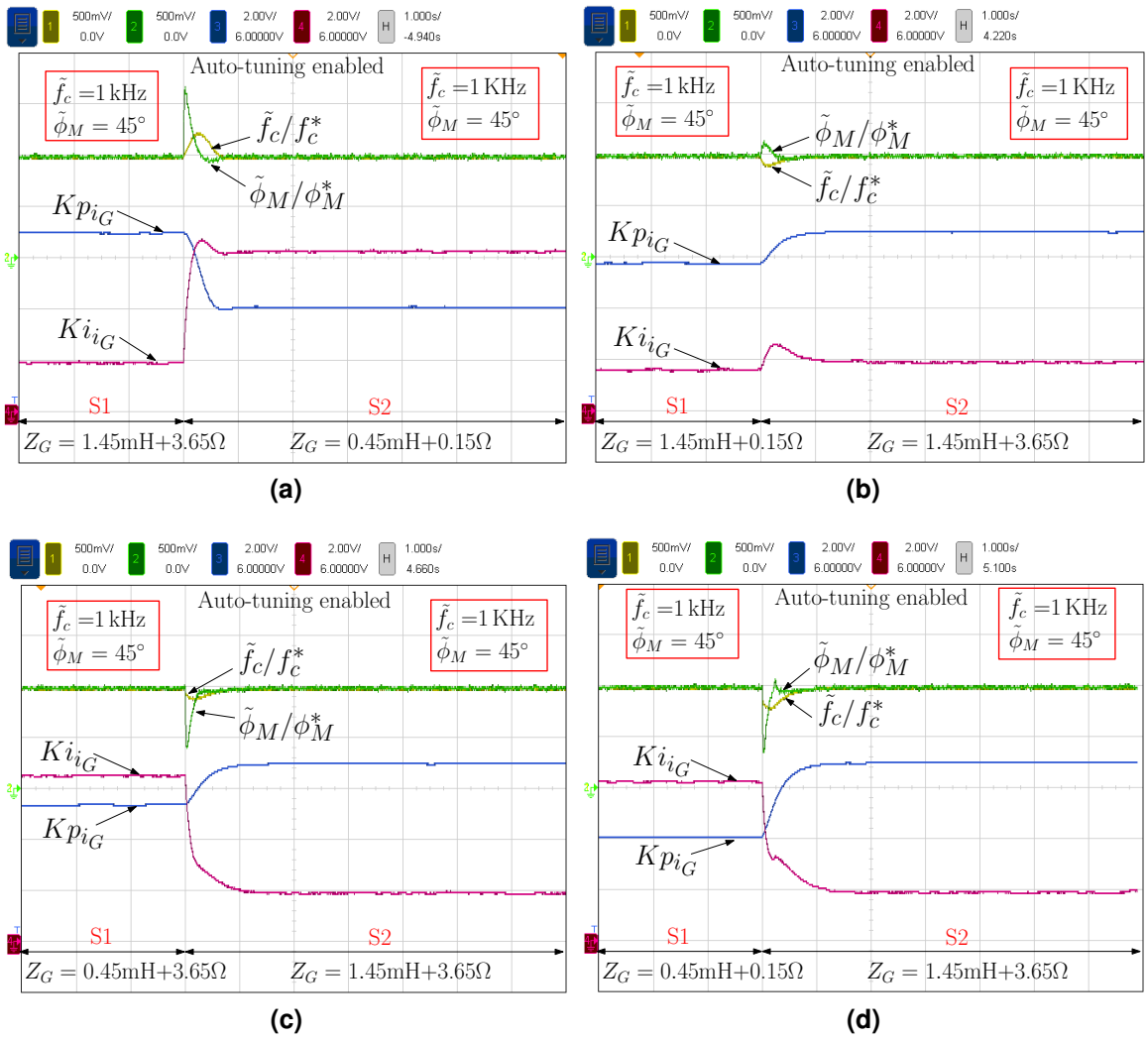


Figure 6-12: Performance of the triple-loop controller equipped with the proposed auto-tuning technique. **(a)** Grid impedance changed from resistive in S1 to inductive in S2. **(b)** Step change of grid resistance from $0.15\,\Omega$ to $3.65\,\Omega$. **(c)** Step change of grid inductance from $0.45\,\text{mH}$ to $1.45\,\text{m}\Omega$. **(d)** As in (a) but reversed.

and 56° in S2 are the measured values when the converter is connected to the considered grid.

6.3.2 Auto-tuning effectiveness

The auto-tuning is now introduced and shown in the basic case in which the converter is connected to a short circuit, with reference crossover frequency of $1\,\mathrm{kHz}$ and phase margin 60°. Initially, the controller of the i_G control loop is set with controller's parameters values computed off-line on the basis of the open loop gain T_{i_G}, the measured converter's parameters in Tab. 2.3, and the output impedance $Z_G = 0$. Fig. 6-9(a) shows the signals x_{in} and x_{out} in steady-state when their amplitude are equal. By definition, it is therefore possible to measure the crossover frequency and the phase margin of the experimental setup for the considered loop, as discussed in Sect. 6.2.1; we found $702\,\mathrm{Hz}$ and 68°, respectively. In these conditions, Fig. 6-10(a) shows the obtained response to a step change of the current reference i_G^*, set as a piecewise constant value for this specific test. The resulting response is consistent with the measurements in Fig. 6-9(a), indeed, a slightly slower and more damped response than expected is obtained, which can be noticed by comparison with the superimposed dashed red line representing the response obtained by the simulation model. The differences in the dynamic responses are due to the unavoidable small mismatches between the modeled and the experimental systems.

Fig. 6-9(b) shows the behavior across the activation of the auto-tuning algorithm, which smoothly corrects the controller parameters values to match the given references of crossover frequency and phase margin. Notably, $Kp_{i_G} : 3.3 \rightarrow 4.3$ while $Ki_{i_G} : 0.14 \rightarrow 0.31$. Fig. 6-9(c) provides a zoomed-in view when the auto-tuning is activated and in steady-state. In this condition, it is possible to measure the final crossover frequency and phase margin after tuning, which actually correspond to the given references. Fig. 6-10(b) shows the step response obtained after tuning: it is possible to notice a close match between the simulation and experimental results, both in terms of obtained waveforms and measured rise-time and overshoot.

6.3.3 Response to grid impedance variations

The behavior of the proposed auto-tuning method while grid-tied is now considered and tested applying different step variations of $Z_G = R_G + j\omega L_G$:

- *Auto-tuning activation Fig. 6-11(b):* with the system initially in the same conditions of S2 in Fig. 6-11(a), the auto-tuning is disabled during S1 and enabled during S2. Remarkably, the auto-tuner smoothly adjusts the parameters K_p and K_i to restore the target values of crossover frequency and phase margin.

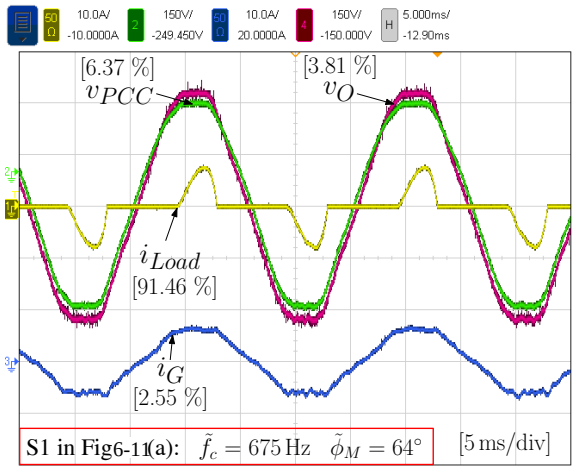
- *From weak to stiff grid in Fig. 6-12(a):* a transition from a weak grid to a stiff grid condition is shown, where the total grid impedance changes from Z_G = $1.45\,\mathrm{mH}$ + $3.65\,\Omega$, SCR = 4.8, in S1, to Z_G = $0.45\,\mathrm{mH}$ + $0.15\,\Omega$, SCR = 85.5, in S2. The coefficients K_p and K_i are smoothly adjusted and $\tilde{f}_c$ and $\tilde{\phi}_M$ are automatically brought to the reference values, within $1\,\mathrm{s}$ from the applied change.

- *Step increase of R_G in Fig. 6-12(b):* a step increase in the grid resistance R_G is shown, where the total grid impedance changes from Z_G = $1.45\,\mathrm{mH}$ + $0.15\,\Omega$ in S1 to Z_G = $1.45\,\mathrm{mH}$ + $3.65\,\Omega$ in S2.

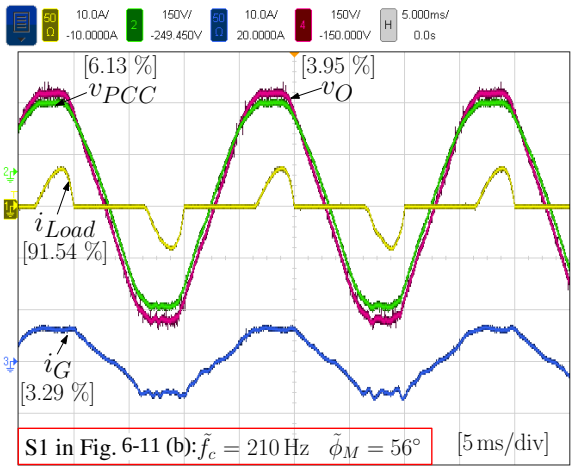
- *Step increase of L_G Fig. 6-12(c):* a step increase in the grid inductance L_G is shown, where the total grid impedance changes from Z_G = $0.45\,\mathrm{mH}$ + $3.65\,\Omega$ in S1 to Z_G = $1.45\,\mathrm{mH}$ + $3.65\,\Omega$ in S2.

- *From stiff to weak grid in Fig. 6-12(d):* a transition from a stiff grid to a weak grid condition is shown, where the total grid impedance changes from Z_G = $0.45\,\mathrm{mH}$ + $0.15\,\Omega$, SCR = 85.5, in S1, to Z_G = $1.45\,\mathrm{mH}$ + $3.65\,\Omega$, SCR = 4.8, in S2. A symmetrical behavior can be observed with respect to Fig. 6-12(a).

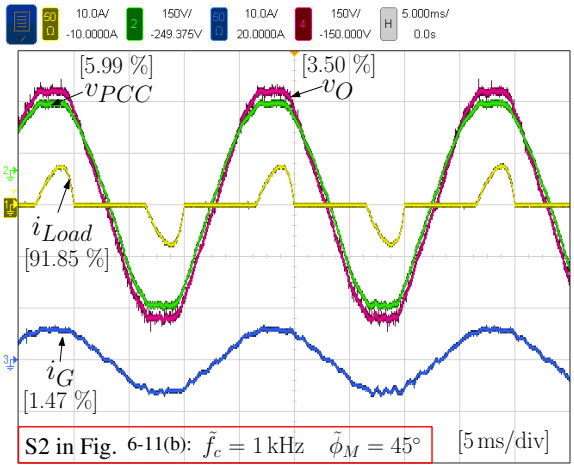
It is possible to remark that the proposed auto-tuner is capable of guaranteeing the desired bandwidth and phase margin in the considered testing conditions despite of significant variations in grid resistance and inductance.



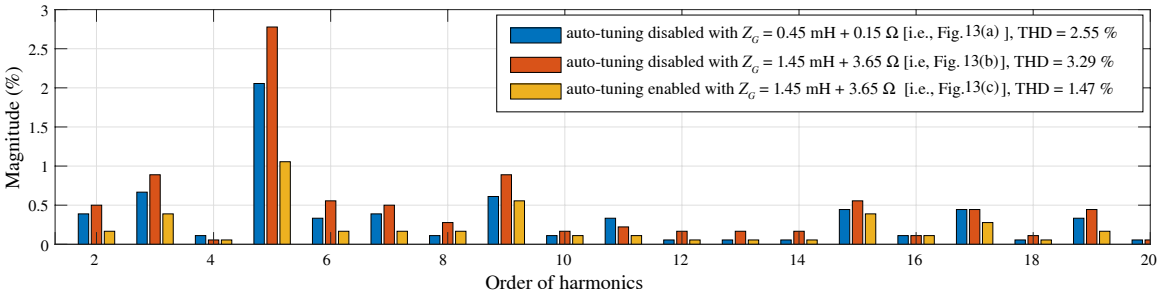
(a) Waveforms during S1 of Fig. 6-11(a)



(b) Waveforms during S1 of Fig. 6-11(b)



(c) Waveforms during S2 of Fig. 6-11(b)



(d) Harmonic content of the grid current i_G in subfigures (a), (b), and (c)

Figure 6-13: Harmonics rejection performance, THD values are reported between brackets.

6.3.4 Harmonic rejection capability

Fig. 6-13(a)-(c) show the waveforms obtained during S1 of Fig. 6-11(a), S1 of Fig. 6-11(b), S2 of Fig. 6-11(b), respectively. The corresponding harmonic spectrum analysis of the grid current is reported in Fig. 6-13(d), grid and load harmonics are reported in Tab. 6.1.

In the cases of Fig. 6-13(a) and Fig. 6-13(b), the auto-tuning is disabled and the measured bandwidth of the grid current loop is $675\,\mathrm{Hz}$ and $210\,\mathrm{Hz}$, respectively. The measured harmonic distortion is $\mathrm{THD}_{i_G} = 2.55\%$ in Fig. 6-13(a) and $\mathrm{THD}_{i_G} = 3.29\%$, in Fig. 6-13(b).

In the case of Fig. 6-13(c) the auto-tuner is active, keeping the grid current control loop crossover frequency always equal to the given reference of $1\,\mathrm{kHz}$. Due to the higher crossover frequency and, consequently, loop gain of the current loop, with respect to the previous case in Fig. 6-13(b), the measured THD of the grid current reduces to 1.47%, as indicated in Fig. 6-13(b). This improvement is achieved without employing any further harmonic suppression provisions.

Finally, it is possible to notice that under the considered various testing conditions the harmonic content fulfills the IEEE Std. 1547 [27].

6.4 Summary

An adaptive, high-performance control scheme is proposed in this chapter that allows a grid-tied inverter to successfully operate even when connected to weak, single-phase grids. An auto-tuning technique is exploited to provide the on-line adjustment of the proportional and integral gains of the outer, grid current controller, that are severely affected by any grid impedance parametric uncertainty. The auto-tuner small-signal model is firstly derived, based on which design criteria are given for each of its inner regulators.

The tuning strategy is then experimentally tested. The experimental results prove that the auto-tuner can improve the grid-tied converter performance in different ways. First of all, robust stability and performance are guaranteed in the presence of time-variant grid impedance characteristics, as often encountered in low-voltage single-phase ac nano-grids. Secondly, a precise and fast control of the injected current is achieved and maintained,

which allows the converter to be safely operated even in the presence of significant grid voltage distortion.

Up to now, all the critical features reviewed in Sec. 3.2 have been implemented for the grid-tied inverter of the nano-grid testbench, essentially leveraging on the large-bandwidth triple-loop controller introduced in Ch. 4. However, only a single-converter case has been considered so far. In the following chapter, the scenario of multiple parallel-connected converters will be considered and discussed.

Chapter 7

Grid-supporting functionalities and parallel operation

So far, the grid-tied current-controlled inverter of the nano-grid testbench considered in this thesis has been supposed to operate exclusively as a stand-alone, dispatchable power source, taking no action to control the PCC voltage. In this chapter, instead, a power flow control scheme is described that makes it capable of automatic grid-supporting and parallel operation functionalities, applicable during islanded conditions.

The approach is inspired by the droop control that is normally used with parallel connected voltage source converters. As a consequence, it automatically realizes power sharing among the different units, without needing any communication or higher-level supervisory controllers. In addition, the implementation of virtual inertia [81, 209] is considered, so as to improve the system performance.

Differently from conventional solutions, however, the power flow controller operates setting the reference of the underlying grid current i_G control loop. As a result, the final implementation of the control structure keeps all the favorable features introduced in previous chapters, with respect to which standard droop control implementations typically suffer of low performance [80].

Notably, the power flow controller is fully compatible with all the previously discussed higher level control functions. The auto-tuner, obviously, can be kept operating in the background even when the power flow controller is active, as it only adjusts the grid current

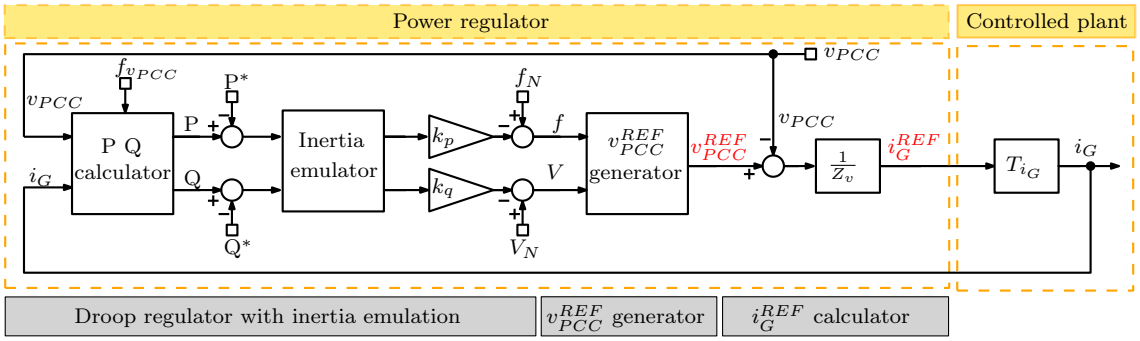


Figure 7-1: The proposed power regulator for current controlled grid-tied inverters. The current reference i_G^{REF} is given as input to the controller in Fig. 4-2.

controller gains so as to keep the target performance levels even if the grid impedance condition change.

As far as the flexible mode transition manager presented in Ch. 5 is concerned, its interaction with the power flow controller requires some policy definition. In general, to successfully join the two, it is necessary to establish the priority of different possible courses of action. A few available options will be discussed in the following section.

7.1 Enabling grid-supporting functionalities and parallel islanded operation

The control scheme presented in Fig. 7-1 to compute the current reference i_G^{REF} for the control structure (see Fig. 4-2) is investigated in this section. The use of block Z_v and of the voltage reference generator block makes the converter behave similarly to a voltage source converter with output impedance Z_v.

The proposed power regulator is composed of three parts: *i*) droop regulator with inertia emulation, *ii*) v_{PCC}^{REF} generator, and *iii*) i_G^{REF} calculator. Each part of the power regulator is described in detail in the following subsections. The output of the power regulator is the reference of the grid current i_G^{REF}, which is sent to the inner triple-loop controller (see Fig. 4-2). It is possible to calculate that the closed-loop transfer function of the triple-loop controller, which yields:

$$W_{i_G}(z) = \frac{H_{i_G}^{PI}(z) W_{v_O}(z)}{Z_{o,i_G}^{PCC}(z) + Z_G(z)}, \tag{7.1}$$

where W_{v_O} is the output voltage closed-loop transfer-function (4.12) and Z_{o,i_G}^{PCC} and Z_G are, respectively, the converter output impedance (6.2) and the grid impedance.

7.1.1 Droop regulator with inertia emulation

In conventional power systems, rotational synchronous machines are commonly employed, which are inherently capable of synchronizing with one another and compensating transient power imbalances thanks to their intrinsic kinetic energy storage [85]. These features guarantee, on the one hand, convenient integration and parallel operation of multiple generators, on the other hand, damped frequency oscillations.

The above characteristics are given by the well-known, main electro-mechanical relationships governing synchronous machines, described by the swing equation [87]:

$$J\,\frac{\mathrm{d}\omega(\mathrm{t})}{dt} = T_m(t) - T_e(t) + D\left[\omega^*(t) - \omega(t)\right], \tag{7.2}$$

where J and ω are the rotational inertia and rotor speed, T_m and T_e are, respectively, the mechanical and electromagnetic torque, ω^* is the reference frequency, D is the damping coefficient, which represents mechanical friction effects, neglected herein for simplicity.

Seen from the perspective of power balance, (7.2) can be rewritten as:

$$J\,\omega(t)\,\frac{\mathrm{d}\omega(\mathrm{t})}{\mathrm{dt}} = P_{in}(t) - P(t)\,, \tag{7.3}$$

where P_{in} is the power delivered by the prime mover (i.e., primary energy resource), which, in a converter with no losses between the energy source and the grid, can be approximated as:

$$P_{in}(t) = \frac{1}{k_p}\left[\omega^*(t) - \omega(t)\right], \tag{7.4}$$

where k_p is the droop coefficient. Combining (7.3) and (7.4) yields:

$$\omega(t) = \omega^*(t) - k_p\,P(t) - k_p\,J\,\omega(t)\frac{\mathrm{d}\omega(\mathrm{t})}{\mathrm{dt}}\,. \tag{7.5}$$

Remarkably, as compared with the conventional droop control, which linearly links active

power with frequency, (7.5) differs only in the non-linear part $k_p\,J\,\omega(t)\,\mathrm{d}\omega(\mathrm{t})/\mathrm{dt}$. By linearizing (7.5) around the operating point $\omega(t) = \omega_N + \hat{\omega}(t)$ ($\omega_N = 2\pi f_N$ is the nominal angular frequency of the grid, $\hat{\omega}$ is the small-signal perturbation), and bringing the model in the Laplace domain, we find:

$$\omega = \frac{1}{1 + k_p\,J\,\omega_N\,s}(\omega_N - k_p\,P)\,. \tag{7.6}$$

As can be seen, the relationship between active power and frequency of synchronous machines is described as a conventional droop controller multiplied by a first-order low-pass filter:

$$H_{LPF} = \frac{1}{1 + k_p\,J\,\omega_N\,s}\,, \tag{7.7}$$

where the cutoff frequency ω_c is $1/(k_p\,J\,\omega_N)$. Therefore, by inserting an inner loop with the first-order low-pass filter H_{LPF} (inertia emulator in Fig. 7-1) inside the conventional droop control loop, grid-tied inverters can simulate the behavior of synchronous machines, at least in a small signal sense, i.e. considering the stability around the nominal operating conditions.

The amplitude of the voltage reference V at the PCC is given by the conventional droop control, which, inspired by the behavior of synchronous machines with automatic voltage regulation, links the amplitude of the PCC voltage linearly to the delivered reactive power:

$$V = V_N - k_q\,Q, \tag{7.8}$$

where V_N is the nominal value of the grid voltage amplitude, k_q is the droop gain and Q is the delivered reactive power.

7.1.2 v_{PCC}^{REF} generator

This block generates the reference PCC voltage on the basis of the frequency and amplitude values provided by the previous power regulators (7.6) and (7.8):

$$v_{PCC}^{REF}(t) = V\sin(\omega t)\,. \tag{7.9}$$

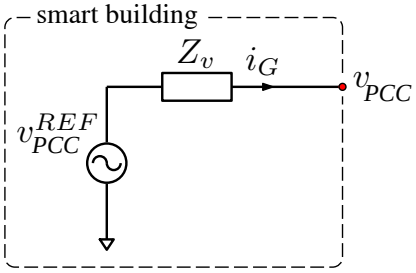


Figure 7-2: Equivalent circuit of the grid-tied inverter.

The grid-tied inverter is then controlled as a voltage source with output impedance and voltage reference v_{PCC}^{REF}, as displayed in Fig. 7-2. So doing, the grid-tied inverter inherits the important capability of working islanded [83].

7.1.3 i_G^{REF} calculator

The droop law is typically used in grids that are mainly inductive, but it can be applied also to generic grids, by using virtual impedance [25]. The adopted current control structure, differently from the voltage controlled ones usually considered, allows to conveniently implement relatively high output inductive impedance at the fundamental frequency and therefore to minimize the sensitivity to the varying and unknown grid parameters [80].

The stator inductance of real synchronous machines typically amounts to about $1.5\,\mathrm{p.u.}$, while the value of the grid-side *L-C-L* filter inductance of grid-tied converters to about $0.05\,\mathrm{p.u.}$ [210]. To ensure the effectiveness of the droop control laws, a purely inductive virtual impedance $Z_v = j\omega L_v$ is then implemented:

$$i_G^{REF}(s) = \frac{v_{PCC}^{REF}(s) - v_{PCC}(s)}{Z_v}\,. \tag{7.10}$$

A relatively large inductance value is considered herein in order to *i*) enhance robustness to grid impedance variations, and *ii*) improve system stability.

7.1.4 Interaction with the mode transition manager

During grid-tied operation, the power flow controller will be practically ineffective whenever the amplitude and frequency of the PCC happen to be equal or close to nominal. It will

instead command a non negligible active and/or reactive power injection in the presence of measurable deviations from the nominal grid voltage parameters. In general, however, the grid current reference calculation must take into account also other commands, such as, for instance, those determined by the battery management system to prevent battery over-charging or excessive discharge.

Therefore, some arbitration function will be needed to integrate the grid supporting functionality and the nano-grid lower level controllers. A solution, not analyzed here, could be to allow the grid supporting mode to be applied only as long as it is compatible with the power balance within the nano-grid. For example, active power injection could be allowed only as long as the battery state of charge was not affected significantly, at which point it would be terminated.

Similar considerations hold for islanded conditions as well. Indeed, in the presence of islanding or any time the PCC voltage is not within specified limits, by default, the mode transition manager described in Ch. 5 operates a transition sequence towards the autonomous mode (A)[1]. Practically, it disconnects altogether from the PCC and just takes care of the local ac loads, i.e. those connected to the internal ac bus of the nano-grid.

However, cooperation with other nano-grids in supporting possible PCC connected loads, while regulating the PCC voltage can be a valuable add-on for the electrical system. It is not difficult to imagine a scenario where, during a grid black-out, a few buildings endowed with the smart nano-grid system devised in this thesis cooperate to supply with power a nearby building that is not.

Once again, some high level configuration, not discussed here, will be needed to define a priority policy between the autonomous and the grid-supporting modes of operation. The policy programming will define, for instance, the minimum battery state of charge upon which cooperation can be started and under which it has to be terminated. It could also be that the administrator does not want his/her nano-grid to cooperate with other units, e.g. any time the power transferred to the PCC is not adequately paid back by the DSO, in which case the autonomous mode would be the default response. Once a satisfactory policy

[1]Except when the deviation is within the specified pattern for a low-voltage-ride-through response, as per Sec. 5.2.3.

Table 7.1: System parameters

Parameter	Symbol	Value	
Droop gain	k_q	23	$\mathrm{V/kVAr}$
P reference	P^*	0	W
Q reference	Q^*	0	VAr
Virtual inertia	J	$6 \cdot 10^{-4}$	$\mathrm{kg\,m^2}$
Virtual stator inductance	L_v	20	mH

is defined, whatever its characteristics, the grid supporting can be seen just as an additional operation mode, to be activated as an alternative to the autonomous one during islanding.

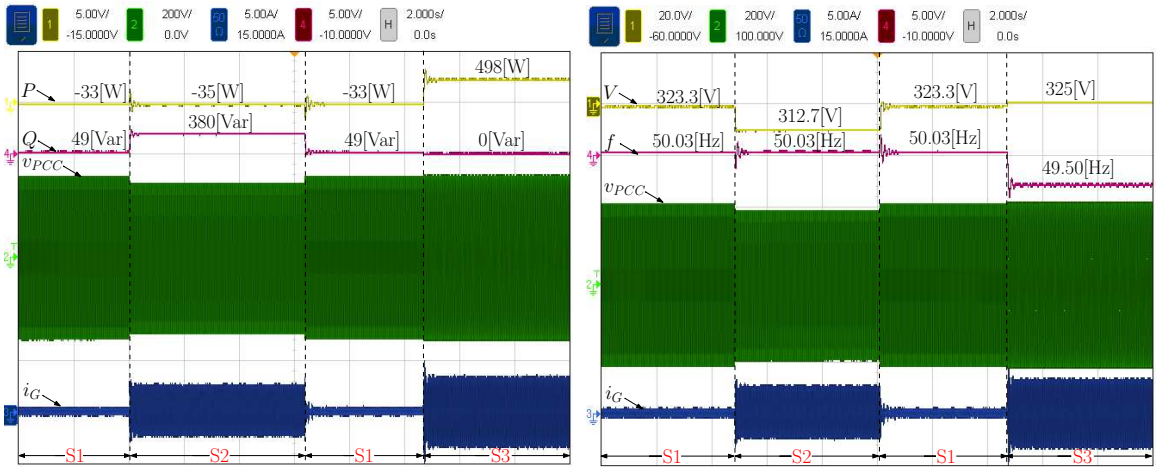
As will be shown in the following, the grid-supporting and parallel operation functionalities are structurally possible for the considered nano-grid organization. The management policy, however, requires a considerable amount of work to be defined in detail and proved functional in all practical cases. For simplicity, in what follows, a policy configuration that simply makes the grid supporting mode the default one is assumed.

7.2 Simulation and experimental results

The proposed control strategy was evaluated by means of computer simulations and experimental tests, considering the single house/building scenario displayed in Fig. 2-3. The grid-tied inverter is controlled by the large-bandwidth triple-loop controller in Fig. 4-2, driven by the the proposed power regulator displayed in Fig. 7-1. The main control system parameters are listed in Tab. 7.1. In the following, the performance of the proposed system is shown *i*) during grid-tied operation, *ii*) across a transition from grid-tied to islanded operation, *iii*) across a transition from islanded to autonomous operation, *iv*) during parallel and islanded operation with multiple converters.

7.2.1 Grid-tied operation

The proposed power regulator is firstly evaluated in the grid-tied mode (i.e., SW_1, SW_2 in Fig. 2-3 closed), the results are shown in Fig. 7-3. During S1 the grid voltage is set at



(a) P and Q **(b)** V and f

Figure 7-3: Grid-tied operation of the inverter with the power regulator in Fig. 7-1. [S1]: nominal grid voltage amplitude and frequency; [S2]: 3% step decrease of the grid voltage amplitude; [S3]: 1% step decrease of the grid voltage frequency. (a) and (b) report different information of the same test.

nominal amplitude and frequency, bringing to a minimal amount of power exchange at the PCC. Then, in S2, a 3% step variation of the grid amplitude is performed. As a result, the injected reactive power increases to 380 VAr. Similarly, a 1% step variation of the grid frequency is applied in S3. According to the reference parameter, the injected active power is regulated automatically to 498 W. As can be seen, the power regulation is automatic, precise, and rapid.

The response to grid variation with different inertia values is shown in Fig. 7-4. In this test, a proper inertia and an over-sized inertia are emulated in (a) and (b), respectively. S1 is the nominal frequency case, S2 indicates a 1% step variation of the grid frequency. As can be seen, the power regulation performance cannot be improved by simply increasing inertia value without limitation; in contrast, a significantly over-sized emulated inertia may impact on system stability.

7.2.2 Transition from grid-tied to islanded operation

The dynamic performance during the grid-tied to islanded (i.e., SW_1 closed, SW_2 open) mode transition with different inertia values is shown in Fig. 7-5. In this test, a 80 Ω resis-

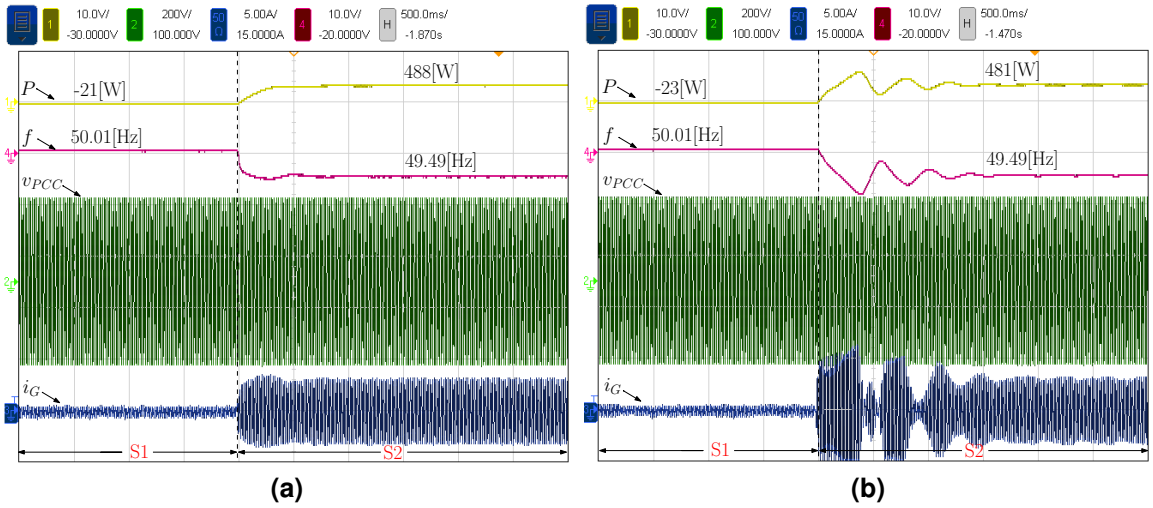
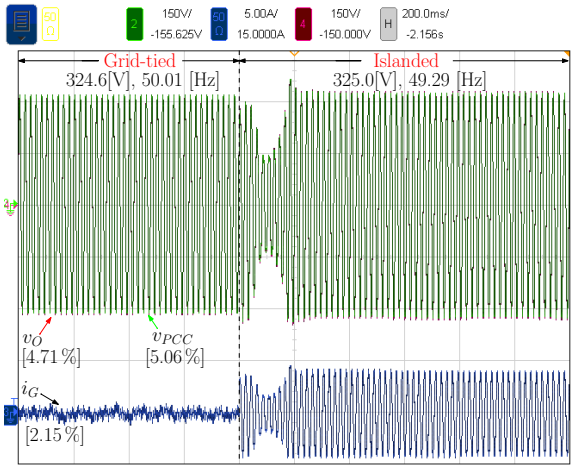


Figure 7-4: Grid-tied operation of the inverter with different inertia values in the power regulator of Fig. 7-1 . [S1]: nominal grid frequency; [S2]: 1 % step change of the grid frequency. (a) Proper inertia; (b) over-sized inertia.

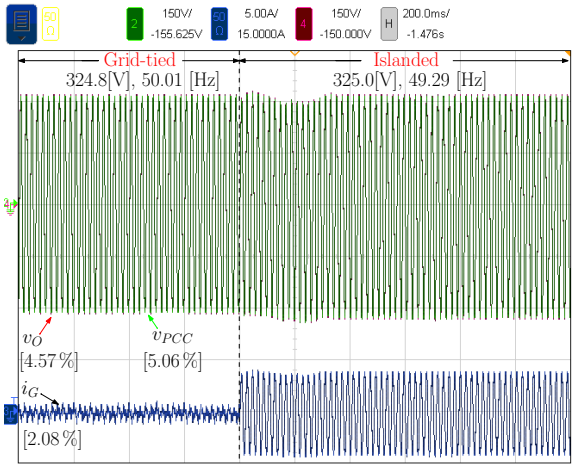
tive load is connected at the PCC and a third harmonic of 5% the nominal grid voltage is superimposed to the grid voltage. During the grid-tied mode, under any of the inertia conditions, the grid current i_G keeps clean ($\text{THD}_{i_G} < 5\%$) despite the significantly distorted grid voltage. This is difficult to achieve with conventional droop solutions based on voltage controlled converters [61,211,212]. Compared with (a), smoother grid-tied to islanded mode transition performance is achieved in case (b) and (c). Noticeably, in islanded mode, the grid-tied inverter can substitute the utility grid in energizing the loads connected at the PCC loads.

7.2.3 Transition from islanded to autonomous operation

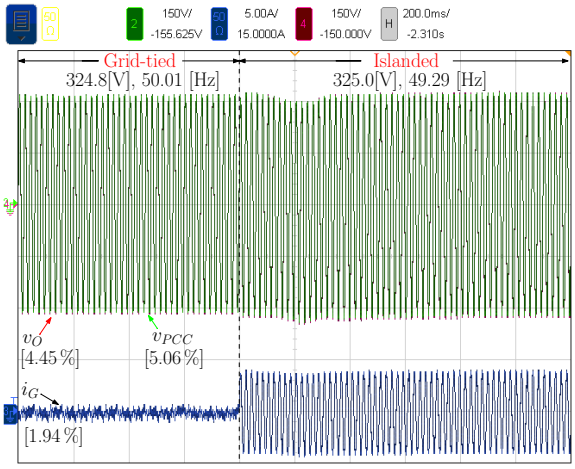
The transition from islanded (i.e., SW_1 closed, SW_2 open) to autonomous (i.e., SW_1 open) mode is shown in Fig. 7-6. In S1, a purely resistive load is connected at the PCC. A corresponding power generation of 580 W by the grid-tied inverter is measured, which results in a corresponding frequency drop of 0.19 Hz. Later on, in S2, the pure resistive PCC load is replaced to with a resistive-inductive one, $Z_{PCC} = 47\,\Omega + (20\,\Omega \parallel 50\,\text{mH})$. In this case, the converter automatically delivers both active and reactive power to meet the needs of the new load, resulting in slight amplitude and frequency drops of the PCC voltage. Finally, in



(a) Without inertia $J = 0\,\mathrm{kg\,m^2}$



(b) With inertia $J = 6 \cdot 10^{-4}\,\mathrm{kg\,m^2}$



(c) With inertia $J = 6 \cdot 10^{-3}\,\mathrm{kg\,m^2}$

Figure 7-5: Transition from grid-tied to islanded mode with different values of emulated inertia. THD values are reported in brackets.

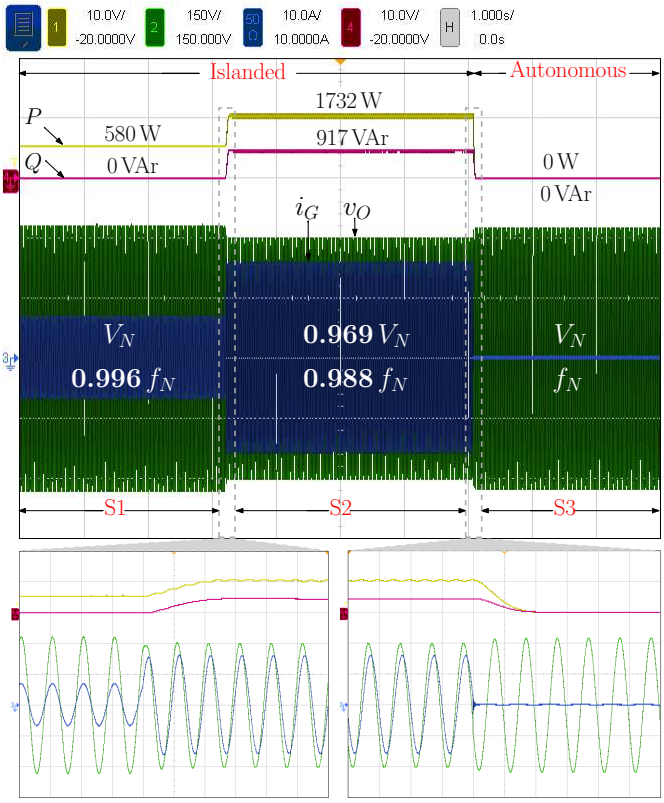
S3, a transition from islanded to autonomous operation mode is performed, which terminates the grid supporting operation. The grid-tied inverter, as a result, ceases to energize the PCC load, but ensures an uninterrupted voltage v_O to its local loads.

7.2.4 Parallel and islanded operation of multiple converters

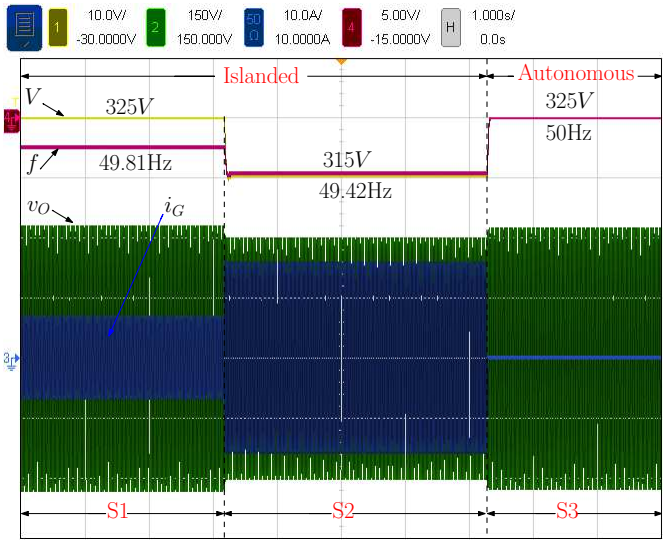
The final performance considering two parallel-connected inverters is verified in Matlab/Simulink and shown in Fig. 7-7. To this purpose, a precise simulation model of the control system in Fig. 4-2 is used [150]. Notably, the considered system operates stably and achieves 1) prompt injected power adaptation to step-variations of the grid frequency and magnitude (S2 and S3 in Fig. 7-7), 2) automatic power sharing in islanded mode (S4 in Fig. 7-7), 3) smooth grid-tied to islanded mode transitions.

7.3 Summary

In this chapter, a power flow controller is presented whose purpose is to allow the nano-grid testbench considered in this thesis to provide grid-support and achieve automatic power sharing among islanded parallel connected units. Indeed, these are considered valuable functionalities for any electrical system, improving the flexibility and the hosting capacity. It has been shown how grid support and parallel operation can be built, once again, on top of the large-bandwidth triple-loop controller that was introduced in Ch. 4. Furthermore, they can be made fully compatible with the previously presented higher level control functions. The only requirement is the definition of a suitable application policy, so as to allow, e.g., the automatic termination of the grid supporting mode whenever this might become detrimental for the nano-grid under consideration.



(a) P and Q



(b) V and f

Figure 7-6: Islanded to autonomous mode transition of the grid-tied inverter with the power regulator in Fig. 7-1. [S1]: $Z_{PCC} = 47\,\Omega$; [S2]: $Z_{PCC} = 47\,\Omega + (20\,\Omega \parallel 50\,\text{mH})$; [S3]: autonomous mode with no local loads. (a) and (b) report different information of the same test.

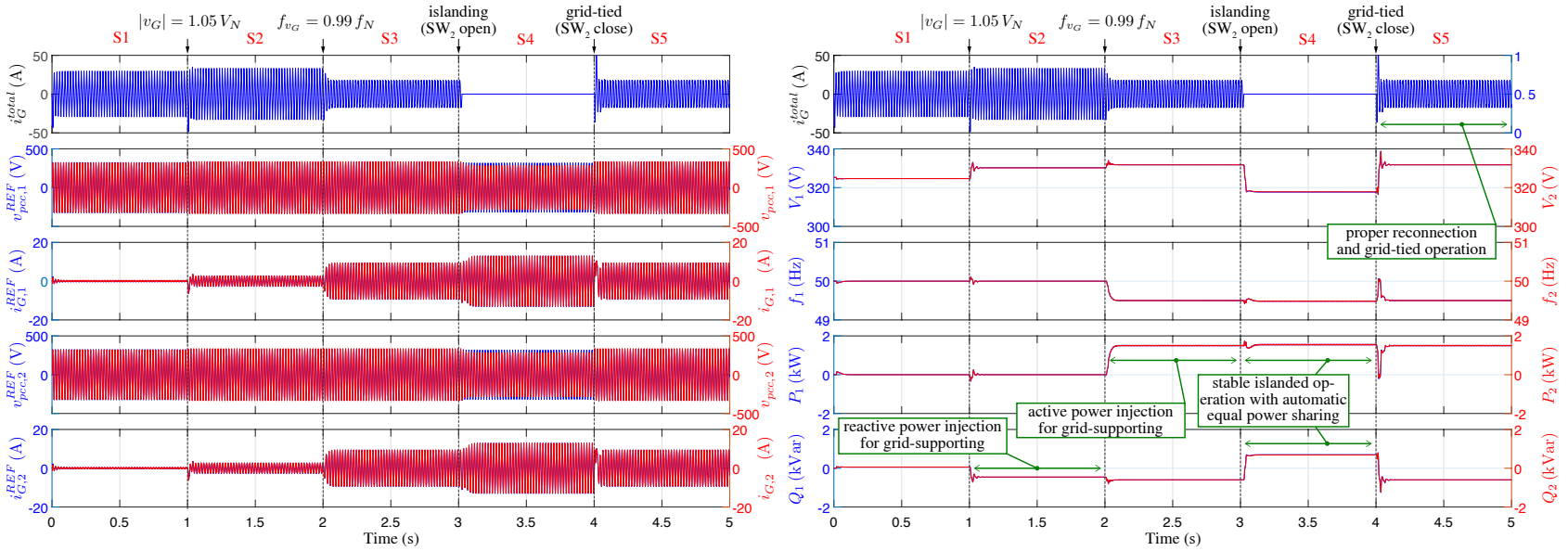


Figure 7-7: Behavior of the system in Fig. 2-3 with two converters implementing the control strategy in Fig. 7-1. $P^* = 0\,\mathrm{W}$, $Q^* = 0\,\mathrm{VA}r$. [S1]: SW$_2$ on, $|v_G| = V_N$, $f_{v_G} = f_N$; [S2]: SW$_2$ on, $|v_G| = 1.05V_N$, $f_{v_G} = f_N$; [S3]: SW$_2$ on, $|v_G| = 1.05V_N$, $f_{v_G} = 0.99f_N$; [S4]: SW$_2$ off, $|v_G| = 1.05V_N$, $f_{v_G} = 0.99f_N$; [S5]: SW$_2$ on, $|v_G| = 1.05V_N$, $f_{v_G} = 0.99f_N$.

Chapter 8

Conclusions

With the rapid development of renewables, the hierarchy of power distributing network is witnessing a transformation from the traditional centralized top-down pattern to a novel distributed bottom-up pattern. The latter is essentially based on nano-grids, the small-scale power networks for single houses or small buildings. It brings along the promise of improved energy efficiency, thanks to the exploitation of local power sources and the integration of storage devices. It also promises better sustainability, as the local energy sources are mostly renewable in nature. It also allows an higher control flexibility for the whole electrical system, as parts of it can seamlessly connect/disconnect from the mains and operate as fully dispatchable sources. This particularly interesting nano-grid scenario delimits the scope of this dissertation.

Although small in power rating, the nano-grid is required by the standards to be highly stable, flexible, scalable and capable of providing important ancillary services. All of these call for novel control strategies for the grid-tied inverter, the crucial component in linking dc and ac sides of nano-grids, as well as the utility grid. From the perspective of a single inverter, the nano-grid application calls for multiple functionalities, with respect to different operation modes and working conditions. For instance, the functionalities of 1) power flow control; 2) grid current harmonics compensation and local distortion filtering; 3) multi-mode operation and seamless mode transitions; 4) resonance damping and stability preserving; 5) resiliency to grid perturbations both in amplitude and frequency; 6) prompt protection; should all be implemented effectively and concurrently.

With the above application scenario in mind, in this dissertation, a high-quality multi-functional control scheme for grid-tied inverters has been proposed, analyzed and experimentally tested, which allows the concurrent realization of all the aforementioned functionalities. It is based on a triple-loop control structure that allows the large bandwidth regulation of the inverter state variables i_L-v_O-i_G (from inner to outer). Indeed, among the numerous control solutions documented in the literature, as discussed in Ch. 3, the triple loop one appears to be the most promising for multi-functional control implementation. However, serious performance limitations are typically implied by the same structure, due to the narrow achievable bandwidth for the the outer loop, the grid current one. With respect to prior art, this work has introduced a novel choice of the regulators, exploiting dead-beat type solutions whenever possible, which has allowed to reach a $1/20$ ratio between the outer loop (grid current loop) bandwidth and the inverter modulation frequency. The design considerations, stability analysis and implementation details of this inverter controller, discussed mostly in Ch. 4, represent the first fundamental contribution offered by this dissertation.

Although the proposed controller brings in many satisfying features, the implementation of all the aforementioned functionalities still remains a challenging task, for two reasons. In the first place, if the realization of each functionality is achieved by a particular, ad hoc, control technique, given the number of different functions to be implemented, a remarkably complicated control system is obtained. In addition, the requirements for implementing different functionalities can sometimes be contradictory, as, for instance, in the case of low-voltage ride through and anti-islanding detection. In spite of that, a systematic solution is devised and proposed in this dissertation that, thanks to the proposed large-bandwidth triple-loop controller organization, is proven able to solve the above issues.

This study, that occupies the second part of this dissertation, is presented in Ch. 5, Ch. 6 and Ch. 7. It has been carried out by taking the following steps: 1) a flexible mode transition manager has been proposed and developed for the realization of multi-mode operation and smooth mode transitions; 2) an auto-tuner has been designed for high quality weak grid operation; and 3) a power flow controller has been implemented to realize grid-supporting functionalities and parallel operation. Items 1)-3) are further original contributions pre-

sented in this dissertation.

Eventually, a high-quality, multi-functional control scheme is established: on top of the large-bandwidth triple-loop controller organization, a flexible mode transition manager, an auto-tuner and a power flow controller are superimposed respectively. These layers do not interfere with one another and pose no stability issue, thanks to frequency range decoupling and suitably defined application policies.

As a result, the final implemented control scheme realizes all the required critical functionalities simultaneously and guarantees high quality of each, with reasonable complexity and no reconfiguration of the underlying controller structure. In addition, the solution is applicable to the weak grid condition, regardless of grid impedance variations, and may allow parallel operation of multiple inverters even when the utility grid is disconnected. All these favorable features have been tested extensively in different conditions, with the only exception of parallel converter operation, that has only been simulated.

The results gathered over time allow to conclude that the proposed control scheme might indeed represent a promising and practical solution for the forthcoming nano-grid and/or smart building scenarios, provided that:

1. the dc sub-grid controller is proven to be as effective as the inverter's one in performing its specific tasks, i.e. tightly regulating the dc link voltage, while managing DERs, dc loads and energy storage devices;

2. the grid-tied inverter controller can be suitably fit into a single board control platform, while keeping all its functionalities and performance levels;

3. a suitable management policy can be devised and built into the control system or, as an alternative, some form of communication with an external grid supervisor can be integrated in the system to properly manage the alternative operation modes (autonomous or grid supporting/parallel).

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