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CICLO XXII

AGEING AND IONIZING RADIATION SYNERGETIC EFFECTS IN DEEP-SUBMICRON CMOS TECHNOLOGIES

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Sommario

I processi termonucleari che si verificano all'interno del sole danno origine a radiazioni ionizzanti, tempeste elettromagnetiche ed emissioni di masse di plasma coronarico ionizzato che possono raggiungere l'atmosfera terrestre. Inoltre gli effetti indotti dai raggi cosmici, la presenza delle fasce di Van Allen, nonché gli ambienti radioattivi artificiali costruiti dall'uomo, espongono i circuiti microelettronici a condizioni di funzionamento estremo nello spazio e sulla terra. Al giorno d'oggi molte attività umane si basano su satelliti geostazionari che devono rimanere funzionanti ed affidabili per lungo tempo: sistemi GPS, comunicazioni audio e video, sistemi di sorveglianza, satelliti meteorologici, applicazioni per la difesa, etc. Inoltre il traffico aereo civile ad alta quota, anch'esso esposto a radiazioni, è sempre in maggiore espansione e naturalmente ogni passeggero si augura di atterrare sano e salvo ogni volta che necessiti di volare. Non da meno le centrali nucleari che forniscono il fabbisogno energetico alle nazioni più avanzate devono assolutamente operare in sicurezza evitando tremendi disastri naturali e sociali. Ognuna di queste applicazioni è tuttavia fortemente dipendente dall'elettronica che gestisce e controlla ogni attività in modo trasparente rispetto all'utente. La sfida principale per ingegneri e scienziati che lavorano in questo ambito, è quella di studiare e progettare microelettronica in grado di operare in ambienti ostili per lungo tempo e in modo affidabile.

Il progresso tecnologico dei dispositivi CMOS verso dimensioni sub-micrometriche gioca un ruolo fondamentale in termini di affidabilità. Infatti, a prescindere dagli effetti delle radiazioni, la riduzione delle dimensioni dei dispositivi e l'implementazione di ossidi ultra sottili influiscono sull'affidabilità dei transistor MOS a causa dell'aumento intrinseco dei campi elettrici che accelerano i naturali processi di degradazione. Per esempio, l'iniezione di portatori caldi è una delle cause più importanti di degradazione in quanto l'energia che gli elettroni possono acquisire è correlata al campo elettrico accelerante. Questa tesi sviluppa questa problematica sia su transistor standard (*Open Layout Transistor, OLT*) che su transistor ad anello (*Enclosed layout Transistor, ELT*), questi ultimi progettati per essere immuni dagli effetti di dose totale (*Total Ionizing Dose, TID*). Sebbene i meccanismi e gli effetti legati ai portatori caldi siano ben documentati nella letteratura di settore, questa tesi è uno dei pochi lavori che si propone di investigare le sinergie con gli effetti indotti dai raggi X, introducendo nuovi e interessanti aspetti legati all'affidabilità. Inoltre la previsione del tempo di vita dell'ossido di *gate* è una delle informazioni più importanti da tenere in considerazione

quando si intende pianificare una missione a lungo termine. Questa tesi dimostra che l'esposizione ai raggi X può alterare i successivi test di affidabilità a causa dell'interazione tra i difetti generati dalle radiazioni e dagli stress elettrici. Di conseguenza, un approccio nuovo va seguito quando si intende valutare l'adeguatezza dei dispositivi da implementare in applicazioni ove siano presenti radiazioni ionizzanti. Senza considerare questi aspetti le previsioni che emergono dai test sperimentali possono in alcuni casi fortunati essere conservative, in altri meno fortunati sottostimare i fenomeni portando a conclusioni fuorvianti e addirittura pericolose per il buon esito di una missione.

Una nuova fonte di incertezza e di sinergia per le tecnologie CMOS avanzate esposte a raggi X riguarda il diverso assorbimento di dose totale indotto dalle interconnessioni metalliche. Infatti la necessità di integrazione sempre più spinta obbliga i progettisti ad incrementare il numero di strati di interconnessione nel *back-end* del dispositivo nonché la riduzione dello spessore dei dielettrici isolanti. Di conseguenza, a fronte di una esposizione ai raggi X, gli elettroni secondari generati dall'interazione con gli strati metallici possono raggiungere più facilmente l'area attiva del transistor degradandolo in modo non uniforme. In questa tesi questo effetto viene studiato grazie all'uso di strutture appositamente progettate, contribuendo cosi allo sviluppo di dispositivi il più possibile immuni da tale fenomeno.

D'altro canto gli effetti indotti da particelle cariche (*Single Event Effect, SEE*) nelle moderne tecnologie stanno diventando la principale fonte di errore. L'elettronica implementata a bordo di navicelle spaziali, satelliti, aerei civili e militari, e perfino al livello del suolo terrestre è affetta da *SEEs*, a volte distruttivi, a volte no. In particolare questa tesi si focalizza sulla rottura istantanea e permanente dell'ossido di *gate* causata dal passaggio di uno ione pesante in presenza di alti campi elettrici (*Single Event Gate Rupture, SEGR*) che, a causa delle sue caratteristiche, lo pone tra gli eventi più rischiosi. In questa tesi vengono studiati diversi fattori: l'influenza del tipo di struttura di test, della polarizzazione mantenuta durante gli esperimenti e l'influenza dei raggi X. Anche in questo caso si dimostra l'esistenza di diverse forme di sinergia tra radiazioni e stress elettrico, fornendo indicazioni circa le metodologie di test e l'uso di strutture che possano fornire risultati realistici riguardo l'incidenza di questo fenomeno nei moderni transistor utilizzati per l'elettronica spaziale.

In conclusione questa tesi vuole essere il primo forte contributo scientifico per lo studio degli effetti sinergici tra radiazione ionizzante e test di vita accelerati su dispositivi CMOS avanzati, da implementare in ambienti radioattivi quali lo spazio o gli esperimenti di fisica delle alte energie.

Abstract

Sun’s radiation, coronal mass ejections, electromagnetic storms, galactic cosmic rays, the Van Allen radiation belts, or artificial radiation environments expose microelectronics circuits to serious conditions in space as well as on Earth.

Nowadays, a lot of human activities rely on satellites orbiting around the Earth such as the GPS system, video and audio communications, surveillance systems, meteorological forecasts, military applications, etc., and they must operate reliably. Civil air traffic is extremely intense around the world and of course everybody wants to land safely each time they fly. Moreover, nuclear power plants that furnish energy to most of the advanced countries on the planet must operate securely in order not to contaminate the environment around, provoking natural and social disasters. Each of these aspects is strongly dependent on electronics that manage and control every activity, permitting us to live our life peacefully. The main challenge for engineers and scientists that work in this sometimes unknown field is to manufacture and design safe electronics able to operate in those environments even for very long times.

The scaling of CMOS technology toward deep-submicron feature sizes plays a fundamental role, regardless of ionizing radiation effects. In fact, as the CMOS devices shrink, featuring ultra-thin gate oxides, the reliability of MOSFETs is affected due to the increase of the operating fields that enhance the natural aging mechanisms. Hot carriers injection from the channel is one of the most important effects, especially in advanced devices because the carrier energy is directly correlated with the electric fields. This thesis in part covers this reliability aspect, both in standard open layout transistors and enclosed layout ones designed to be total-dose hard. A vast literature is available concerning hot carrier mechanisms but this work is one of the only to show the synergies with X-ray induced defects (Total Ionizing Dose, or TID). Indeed, CMOS transistors with feature size equal or below the 130-nm technological node exhibit these kinds of effects, introducing new and interesting aspects. As a result, a different approach must be followed when evaluating the suitability of devices intended for rad-applications since hot-carrier degradation for example can decrease or increase due to previous irradiation.

Furthermore, the prediction of oxide lifetime is one of the main types of analysis in the field of CMOS reliability, extremely important to evaluate the quality of the dielectrics. This thesis proves that exposure to TID may affect reliability predictions due to interplay between defects, traps, and trapped charge generated by both

accelerated tests. Without these aspects in mind the results can be conservative (when lucky), or can even underestimate the phenomena leading to misleading and dangerous conclusions.

Total dose enhancement effects due to interconnects is also a new source of uncertainty in scaled technologies subjected to X-ray irradiation. In fact, the need to have high device density leads to an increase in the number of metal layers as well as a decrease in the inter-metal dielectric thickness, permitting secondary electrons generated by the interaction of X rays with metal tracks to reach the transistors' active area. This aspect is studied in this thesis through the use of dedicated test structures with different metal layer layouts. The experimental results, coupled with device simulations, give radiation-IC designers some guidelines to avoid systematic criticality and better total dose results.

Combined total dose and ageing related effects is not the only focus of this thesis since single events produced by charged particles have become the main source of errors in scaled technologies. Electronics mounted on spacecraft, satellites, aircraft and even at ground level are affected by single event effects, sometimes destructive, sometimes not. In particular, this thesis covers the single event gate rupture (SEGR) phenomenon induced by heavy ions, which is the most risky event during long-term missions. Various aspects have been analyzed in order to fill some gaps present in the literature, starting from the impact of device layout, the influence of the bias applied during accelerated tests and the effects of previous X-ray irradiation. The results presented here demonstrate that different sources of interplay may exist during SEGR tests. Moreover, the provided data strongly indicate use of test structures as close as possible to real scaled transistors instead of large area capacitors to have a straightforward assessment of gate rupture in modern CMOS technologies.

In conclusion, this thesis wants to be the first strong contribution for combined radiation and long-term reliability studies in advanced CMOS technologies implemented in harsh radiation environments.

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Research is freedom

Pursuing a Ph.D. is a highly demanding task from both a practical and a psychological point of view. Much effort must be committed to achieve professional and scientific results and credibility in the international scientific community. This has only been realized with the strong motivation and contribution of the many people that I encountered during my course.

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Nothing is the same without you, I love you.

Marco Silvestri
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List of Acronyms

ASA	Area Self Aligned
CHC	Channel Hot Carrier
CME	Coronal Mass Ejection
CMOS	Complementary Metal Oxide Semiconductor
CMS	Compact Muon Solenoid
CNT	Carbon Nano Tubes
COTS	Commercial Off The Shelf
CVS	Constant Voltage Stress
ECBT	Electrons Conduction Band Tunneling
ELT	Enclosed Layout Transistor
ESD	Electrostatic Discharge
EVBT	Electrons Valence Band Tunneling
FinFET	Fin Field Effect Transistor
FN	Fowler Nordheim
HB	Hard Breakdown
HBD	Hardness By Design
HCI	Hot Carrier Injection
HEMT	High Electron Mobility Transistor
HEP	High Energy Physics
HF	High Flux
HT	High Temperature
HVBT	Holes Valence Band Tunneling
IC	Integrated Circuit
LDD	Lightly Doped Diffusion
LET	Linear Energy Transfer
LF	Low Flux
LHC	Large Hadron Collider
MEMS	Micro Electrical Mechanical Systems
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MUGFET	MUltiple Gate Field Effect Transistor
NBTI	Negative Bias Temperature Instability
OLT	Open Layout Transistor

PSA	Perimeter Self Aligned
RILC	Radiation-Induced Leakage Current
RSB	Radiation-induced Soft Breakdown
RVS	Ramped Voltage Stress
SAA	South Atlantic Anomaly
SBD	Soft Breakdown
SEB	Single Event Burnout
SEE	Single Event Effect
SEGR	Single Event Gate Rupture
SEL	Single Event Latch-up
SET	Single Event Transient
SEU	Single Event Upset
SILC	Stress-Induced Leakage Current
SLHC	Super Large Hadron Collider
SOI	Silicon On Insulator
SRAM	Static Random Access Memory
STI	Shallow Trench Isolation
TCAD	Technology Computer-Aided Design
TDDB	Time-Dependent Dielectric Breakdown
TID	Total Ionizing Dose

Publications List

International Journal Contribution

J1. L. Gonella, F. Faccio, M. Silvestri, S. Gerardin, D. Pantano,V. Re, M. Manghisoni, A. Ranieri, "Total ionizing dose effects in 130-nm commercial CMOS technologies for HEP experiments", *NIM-A*, vol. 582, pp. 750-754, 2007.

J2. M. Silvestri, S. Gerardin, A. Paccagnella, F. Faccio, L. Gonella, "Channel hot carrier stress on irradiated 130-nm NMOSFETs", *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 1960-1967, August 2008.

J3. M. Silvestri, S. Gerardin, A. Paccagnella, F. Faccio, "Degradation induced by X-ray irradiation and channel hot carrier stresses in 130-nm MOSFETs with enclosed layout", *IEEE Trans. Nucl. Sci.,* vol. 55, no. 6, pp. 3216-3223, December 2008.

J4. M. Silvestri, S. Gerardin, A. Paccagnella, G. Ghidini, "Gate rupture in ultra-thin gate oxides irradiated with heavy ions", *IEEE Trans. Nucl. Sci.,* vol. 56, no. 4, August 2009.

J5. A. Griffoni, M. Silvestri, S. Gerardin, G. Meneghesso, A. Paccagnella, B. Kaczer, M. de P. de ten Broeck, R. Verbeeck, and A. Nackaerts "Dose enhancement due to interconnects in deep-submicron MOSFETs exposed to X-rays", *IEEE Trans. Nucl. Sci,* vol. 56, no. 4, pp. 2205-2212, August 2009.

J6. A. Kalavagunta, M. Silvestri, M. J. Beck, S. Dixit, R. D. Schrimpf , R. Reed, D. M. Fleetwood, L. Shen, U. K. Mishra, "Impact of proton irradiation-induced bulk defects on gate-lag in GaN HEMTs", *IEEE Trans. Nucl. Sci.,* vol. 56, no. 6, pp. 3192-3195, December 2009.

J7. M. Silvestri, S. Gerardin, F. Faccio, R. D. Schrimpf, D. M. Fleetwood, and A. Paccagnella, "The role of irradiation bias on the time dependent dielectric breakdown of 130-nm MOSFETs exposed to X-rays", *IEEE Trans. Nucl. Sci.,* vol. 56, no. 6, pp. 3244-3249, December 2009.

J8. M. Silvestri, S. Gerardin, F. Faccio, A. Paccagnella, "Single event gate rupture in 130-nm CMOS transistor arrays subjected to X-ray irradiation", *IEEE Trans. Nucl. Sci.*, in press.

Conference Contribution

C1. L. Gonella, M. Silvestri, S. Gerardin on behalf of DACEL-CERN collaboration, "Total ionizing dose effects in 130-nm commercial CMOS technologies for HEP experiments", *Vertex workshop*, Perugia, Italy, 2006.

C2. M. Silvestri, S. Gerardin, A. Paccagnella, F. Faccio, L. Gonella, D. Pantano, V. Re, M. Manghisoni, L. Ratti, A. Ranieri, "channel hot carrier stress on irradiated 130-nm MOSFETs: impact of bias conditions during X-ray exposure", *9th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Deauville, France, 2007.

C3. M. Silvestri, S. Gerardin, A. Paccagnella, F. Faccio, "Degradation induced by X-ray irradiation and channel hot carrier stresses in 130-nm MOSFETs with enclosed layout", *2008 IEEE Nuclear and Space Radiation Effects Conference (NSREC)*, Tucson-AZ, USA, 2008.

C4. M. Silvestri, S. Gerardin, A. Paccagnella, G. Ghidini, "Gate rupture in ultra-thin gate oxides irradiated with heavy ions", *8th European Workshop on Radiation and Its Effects on Components and Systems (RADECS)*, Jyvaskyla, Finland, 2008.

C5. A. Griffoni, M. Silvestri, S. Gerardin, G. Meneghesso, A. Paccagnella, B. Kaczer, M. de P. de ten Broeck, R. Verbeeck, and A. Nackaerts "Dose enhancement due to interconnects in deep-submicron MOSFETs exposed to X-rays", *8th European Workshop on Radiation and Its Effects on Components and Systems (RADECS)*, Jyvaskyla, Finland, 2008.

C6. Y. S. Puzyrev, M. J. Beck, B. Tuttle, M. Silvestri, R. D. Schrimpf, D. M. Fleetwood, S.T. Pantelides, "Interaction of hydrogen with defects in GaN", *Applied Physics Symposium*, 2009.

C7. A. Kalavagunta, M. Silvestri, M. J. Beck, S. Dixit, R. D. Schrimpf , R. Reed, D. M. Fleetwood, L. Shen, U. K. Mishra, "impact of proton irradiation-induced bulk defects on gate-lag in GaN HEMTs", *2009 IEEE Nuclear and Space Radiation Effects Conference (NSREC)*, Quebec City, Canada, 2009.

C8. M. Silvestri, S. Gerardin, F. Faccio, R. D. Schrimpf, D. M. Fleetwood, and A. Paccagnella, "The role of irradiation bias on the time dependent dielectric breakdown of 130-nm MOSFETs exposed to X-rays", *2009 IEEE Nuclear and Space Radiation Effects Conference (NSREC)*, Quebec City, Canada, 2009.

C9. M. Silvestri, S. Gerardin, F. Faccio, A. Paccagnella, "Single event gate rupture in 130-nm CMOS transistor arrays subjected to X-ray irradiation", *10th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Brugges, Belgium, 2009.

Conference Proceedings

CP1. **Outstanding conference paper**
M. Silvestri, S. Gerardin, A. Paccagnella, F. Faccio, L. Gonella, D. Pantano, V. Re, M. Manghisoni, L. Ratti, A. Ranieri, "Channel hot carrier stress on irradiated 130-nm MOSFETs: impact of bias conditions during X-ray exposure", *in Proc. 9th European Conference on Radiation and Its Effects on Components and Systems (RADECS) 2007*.

CP2. M. Silvestri, S. Gerardin, A. Paccagnella, G. Ghidini, "Gate rupture in ultra-thin gate oxides irradiated with heavy ions", *in Proc. 8th European Workshop on Radiation and Its Effects on Components and Systems (RADECS) 2008.*

CP3. A. Griffoni, M. Silvestri, S. Gerardin, G. Meneghesso, A. Paccagnella, B. Kaczer, M. de P. de ten Broeck, R. Verbeeck, and A. Nackaerts "Dose enhancement due to interconnects in deep-submicron MOSFETs exposed to X-rays", *in Proc. 8th European Workshop on Radiation and Its Effects on Components and Systems (RADECS) 2008.*

CP4. M. Silvestri, S. Gerardin, F. Faccio, A. Paccagnella, "Single event gate rupture in 130-nm CMOS transistor arrays subjected to X-ray irradiation", *in Proc. 10th European Conference on Radiation and Its Effects on Components and Systems (RADECS) 2009.*

Table of Contents

Chapter 1

Introduction

The reliability of microelectronic devices and circuits implemented in a radiation environment is a major factor that determines both their manufacturability and application lifetime. The functionality of spacecraft, satellites, nuclear reactors, or particle detectors depends on a large amount of electronics that must be reliable for a long time under extreme operating conditions. The specific reliability problem studied in this Ph.D. regards the interplay between accelerated electrical lifetime tests and ionizing radiation effects.

1.1. Space Radiation Environment

Spacecraft and satellites are continuously exposed to a variety of radioactive phenomena, mainly generated by the Sun. The Sun's outer atmosphere (the corona) emits a continuous stream of particles called the solar wind, composed of protons, electrons, alphas, and heavy ions [Barth09]. Thanks to the very high temperature of the Sun's surface, these particles can gain sufficient energy to escape the gravitational force of the Sun and travel in the outer space, reaching the Earth's magnetosphere as well. A massive emission of ionized plasma from the Sun, called a Coronal Mass Ejection (CME), can approach the Earth within minutes, possibly provoking serious damage to electronics in orbit.

The Earth's magnetosphere is formed by the interaction of the Earth's magnetic field and the solar wind. It is compressed on the solar side and deeply extended on the anti-solar side as sketched in Fig. 1.1. This asymmetry is reached to balance the solar wind

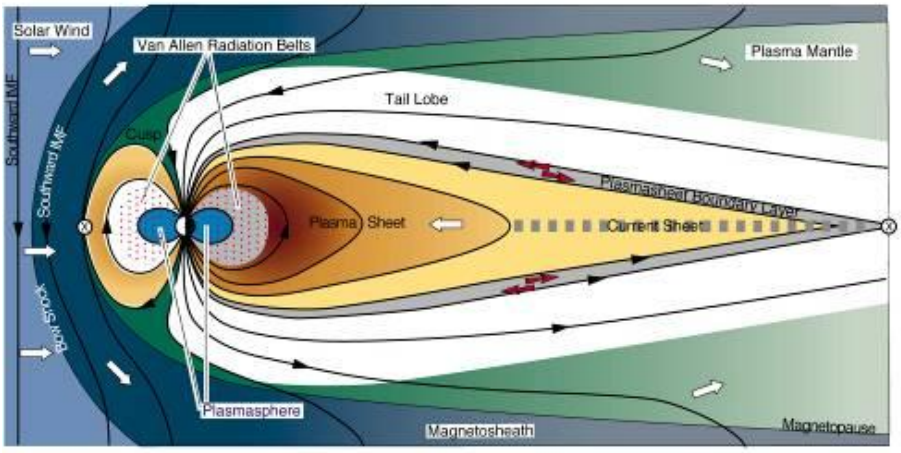


Fig. 1.1 Earth magnetosphere [Barth09].

and the geomagnetic field pressure. At the level of the poles, the magnetosphere gives the possibility for particles to penetrate into the upper Earth atmosphere.

Close to the Earth a small percentage of the charged particles that pass around the magnetosphere can be trapped in the inner Van Allen radiation belts that can catch electrons with energies up to tens of MeV and protons up to hundreds of MeV, as well as heavy ions [Barth03].

The Van Allen Radiation Belts (Fig. 1.2) consist of two regions of trapped particles:

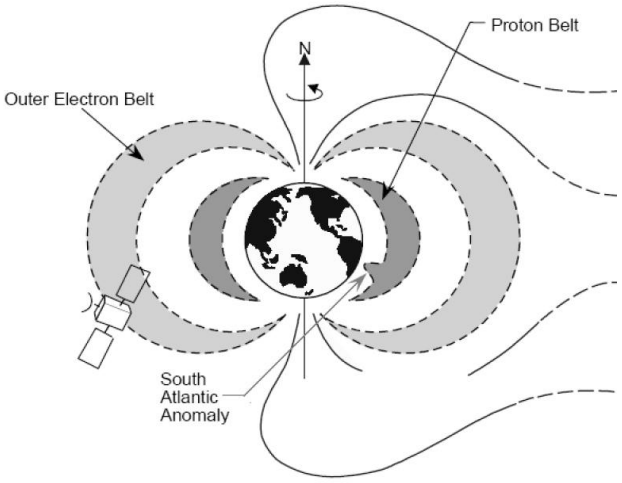


Fig. 1.2 Van Allen radiation belts [Ma89].

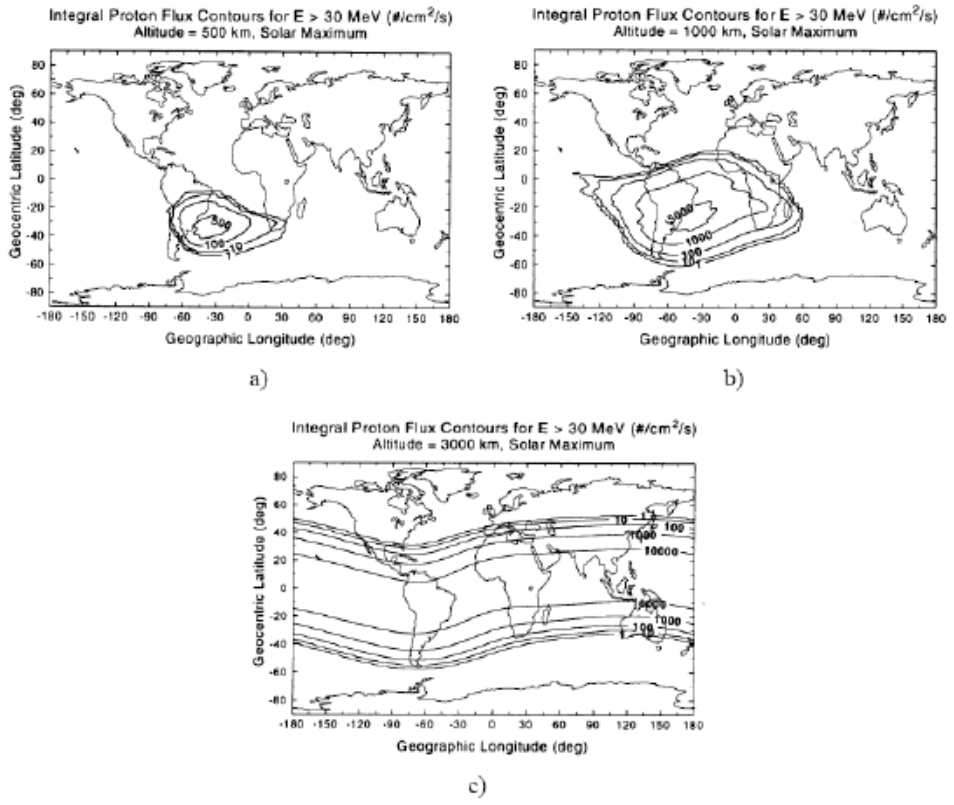


Fig. 1.3 Integral proton flux contour for proton energy greater than 30 MeV as a function of altitude and geographic longitude [Dodd99].

an inner proton belt and an outer electron belt, separated by a region of reduced particle flux (the so-called *slot* region).

Although the origin of trapped particles in the near-Earth environment is not completely understood, sources include the solar wind and transient solar events, cosmic ray particles from interplanetary space, and reaction products from cosmic ray collisions with the Earth's atmosphere [Xapsos07].

The difference between the Earth geographic spin axis and its magnetic axis causes a localized region of lower magnetic field over the South Atlantic, called the South Atlantic Anomaly (SAA) [Xapsos07]. In this region the proton flux (E > 30 MeV) at altitudes less than 1000-2000 km is greatly increased as compared to an equivalent altitude over other regions of the Earth.

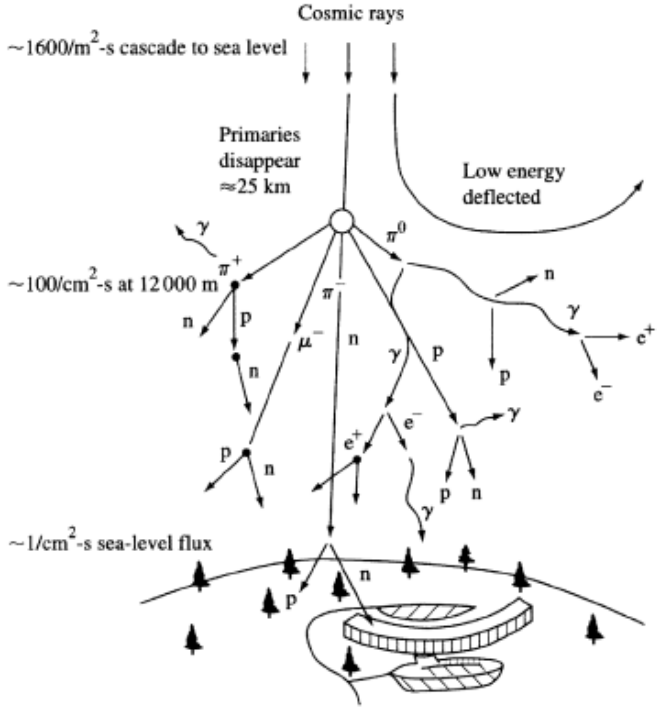


Fig. 1.4 Particle shower generated by high energetic GCR in the upper part of the atmosphere [Dodd99].

In Fig. 1.3 SAA is reported as a function of the geographic longitude and altitude during the solar maximum. As the altitude is reduced the integral particle flux becomes highly localized over the Brazil coast 1.3a. In contrast, the Van Allen belt structure reappears for higher altitudes, 1.3c [Dodd99].

When dealing with the space environment the radioactive phenomena produced by the Sun are not the only ones. Galactic Cosmic Rays (GCR) are high-energy charged particles originating outside of the solar system, probably caused by explosions of stars. They are composed of about 83% protons, 13% alphas, 3% electrons, and about 1% heavier ions [Barth09]. The energies of GCRs can reach TeVs and when they enter the top of the Earth's atmosphere they interact with nitrogen and oxygen atoms producing the so called *particle shower,* as reported in Fig. 1.4.

The secondary particles generated by the collisions are protons, electrons, neutrons, heavy ions, muons, and pions that can interact with avionics of aircraft producing soft or even hard single events (especially neutrons with energies up to hundreds of MeV). For very high energy GCRs the secondary particles, especially neutrons, may reach also the ground level possibly provoking SEEs.

1.2. High Energy Physics Radiation Environment

Artificial radiation environments like a particle tracker in a High Energy Physics (HEP) experiment, or a nuclear power plant, are very challenging in terms of ionizing radiation. In fact the levels of dose and particle fluxes are orders of magnitude above the ones present in space.

The most important and biggest particle collider, namely, the Large Hadron Collider (LHC) built by the European Organization for Nuclear Research at CERN, Geneva, is expected to accelerate two proton beams up to an energy of 7 TeV along the 27 km tunnel 100-m underneath the Swiss and French ground. Four different experiments are planned to work along the accelerating ring: CMS, ATLAS, LHC-b, and ALICE [CERN].

In each of these four experiments the two beams collide, producing at the collision point an energy of 14 TeV. The fragments formed during this process are tracked by millions of silicon detectors inside a very high magnetic field in order to detect the sub-particle type, energy, and momentum. As a consequence, a large quantity of electronics

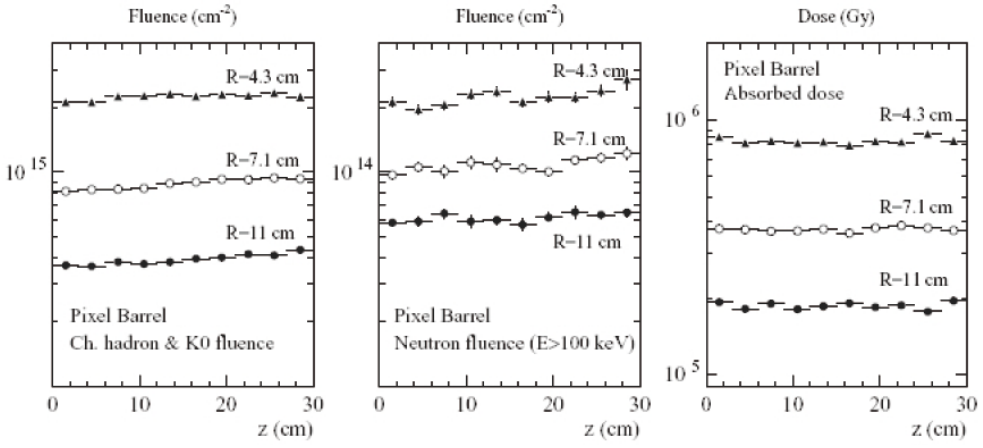


Fig. 1.5 Expected hadron fluence, neutron fluence, and TID as a function of barrel tracker position for the CMS experiment at the LHC [CMS98]

devoted to read-out the detectors is mounted around the collision point and subjected to extreme work conditions.

In Fig. 1.5, for example, are reported the expected values of hadron and neutron fluences as well as TID absorbed, as a function of the distance from the collision point, in the CMS barrel tracker of LHC [CMS98]. Hadron fluences as large as 10^{15} cm^{-2}, as well as doses up to 100 Mrad are expected in ten years of operation in the pixel barrel (the innermost detector).

1.3. Ionizing Radiation Challenges for Deep-Submicron CMOS Technology

1.3.1. Total Ionizing Dose

The need to follow, as much as possible, Moore's law, pushes the commercial manufacturer to increase the device density of modern Integrated Circuits (ICs) down to the feasibility limit [Veloso07], [Dennard07]. Intel's 45-nm higk-κ microprocessors are now available on commercial market, though, looking at the next step down to 32 nm [Skotnicki07]. This scaling trend impacts the ionizing radiation response as well introducing new challenges while removing some historical issues.

The main degradation mechanism that occurs in a MOS device subjected to ionizing radiation is the oxide charge trapping [Schwank02], [Oldham03], [Barnaby06]. A schematic band diagram for a NMOS device is reported in Fig. 1.6. Immediately after electron-hole pair generation induced by radiation the electrons and holes that survive the initial recombination are split by the electric field and drift toward the Si/SiO_2 interface (holes) and gate (electrons). As the holes arrive at the interface, some fraction are trapped in pre-existing localized defects, leading to a net positive charge N_{ot}.

Positively charged hydrogen can be released as well from the gate/oxide interface and drift to the Si/SiO_2 interface where it can react, forming interface traps, N_{it} [Pantelides07]. Both interface traps, which can be negatively or positively charged, and trapped charge influence the electrostatics of CMOS transistors, affecting the main parameters such as threshold voltage, drain current, transconductance, and carrier mobility [Barnaby06].

The thinning of the gate oxide below 5 nm has significantly mitigated the Total Ionizing Dose (TID) effects, reducing the charge trapping phenomena that plagued the older technologies built with thicker oxides when employed in radiation environments [Saks84].

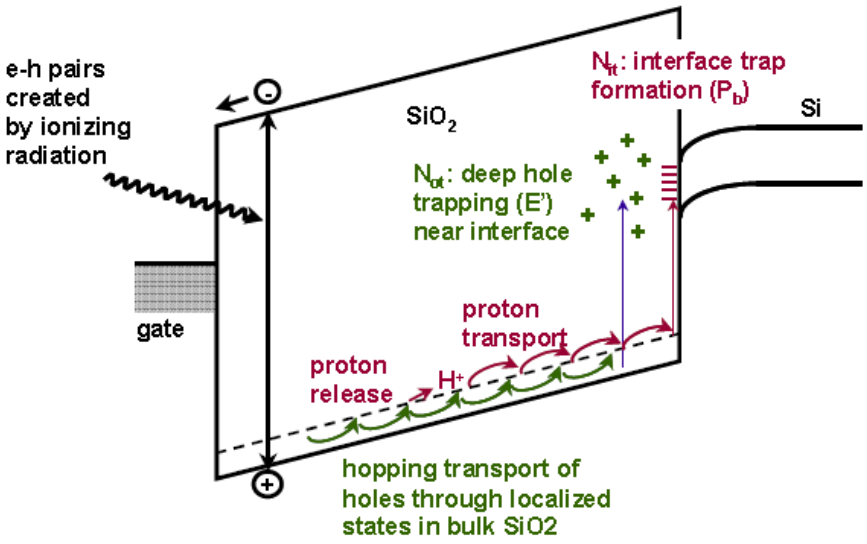


Fig. 1.6 Schematic representation of the damage induced by radiation in a MOS structure [Schwank02].

In contrast, the very thick lateral oxide (STI) has become the Achilles heel of modern CMOS transistors exposed to ionizing radiation. In fact, the large amount of charge that can be trapped at the edges of the device influence the electrostatics of the transistor, leading to large shifts of the characteristics parameters [Faccio05].

As a consequence, the lateral isolation engineering will be one of the key points to have commercial electronics with a good resilience to total ionizing dose effects [Shaneyfelt98]. However, despite the increased STI sensitivity, the total dose hardness of commercial CMOS devices increased during the last ten years as sketched in Fig. 1.7, featuring for the 130-nm and 90-nm technology nodes a TID tolerance of about 200 krad(SiO_2) [Dodd09], doses of interest for space applications.

Unfortunately, as sketched in Fig. 1.8, in addition to radiation effects, ultra-scaled CMOS devices are affected also by an ever increasing chip-to-chip, lot-to-lot, and foundry-to-foundry variability that can affect the performance of the devices, introducing an additional source of variability when TID hardness is evaluated [Felix06].

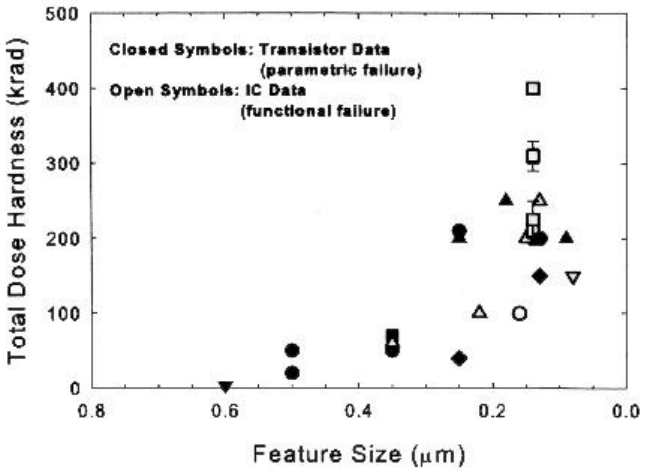


Fig. 1.7 Total dose failure level as a function of the feature size for submicron and deep-submicron CMOS technologies [Dodd09].

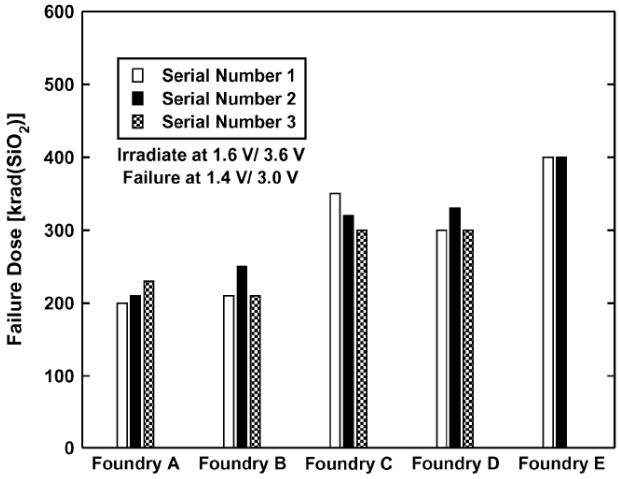


Fig. 1.8 Summary of the failure dose for three nominally identical 130-nm commercial SRAM manufactured in five different foundries [Felix06].

From the plot in Fig. 1.8 is evident that even nominally identical samples from the same manufacturer display different failure doses and almost a factor of two is present among the foundries. This suggests that it is more and more difficult to consider in absolute terms the TID response of a particular scaled technology without appropriate qualification, screening, and manufacturing control.

1.3.2. Single Event Effects

Differently from the TID trend with technology scaling, the effects induced by a single particle have become the main source of soft damage (i.e., recoverable) in ICs circuitry built with modern CMOS transistors [Baumann05]. Single Event Upset (SEU) and Single Event Transient (SET) are the main contributors to the Soft Error Rate (SER) of many modern commercial CMOS technologies not only when employed in radiation environments but even at high altitude and ground level.

Charge collection is the basic mechanism for Single Event Effects (SEEs) and it depends on ion LET, ion energy, strike trajectory, and stricken device. The reverse-biased p-n junction, like the source- or drain-bulk junction in a CMOS transistor, is the most sensitive part of a circuit exposed to particle irradiation such as alphas, protons, or heavy ions. The magnitude of the collected charge depends on several factors including the size of the device, the bias applied, the substrate doping, the ion characteristics, etc., ranging between ~1 fC to hundreds of fC [Baumann05].

The use of Silicon On Insulator (SOI) transistors is one of the ways to reduce the amount of collected charge after the particle strike ameliorating the robustness of

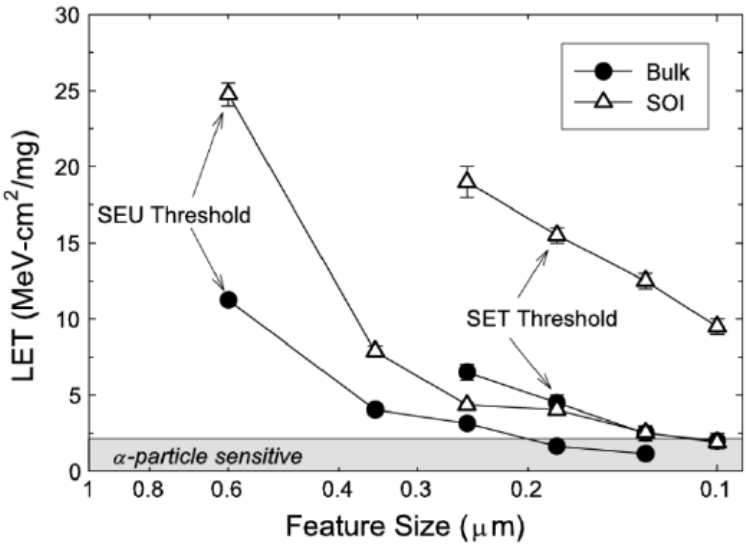


Fig. 1.9 Simulated critical LET for SET and SEU as a function of scaling for both Bulk and SOI CMOS technologies [Dodd04].

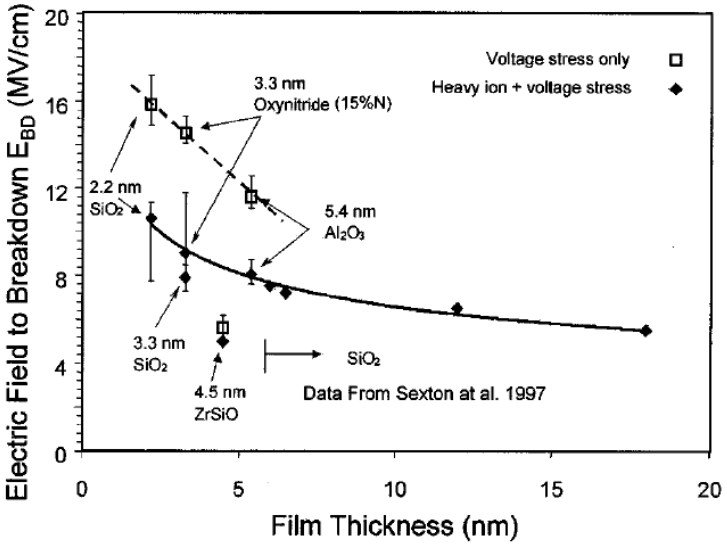


Fig. 1.10 Critical electric field to breakdown under voltage stress and exposure to 342-MeV Au ions for different CMOS capacitors [Massengill01].

circuitry built with this technology [Ferlet06]. In fact, the presence of the buried oxide underneath the source and drain diffusions, as well as the partially or fully depleted thin bulk, reduce the volume for charge collection, lowering the SEE sensitivity [Schwank04].

As sketched in Fig. 1.9, the simulated threshold LET for SEU in SRAMs and for SET propagation in inverter-chains as a function of the feature size is larger in SOI than in bulk technology due to the reduction of the collected charge [Dodd04]. However, even if SOI exhibits an intrinsic radiation robustness, the buried oxide is still sensitive to charge trapping and microdose effects [Griffoni07] and the processing techniques to make hardened buried oxides are too expensive and now commercially unavailable [Dodd09].

Unfortunately, not all SEEs are recoverable and, when long term reliability is evaluated, it is essential to avoid any destructive event like Single Event Latchup (SEL), Single Event Burnout (SEB), or Single Event Gate Rupture (SEGR) [Sexton03]. In fact, the impracticability to maintain electronic circuits in space or the difficulty to replace circuitry in very complex high energy physics experiments make hard errors very risky.

While SEB regards mostly power devices and SEL can be prevented by a smart design, SEGR can occur in both power and digital MOSFETs in an unpredictable manner. The damage is characterized by the sudden rupture of the gate dielectric and is mainly driven by the oxide electric field and particle Linear Energy Transfer (LET).

Differently from soft errors, the SEGR occurrence in logic devices is mitigated thanks to the technology scaling as reported in Fig. 1.10, where the critical electric field to breakdown, with and without Au-ion irradiation, is reported as a function of the oxide thickness [Massengill01]. During the last ten years the SEGR scenario is radically changed due to the intrinsic radiation hardness of thin oxides alleviating some dependencies such as temperature, incident particle angle, and TID [Sexton03]. However almost all works reported in the literature use large area capacitors that cannot straightforwardly be correlated to real scaled MOSFETs.

1.4. Long-Term Reliability in Harsh Radiation Environment

The long-term reliability requirements needed by the rad-electronics market (i.e., space and HEP) are definitely different from the ones expected by the consumer market. The use of advanced CMOS technologies in such environments is often limited and lies generations behind state-of-the-art commercial ICs.

However, the need for high performance and scalability in satellites, spacecrafts, and particle detectors, pushes the designers to use electronics that are closer to modern technology nodes. Unfortunately, this approach raises some concerns about the long-term reliability because of the simultaneous increase of the intrinsic operating electric field as sketched in Fig. 1.11 [Dennard07]. Indeed, the gate oxide thickness, as well as the channel length, shrink faster than the nominal operating bias [ITRS], leading to the overall increase of the electric field. Consequently, the use of modern devices raises a lot of concerns relating to both radiation and intrinsic device reliability especially when applications must be designed to last many years in harsh radiation environments.

For instance, the planned upgrade of the large hadron collider, namely, Super Large Hadron Collider (SLHC), is expected to increment the machine luminosity from 10^{34} to 10^{35} cm^{-2} s^{-1}, requiring the read-out electronics to work under fast hadron fluences as large as 10^{16} cm^{-2} and TID levels above 100 Mrad remaining reliable for ten years [Candel05]. Similarly, the upcoming NASA/ESA space mission Europa Jupiter System Mission (EJSM), intended to be launched around 2020, must be designed to last about ten years in deep space under an extreme radiation environment [JPL].

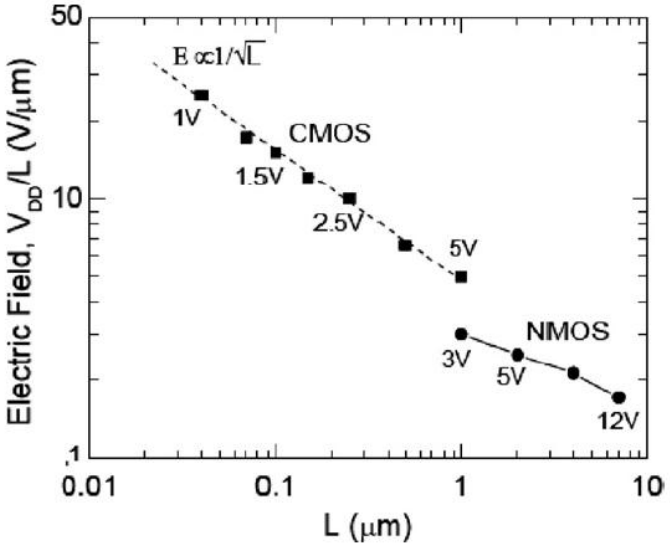


Fig. 1.11 Electric field as a function of the channel length for advanced CMOS technology [Dennard07].

In addition to radiation effects, a plethora of failure mechanisms must be considered to ensure long-term reliability, such as Channel Hot Carrier (CHC) degradation [Groes99], Time-Dependent Dielectric Breakdown (TDDB) [Stathis01], Negative Bias Temperature Instability (NBTI) [Stathis06], electromigration, and Electrostatic Discharge (ESD), each of those with a different trend with CMOS scaling. In this Ph.D. the combined effects produced by radiation, CHC, and TDDB are analyzed.

1.5. Radiation and Ageing Synergetic Effects

The common thought about the effects of radiation and ageing of CMOS devices is that they can be summed. In fact, in the real high-reliability long-term missions the evolution of the degradation over time is due to both electrical- and radiation-induced damage. However, with the CMOS scaling that pushes the feature size smaller and smaller, the combined irradiation and accelerated ageing mechanisms are going to introduce additional issues.

The first strong message has been given during the *2009 IEEE – Nuclear and Space Radiation Effects Conference (NSREC)*: "Radiation interaction with standard reliability

predictions is often not considered. Radiation measurements tend to be made separately from reliability measurements and vice versa. However, the processes are intimately related at a physical level" [Sheldon09]. In fact, the effect of ionizing radiation is to produce electron/hole pairs that recombine or become trapped in the oxide layers affecting the electrostatic of the transistors. Similarly, the production of traps over time, for example due to NBTI in PMOSFETs or CHC in NMOSFETs, leads to similar effects. However, if radiation and electrical stress are applied simultaneously or subsequently the behavior of one can be influenced by the effects of the other one and vice versa.

Pioneer work performed in the 80's investigated possible synergetic effects using devices with thick gate oxide (33 nm), finding that for sufficiently high doses, radiation damage completely overwhelms the effects of subsequent CHC stresses due to the massive production of interface traps during irradiation [McBrayer85], [McBrayer87].

More recently combined irradiation and NBTI experiments demonstrate that the NBTI degradation is enhanced when devices are previously irradiated with γ-rays as compared to NBTI performed alone [Fleetwood07].

In this framework, this Ph.D. and only a few other works, have begun to characterize the interactions of these mechanisms in deep-submicron CMOS devices, leading to interesting and innovative results.

1.6. Objectives of the Thesis

The aim of this thesis is to study the synergetic effects between ionizing radiation and electrical accelerated lifetime tests using 130-nm CMOS transistors.

The first objective concerns the interaction between TID and the two most common ageing mechanisms, namely CHC and TDDB. In particular this research is focused on X-ray related effects. To achieve this goal a large number of X-ray irradiations have been performed, followed by different electrical stresses studying the influence of temperature, transistor geometry, oxide thickness, and device layout. In fact, not only standard open layout transistors have been analyzed but also enclosed layout ones (edgeless) since this thesis is intended for long-life missions in very harsh radiation environments such as HEP and deep space.

The second goal of this thesis is to shed light on hard ruptures (SEGR) induced by heavy ions studying the interplay between voltage stress procedure, sample layout, previous TID, and bias polarity. The use of structures, much closer to real scaled CMOS transistors and the influence of the stress procedure on SEGR occurrence are the most striking results of this part of the research. In fact, almost all SEGR works

that can be found in literature focus on large area capacitors often without comments on the influence of the indispensable high bias applied to the gate.

1.7. Outline of the Thesis

The thesis is organized as follows and the different chapters are briefly summarized.

Chapter 2: Channel Hot Carrier Degradation in X-ray Irradiated Open Layout Transistors

In this chapter the influence of X-ray exposure on the long-term reliability of 130-nm NMOSFETs as a function of device geometry and irradiation bias conditions is analyzed. In particular the focus is on CHC electrical stresses on n-channel MOSFETs performed after irradiation with X-rays up to 136 Mrad(SiO_2) in different bias conditions. Irradiation is shown to negatively affect the degradation during subsequent hot carrier injection. Increasing the bias during irradiation slightly reduces the impact on following electrical stress in core MOSFETs. These effects are attributed to enhanced impact ionization at the bulk-STI interfaces due to radiation-induced trapped charge and defects.

Chapter 3: Channel Hot Carrier Degradation in X-ray Irradiated Enclosed Layout Transistors

Channel hot carrier degradation of enclosed layout transistors as a function of previous accumulated total ionizing dose, stress temperature, and transistor geometry, is presented. The parametric degradation follows a power law, whose exponent is higher than in conventional open layout transistors as reported in the previous chapter, possibly due to a different diffusion geometry of hydrogen. Device physical simulations suggest a distorted electric field at the device corners, which leads to a non-uniform impact ionization.

Chapter 4: Dielectric Breakdown: The Role of Bias During X-ray Irradiation

This chapter presents the effects of biased and unbiased X-ray irradiation on the subsequent Time-Dependent Dielectric Breakdown (TDDB) of 130-nm MOSFETs irradiated up to 1 Mrad(SiO_2). A small but measurable increase in TDDB lifetime after irradiation at the worst-case irradiation bias is found especially in PMOSFETs. The increased TDDB lifetime and the irradiation-bias dependence are attributed to the

influence of radiation-induced traps on the stressing current during the subsequent reliability testing.

Chapter 5: X-ray Irradiation: Dose Enhancement Due to Metal Interconnects

This chapter is focused on dose-enhancement effects due to interconnects in deep-submicron CMOS using ad-hoc designed MOSFETs with different metal layouts. The presence of metal-1 tracks in the proximity of the device active areas may significantly modify the response to X-rays. The results reported here demonstrate that not only radiation and electrical stresses interact but also the device layout can impact the response to radiation.

Chapter 6: Single Event Gate Rupture: Impact of Bias and Device Layout

The combined effect of heavy-ion irradiation and large applied bias on the dielectric breakdown of ultra-thin gate oxides is reported. Moreover, the impact of the border regions is analyzed through dedicated test structures. Bias polarity plays a fundamental role, with the inversion regime being more detrimental than the accumulation regime for the onset of gate rupture. Moreover, the average voltage to breakdown is, under certain conditions, lower in structures more closely resembling real MOSFETs, as compared to those commonly used for the evaluation of Single Event Gate Rupture.

Chapter 7: Single Event Gate Rupture: Impact of X-ray Exposure

Through the use of dedicated test structures the response to heavy ion irradiation under high stress voltages of devices previously irradiated with X-rays is shown. Only a slight impact is found on the gate rupture critical voltage at a LET of 32 MeV cm^2 mg^{-1} for devices previously irradiated up to 3 Mrad(SiO_2), and practically no change for 100 Mrad(SiO_2) irradiation, doses of interest for the future Super Large Hadron Collider.

Chapter 8: Conclusions and Future Work

The main results reported in this manuscript are summarized and a brief overview of the future work is given.

Chapter 2

Channel Hot Carrier Degradation in X-ray Irradiated Open Layout Transistors

In this chapter the interaction between X-ray irradiation and channel hot carrier degradation in open-layout bulk NMOSFETs is analyzed. In particular, the impact of irradiation bias on the device response to subsequent Channel Hot Carrier injection is presented through experimental data and device simulations.

2.1. Introduction

The thinning of the gate oxide has greatly enhanced the radiation hardness of CMOS technology. State-of-the-art devices feature gate oxides thinner than 2 nm, for which fixed charge trapping is minimal due to the very short tunneling distance [Barnaby06]. Due to scaling, MOSFETs built with feature sizes below 130 nm can still work up to extremely high doses of 100 Mrad(SiO_2) even without using hardness-by-design solutions, such as enclosed layout and guard rings, at least for some digital applications [Faccio05]. Whilst more radiation resistant, modern CMOS devices may be intrinsically less reliable. During the years, the operating voltage has been scaled less rapidly than the feature size, causing ever-increasing electrical fields inside the device, which may be detrimental for the long-term reliability. For instance, Channel Hot Carrier (CHC) degradation is particularly important in NMOSFETs, because of higher

electric fields and impact ionization near the drain region as compared to PMOSFETs [Groes99]. Interplay between radiation effects and the aging of devices with ultra-thin gate oxide has been recently shown in the case of heavy ion strikes, where reduction in Time-To-Breakdown and alterations in the degradation kinetics of the transistor parameters were observed [Cester03], [Choi02]. Possible synergetic effects between hot-electron and γ-rays have been studied in devices with thick gate oxide in the 80's [McBrayer85], [McBrayer87], but, to the best of our knowledge, never with modern devices featuring ultra-thin gate oxides.

2.2. Experimental and Devices

We studied n-channel MOSFETs manufactured by a commercial foundry in a standard (non radiation-hard) 130-nm CMOS technology. A custom-developed test structure, named TID1, was used to explore the reliability of this process in the S-LHC environment. The samples, integrated in TID1, belong to two groups:

- Core-NMOSFETs with gate oxide t_{ox} = 2 nm, channel length L = 0.12 μm and width (W) ranging from 0.16 μm to 2 μm, nominal operating voltage V_{dd} = 1.5 V.
- I/O-NMOSFETs with gate oxide t_{ox} = 5 nm, channel length L = 0.24 μm and width ranging from 0.36 μm to 2 μm, nominal operating voltage V_{dd} = 2.5 V.

Core devices are meant for the internal logic of the chip, while I/O devices are used for high swing input-output circuitry where 2.5 V supply is required.

Irradiation was performed at CERN, Geneva, Switzerland, using an automatic wafer probe station equipped with a 10-KeV X-ray tube system and a custom-developed probe card. After irradiation we subjected the devices to accelerated electrical stresses in order to analyze the degradation kinetics of the main parameters as a function of stress time. All electrical measures were taken by using an Agilent 4156B parameter analyzer. During irradiation the devices were biased in different conditions: V_{gs} = 0 V, $V_{gs} = V_{dd}/2$, and $V_{gs} = V_{dd}$ keeping source, drain, and bulk grounded. We irradiated the samples in logarithmic steps up to 136 Mrad(SiO_2) at a fixed dose rate of 25 krad(SiO_2)/min. The irradiation was periodically interrupted to measure the DC characteristics of the devices: the drain current vs. gate voltage (I_{ds}-V_{gs}), and the drain current vs. drain voltage (I_{ds}-V_{ds}).

Irradiated devices and reference unirradiated devices were submitted to channel hot carrier stresses. The stress voltage was chosen to maximize the substrate current. Usually $V_{gs} \approx V_{ds}/2$ is the condition that generates the maximum amount of holes (and as a result the bulk current) in the substrate due to impact ionization at the drain region [Groes99]. Measuring the I_{sub} vs. V_{gs} for different drain voltages, we found the

following stress voltages to maximize the bulk current and produce appreciable damage in a limited amount of time:

- Core NMOSFETs: V_{gs} = 2 V and V_{ds} = 2.2 V
- I/O NMOSFETs: V_{gs} = 2.4 V and V_{ds} = 4 V.

These voltages are larger than the operating ones, to accelerate the degradation experienced in real conditions, as commonly done in the field of reliability testing; proper models exist to extrapolate the accelerated data to nominal conditions [Groes99].

We periodically interrupted the electrical stresses to measure I_{ds}-V_{gs} and I_{ds}-V_{ds} curves, in order to extract the main parameters, such as threshold voltage (extracted by linearly fitting the I_{ds}-V_{gs} at the point of maximum transconductance), transconductance, and sub-threshold swing. We assumed a 10% variation in the transistor transconductance as the failure criteria. About 1000 seconds of stress were necessary to reach this degradation level.

2.3. Experimental Results

2.3.1. Core NMOSFETs

Fig. 2.1 shows the I_{ds}-V_{gs} curves (V_{ds} = 20 mV) for two devices which were irradiated up to 136 Mrad(SiO_2) in different bias conditions, V_{gs} = 0 V and V_{gs} = V_{dd}, and then subsequently stressed with 1000-s long CHC injection, and for a reference device which was subjected only to electrical stress.

Interestingly enough, the unirradiated sample degradation is the smallest one after the CHC stress, showing a post-CHC drop in the maximum drain current (ohmic region) of about 8 % and a threshold voltage shift of about 25 mV.

Previous works show that the samples irradiated at V_{gs} = V_{dd} display a larger radiation-induced maximum degradation (for our conditions this corresponds to about 1 Mrad) than the samples irradiated at V_{gs} = 0 V [Faccio05], [Gonella07]. At very high doses, the differences induced by the irradiation bias tend to vanish because of the rebound effect (generation of interface states) and, as shown in Figs. 2.1-2.3, the sample irradiated at V_{gs} = 0V has slightly larger degradation than the one at V_{gs} = V_{dd}. Nevertheless, V_{gs} = V_{dd} remains the worst-case bias condition, since it has the highest probability of causing circuit failure, due to threshold voltage shift and leakage current around 1 Mrad(SiO_2) [Faccio05], [Gonella07]. Both at 1 and 136 Mrad(SiO_2) this condition produces the highest accumulation of trapped charge and interface states in the STI as well as in the gate oxide, even though these two contributions may

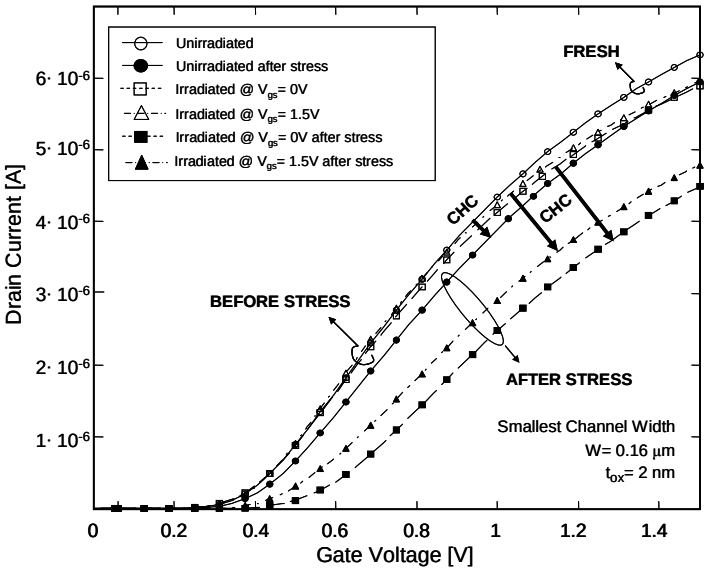


Fig. 2.1 I_{ds}-V_{gs} curves of NMOSFETs (W/L = 0.16 µm / 0.12 µm, V_{ds} = 20 mV) unirradiated and irradiated up to 136 Mrad(SiO_2) at different bias conditions, and subsequently stressed with CHC injection (1000 s at V_{gs} = 2 V and V_{ds} = 2.2 V).

compensate differently as a function of dose and irradiation bias.

After CHC stress we found that the larger the irradiation bias the smaller the subsequent CHC-induced degradation. The sample irradiated at $V_{gs} = V_{dd}$ displays a drop of 20% of drain current in the ohmic region (post-CHC I_{ds} over post-rad I_{ds}) and a threshold voltage shift of 100 mV. In the case of the device irradiated at V_{gs} = 0 V we found a drop of 25% of drain current and 180 mV threshold voltage shift.

This effect is present especially in devices with small channel width (W < 0.48 µm), as shown in Fig. 2.2. Regardless of the transistor geometry and irradiation bias, ΔV_{th} follows a power-law of the form $\Delta V_{th} = A \cdot (T_{stress})^B$, where A and B are fitting parameters. For these devices, the exponent B is independent of the channel width and is about 0.5 for irradiated samples and 0.75 for unirradiated ones.

For small-width irradiated MOSFETs (W < 0.48 µm) the pre-factor A increases for decreasing bias during irradiation, ranging from $0.25 \cdot 10^{-3}$ at V_{gs} = 1.5 V to $7 \cdot 10^{-3}$ at V_{gs} = 0 V. For unirradiated devices, the pre-factor A increases with channel width, showing a clear geometry dependence: the narrower the transistor the smaller the stress-induced degradation. The unirradiated sample with W = 0.16 µm does not show any variation with respect to the pre-stress value in threshold voltage until about 180 s,

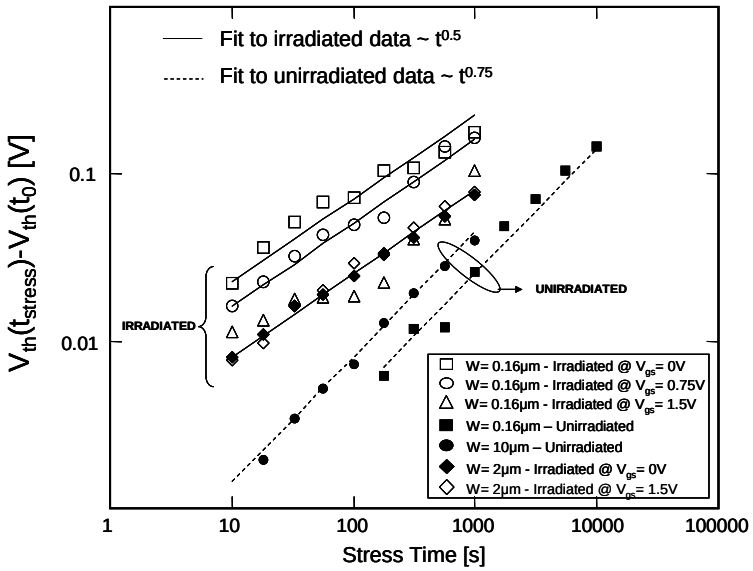


Fig. 2.2 Threshold voltage variation as a function of stress time (at V_{gs} = 2 V and V_{ds} = 2.2 V) for unirradiated devices (W = 0.16 µm and 10 µm), and for irradiated devices (W = 0.16 µm and 2 µm) in different bias condition during irradiation.

while the V_{th} of the larger one starts degrading immediately at the beginning of the stress.

Fig. 2.3 displays the sub-threshold region of the same devices of Fig. 2.1. The curves relative to irradiated samples before stress are not reported because they feature only slight differences with unirradiated one. This is because at high doses the interplay between positive trapped charge and interfacial traps especially in the STIs causes the devices to recover the variation of the threshold voltage (rebound effect) as found before for the same technology [Faccio05], [Gonella07].

As shown, all transistors feature a threshold voltage shift to more positive values after the CHC stress. Yet, ΔV_{th} is more pronounced in the device irradiated at V_{gs} = 0 V due to an increased sub-threshold swing (about 15 mV/decade more than before the stress). Fig. 2.4 reports in detail the variation of the sub-threshold swing as a function of stress time for the devices with W = 0.16 µm. While the unirradiated device obviously starts from zero degradation, the irradiated samples have an initial sub-V_{th} swing degradation of about 5 mV/decade due to radiation. In the first phase of the CHC stress the sub-V_{th} swing does not appreciably change for the sample irradiated at V_{gs} = 1.5 V and for the unirradiated sample. After 350 s and about 1000 s respectively,

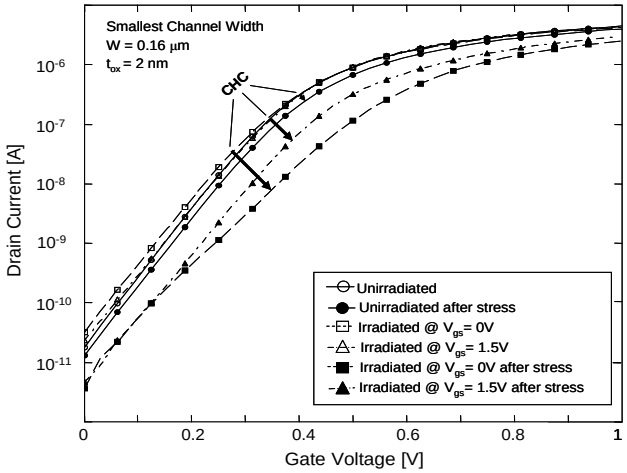


Fig. 2.3 Sub-threshold region of the same NMOSFETs of Fig. 1.

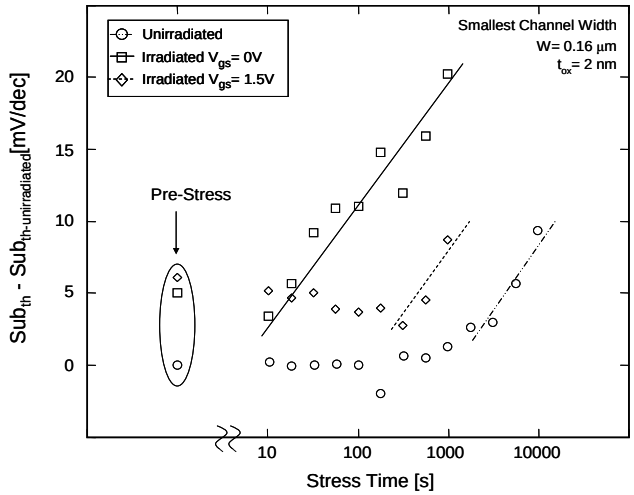


Fig. 2.4 Evolution of sub-threshold swing as a function of stress time (at V_{gs} = 2 V and V_{ds} = 2.2 V) for an unirradiated sample and two devices irradiated in different bias conditions (W = 0.16 μm).

the sub-V_{th} swing degrades at the same rate in the two devices. In contrast, the swing increases immediately from the stress beginning in the device previously irradiated at V_{gs} = 0 V.

The evolution of the transconductance peak during stresses is strongly affected by irradiation as well (Fig. 2.5). Indeed, after 1000 s of stress the g_m drop reaches 25-30 % in the irradiated samples, and only 10 % in the unirradiated device. While the

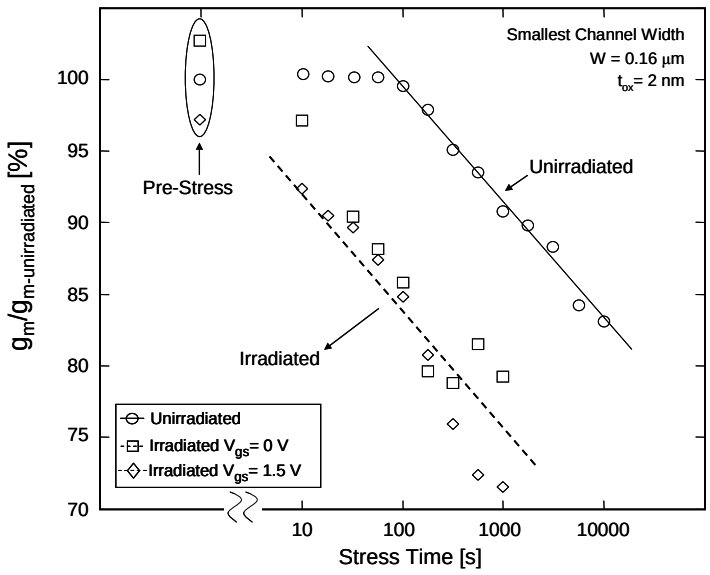


Fig. 2.5 Evolution of the transconductance peak (V_{ds} = 20 mV) as a function of stress time (at V_{gs} = 2 V and V_{ds} = 2.2 V) for an unirradiated device and two devices irradiated in different bias conditions (W = 0.16 μm).

unirradiated device does not show any appreciable g_m drop up to 100 s of stress, the transconductance in the irradiated samples has already dropped by about 15 % after the same amount of time. Beyond 100 s all curves show the same degradation rate until the end of the stress.

The average values of bulk and drain currents (normalized to unirradiated devices) during electrical stresses are reported in Table 2.1 for the devices with W = 0.16 μm. The device irradiated with V_{gs} = V_{dd} exhibits a larger drain current than the one irradiated with the gate grounded. However, the bulk current shows an opposite trend.

Devices	Normalized Bulk Current	Normalized Drain Current
Unirradiated	1	1
Irradiated @ V_{gs} = 0 V	1.3	1.13
Irradiated @ V_{gs} = 1.5 V	1.2	1.19

Table 2.1: Measured average bulk and drain currents during CHC stress at stress voltage (V_{gs}= 2 V, V_{ds} = 2.2 V) for minimum-size core NMOSFETs (W/L = 0.16 μm / 0.12 μm).

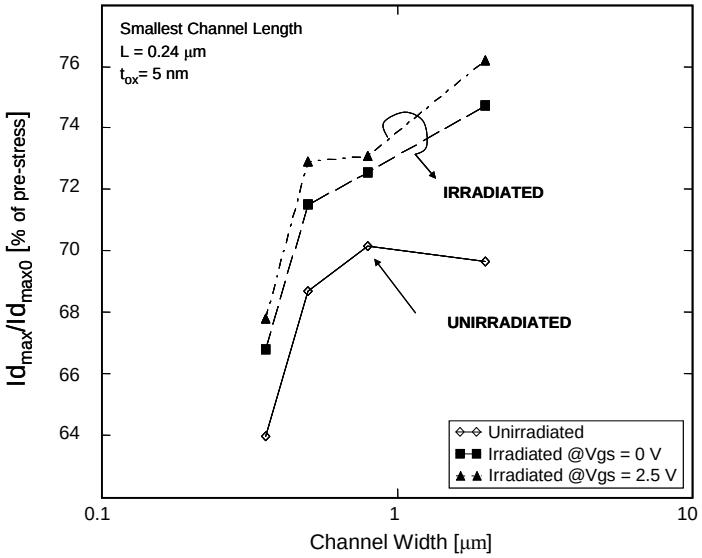


Fig. 2.6 Variation of the maximum drain current (V_{gs} = 2.5 V V_{ds} = 20 mV) with respect to the pre-stress values for irradiated and unirradiated I/O NMOSFETs (L = 0.24 μm).

2.3.2. I/O NMOSFETs

In irradiated devices, transconductance and drain current in the ohmic region monotonically degrade by up to 20-25 % during CHC stress performed after X-ray exposure, and more, up to 30-40 %, in unirradiated samples. Fig. 2.6 reports the percentage variation of the maximum drain current in the ohmic region as a function of channel width after electrical stress for the devices with the smallest channel length (L = 0.24 μm): there is a remarkable degradation reduction in irradiated transistors compared to unirradiated ones. The substrate current during CHC stress correlates with the observed parameter degradation at the end of the stress. In particular I_{sub} is 30 % larger in unirradiated devices. Irradiation bias conditions affect V_{th}, gm, and sub-threshold slope during subsequent CHC stresses only for a few per cent.

2.4. Physical Simulations

To gain more insight into these phenomena, we performed TCAD physical device simulations with the ISE TCAD DESSIS simulator. We do not have precise technological information about our devices, so we based our simulations on standard

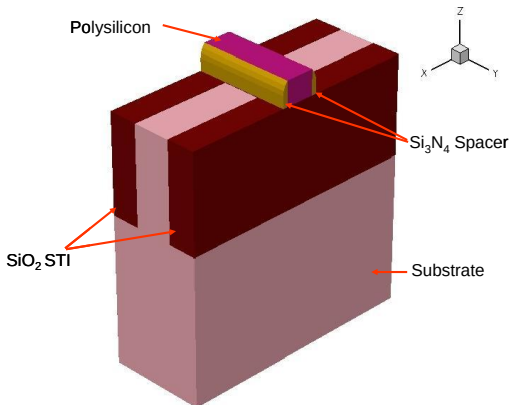


Fig. 2.7 3-D structure of the NMOSFET used in our simulations (W = 0.16 µm L = 0.12 µm).

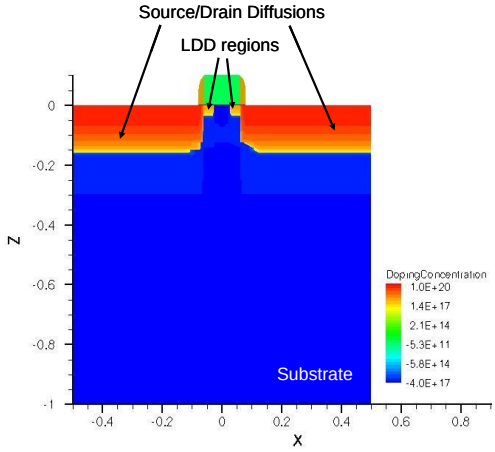


Fig. 2.8 Doping profiles of the NMOSFET depicted in Fig. 7.

values available in the literature for 130-nm technologies [Sze01], [ITRS].

The full 3-D physical structure of the device used in these simulations is illustrated in Fig. 2.7. Lateral spacers and STI were inserted using Si_3N_4 and SiO_2, respectively. The gate oxide was SiO_2 with a thickness of 2 nm.

For the gate contact we used n-type polysilicon with a thickness of 100 nm. The p-type substrate was uniformly doped with $4 \cdot 10^{17}$ cm^{-3} boron ions. The n-type arsenic-doped source and drain diffusions were 100-nm deep and with a Gaussian profile with values ranging from $1 \cdot 10^{20}$ As cm^{-3}, at the silicon-oxide interface, to 10^{17} As cm^{-3} at

the diffusion ending, as shown in Fig. 2.8. Arsenic-doped LDD regions were included with a depth of 50 nm and with a Gaussian profile ranging from $1 \cdot 10^{18}$ to $1.6 \cdot 10^{17}$ As cm^{-3}. All simulations were performed using hydrodynamic model with high-field saturation and mobility degradation models including doping-dependence and carrier-carrier scattering.

2.4.1. Simulated Irradiation

We tried to qualitatively fit our experimental data (in particular the I_{ds}-V_{gs} curves), obtaining trapped charge and interface state densities consistent with previous reports [Barnaby06], [Turowsky05]. Unfortunately, since we do not have the exact technological information (doping profiles, junction depth and so on), our fits are not optimal. Nevertheless, our simulations qualitatively reproduce our experimental data at different doses. We modeled the shift of threshold voltage towards more negative values with positive trapped charge in the lateral STIs. In order to reproduce the irradiation bias dependence at a given dose, we introduced a variable volumetric density of charge in the STI oxide ranging from $1 \cdot 10^{16}$ cm^{-3} to $4 \cdot 10^{16}$ cm^{-3}.

On the other hand, to reproduce the opposite shift of the threshold voltage, we inserted acceptor-like traps at the silicon-STI interfaces [McWhorter88]. In the same way, in order to reproduce the irradiation bias dependence at a given dose, the areal density was varied from $1 \cdot 10^{11}$ cm^{-2} to $5.5 \cdot 10^{11}$ cm^{-2}. These values were adjusted in order to qualitatively reproduce the growth and the subsequent recovery of the leakage current and threshold voltage we have found in our measurement.

Fig. 2.9 shows the I_{ds}-V_{gs} in linear region (drain contact kept at 20 mV), resulting from our simulations at different TID and irradiation bias: (i) before irradiation, (ii) with only fixed charge trapping in the STI (corresponding to 3Mrad(SiO_2)), where the negative threshold voltage shift peaked), and (iii) after the creation of a significant number of interface states in the same region, which mimic the rebound effect after 136 Mrad(SiO_2) [Faccio05]. To understand the impact of subsequent channel hot carrier stresses, we focused on the simulations that reproduce the effects of 136 Mrad(SiO_2) (i.e., the dose after which the stresses have been carried out) in different bias conditions.

2.4.2. Simulated CHC Stress

Simulated electrical stress was performed using the DESSIS degradation model with avalanche generation due to impact ionization at drain. The initial trap concentration at the silicon-gate oxide interface was $1 \cdot 10^{8}$ cm^{-2} and, in the process of degradation, was

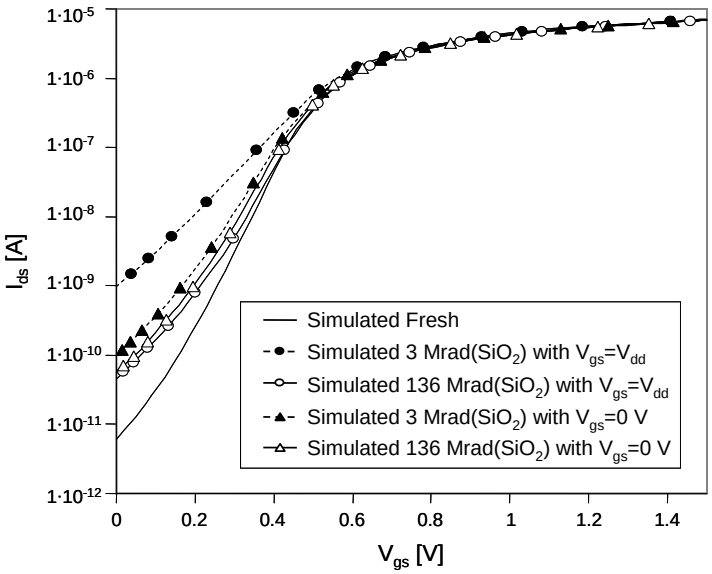


Fig. 2.9 Simulated I_{ds}-V_{gs} curves (V_{ds} = 20 mV) for different amounts of trapped charge and bulk-STI interface traps for a minimum size NMOSFET (W = 0.16 µm L = 0.12 µm).

increased up to $1 \cdot 10^{12}$ cm^{-2}

Firstly we investigated the magnitude of the bulk current generated during electrical stress which is the main indicator of impact ionization at drain. The larger the bulk current during electrical stress, the heavier the degradation of the device at the end of the stress. Table 2.2 shows the normalized values of simulated bulk and drain currents during stress (simulated in the same experimental bias conditions), for different amounts of positive trapped charge and interface traps. As in our experiments, the device with the largest amount of radiation-induced trapped charge and interface states shows the smallest bulk current during stress. We can conclude that the presence of positive charge in the lateral STI and traps in the bulk-STI interfaces modifies the device response to electrical stress.

Fig. 2.10 shows the impact ionization at the drain along the channel width obtained by cutting the 3-D structure along the y-z plane at the point x of maximum ionization as depicted in Fig. 2.10a (see Fig. 2.7 for the axis orientation). In Fig. 2.10b the profile of impact ionization for an unirradiated device is reported, and Fig. 2.10c shows the difference between the ionization profiles of the device irradiated with the gate grounded and the unirradiated one. Simulations show that the impact ionization is more pronounced in irradiated devices (Fig. 2.10c) with an enhancement at the bulk-

Simulation	Charge trapped [cm^{-3}]	Interface Traps [cm^{-2}]	Normalized Bulk Current	Normalized Drain Current
Unirradiated	0	0	1	1
Irradiated @ V_{gs} = 0 V	$2 \cdot 10^{16}$	$1 \cdot 10^{11}$	1.224	1.41
Irradiated @ V_{gs} = 1.5 V	$4 \cdot 10^{16}$	$5.5 \cdot 10^{11}$	1.104	1.38

Table 2.2: Normalized bulk and drain currents during simulated CHC stress (at stress voltages V_{gs} = 2 V and V_{ds} = 2.2 V) for minimum-size core NMOSFETs (W/L = 0.16 µm / 0.12 µm)

STI interfaces (Fig. 2.10b).

Fig. 2.11 displays the differences between the devices irradiated at $V_{gs} = V_{dd}$ and the sample irradiated at V_{gs} = 0V (simulated using a different amount of trapped charge and interface states). The electron density and electric field cross sections along the channel width of the device at the point of maximum ionization (Fig. 2.10a) are shown (sample irradiated at $V_{gs} = V_{dd}$ minus sample irradiated at V_{gs} = 0V).

Fig. 2.11a shows that the electric field is larger in the sample irradiated at $V_{gs} = V_{dd}$ (especially at the edges); whereas Fig. 2.11b shows that electron density is much lower at the edges and slightly larger in the center in the same sample. The net result obtained combining electric field and electron density is an increased bulk current in the device irradiated at V_{gs} = 0 V.

2.5. Discussion

2.5.1. Core MOSFETs

As we have shown in the previous sections, the degradation of irradiated core devices under CHC injections is different from that of unirradiated samples. The devices which were exposed to X-rays degrade faster than those that were not (Figs. 2.1-2.5). Furthermore, the bias applied during the irradiation plays an important role not only on the parameters degradation during the exposure, but also on the outcome of subsequent accelerated tests.

Interestingly enough, the bias condition usually considered the worst case during irradiation [Shaneyfelt90], generates the smallest degradation during CHC accelerated

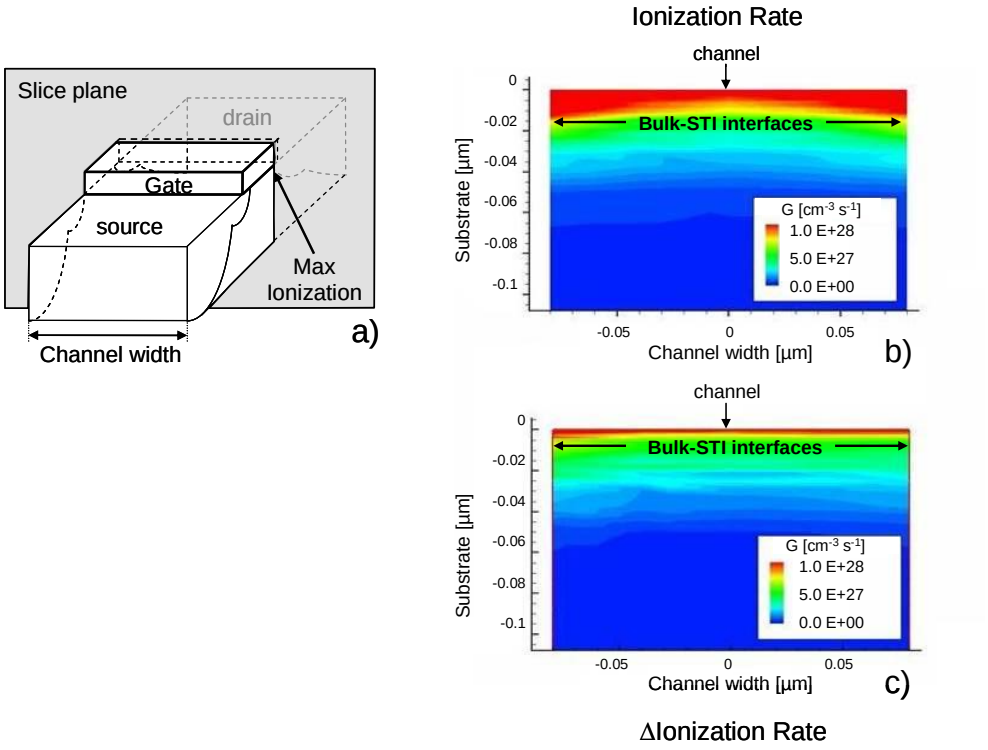


Fig. 2.10 Cross section of the silicon substrate below the gate oxide along the channel width at the point of maximum ionization along the channel length (at stress voltages V_{gs} = 2 V and V_{ds} = 2.2 V). The 0 in the x- and y- axes is the center of the channel, and the channel gate-oxide interface, respectively. (a) View of the slice plane (not to scale) (b) simulations of impact ionization rate G (during CHC injection) due to high energy electrons for an unirradiated device (W/L = 0.16 / 0.12 µm); (c) difference between ionization rate profiles of irradiated and unirradiated devices. More impact ionization occurs in the irradiated device, especially at the bulk-STI interfaces.

tests. In the case of NMOSFETs, it is well known that the larger the (positive) bias applied during irradiation, the bigger the degradation. This happens because of the larger electric field for increasing gate voltage.

When performing the irradiation at V_{gs} = V_{dd}, much more positive charge is trapped and more interface states are created in the STI, as well as in the gate oxide, than at V_{gs} = 0 V due to the larger electric field [Schwank02]. Small-width samples (W < ~ 0.48 µm) are the most affected, since the fixed charge and traps in the lateral isolation can alter the characteristics of the drawn transistor, in addition to the lateral parasitic

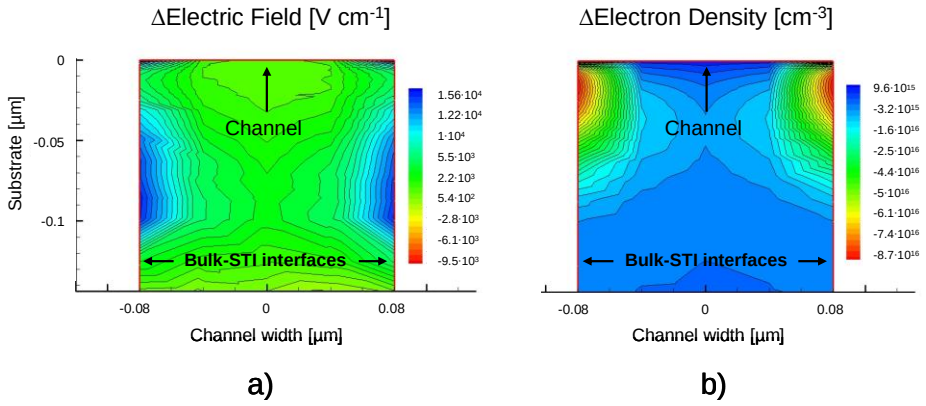


Fig. 2.11 Simulated differences in electric field and electron density (at stress voltages V_{gs} = 2 V and V_{ds} = 2.2 V) between a device irradiated at V_{gs} = V_{dd} and one irradiated at V_{gs} = 0 V (different amounts of trapped charge and interface states are used to model the two samples) slicing the 3-D structure as in Fig. 3.10a. Negative areas mean a larger value in the device irradiated at V_{gs} = 0 V. Less impact ionization occurs in the device irradiated at V_{gs} = V_{dd} in spite of the larger electric field, because the electron density is smaller in the high-field regions.

ones.

CHC injections degrade the device DC parameters by creating defects in the gate oxide in the regions surrounding the drain [Groes99], [Cretu02], as shown in Figs 2.1-2.6. The sub-threshold swing and the transconductance behavior (Figs. 2.4-2.5) suggest that irradiation leads to either or both of two mechanisms [Kaval96] which may alter the degradation during CHC stress:

1) defect generation
2) different spatial distribution of the interface traps

These two phenomena are more pronounced in devices irradiated at V_{gs} = 0 V relative to those irradiated at V_{gs} = V_{dd}. Our simulations give credit to both 1) and 2). Indeed, the impact ionization is larger in irradiated devices as compared to unirradiated ones (Fig. 2.10c), due to the higher electric field at the bulk-STI edges induced by the unscreened positive trapped charge in the STIs. A large impact ionization leads to a heavier injection of energetic carriers into the gate oxide, and, consequently, to a faster defect generation during accelerated CHC stresses. There is also experimental evidence supporting this claim: the substrate current I_{sub}, a good monitor of the amount of impact ionization taking place in a device, correlates well with the degradation level after the electrical stresses, as shown in section 2.3.

Concerning the impact of the irradiation bias on the stress-induced degradation, the explanation is less straightforward. Even though the electric field which produces the hot carriers is higher in the device irradiated at $V_{gs} = V_{dd}$ (Fig. 2.11a) due to a higher concentration of radiation-induced charge in the STIs, the impact ionization and bulk current are larger in the one irradiated at $V_{gs} = 0$ V, because of the different carrier distribution in the high-field region close to the bulk-STI interfaces at the point of maximum ionization. Comparing Figs. 2.11a and 2.11b, we notice that the reduction in electron density offsets the increase in electric field, in such a way that the overall impact ionization is reduced as compared to the device irradiated at $V_{gs} = 0$ V. Thus the different distributions of radiation-induced effects in the STIs (positive trapped charge and interface traps) due to a different bias during irradiation can locally modify, during subsequent CHC stress, the distribution of the carrier density in the channel near bulk-STI interfaces, causing the reported behavior.

The second hypothesis (alteration in the spatial distribution of interface traps) is also supported by both experimental evidence and simulations. Whereas the behavior of the output resistance during electrical stresses does not depend on the irradiation bias, suggesting that the profile of the defects along the channel length is always the same regardless of irradiation dose and bias, the same is not true for the trap density profile along the channel width. An enhanced defect generation rate takes place especially at the STI-bulk interfaces as displayed in our simulations (Figs. 2.10-2.11), and as proved by the fact that in wide MOSFETs the irradiation bias has a minor impact on the outcome of subsequent electrical stresses (Fig. 2.2).

We must remark that an enhanced degradation with CHC is observed in small-width (unirradiated) devices, as shown in Fig. 2.2. This effect is not fully understood and has been tentatively attributed to enhanced defect generation near the isolation edge due to mechanical stress [Ishimaru99], [Li03], so spatial non-uniformity of stress-induced defects along the channel width are present even in unirradiated oxides.

2.5.2. I/O MOSFETs

Contrary to core MOSFETs, irradiated devices exhibit a smaller degradation during CHC stress than unirradiated samples and the experimental results on I/O MOSFETs show little dependence of the stress outcome on the channel width and irradiation bias conditions. This is due to a decreased hot carrier generation after irradiation. Indeed, in the case of small-width I/O MOSFETs the substrate current is 30 % larger in stressed unirradiated devices as compared to samples irradiated at $V_{gs} = V_{dd}$. Early work performed by J. D. McBrayer et al. [McBrayer85], [McBrayer87] with γ-rays on MOS transistors with much thicker gate oxide (33 nm) showed that for sufficiently high

doses, radiation damage completely overwhelms the effects of subsequent channel hot carrier stresses. This is not the case for our samples, which are degraded by channel hot carrier stresses even after they received 136 Mrad(SiO_2).

I/O MOSFETs differ from core devices because the thicker gate oxide used in the first ones is more subjected to TID damage, contrary to the ultra-thin dielectric used in the second ones. Radiation-induced trapped charge and interface states in the gate oxide reduce the fields in the device during subsequent electrical stresses, leading to the results shown in Fig. 2.6.

2.6. Conclusions

This chapter provides new insights into the behavior of deep-submicron CMOS transistors exposed to X rays and submitted to hot carrier injection.

Core devices (t_{ox} = 2.2 nm) irradiated in different bias conditions V_{gs} = 0 V and $V_{gs} = V_{dd}$ up to 136 Mrad(SiO_2) display a similar drain current drop after irradiation. However, after CHC stress the sample irradiated at $V_{gs} = V_{dd}$ displays a drain current drop of 20 % and V_{th}-shift of 100 mV and the drain current of the device irradiated at V_{gs} = 0 V drops of 25% with 180 mV of threshold voltage shift. As a consequence the worst case bias condition for irradiation ($V_{gs} = V_{dd}$) leads to a lower degradation after CHC stress. In contrast, the irradiation best case (V_{gs} = 0 V) leads to a larger drop after CHC stress. It is important to note that only narrow transistors show this behaviour confirming that the lateral isolations play an important role on this mechanism.

In contrast, irradiated I/O samples (t_{ox} = 5 nm) exhibit a smaller degradation during CHC stress than unirradiated ones showing a little irradiation-bias dependence. The thicker gate oxide in this case are more sensitive to radiation and the amount of traps generated during irradiation increases the barrier felt by hot electrons reducing the degradation induced by CHC stress in irradiated devices.

TCAD simulations confirm that the radiation-induced trapped charge at the edges of the transistor, that is different for the different bias conditions, influence the carrier density, the electric field and then the overall impact ionization as explained in 2.5.1.

Chapter 3

Channel Hot Carrier Degradation in X-ray Irradiated Enclosed Layout Transistors

This chapter is focused on ELTs degradation due to both radiation and CHC stress, highlighting the differences with conventional open layout transistors as reported in the previous chapter. In particular the influence of X rays, device geometry, stress temperature, and gate oxide thickness on CHC degradation kinetic is studied through experimental data and 3D device physical simulations.

3.1. Introduction

The resilience of electronics to very high doses is of great interest for the high energy physics community. To ensure reliability in such environments, some critical applications might need Hardness-By-Design (HBD) solutions, such as Enclosed Layout Transistors (ELT) and guard rings [Snoeys00].

Although HBD solutions have some drawbacks in terms of power consumption, area, and costs, they permit one to eliminate radiation-induced edge effects due to charge trapping and interface states generation in the Shallow Trench Isolation (STI), the primary cause of concern in scaled technologies [Lacoe00].

For devices that need to operate for very long times in harsh environments, long term reliability must be considered in addition to radiation hardness. Interplay between radiation effects and the aging of devices is in fact possible. For instance, it has been shown that heavy ion strikes reduce gate oxide time-to-breakdown and may alter the parametric degradation of MOSFETs [Cester03], [Choi02].

Comparatively less is known about the interplay between radiation and channel hot carrier degradation, which is particularly important in NMOSFETs, because the impact ionization rate is larger than in PMOSFETs at the same electric field.

3.2. Experimental and Devices

The devices used in our experiments were n-channel enclosed layout transistors manufactured by a commercial foundry in a 130-nm CMOS process. The devices belong to two groups:

- core ELT: t_{ox} = 2.2 nm, V_{dd} = 1.5 V, L = 0.12 µm, W/L ~ 17
- I/O ELT: t_{ox} = 5.2 nm, V_{dd} = 2.5 V, L = 0.26 µm, W/L ~ 15.

The samples were first irradiated and then submitted to accelerated electrical stresses. Irradiation was performed at CERN with a 10-KeV X-ray system, keeping the samples biased in the worst case condition ($V_{gs} = V_{dd}$, other terminals grounded).

CHC stresses were performed on irradiated and unirradiated devices keeping the drain voltage 50 % higher than nominal V_{dd}. We carried out the CHC stresses with the drain contact inside, since, as found by Mayer et al. [Mayer04], this is the worst-case condition.

The constant gate voltage has been chosen and adjusted in all samples in order to reach maximum bulk current generated by impact ionization at the drain (at the beginning of the stress), while source and bulk terminals were grounded. This high gate and drain bias are used to accelerate the degradation experienced by the device during its operating life [Groes99].

We periodically interrupted the electrical stresses to measure I_{ds}-V_{gs} and I_{ds}-V_{ds} curves, in order to extract the main parameters, such as threshold voltage (extracted by linearly fitting the I_{ds}-V_{gs} at the point of maximum transconductance), transconductance, and sub-threshold swing.

Temperature effects on electrical stresses were studied at 27 °C and 80 °C, using a thermally-controlled chuck. Annealing was performed with a temperature-controlled oven.

3.3. Experimental Results

3.3.1. I/O ELTs

Fig. 3.1 features the linear drain current (V_{ds} at 20 mV) as a function of gate voltage before irradiation (fresh), after X-ray exposure (TID = 136 Mrad(SiO_2)), and after several steps of CHC injection (on the irradiated device) up to a total duration of 10^4 s (V_{gs} at maximum bulk current, V_{ds} = 3.75 V).

Defects generated in the 5-nm gate oxide by the irradiation caused a threshold voltage shift towards more positive V_{gs} values of about 150 mV and a drop of the drain current (V_{gs} = 2.5 V) of about 15 %.

The irradiated sample was then stressed for 10^4 s, showing a large degradation in both threshold voltage and drain current as well as sub-threshold swing, as depicted in Fig 3.2. In fact Fig. 3.2 reports the linear transconductance for the same transistor as in Fig. 3.1, after irradiation and subsequent CHC stress. The g_m-peak decreases about 20 % due to TID and 25 % due to CHC stress. Furthermore the decrease in the g_m-rising-slope indicates that the sub-threshold swing is affected by both kinds of degradation, ranging from about 80 to 170 mV/decade.

Fig. 3.3 displays the V_{th} shift as a function of stress time for an unirradiated device and for two samples irradiated at different high doses (64 and 136 Mrad(SiO_2)). The

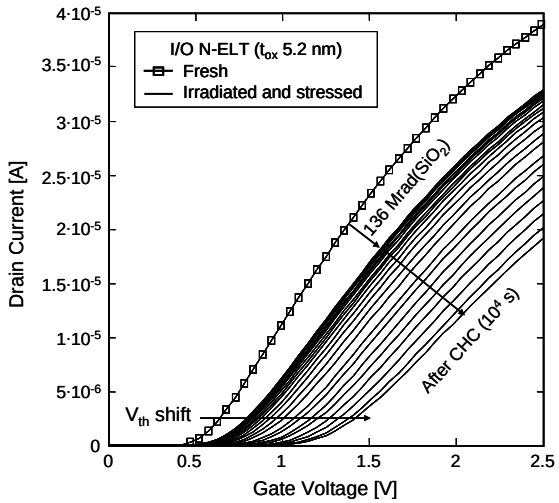


Fig. 3.1. Linear I_{ds}-V_{gs} (V_{ds} = 20 mV) before irradiation (fresh), after 136 Mrad(SiO_2), and after several CHC steps up to 10^4 s for an I/O sample. V_{th} shifts towards more positive values.

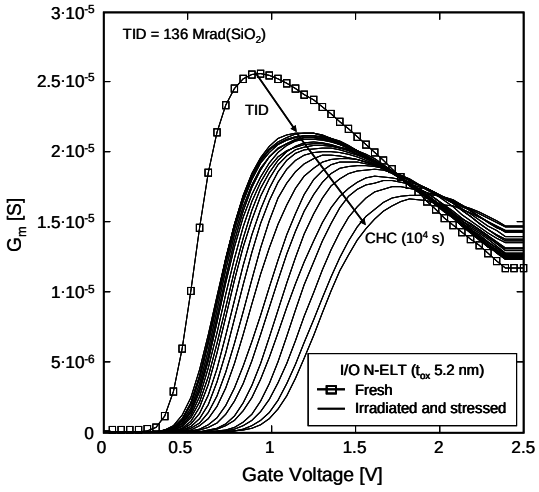


Fig. 3.2. Linear transconductance (V_{ds} = 20 mV) before irradiation (fresh), after 136 Mrad(SiO_2), and after several CHC steps up to 10^4 s for an I/O sample. The peak degrades monotonically, V_{th} shifts towards more positive values.

threshold voltage shift during the CHC stress is related to the unirradiated and unstressed transistor, in order to observe the combined effects of radiation and electrical stress. The degradation follows a power law of stress time. The unirradiated device features an exponent of about 0.75 up to 200 s then it decreases down to 0.4 for longer stress time, and finally tends to saturate toward the end of the stress. Contrary to the unirradiated transistor, the samples previously irradiated show a very low slope (< 0.2) up to 200 s, then the slope increases to 0.4 and all the curves rejoin.

After the high temperature annealing step, performed while keeping the devices unbiased for 2 hours at 300 °C, a large recovery appears especially in the irradiated devices: the improvement in V_{th} for the unirradiated sample is about 70 %, instead of 95 % for the irradiated ones. The V_{th} shift now related to the value immediately before the stress is reported in Fig. 3.4, where it is compared with other stresses performed at higher temperature. Both TID and temperature improve the device response to Hot Carrier Injection (HCI). In fact the V_{th} evolution of the unirradiated device stressed at 25 °C (filled squares) shows the largest degradation, even though the slope is close to 0.75 in all conditions. Data related to irradiated open layout transistors (empty diamonds) are also reported featuring a lower slope ~ 0.5 typical of CHC experiments.

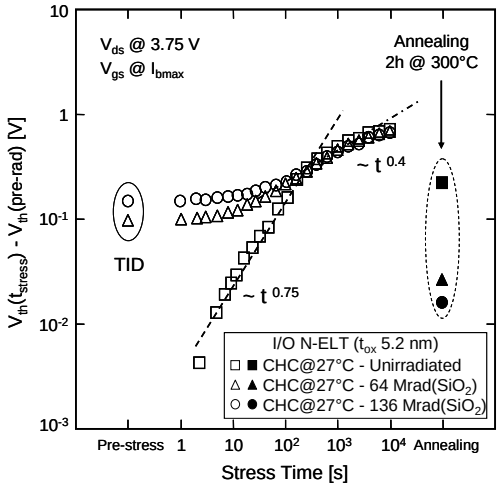


Fig. 3.3. Evolution of the V_{th} shift during CHC stress and after a high temperature annealing step for I/O devices unirradiated and previously irradiated up to different TID.

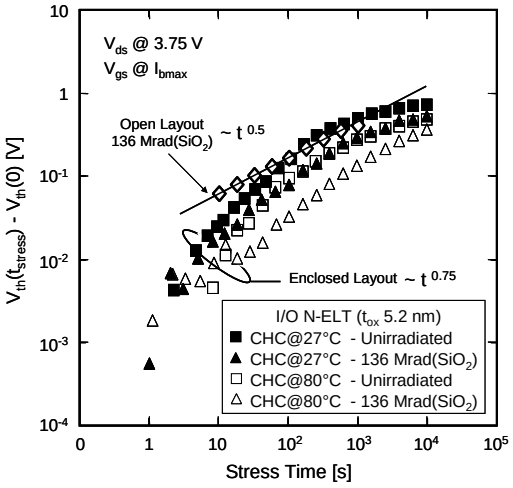


Fig. 3.4. Evolution of the V_{th} shift during CHC stress performed at 25 °C and 80 °C for I/O devices unirradiated and previously irradiated up to 136 Mrad(SiO_2). The degradation for an irradiated open layout transistor is also reported.

3.3.2. Core ELTs

Fig. 3.5 shows the V_{th} degradation in core transistors as in Fig. 3.4. Irradiation in these devices does not impact the evolution of the CHC stress, contrary to I/O samples (Fig. 3.4), up to very high doses.

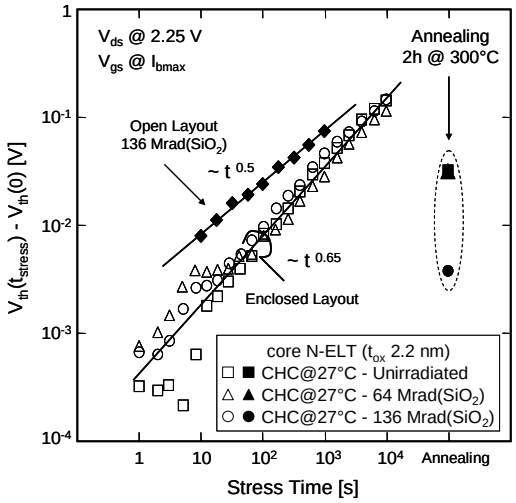


Fig. 3.5. Evolution of the V_{th} shift during CHC stress and after a high temperature annealing step for core devices unirradiated and previously irradiated up to different TID. The degradation for an irradiated open layout transistor is also reported.

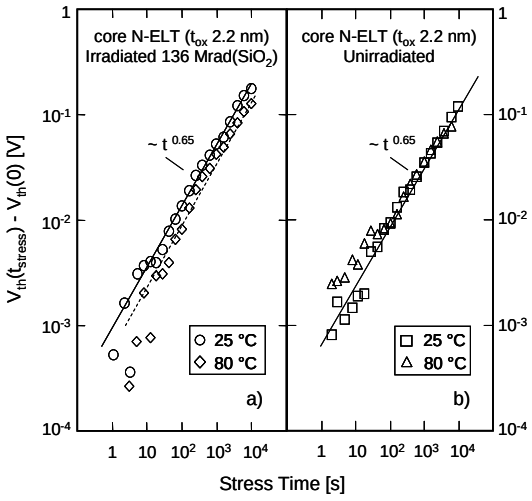


Fig. 3.6. Degradation of threshold voltage during CHC stress as a function of stress temperature for irradiated (left side) and unirradiated (right side) core ELTs.

The data related to unirradiated and irradiated devices overlap each other, with the same slope of about 0.65, and without saturation at the end of the stress. It is interesting to note that, also in this case, the slope is different and larger than the one exhibited by conventional OLT (about 0.5), as shown in the same figure with filled

diamonds. Here again (compare Fig. 3.3), the sample irradiated up to 136 Mrad(SiO_2) and then stressed exhibits the largest recovery after high temperature annealing step. Moreover for the chosen stress voltage the core ELTs degrade less than the OLT ones especially at early times independently from previous radiation (Fig. 3.5). This comparison is reasonable because both I/O and core open layout samples were provided by the same manufacturer with the same oxide thickness.

Fig. 3.6 reports the influence of stress temperature on CHC degradation of irradiated (left side) and unirradiated (right side) core devices. Similarly to I/O samples, the accelerated electrical stress performed in irradiated transistor at 80 °C produces less degradation (only a slight percentage reduction compared to thicker I/O samples) with no change in slope (~ 0.65). The unirradiated ELT sample stressed at 25 °C shows minor differences compared to the one stressed at 80 °C, maintaining the same slope ~ 0.65.

Fig. 3.7 summarizes the post-stress degradation of the linear drain current (V_{ds} at 20 mV) as a function of stress temperature for irradiated and unirradiated core and I/O ELT devices. Both stress temperature and TID reduce the degradation of about 10 % in I/O samples. Conversely, irradiation in core transistors has no influence at 25 °C and causes a slight CHC degradation decrease at 80 °C. High temperature lowers the CHC degradation by 4 % and 6 % in irradiated and unirradiated devices, respectively.

Fig. 3.8 shows the degradation of the threshold voltage during stress for unirradiated devices with different channel lengths. The drain voltage during these stresses was higher (V_{ds} = 2.7 V) than previously (V_{ds} = 2.25 V), in order to quicken the degradation of long-channel MOSFETs, which is quite time consuming.

Contrary to those in Fig. 3.5, these higher stress voltages lead to a visible saturation of the degradation at the end of the stress for I/O transistors. Moreover, as expected, the longer the channel the smaller the CHC degradation for a given stress voltage. The degradation slope does not depend on channel length. In fact every sample exhibits the same slope of about 0.75 before the saturation (t_{stress} < 200 s); however comparing Fig. 3.5 and 3.8 the slope is larger in the samples stressed with higher drain voltage.

3.4. Discussion

It is well known that radiation and channel hot carriers degrade MOSFETs due to generation of interface states and oxide charge trapping [Barnaby06], [Mayer04].

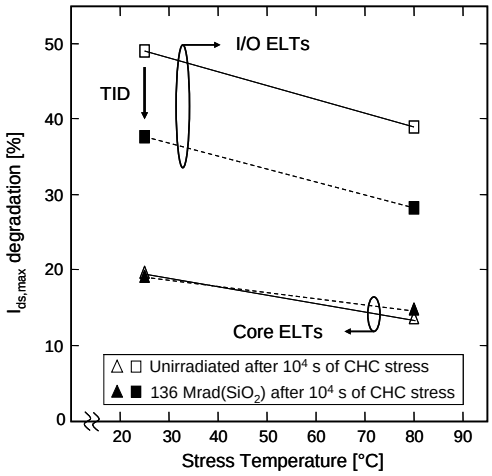


Fig. 3.7. Degradation of linear drain current (V_{gs}=V_{dd}, V_{ds} = 20 mV) after 10^4 s of CHC stress as a function of stress temperature for irradiated and unirradiated core and I/O ELTs.

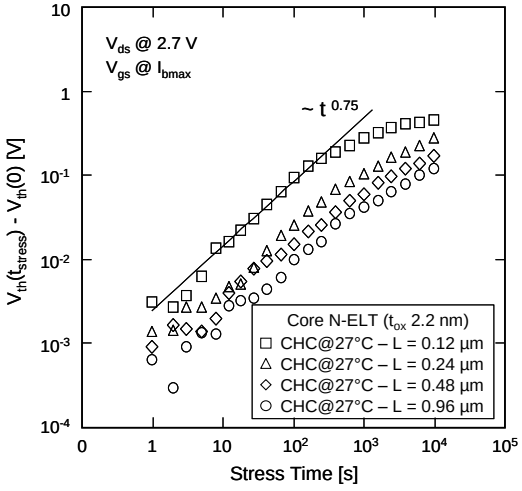


Fig. 3.8. Evolution of the V_{th} shift during CHC stress for unirradiated core devices with different channel length. The shorter the channel, the larger the degradation.

Concerning ultra-thin gate oxides, the threshold voltage shift due to fixed oxide charge is negligible due to the short tunneling distance, leaving the generation of interface states and border traps, uniformly after irradiation and close to the drain after CHC stresses, as the main degradation mechanism. Charge trapping is still an issue for

the thick oxides used for the lateral isolation (STI), but ELTs eliminate this problem altogether. As depicted in Figs. 3.1 and 3.2, radiation contributes to shift the V_{th} toward more positive V_{gs} values and, at the same time, reduces the drain current and the channel mobility as well. Accelerated CHC stresses performed on unirradiated or irradiated devices induce similar effects. These general considerations apply to open as well as to enclosed layout transistors, although with some peculiar features.

Under CHC stresses, ELT parametric degradation, in particular the time exponent, is different than that of OLTs, regardless of gate oxide thickness.

As we have shown in the previous section, with 2.2-nm gate oxide, the effects of radiation and subsequent CHC stress are mostly additive, meaning that the total degradation of a stressed, irradiated transistor is equal to the sum of the degradations of two transistors, one irradiated and the other one stressed. With 5.2-nm gate oxide, subtle interplay instead may exist.

3.4.1. CHC Degradation Slope

Concerning the degradation slope, the evolution of the threshold voltage shift in both core and I/O ELTs is quite similar (Figs. 3.3-3.8 display slope between 0.65 and 0.75). These values are quite high compared to our results on OLTs (Figs. 3.4 and 3.5), which feature slopes ~ 0.5, in agreement with data in the literature [Groes99], [Küflü04].

Recently Alam et al. [Alam07] proposed that CHC degradation could be explained by the same Reaction and Diffusion (R-D) theory applied to Negative Bias Temperature Instability (NBTI). The power-law degradation experienced by devices during accelerated tests could be modeled in terms of neutral hydrogen diffusion in the gate oxide, released from Si/SiO_2 interface after reaction with energetic carriers [Küflü06].

Concerning the defect creation mechanism, Pagey and coworkers [Pagey01] proposed that hydrogen is released as H^+ by energetic carriers at the poly-Si interface. Subsequently, H^+ driven by the positive gate bias drifts toward the oxide/channel interface and then reacts with Si-H bonds through $Si\text{-}H + H^+ + e^- \rightarrow D + H_2$, where D is a dangling bond. Moreover they found that the direct depassivation $Si\text{-}H + H^+ \rightarrow D + H_2$ is also possible and is probably the main mechanism during normal operative conditions (nominal voltages) [Pantelides07]. Regardless of the defect generation mechanism, the time exponent of the parametric degradation of the transistor is governed by the diffusion of H/H_2 from the Si/SiO_2 interface.

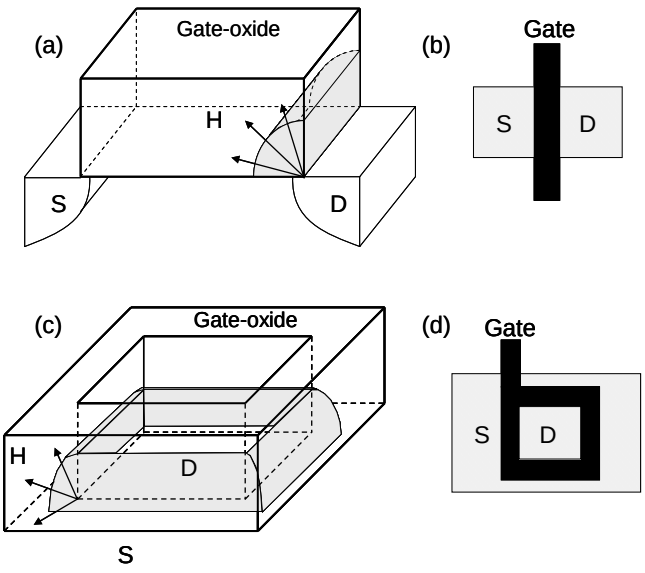


Fig. 3.9 (a) Diffusion of hydrogen in open layout transistors, adapted from [21] (not to scale). (b) Top view of a typical open layout transistor. (c) Diffusion of hydrogen in enclosed layout transistors. (d) Top view of an enclosed layout transistor.

The analytical model by Alam et al. based on 2-D diffusion provides a theoretical justification for the time-exponent 0.5 in OLTs (Fig. 3.9a) [Küflü04]. Later, it was also shown that in reduced cross section MOSFETs, this exponent could reach 0.75, due to H diffusion going from 2-D to 3-D in very small devices [Küflü06].

The difference in slope between open- and enclosed- layout transistors could be interpreted in similar terms. In fact, as depicted in Fig. 3.9d, enclosed devices have a square shape, leading to possible corner effects that can affect the geometry of H diffusion (Fig. 3.9c).

Fig. 3.10 illustrates the corner of the core ELT device where L is the channel length, d is the size of central drain diffusion, d' is the location where the corner cut, with length c, starts. For this technology the maximum channel length at the corner is $L_{max} \sim 1.4 \cdot L$, ranging from 0.12 µm (Region A in Fig. 3.10) to 0.17 µm (Region B in Fig. 3.10). In principle the regions in which the channel length is longer should be the least affected by CHC stresses, since the electric field is lower. Indeed, our previous analysis concerning the impact of channel length on CHC response (Fig. 3.8) shows that the device with L = 0.24 µm degrades before saturation (stress time < 10^3 s) 70 % less than the one with L = 0.12 µm. Of course, here we are comparing the degradation

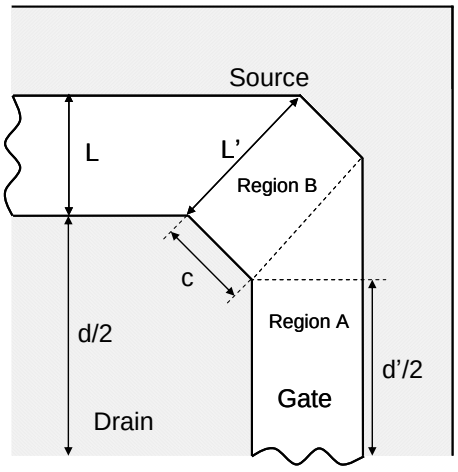


Fig. 3.10 Particular of the gate at the corner (not to scale).

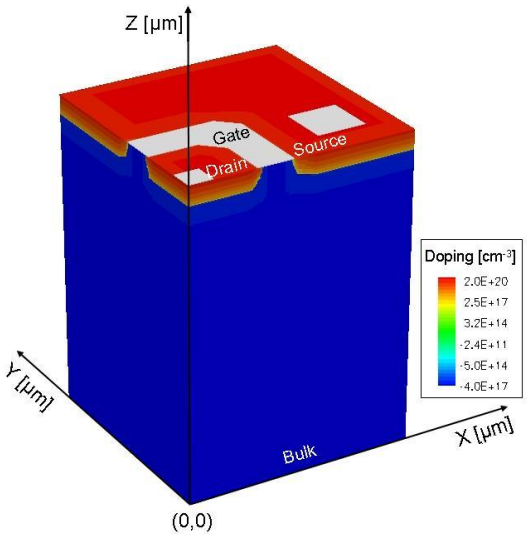


Fig. 3.11. Quarter of the whole ELT transistor used for the simulations.

of two devices with different channel lengths with the degradation of two parts of the same device featuring different gate lengths, so our considerations may not be conclusive.

Physical simulations performed with ISE-TCAD DESSIS simulator can help us gain more insight. Thanks to the symmetry of the device, we simulated only a quarter of the

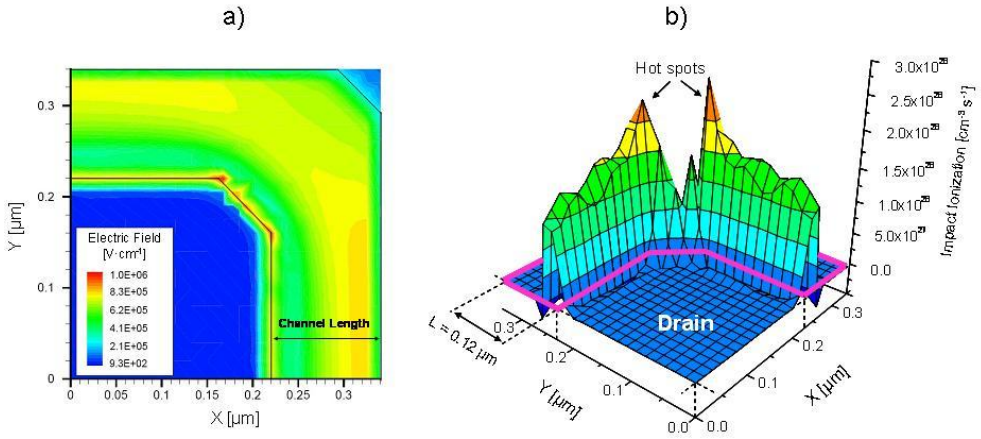


Fig. 3.12 a) Simulated electric field at silicon-oxide interface. The gate oxide field in the corners area is generally reduced by the cut. However this cut leads to two points where the field is enhanced. b) Impact ionization profile along the corner of an ELT transistor. Impact ionization peaks at the edges of the cut while dropping in the middle.

whole transistor as sketched in Fig. 3.11, thus obtaining a more detailed mesh. The device dimensions have been taken from the layout, but the exact doping profiles were not available and those used are approximated from data in the literature [ITRS].

Fig. 3.12a reports the electric field simulated at stress conditions (V_{ds} = 2.25 V, V_{gs} at maximum bulk current) at the oxide/silicon interface for the 3-D structure reported in Fig. 3.11. In the middle of the corner area (Region B in Fig. 3.10) the gate-oxide electric field is reduced compared to the lateral side (Region A). However the inner corner cut leads to two locations where the electric field peaks. As a consequence the non-uniformity of the electric field affects the hot carrier generation as depicted in Fig. 3.12b. The impact ionization peaks exactly at the edges of the cut, while dropping in the center of the corner. On the contrary, along the lateral sides (Region A) the impact ionization is quite uniform, like in a traditional open layout transistor. As a consequence a higher release of H is expected in the inner corner cut, which may then diffuse in three directions, shifting the time exponent from 0.5 toward 0.75, in agreement with [Küflü06].

Moreover we found that the shift is enhanced when the drain voltage grows. In order to explain that, we performed simulations with higher drain voltage (V_{ds} = 2.7 V and V_{gs} at maximum bulk current). We found that the impact ionization profile is

substantially the same as sketched in Fig. 3.12b, but with some differences in the profile, which may explain the rise in the parametric degradation exponent from 0.65 at V_{ds} = 2.25 V (Fig. 3.5) to 0.75 at V_{ds} = 2.7 V (Fig. 3.8). We can conclude that the higher the stress voltage, the higher the hydrogen release at the edges of the corner-cut.

3.4.2. Influence of the Gate-Oxide Thickness

The thickness of the gate oxide determines whether X-ray and CHC damages are simply additive or if there is a reduction of CHC degradation in irradiated devices.

Generally, thin gate oxides (e.g. core transistors) are more reliable than thick ones (e.g., I/O transistors) in terms of CHC degradation [Toyo90]. In fact this is true in our samples because after 10^4 s of stress the V_{th} shift of core-ELTs is smaller than I/O-ELTs. This comparison is meaningful since both types of transistors were stressed at V_{ds} 50 % larger than the nominal V_{dd} (assuming that the V_{dd} for one type of transistor is not specified more conservatively than for the other). For the stress time and voltages of Fig. 3.5, thin samples do not show any saturation differently from thick ones, where the degradation saturates at the end of the stress (compare Figs. 3.4 and 3.5). Saturation appears also in core transistors, when a larger bias is applied during the stress (Fig. 3.8), or a longer stress is carried out. In all cases, saturation occurs when ΔV_{th} > 100 mV. This saturated behavior has been attributed to a self-limiting effect, due to stress-induced defects (negatively charged during stress) that raise the energy barrier felt by hot electrons, pushing them away from the SiO_2-Si interface [Liang92].

A similar argument can be used to explain the reduced CHC degradation in the irradiated I/O devices (about 30 % less V_{th} shift compared to the unirradiated sample, Fig. 3.4). Indeed, the radiation-induced defects at 136 Mrad(SiO_2) may increase the potential barrier for injection of hot electrons in the gate oxide. On the contrary, with thin oxides, the same dose produces a smaller amount of defects [Saks86] which do not affect subsequent CHC stresses. In summary, previous radiation-induced defects influence the dynamics of the degradation in thick oxides (5 nm), but not in thin ones, at least at 25 °C.

3.4.3. Temperature Effects

High temperature during the CHC electrical stresses does not influence the slope of V_{th}-degradation as shown in Figs. 3.4 and 3.6, but contributes with previous radiation to limit the V_{th}-shift especially in I/O samples.

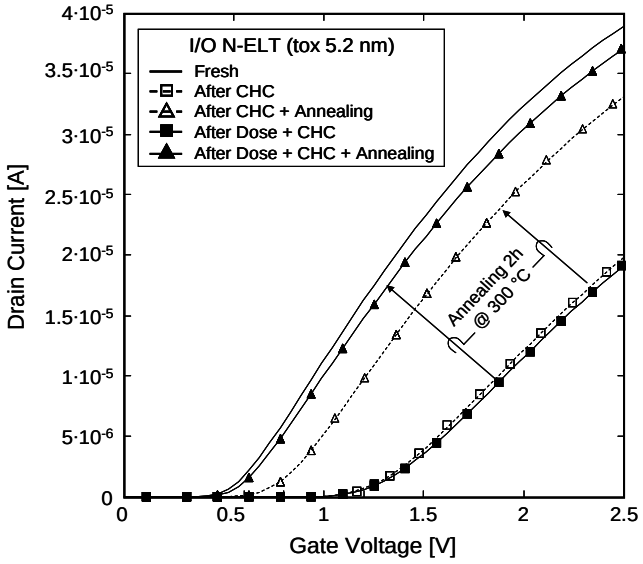


Fig. 3.13. Linear I_{ds}-V_{gs} (V_{ds} = 20 mV) of a fresh device, after 10^4 s of CHC stress, after 136 Mrad(SiO_2) and 10^4 s of CHC stress, and after a 2-h annealing step at 300 °C. Irradiated and stressed devices recover more than the ones only stressed.

It is known that the increase in temperature during CHC stress reduces the mobility of the carriers in the channel, and in the high field region. This effect is driven by a reduction in the mean free path and leads to less impact ionization and consequently less degradation at the drain region [Hsu84], [Chen05]. This is evident in Fig. 3.4 for I/O-ELTs, where the drain current degradation decreases for increasing stress temperature (and pre-stress TID). Similar data have been obtained also with core transistors (Fig. 3.7), even if the temperature dependence of CHC damage is slightly influenced by previous irradiation.

We performed a high temperature (HT) annealing step in order to recover the interfacial states generated from radiation and CHC stress, starting from the results obtained on the same 130-nm technology [Faccio05]. We kept the devices unbiased for two hours at 300 °C in a thermally controlled oven. The annealing results reported in Figs. 3.3, 3.5, and 3.13 give some preliminary interesting information about the interplay between damage produced by radiation and electrical stress. The linear drain current (V_{ds} = 20 mV) reported in Fig. 3.13 shows a different recovery after HT step

for irradiated and unirradiated stressed devices. In the irradiated ones, the drain current and threshold voltage recover 10 % and 25 %, respectively, more than in the unirradiated ones. Further data are needed to understand this behavior, but it may be possible that hydrogen is stored in different ways (e.g., different locations) in stressed devices, depending on previous irradiation, so that recovery during annealing steps occurs with different kinetics [Schwank02], [Lelis91].

3.5. Conclusions

In this chapter the degradation of enclosed layout transistors submitted to channel hot carrier stresses and X-ray irradiation have been analyzed.

Degradation of the main parameters have been observed after 136 Mrad(SiO_2) X-ray irradiation as well as after CHC stress. The dynamic of CHC stress is not influenced by previous irradiation in Core ELTs as compared to Core OLT due to the lack of STIs. In contrast, irradiated I/O ELTs submitted to CHC stress show a reduced parameter degradation as compared to the unirradiated ones due to the influence of the oxide traps that modify the barrier for hot carriers reducing the CHC-induced degradation.

Moreover a faster degradation kinetic during CHC stress has been observed in ELT devices as compared to OLTs featuring ΔV_{th}-degradation slopes between 0.65 and 0.75 instead of the common value of ~ 0.5. Moreover we found the degradation slope to be independent of channel length.

Through the use of TCAD simulations we observed a distorted electric field at the corners of the devices. Even if a cut is done to relax the electric field in these zones there are two smoother angles (as sketched in Fig. 3.10) that still lead to an enhancement of the field. This behavior impacts the hot carrier generation and the formation of traps with the relative hydrogen release at the corners. As a consequence, in agreement with many works reported in literature, the hydrogen diffusion is then modified due to the geometry of the transistor leading to the observed slope change.

Temperature does not affect the degradation kinetics of either irradiated or unirradiated core ELTs during CHC stress. In contrast, high temperature contributes to reduce the degradation especially in I/O devices due to the reduced mobility in the conductive channel that lowers the electrons' kinetic energy.

Chapter 4

Dielectric Breakdown: The Role of Bias During X-ray Irradiation

In this chapter we analyze MOSFETs irradiated with 10-keV X rays under different bias conditions and subsequently stressed in inversion mode under Fowler-Nordheim injection. The effects of radiation exposure on time and charge to breakdown are evaluated, and the mechanisms responsible for the observed phenomena are discussed.

4.1. Introduction

The main issue with respect to radiation effects has become the lateral isolation, because radiation-induced defects in such zones can affect the drawn transistor, enhancing narrow channel effects, increasing the off-current, and shifting the device threshold voltage [Faccio05].

On the other hand, the gate dielectric reliability is seriously affected by the increase of the electric field inside modern devices where the oxide thickness is scaled down below 2 nm, due to the slower decrease of the operating voltage as compared to feature size. It has been demonstrated that just a few defects can cause the onset of dielectric breakdown, leading the transistor to fail [Stathis01]. Moreover, Stress Induced Leakage Current (SILC) and the onset of Soft Breakdown (SBD) are common events when ultrathin gate oxides are investigated [Suñè06].

Studies about the interplay between heavy-ion effects and electrical stress have been carried out, especially in the framework of Single Event Gate Rupture (SEGR), often utilizing capacitors, or structures more similar to CMOS transistors [Silvestri09]. The results from heavy ion experiments show reduced gate oxide electrical-stress lifetime after irradiation for many device types and exposure conditions [Cester03], [Choi02], but comparatively fewer works report data about γ- or X-ray influence on gate oxide lifetime. Indeed, TID is an issue for space applications, but even more for high energy physics experiments and future fusion reactors.

The effects of electrical stress on γ-ray irradiated silicon micro-strips detectors were investigated in [Pacca96], showing that the TDDB was either unaffected by irradiation, or larger than that obtained by stressing unirradiated samples. More recently, Suehle et al. [Suehle02] reported similar behavior for CMOS capacitors after γ-ray exposure at different total doses, concluding that the shift of the TDDB failure distributions after irradiation was not statistically relevant. However, both works used devices that cannot be straightforwardly correlated to highly scaled MOSFETs. Moreover, the samples were irradiated unbiased and electrically stressed in accumulation. Similarly, only slight effects on TDDB were found after X-ray exposure performed under bias up to 20 Mrad(SiO_2) on 7-nm thermal and nitrided oxides, subsequently stressed with a temperature ramp technique, by Fleetwood et al. [Fleetwood00].

4.2. Experimental and Devices

We report results for n- and p-channel MOSFETs manufactured by a commercial foundry in a standard 130-nm CMOS technology. A dedicated test chip was designed to accommodate the electrical stress needs. All sources, drains, and substrates are connected together on chip, keeping all gates separated and bonded to different pads, each of which is protected by a double diode in order to prevent Electrostatic Discharge (ESD) damage. Moreover, a simple small diode connects each gate-pad to the metal-1 track.

The gate-oxide thickness is 2.2 nm with a nominal operating voltage of V_{dd} = 1.5 V. Two transistor sizes have been chosen for the study:

- Small area MOSFETs (A_{SMALL} = $1.92 \cdot 10^{-10}$ cm^2): L = 0.12 μm, W = 0.16 μm.
- Large area MOSFETs (A_{LARGE} = $2.25 \cdot 10^{-5}$ cm^2): ten individual transistors in parallel, with channel length L = 15 μm and total width W = 15 μm.

Irradiation was performed at CERN using an automatic probe station equipped with a

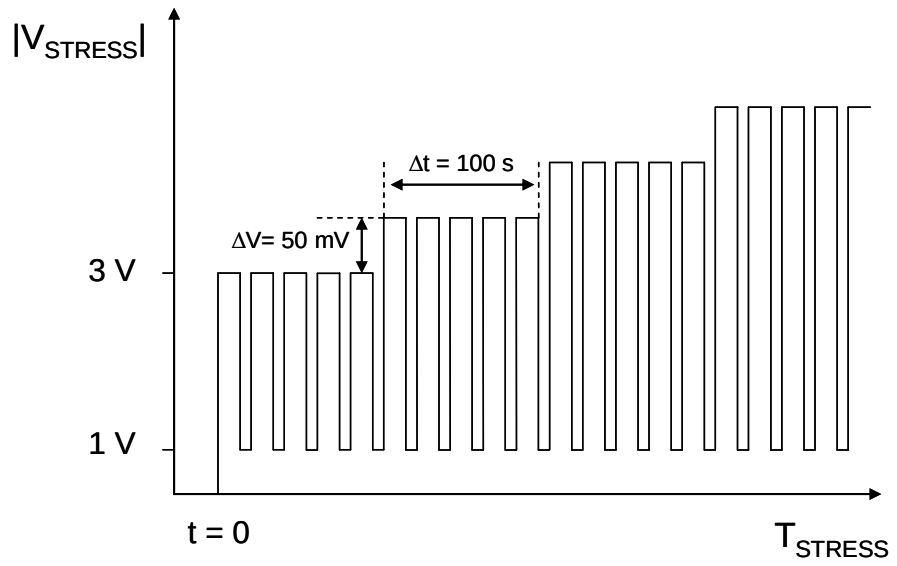


Fig. 4.1. Simplified representation of the Ramped Voltage Stress (RVS) used in our experiments. It starts from 3 V and is updated by 50 mV every 100 s until breakdown occurs. Periodically we sample the current at 1 V in order to detect soft breakdown events.

10-keV X-ray system. During the irradiation some samples were unbiased and others were biased in the worst-case condition: all pins grounded except the NMOS gates biased at V_{dd}. We irradiated the samples up to 1 Mrad(SiO_2) at a fixed dose rate of 25 krad(SiO_2)/min.

After irradiation we subjected the devices to accelerated Ramped Voltage Stress (RVS) with a ramp rate of 0.5 mV s^{-1} starting from 3 V, as shown schematically in Fig. 4.1. After each 100-s stressing interval, we measured the I_g-V_{gs} curve; then the gate voltage was automatically increased by 50 mV until breakdown occurred. All other terminals were grounded in the case of NMOSFETs. The same procedures, with negative voltages, were performed for PMOSFETs.

During stress the gate current was monitored at the stress voltage and at low voltage (1 V, sampled periodically) in order to detect soft-breakdown events [Silvestri09]. The breakdown voltage is defined as the voltage at which the gate current suddenly increases by at least one order of magnitude or drops down due to failure in the interconnection caused by the BD current. Correspondingly, the time at which the breakdown occurred is called T_{FAIL}. All measurements were performed with a

semiconductor parameter analyzer (Agilent 4156B).

The collected T_{FAIL} values have been analyzed using Weibull plots [Degraeve98]. The cumulative failure distribution $F[T_{FAIL}(i)]$ has been calculated with:

$$F[T_{FAIL}(i)] = \frac{i - 0.3}{n + 0.4} \tag{1}$$

where i is the i-th failure, $T_{FAIL}(i)$ is the i-th T_{FAIL}, and n is the total number of samples for each experiment. We define $t_{63\%}$ as the time at which the failure distribution is 63% ($F_{63\%}$); this corresponds to zero on the $ln(-ln(1-F))$ scale.

4.3. Experimental Results

4.3.1. n-channel MOSFETs

Fig. 4.2 shows the cumulative failure distribution, reported in a Weibull plot, of X-ray irradiated (unbiased or worst case bias during irradiation) and unirradiated (as processed) large area transistors stressed under the same electrical conditions (RVS) of Fig. 4.1. Irradiated devices show a small but measurable shift of the failure distributions toward larger time values, featuring a $t_{63\%}$ around $2 \cdot 10^3$ s as compared to $8 \cdot 10^2$ s exhibited by unirradiated devices. Moreover, the distributions for the irradiated devices do not show a large irradiation-bias dependence, although a slightly larger $t_{63\%}$ is observed in the worst-case irradiated samples. The slopes of the three distributions are almost the same regardless of the irradiation and the bias condition during irradiation.

Fig. 4.3 reports the cumulative failure distribution for unirradiated and irradiated small area samples after RVS. As in Fig. 4.2, irradiated devices show a shift of the distributions toward larger T_{FAIL}, with no clear bias dependence. The time distributions of both sets of irradiated devices are similar, but they differ significantly from the unirradiated ones as shown in Fig. 4.2.

4.3.2. p-channel MOSFETs

Fig. 4.4 shows the cumulative failure distribution for large area p-channel devices. The distribution of samples irradiated in the worst-case bias condition shows a $t_{63\%}$ around 450 s, as compared to about 200 s exhibited by irradiated samples in the unbiased condition.

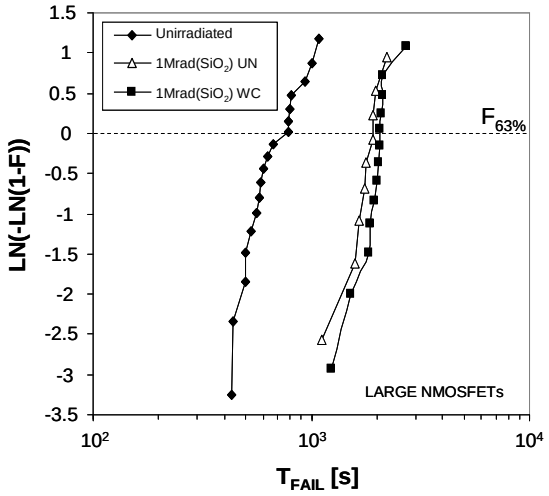


Fig. 4.2 Cumulative failure distribution reported in a Weibull plot of large area NMOSFETs, unirradiated (as processed), and irradiated up to 1 Mrad(SiO_2) unbiased (UN) and in the worst case (WC) condition.

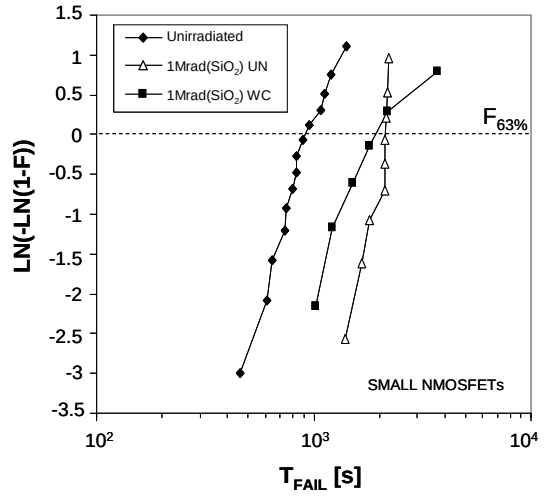


Fig. 4.3 Cumulative failure distribution reported in a Weibull plot of small area NMOSFETs, unirradiated (as processed), and irradiated up to 1 Mrad(SiO_2) unbiased (UN) and in the worst case (WC) condition.

Hence, the influence of the irradiation bias on the failure distribution in PMOSFETs is more significant, since the devices irradiated unbiased show a failure distribution close to that of the unirradiated transistors.

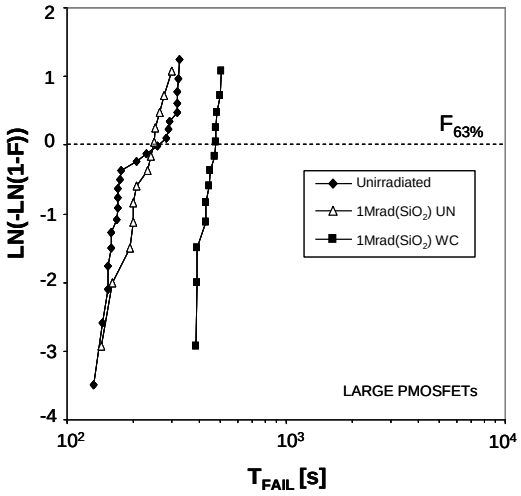


Fig. 4.4 Cumulative failure distribution reported in a Weibull plot of large area PMOSFETs, unirradiated (as processed), and irradiated up to 1 Mrad(SiO_2) unbiased (UN) and in the worst case (WC) condition.

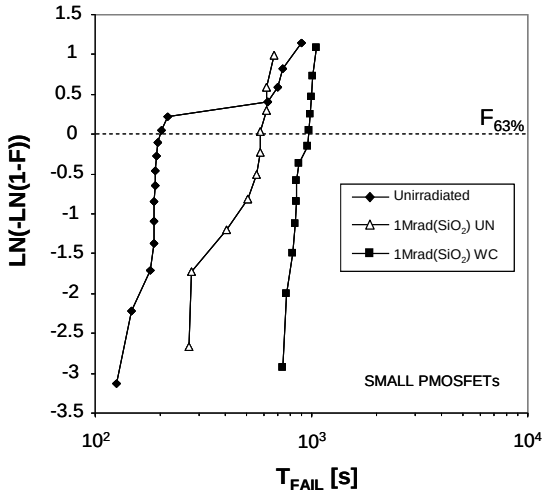


Fig. 4.5 Cumulative failure distribution reported in a Weibull plot of small area PMOSFETs, unirradiated (as processed), and irradiated up to 1 Mrad(SiO_2) unbiased (UN) and in the worst case (WC) condition.

Comparable results are shown in Fig. 4.5 for small area devices. Similar to the large area samples, the irradiation performed in the worst-case bias condition leads to a longer lifetime after stress, while the distribution of transistors irradiated unbiased lies

between that of the unirradiated devices and the devices irradiated with worst-case bias. The distribution of the devices irradiated unbiased crosses that of the unirradiated devices around 600 s.

4.4. Discussion

Accelerated electrical stress by Fowler Nordheim (FN) injection is one of the most accepted and widely used procedures to evaluate the quality of dielectrics and, through conventional reliability techniques, a good way to predict the lifetime at operating conditions (bias, temperature, etc.) [Stathis01]. The common way to do this kind of test is to bias the gate contact of the devices with a constant high voltage (CVS) for enough time to cause gate rupture. Unfortunately, the CVS technique is time consuming, and ramped voltage stresses, with very fast ramp rates, are commonly used to degrade the oxides more quickly [Aal07]. As shown in Fig. 4.1, we used a very slow ramp rate RVS to accelerate the degradation process, which allows detection of events like soft or progressive breakdown [Suñè06], [Monsieur02], which otherwise can be masked by extremely fast ramp rates.

The gate oxide degradation typically is driven by uniformly generated defects, in the case of FN stress, or localized at the drain edge in the case of Channel Hot Carrier (CHC) stress [Groes99]. Both kinds of accelerated aging mechanisms are based on the injection of carriers through the gate oxide, which adds new defects to the intrinsic ones. As a consequence, the flow of these energetic carriers produces defects until a critical number is reached and a conductive path across the gate oxide can lead to hard breakdown [Stathis01].

The tunneling process (Fowler Nordheim) depends strongly on the bias applied to the gate, which changes the barrier experienced by electrons or holes, as schematically shown in Fig. 4.6. According to [Denais04], electron conduction band tunneling (ECBT) is the main injection process during the stress of inverted NMOS devices. When the bias is high enough, another tunneling process from the bulk-silicon valence band (EVBT) starts to take place, enhancing the total electron injection. In contrast, in inverted PMOSFETs, the injection of holes from the valence band (HVBT) is the main process, but it is coupled with the electron injection from the gate and valence band. As a consequence, the injection of both electrons and holes in PMOS devices can explain the shorter lifetime we found in unirradiated devices (compare Figs. 4.2 and 4.4), in agreement with [Stathis01].

Furthermore, boron diffusion from the p+ polysilicon gate into the oxide layer can

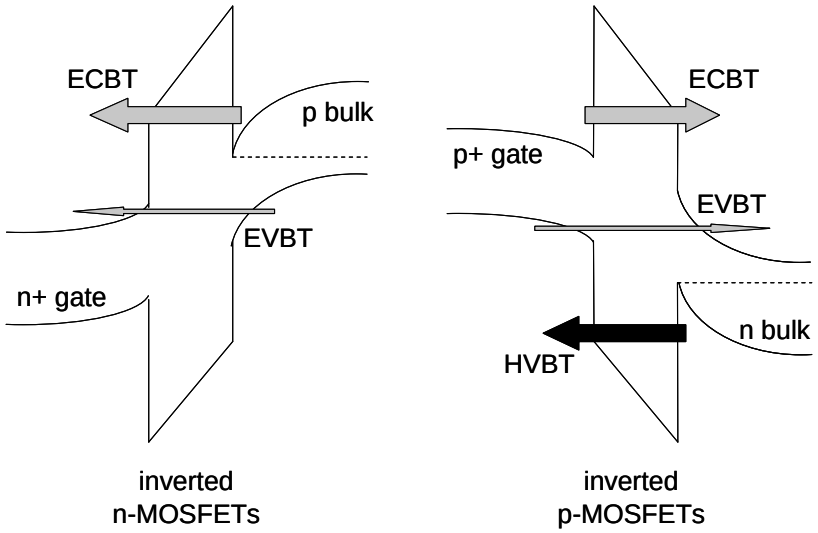


Fig. 4.6 Schematic band diagram that shows the main tunneling processes in inverted p- and n-channel MOSFETs.

lead to additional defects that can shorten the dielectric lifetime of PMOS transistors [Wristers96]. However, some authors report PMOSFET lifetimes larger than those of NMOSFETs in the case of constant voltage stress on ultrathin dielectric devices (1.1 nm) [Wristers96].

From the Weibull distributions reported in Figs. 4.2-4.5, it is clear that X-ray irradiation can influence significantly the results of subsequent electrical FN stress. The increase in the lifetime after irradiation is clear for all of the devices, both PMOS and NMOS, especially when irradiated in the worst-case bias condition. The damage induced by radiation, before electrical stress, influences the dynamics of carrier trapping and consequently the charge that flows across the gate oxide during FN experiments. Consequently, the gate current during stress is a good monitor to observe this behavior. This is shown in Fig. 4.7 for unirradiated and irradiated PMOS devices in the two different bias conditions: unbiased (UN) and worst case (WC). The gate current is reduced after the exposure, depending on the irradiation bias. We found a reduction of about 5 % and 25 % for PMOS devices irradiated unbiased and in the worst case, respectively.

The correlation between the T_{FAIL} and the gate current taken at the initial V_{STRESS} $(t = 0)$ for unirradiated and irradiated large PMOSFETs is reported in Fig. 4.8. The bimodal nature of the distributions of unirradiated PMOS devices, shown in Figs. 4.4

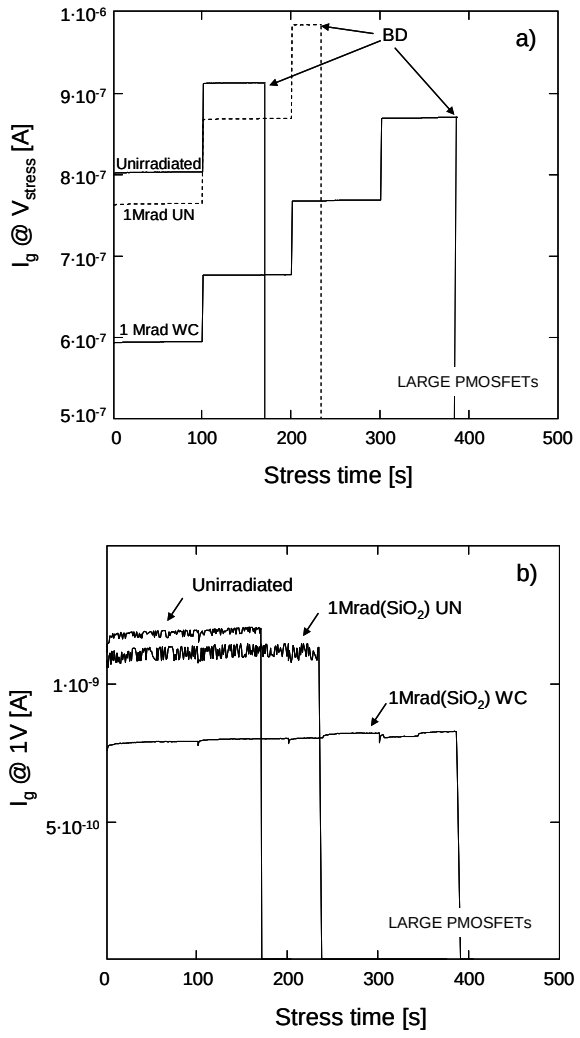


Fig. 4.7 Gate leakage current during stress for unirradiated (as processed) and irradiated up to 1 Mrad(SiO_2) (unbiased and in the worst case condition) large area PMOSFETs: a) taken at stress voltage, b) taken at low voltage (1 V).

and 5, is explained by the data reported in Fig. 4.8.

The lower T_{FAIL} corresponds to a higher initial gate stress current. Unirradiated devices exhibit two distinct families of points displayed in clusters around I_g values of ~ 750 nA and 800 nA (empty squares in Fig. 4.8), which correspond to the edges of the unirradiated distribution reported in Fig. 4.4. Moreover the data for the devices irradiated unbiased (filled triangles in Fig. 4.8) overlap the long life-time tail (around

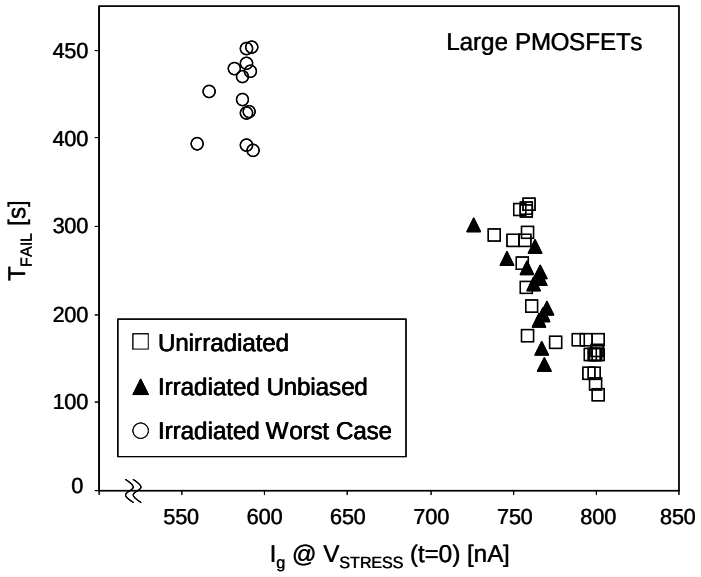


Fig. 4.8 Time to breakdown (T_{FAIL}) as a function of gate current (taken at the stress beginning) for unirradiated (as processed) and irradiated large area PMOSFETs. The higher the gate current the lower the T_{FAIL}.

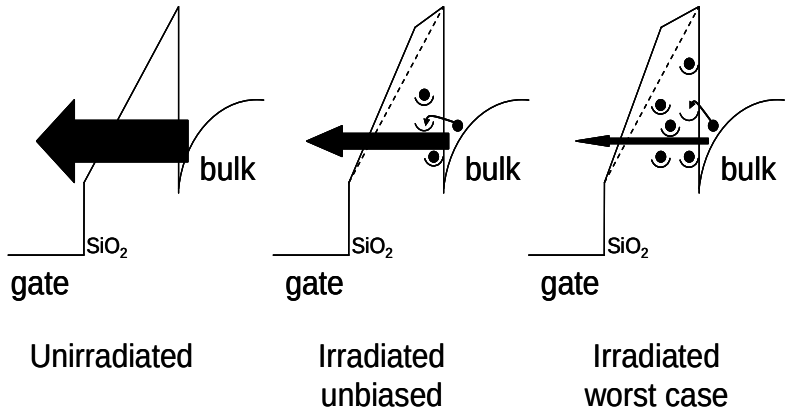


Fig. 4.9 Schematic representation of radiation-induced traps as a function of the irradiation bias in NMOSFETs. The traps change the net barrier height, reducing the gate current during subsequent stress.

300 s) of the unirradiated transistors as in Fig. 4.4.

In contrast, the data points of samples irradiated in the worst-case bias condition fall away at lower gate currents and correspondingly longer values of T_{FAIL}. The correlation reported in Fig. 4.8 indicates that some unirradiated devices have an

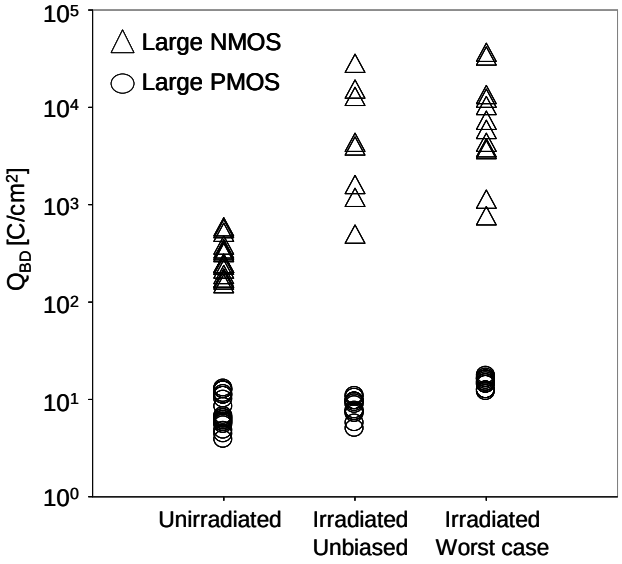


Fig. 4.10 Charge to breakdown (after RVS) for large area N and PMOSFETs unirradiated (as processed), irradiated unbiased and irradiated in the worst case.

initially higher as-processed interface-trap density than others. These as-processed traps introduce a variation into the potential barrier and consequently affect the current through the gate oxide, leading to the discontinuity exhibited by the data in Figs. 4.4 and 4.5, consistent with other reports in the literature [Pacca96], [Monsieur02].

In Fig. 4.9 we show schematically the influence of traps on the barrier height for NMOSFETs. The larger the density of negatively charged traps near the interfaces, the larger the barrier experienced by electrons, and consequently the lower the gate current. This is in agreement with [Martin96], where electrically pre-damaged oxides have been found to be more robust to subsequent electrical FN stress, as compared to virgin ones.

Fig. 4.10 shows the charge to breakdown Q_{BD}, normalized to the gate area, for large area N and PMOSFETs as a function of the irradiation bias and, as a reference, for the unirradiated samples. Q_{BD} has been calculated with (2) after RVS and not from constant voltage stresses as usually reported in literature [Wu02]:

$$Q_{BD} = \sum_{i=1}^{BD} I_{g-HV_i} \cdot t_{Step_i} \tag{2}$$

Here *i* is the *i-th* step of the staircase stress voltage until breakdown occured, $I_{g\text{-}HVi}$ is

the gate current taken at the *i-th* stress voltage step, and t_{Stepi} is the duration of every step (see Figs. 4.1 and 4.7a).

Unirradiated and irradiated unbiased PMOSFETs exhibit almost the same Q_{BD}, while the worst case bias condition leads to a slight larger one. For the NMOSFETs, irradiated devices display an increase in Q_{BD} (regardless of the bias condition) as compared to unirradiated samples. When bias is applied during irradiation, the amount of damage in the oxide is enhanced, affecting the current injected during the subsequent stress, as demonstrated by comparing the unbiased and worst case curves reported in Fig. 4.7 and the Q_{BD} reported in Fig. 4.10. Note that the worst-case irradiation bias condition leads to a more useful upper bound of device degradation than irradiation with floating contacts, which is best avoided, owing to unpredictable charging effects during exposure [Schwank02]. Moreover, from the results reported in Fig. 4.10 it is remarkable that the dielectric breakdown experienced in these experiments is not a simple function of the injected charge through the gate oxide since (at least for NMOSFETs) Q_{BD} is not constant. In fact, the RVS and the radiation-induced traps can interact in a complicated way, leading to different Q_{BD} as found in [Martin96].

The degradation process during irradiation for these ultrathin oxides is primarily the release of positively charged hydrogen (H^+) that migrates toward the interfaces (depending on bias), where it can interact with Si-Si bonds or passivated dangling bonds [Pantelides07], creating defects. Hydrogen is introduced on purpose during device processing to passivate the defects at the Si/SiO_2 interface in order to improve the carrier mobility in the conductive channel by reducing the as-processed interface-trap density. Moreover, hydrogen is introduced from silane gas as a result of process operations (such as polysilicon deposition) and usually is also present in a relatively large quantity in the bulk attached to some of the dopant atoms (boron or phosphorus) [Pantelides07].

The consequence of bias during irradiation is that the hydrogen is driven either toward the Si/SiO_2 or the poly-Si/SiO_2 interface, as schematically illustrated in Fig. 4.11, where it can create defects. The electric field across the gate oxide is positive when the NMOSFETs are biased with a gate voltage V_{GS} larger than the flat-band voltage $V_{FB} < 0$ V (~ -1 V). As a consequence, H^+ drifts toward the oxide/channel interface and then reacts with Si-H bonds through the reaction $Si\text{-}H + H^+ \rightarrow D + H_2$, where D is a dangling bond [Pantelides07], [Rashkeev01].

In contrast, V_{FB} is positive in PMOSFETs (~ 1 V); when the contacts are grounded (worst case), the net field across the oxide is negative (directed to the gate). In this

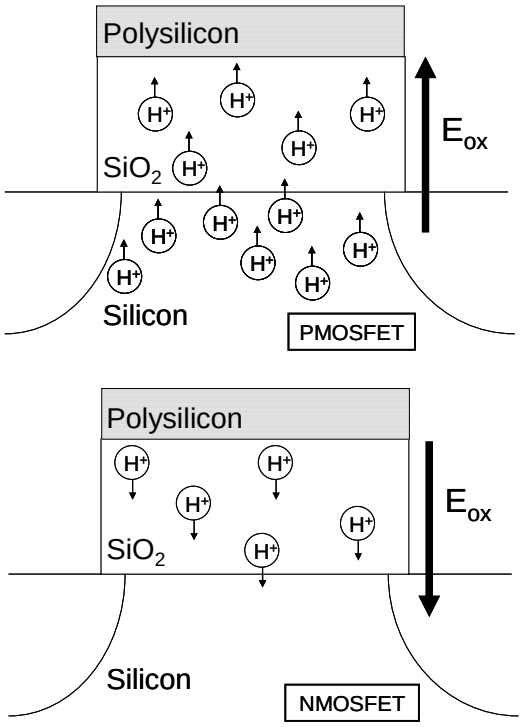


Fig. 4.11 Schematic representation (not to scale) of hydrogen drift in P and NMOSFETs biased during irradiation. A large contribution of hydrogen drift from the bulk can be present in p-channel devices leading to a larger degradation and bias dependence.

case, once the hydrogen in the Si bulk is released from dopants by radiation, it can drift toward the oxide, creating defects at the Si/SiO_2 interfaces. The mechanism is similar to the one invoked to explain the Negative Bias Temperature Instability (NBTI) phenomenon [Tsetseris07].

It is likely that more hydrogen is contained in the near-interfacial Si bulk than in the ultra-thin oxides for these devices, just due to the differences in volumes. This may well account for the greater sensitivity of the PMOS devices to trap buildup and change in lifetime. However, it is also possible that hole tunneling is more sensitive to the buildup of defects than electron tunneling [Ceschia98]. These two effects likely account for the differences in the radiation bias dependences for NMOS and PMOS devices reported here.

4.5. Conclusion

In this chapter the effect of X-ray irradiation performed with different bias conditions on TDDB has been analyzed.

Irradiated NMOS and PMOS devices show a shift of the failure distributions toward larger time values as compared to the distribution of unirradiated transistors. Moreover a remarkable irradiation bias dependence on TDDB has been found in PMOSFETs and to a lesser extent in NMOS devices.

The X-ray irradiation influence the subsequent FN stress changing the barrier thickness felt by the electrons reducing the tunneling current and consequently the gate oxide damage. In fact, after irradiation, during FN stress, a stress current reduction of about 5 % and 25 % have been found in PMOS devices irradiated unbiased and in the worst case, respectively.

Moreover, the enhanced irradiation bias dependence found in PMOSFETs is attributed to a different hydrogen diffusion. In fact, when PMOS devices are irradiated in the worst case (pins grounded) the hydrogen can drift from the bulk where it is abundant attached to dopant atoms producing more defects at the oxide interface as compared to the ones generated in NMOSFETs where hydrogen can drift only from polysilicon.

Chapter 5

X-ray Irradiation: Dose Enhancement Due to Metal Interconnects

In this chapter is studied how the first metal layer alters the total-dose effects after X-ray exposure in devices manufactured with a 90-nm CMOS process and designed with different ad-hoc interconnect layouts. These results are important to understand how many sources of combined effects may exist when scaled devices are irradiated.

5.1. Introduction

The radiation qualification of Commercial Off The Shelf (COTS) electronic components is an expensive and time-consuming task, made more complex by the ever-increasing process-to-process and chip-to-chip variability of modern Integrated Circuits (ICs) [Hughes03], [McLain07]. To measure the sensitivity to the different effects a whole set of radiation tests normally needs to be performed: Total Ionizing Dose (TID) using an X-ray source, Co^{60} γ-ray source, electron or proton beams; displacement damage using neutrons from a nuclear reactor or special neutron sources. Single event tests using high energy proton beams (60 MeV and above) and ion beams are also performed to assess the threat of single event upsets and latch-up.

Concerning total ionizing dose effects, Co^{60} γ-ray sources or proton/electron beam

irradiations are required to comply with the military and space standards [Fleetwood03]. On the other hand, cheaper and more accessible X-ray facilities are often used to perform total-dose tests, even though they have some shortcomings.

Secondary electrons emitted by metal layers during X-ray exposure may reach the MOSFET dielectrics, causing significant dose-enhancement [Schwank02], [Fleetwood85], which may be difficult to evaluate. These phenomena have been deeply investigated for the gate electrode and oxide, which was once the major source of concern in old technologies [Scarpa97], [Ceschia98], [Ceschia00], but rarely considered for interconnects. The ever shrinking geometries of CMOS technology and the very high transistor density of modern ICs have caused the number and thickness of interconnect metal layers to increase from generation to generation. The presence of these layers must be carefully evaluated, especially since the switch from aluminum to copper interconnects.

Below the 0.25-μm technology node Shallow-Trench Isolation (STI) is the only viable scheme to achieve device isolation with the required packing density and speed performance, improving also active area pitches and planarity [Peters99]. This makes the STI the central focus for total dose hardening [Shaneyfelt98]. In fact, the presence of interconnect metal layers just a few hundreds of nanometers over the STIs and, more in general, over the MOSFET active areas, may significantly affect the outcome of irradiation performed with X rays.

5.2. Experimental and Devices

We studied n-channel MOSFETs specifically designed and manufactured for this study by IMEC (Leuven, Belgium) in a standard 90-nm bulk CMOS process. The gate electrode was n-type polysilicon. The oxynitride (SiON) gate-oxide thickness was 1.6 nm. The back-end interconnections were manufactured with dual damascene copper in order to reduce the overall resistance, while a silica-based low-κ dielectric was used as inter-layer. All the metal layers were made of copper. The maximum operating voltage (V_{DD}) is 1.5 V. Devices with channel width (W) 1 μm and 0.15 μm and channel length (L) 0.13 μm were used. The transistors were designed with three different metal-1 (*M1*) layouts (Figs. 5.1 and 5.2):

i. poly-*M1* spacing = 1 μm (in the following '$L_{poly\text{-}M1}$ = 1 μm'): the distance between the polysilicon gate and the *M1* track connected to source and drain is 1 μm;
ii. poly-*M1* spacing = 1 μm + *M1* plate (in the following '$L_{poly\text{-}M1}$ = 1 μm +

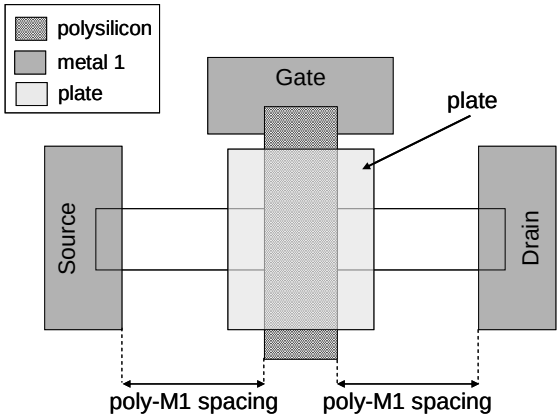


Fig. 5.1: Schematic layout (not to scale) of the MOSFETs studied.

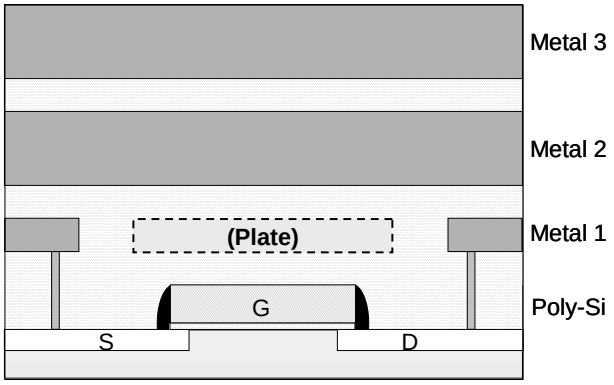


Fig. 5.2: Schematic cross-section (not to scale) of a processed wafer.

plate'): the same layout as i. plus a floating *M1* area over the gate;

iii. poly-*M1* spacing = 0.1 µm (in the following '$L_{poly\text{-}M1}$ = 0.1 µm'): same as i. but the spacing between the polysilicon gate and the *M1* track connected to source and drain is 0.1 µm.

Apart from the *M1* layout, the transistors are perfectly identical (including source/drain vias) and located close one another in the wafer to minimize device-to-device variability.

Irradiation was performed at the SIRAD 10-keV X-ray facility of the INFN Laboratori Nazionali di Legnaro, Italy. The samples were irradiated at room

temperature in steps up to a total ionizing dose of 30 Mrad(SiO_2) with dose rate of 28 krad(SiO_2)/min.

The irradiation was done keeping source and body terminals grounded, drain terminal at 10 mV and the gate at V_{DD}. The low bias at the drain (V_{DS} = 10 mV) does not appreciably influence the radiation response of the device and makes it possible to monitor the drain current during the irradiation.

Before irradiation and after every irradiation step, we measured the gate current versus the gate voltage (I_G-V_G), the drain current versus the gate voltage (I_{DS}-V_{GS}) for different body voltages (V_{BS} = 0 V, - 0.2 V, and -0.4 V), and the drain current versus the drain voltage (I_{DS}-V_{DS}) for different gate voltages (V_{GS} = 0.9 V, 1.2 V, and 1.5 V) on each MOSFET.

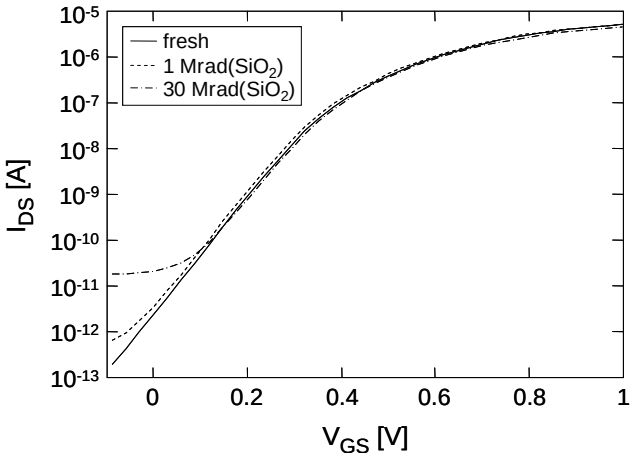
5.3. Experimental Results

Fig. 5.3 shows the I_{DS}-V_{GS} characteristics in semi-logarithmic (Fig. 5.3a) and linear scale (Fig. 5.3b) of a n-channel MOSFET with $L_{poly\text{-}M1}$ = 1 μm and *W/L* = 0.15 μm/0.13 μm.

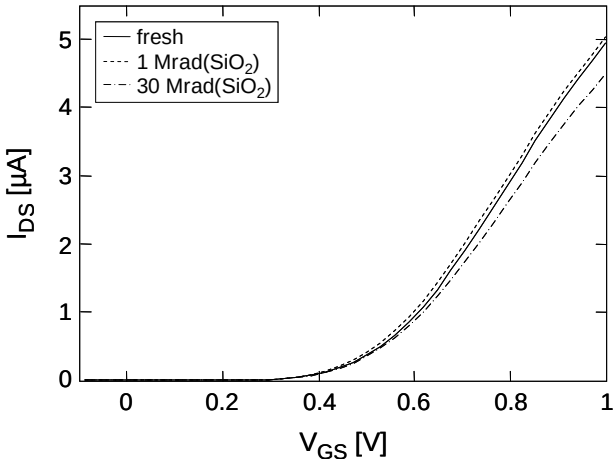
Contrary to some results on comparable and older technologies [Barnaby06], [Gonella07], [Oldham03], [Re07], these transistors exhibit only modest subthreshold humps, related to the activation of parasitic transistors at the poly/STI corners [Shaneyfelt98], [Turowsky05]. This remains true also biasing the body terminal with negative voltages (V_{BS} < 0 V), as shown in Fig. 5.3. This is the best bias condition to better notice the influence of the parasitic MOSFET on the I_{DS}-V_{GS} curves, because it allows us to detect charge trapped deeper in the STIs than at V_{BS} = 0 V, due to the larger depletion region [Shigyo99].

Furthermore, Fig. 5.3 shows that the threshold voltage (V_{TH}) shift is modest in such samples. In fact, $|\Delta V_{TH}|$ < 15 mV for the devices with *W* = 0.15 μm (in the following 'narrow-channel MOSFETs'), while for the samples with *W* = 1 μm (in the following 'wide-channel MOSFETs') the V_{TH} shift is less than 5 mV up to 30 Mrad(SiO_2).

In order to analyze the dependence on the *M1* layout and device geometry we will focus on $I_{DS,ON}$ (i.e. the drain current at V_{GS} = 1.5 V, V_{DS} = 25 mV, and V_{BS} = 0 V) and $I_{DS,OFF}$ (i.e. the drain current at V_{GS} = 0 V, V_{DS} = 25 mV, and V_{BS} = -0.4 V). These quantities are highly indicative of MOSFET degradation, and can be used to detect changes in threshold voltage, mobility, series resistance (R_s), and parasitic transistor leakage. We want to remark that the data reported in Figs. 5.4 and 5.5 and presented in the following part are measured on transistors belonging to the same die.



a)



b)

Fig. 5.3: I_{DS}-V_{GS} characteristics (V_{DS} = 25 mV and V_{BS} = -0.4V) in a) semi-logarithmic and b) linear scale before irradiation, after 1 Mrad(SiO_2), and after 30 Mrad(SiO_2) for a NMOSFET with $L_{poly\text{-}M1}$ = 1 µm and W/L = 0.15 µm/0.13 µm.

Even though we found some die-to-die variability in the MOSFET parameters, the same quantitative relations between the degradation of the different layouts were observed in each tested die.

5.3.1. Drain Current Degradation

Fig. 5.4 shows the typical relative variation of $I_{DS,ON}$ ($\Delta I_{DS,ON}(TID)/ I_{DS,ON}(fresh)$) as a function of the received dose for different layouts and channel widths.

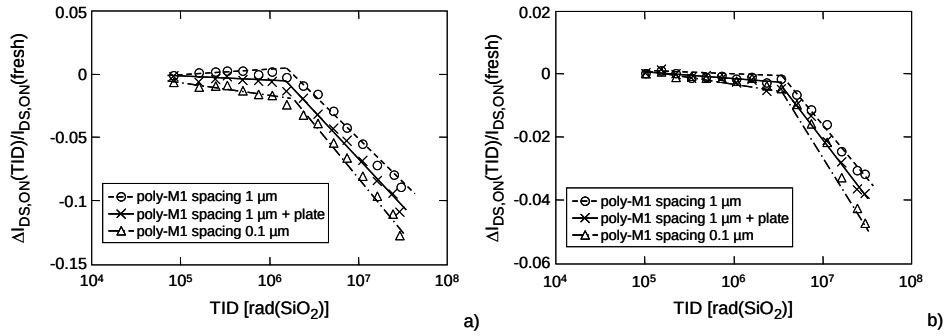


Fig. 5.4: Typical relative $I_{DS,ON}$ variation (V_{GS} = 1.5 V, V_{DS} = 25 mV, and V_{BS} = 0 V) as a function of the Total Ionizing Dose (TID) for NMOSFETs with different metal-1 layouts and with a) *W/L* = 0.15 µm/0.13 µm and b) *W/L* = 1 µm/0.13 µm.

For each transistor the degradation kinetics of $I_{DS,ON}$ can be divided in two phases, based on the changing slope of the curves. This behavior depends on channel width: the slope change occurs at lower doses (between 1 and 1.5 Mrad(SiO_2)) in narrow-channel MOSFETs than in wide-channel ones (between 2.3 and 3.4 Mrad(SiO_2)).

Furthermore narrow MOSFETs are more affected than wide ones. For example, at the end of the irradiation (TID = 30 Mrad(SiO_2)) the drain current drop is larger than 10 % for narrow MOSFETs, while less than 6 % for wide ones.

Concerning the dependence on the *M1* layout, the degradation of $I_{DS,ON}$ depends on the chosen layout for both channel widths. The drain current related to MOSFETs with the larger poly-*M1* spacing degrades less than the other samples, independently from channel width. In other words, the slope is smaller in MOSFETs with $L_{poly\text{-}M1}$ = 1 µm than in samples with $L_{poly\text{-}M1}$ = 1 µm + plate or $L_{poly\text{-}M1}$ = 0.1 µm, indicating that the first one is less affected by radiation. Moreover, in the first irradiation phase, narrow transistors with $L_{poly\text{-}M1}$ = 1 µm experience an increase in $I_{DS,ON}$ while the wide counterparts remain unaltered.

On the contrary, in the devices with other layouts the drain current degradation slope decreases monotonically. Moreover, Fig. 5.4 shows that the transistors with $L_{poly\text{-}M1}$ = 0.1 µm exhibits the largest degradation regardless of the channel width. Indeed, the slope is larger in MOSFETs with $L_{poly\text{-}M1}$ = 0.1 µm than in the ones with $L_{poly\text{-}M1}$ = 1 µm or $L_{poly\text{-}M1}$ = 1 µm + plate.

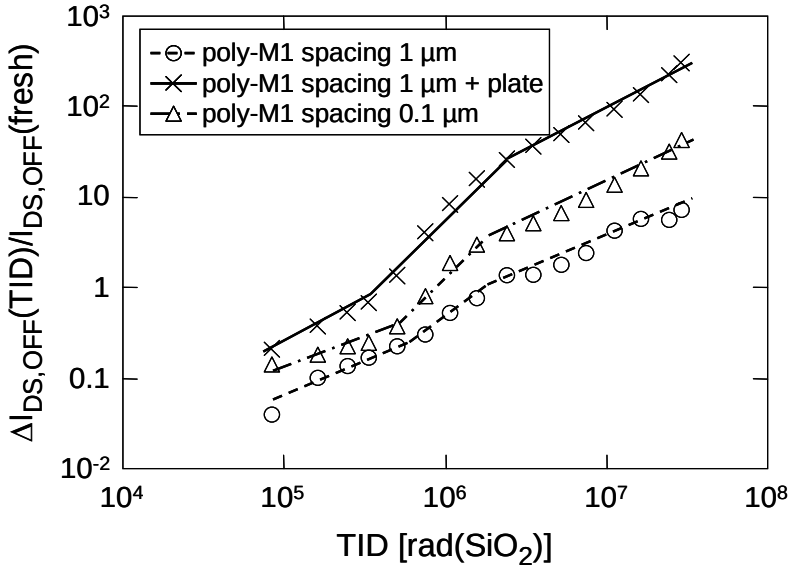


Fig. 5.5: Typical relative $I_{DS,OFF}$ variation (V_{GS} = 0 V, V_{DS} = 25 mV, and V_{BS} = -0.4 V) as a function of the Total Ionizing Dose (TID) for NMOSFETs with different metal-1 layouts and with W/L = 0.15 µm/0.13 µm.

5.3.2. Off Current Degradation

Concerning the degradation kinetics of $I_{DS,OFF}$, Fig. 5.5 shows the typical relative variation of $I_{DS,OFF}$ *(*$\Delta I_{DS,OFF}$*(TID)/* $I_{DS,OFF}$*(fresh))* as a function of the dose for narrow-channel MOSFETs with different layouts. Wide-channel devices do not exhibit any dependence on the layout and the increase in relative $I_{DS,OFF}$ variation is less than 10 %. For each layout the kinetics can be divided in three phases; each of them follows a power law of the dose of the form:

$$\Delta I_{DS,OFF}(\text{dose}) / I_{DS,OFF}(\text{fresh}) = A \cdot \text{dose}^{k} \qquad (1)$$

where A and k are fitting parameters. The exponent k is different for each of the three mentioned phases, but (in first approximation) does not depend on the layout: k is equal to ~ 0.8 – 0.9 in the first phase (dose ≤ 650 krad(SiO_2)), ~ 2.5 in the second phase (650 krad(SiO_2) < TID < 2.6 Mrad(SiO_2)), and ~ 1 the last one (dose ≥ 2.6 Mrad(SiO_2)). On the other hand, the factor A depends mainly on the metal-1 layout. As reported in Fig. 5.5 the $I_{DS,OFF}$ degradation is smaller in devices with $L_{poly\text{-}M1}$

= 1 μm. On the contrary, samples designed with the plate exhibit the largest $I_{DS,OFF}$ degradation, differently from what we observe for $I_{DS,ON}$ degradation.

5.4. Discussion

As we have shown in the previous section, the kinetics degradation of a given parameter considered in this work is qualitatively the same, irrespective of the layout. Therefore, the first part of the discussion will be devoted to analyzing the mechanisms underlying the device response to total ionizing dose, whereas the second part will investigate the impact of the metal-1 layout on those mechanisms.

5.4.1. MOSFET Degradation

The drain current decrease as a function of the received dose (Fig. 5.4) may be due to different causes:

a) threshold voltage shift and mobility degradation due to charge trapping and interface state generation at the gate oxide/Si channel interface;
b) threshold voltage shift and mobility degradation due to charge trapping and interface state generation at the STI/Si channel interfaces;
c) increased series resistance due to negative charge build-up in the LDD spacers (the nitrided LDD spacers, differently from STIs, are prone to trap electrons [Wrazien03], [Gerardin06]).

Concerning mechanism a), the increase in the interface state density at the gate oxide/Si channel interface can account only for a small degradation of the drain current. Indeed, the change in the subthreshold swing is less than 2 mV/decade after 30 Mrad(SiO_2), corresponding to an increase in the interface state density smaller than 10^{11} cm^{-2}, and the threshold voltage shift is unappreciable. This indicates that the generation of interface states and charge trapping due to radiation is very limited, as expected in an ultra-thin gate oxide [Saks86].

Mechanism b) is usually invoked to explain differences in the degradation between narrow and wide channel device [Faccio05] and is known to generate a hump in the subthreshold characteristic, similar to that visible in Fig. 5.3a. Indeed, $I_{DS,OFF}$ degradation (Fig. 5.5) can be ascribed to a change in the threshold voltage of parasitic transistors caused by radiation-induced trapped charge in the STI [Faccio05].

But neither a) nor b) can alone explain the degradation of series resistance that seems to characterize the behavior of these transistors. To evaluate the impact of mechanism c) we performed TCAD physical device simulations with the ISE TCAD

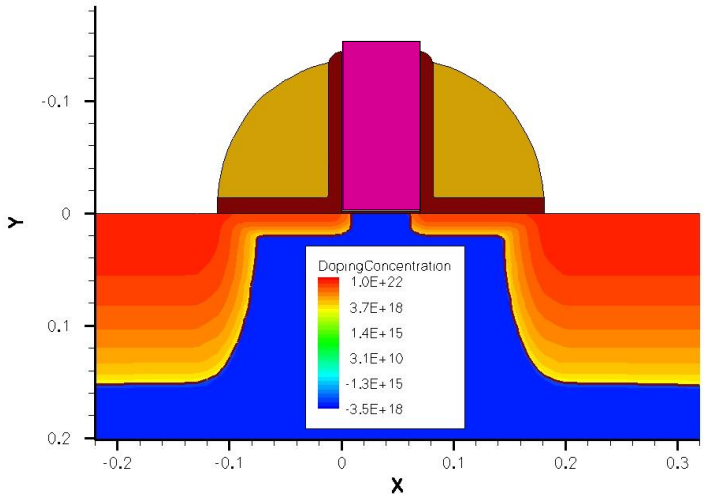


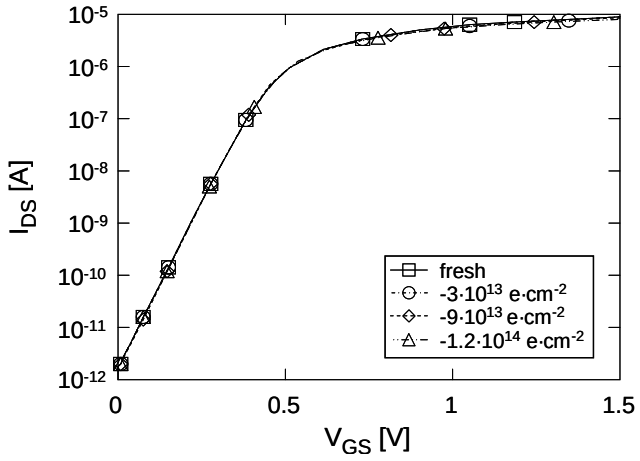
Fig. 5.6: 2-D structure of the NMOSFET used in our simulations (W/L = 0.15 µm / 0.09 µm).

DESSIS simulator. We based our simulations on standard values available for 90-nm IMEC technologies (see Fig. 5.6), using the hydrodynamic model with high-field saturation and mobility degradation models including doping-dependence and carrier-carrier scattering.

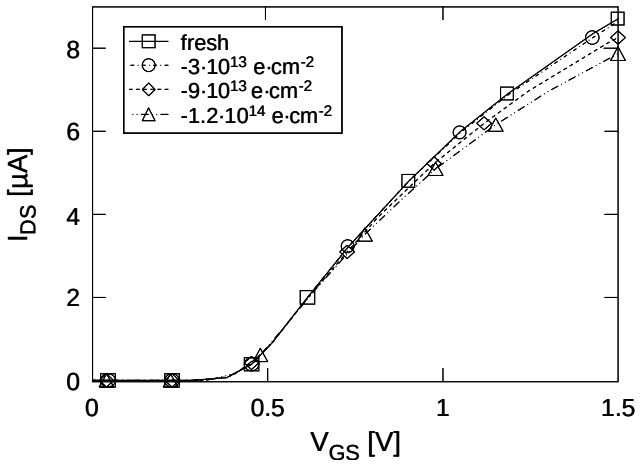
Fig. 5.7 shows the simulated I_{DS}-V_{GS} curves in linear and semi-logarithmic scale for different amounts of negative trapped charge in the LDD spacers that measure 90 nm and 120 nm in length and height, respectively (see Fig. 5.6)

Radiation-induced charge trapping was simulated using an equivalent negative sheet of charge inserted at the spacer/silicon interface ranging from $1 \cdot 10^{11}$ to the very high value of $1.5 \cdot 10^{14}$ cm^{-2}. In agreement with the experimental results reported in Fig. 5.3, a negligible increase in subthreshold swing and a modest increase in V_{TH} (up to ~ 10 mV) are observed in the simulated electrical DC characteristics. At the same time the simulations reproduce qualitatively very well the behavior at high gate voltage. Obviously, the simulated characteristics does not show any increase in $I_{DS,OFF,}$ as no positive trapped charge has been introduced in the STIs.

Fig. 5.8 shows the simulated relative $I_{DS,ON}$ degradation as a function of the amount of negative trapped charge in the LDD spacers. Based on the changing slope of the curve, the simulated degradation kinetics of $I_{DS,ON}$ can be divided in two phases: in the



a)



b)

Fig. 5.7: Simulated I_{DS}-V_{GS} curves (V_{DS} = 25 mV and V_{BS} = 0 V) in a) semi-logarithmic and b) linear scale for different amounts of negative charge trapping in the LDD spacers for a NMOSFET (W/L = 0.15 µm/ 0.13 µm).

first one ($Q^- < 3 \cdot 10^{13}$ e·cm^{-2}) $I_{DS,ON}$ slowly decreases, whereas in the second phase ($Q^- > 3 \cdot 10^{13}$ e·cm^{-2}) the change is much more pronounced.

This trend is qualitatively in good agreement with the experimental results shown in Fig. 5.4 (of course a correlation between trapped charge and dose would be required for a full assessment). What our 2-D simulations cannot explain is the different amount of degradation between wide and narrow devices (see again Fig. 5.4). This fact

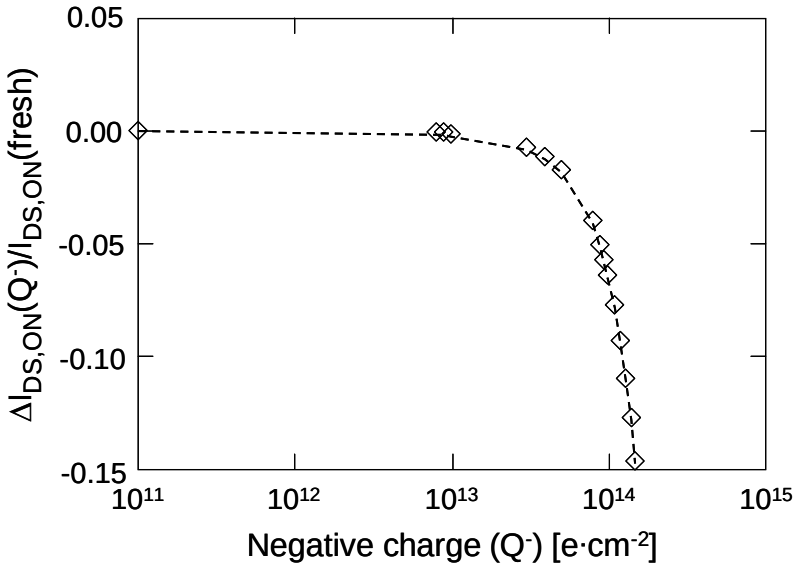


Fig. 5.8: Simulated relative $I_{DS,ON}$ variation (V_{GS} = 1.5 V, V_{DS} = 25 mV, and V_{BS} = 0 V) as a function of the negative charge trapping density in LDD spacers (Q^-) for a NMOSFET *W/L* = 0.15 µm/0.13 µm.

can be justified assuming that the increase in series resistance is enhanced in narrow devices possibly due to the larger influence of the negatively charged interface states that may be present in the upper part (close to the gate oxide) of the STI sides (along the device length) [Faccio05], [Turowsky05].

Latent pre-existing defects, which may lead to defects after X-ray exposure, generated from mechanical stress to the atomic structure cannot be excluded. This phenomenon is certainly emphasized at the LDD-STI corners as shown in Fig. 5.9, affecting the series resistance especially in narrow devices (W = 150 nm) and to a lesser extent in wide ones (W = 1 µm).

5.4.2. Layout Dependence

Before going on with the discussion, we want to further remark that the different types of transistors we tested are identical but for the *M1* layout, as described in the experimental and devices section. The higher degradation of $\Delta I_{DS,ON}(TID)/I_{DS,ON}(fresh)$ in MOSFETs with $L_{poly\text{-}M1}$ = 0.1 µm as compared to the ones with $L_{poly\text{-}M1}$ = 1 µm can be explained by dose enhancement effects due to the copper metal-1 layer. In fact,

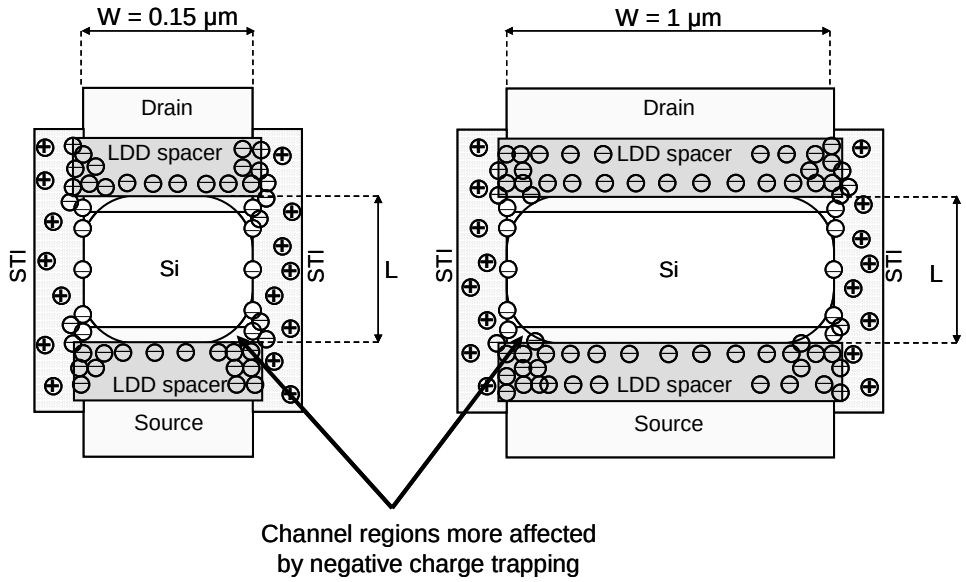


Fig. 5.9: Schematic top view (not to scale) for a narrow (on the left) and wide (on the right) channel MOSFETs. For narrow devices the series resistance is further increased by negatively charged interface states in the STIs close to the drain/source junction.

secondary electrons generated in the overlap area between metal 1 and the source/ drain junctions may cause enhanced charge trapping and interface state generation in the regions directly above the source and drain junctions. A smaller $L_{poly\text{-}M1}$ means that the metal track is closer to the LDD spacers, whose degradation, as we have suggested in the previous section, could be the main cause of the increase in series resistance, that leads to the reduction of $I_{DS,ON}$ with dose in these devices.

Electrons transport code [CASINO] was run to look at the range of 10-keV secondary electrons with initial momentum normal to the layers in low-κ dielectrics for a typical 90-nm CMOS process. Here, the isolation between two consecutive metal layers is ~ 200 nm, the polysilicon is ~ 150 nm, metal 1 is ~ 150 nm, and metals 2 and 3 are ~ 250 nm [Thompson02].

The electron distributions reported in Fig. 5.10 show that the secondary electrons emitted by metal 1 (made of copper) can easily be deposited in the active device area. On the contrary, a smaller amount of secondary electrons emitted by metal 2 (the tail of the distribution) and no one by metal 3 can get to such area. For this reason, a contribution in dose enhancement effects should be expected by only metal 1, the

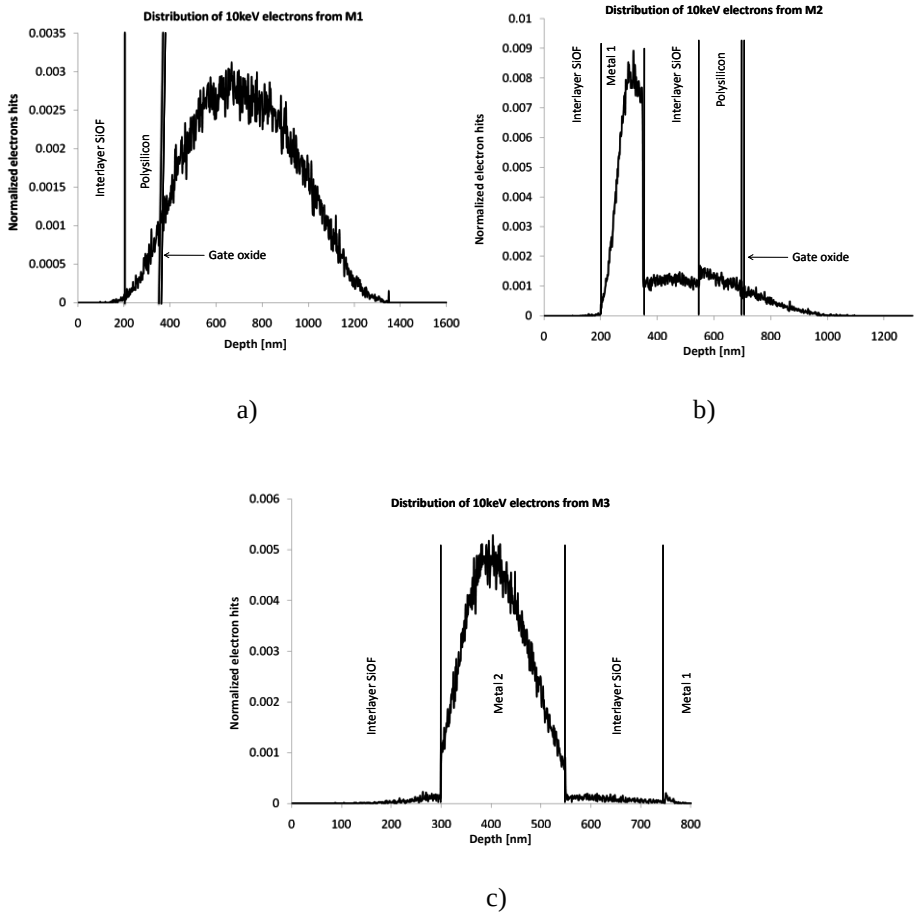


Fig. 5.10: Normalized distribution of 10-keV electron hits emitted by a) Cu metal 1, b) Cu metal 2, and c) Cu metal 3 in a typical 90-nm CMOS process. Notice that the initial momentum of the electrons is normal to the layers.

more because metal layers are made of copper [Solin00].

On the contrary, metals 2 and 3 should not influence appreciably the response of the MOSFET under X-ray exposure, since they are too far from the sensitive regions.

In a similar way, the secondary electrons emitted by the *M1*-plate increase total-ionizing-dose effects in the LDD spacers, and STI. As a result, $I_{DS,ON}$ degradation is larger with the *M1* plate, for a given *M1*-poly spacing.

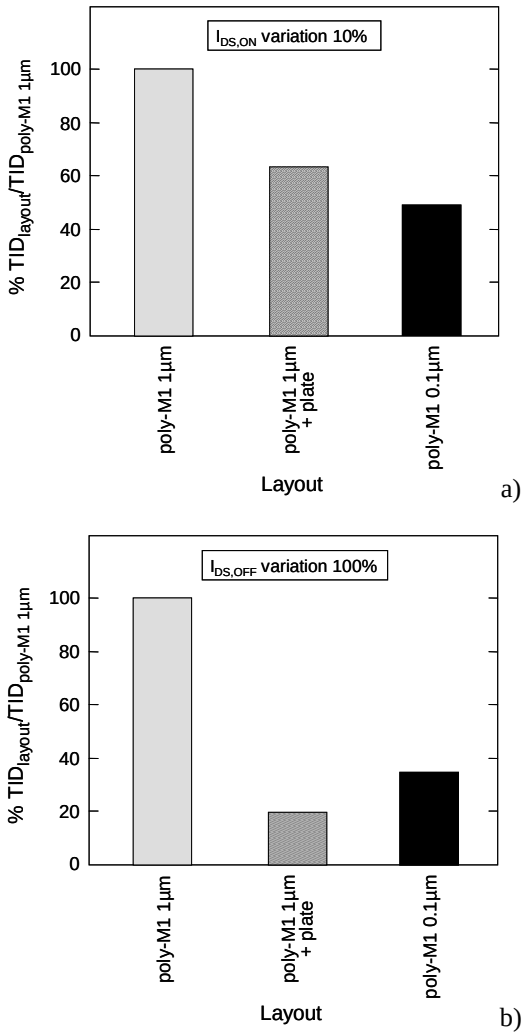


Fig. 5.11: Normalized TID enhancement in a) $I_{DS,ON}$ and b) $I_{DS,OFF}$ as a function of the device layout for transistors with W/L = 0.15 µm/0.13 µm. The normalized TID for each layout is calculated as the TID at which $I_{DS,ON}$ decreases of 10 % or $I_{DS,OFF}$ increases of 100 % normalized to the corresponding TID for a NMOSFET with $L_{poly\text{-}M1}$ = 1 µm and W/L = 0.15 µm/0.13 µm.

Concerning the drain-source leakage current, as we mentioned, $I_{DS,OFF}$ degradation is related to the shift in threshold voltage of the parasitic lateral transistors due to radiation-induced trapped charge in the STI [Faccio05]. Reducing $L_{poly\text{-}M1}$ has a detrimental effect on $I_{DS,OFF}$, since it increases dose enhancement in the lateral isolation. The presence of the metal-1 plate is even more harmful for $I_{DS,OFF}$, because

the overlap area with the STI is larger in this case.

To summarize, the dose to failure of $I_{DS,ON}$ and $I_{DS,OFF}$ as a function of layout is presented in Fig. 5.11 for narrow-channel transistors. The dose to failure for each layout is calculated as the dose at which $I_{DS,ON}$ decreases by 10 % in Fig. 5.11.a, and $I_{DS,OFF}$ doubles in Fig. 5.11.b. All values are normalized to the corresponding dose value of the reference device with $L_{poly\text{-}M1}$ = 1 μm and no plate.

Concerning $I_{DS,ON}$, the presence of *M1* plate reduces the dose at which the device goes out of specification (with respect to the reference sample) by 37 %. A similar result is obtained reducing $L_{poly\text{-}M1}$ from 1 μm to 0.1 μm (48 % of the corresponding dose for a reference sample). Concerning drain-source leakage current, the presence of the *M1*-plate drastically reduces the dose at which $I_{DS,OFF}$ doubles (by 80%). Reducing $L_{poly\text{-}M1}$ has also a very strong impact on $I_{DS,OFF}$, causing a 63% decrease in the dose to failure. These results are quite remarkable compared to the ones in the literature [Hughes03], [Fleetwood03], [McLain07], but we have to remark that the metal layers of our process are made of copper instead of aluminum, which are usually employed, especially as metal 1.

Dose enhancement with gamma-rays due to metal layers is expected to be much smaller than with X rays for two reasons. Photons produced by X rays (~ 10 keV) interact with matter primarily via the photoelectric effect, which scales with Z. On the other hand, higher-energy photons generated by Co^{60} (~ 1 MeV) interact with matter primarily via the Compton effect, which is largely independent of Z. As a consequence secondary electron generation changes considerably from material to material in the first case, and much less in the second [Fleetwood85]. Furthermore, because of the very different range of the secondary electrons generated by X- and γ-rays, only regions close to the area of interest may enhance the dose in the first case. For gamma rays instead, also regions further away can contribute, thus making the overall contribution of metal 1 less important.

5.5. Conclusions

In this chapter a different form of interplay between X rays and device layout has been studied.

Three different devices have been designed with different copper Metal-1 layout in order to understand the influence of the tracks in the proximity of the transistor.

Monte Carlo electrons simulations confirm that only *M1* can influence the device because only secondary electrons from *M1* can reach the active area and the

surrounding device isolations (STI, LDD).

The threshold voltage shift after irradiation up to 30 Mrad(SiO_2) has been found to be small regardless the *M1* layout, $|\Delta V_{TH}| < 15$ mV for the devices with $W = 0.15$ μm and less than 5 mV for samples with $W = 1$ μm. Moreover, no parasitic transistor is visible after irradiation (no humps) and the sub-threshold swing degradation is small as well.

Considering the *M1* layout, the large poly-*M1* spacing affects the drain current after irradiation less than the other samples, independently from transistor geometry. In contrast, concerning drain-source leakage current, the presence of the *M1*-plate drastically enhances the degradation.

The drain current dose to failure for each layout, normalized to the corresponding failure dose of the reference device, shows that the presence of *M1* plate or the shrunk poly-*M1* spacing reduces the dose at which the device goes out of specification (degradation larger than 10 %) by 37 % and 48 %, respectively.

Similarly, concerning the off current, the dose at which $I_{DS,OFF}$ doubles is reduced by 80 % and 63 % if *M1*-plate or the shrunk poly-*M1* spacing is present.

TCAD simulations shows that the only possible way to reproduce the experimental results is to put negative charge in the LDD spacers that are known to be prone to trap electrons. This negative charge possibly leads to an increase in the series resistance consequently reducing the drain current marginally affecting the sub-threshold swing, the threshold voltage and obviously the off current that is due to positive charge in the STIs.

Chapter 6

Single Event Gate Rupture: Impact of Bias and Device Layout

In this chapter, we aim to shed some light on Single Event Gate Rupture in ultrathin oxides by using specially designed capacitors, which are much closer to scaled MOSFETs and that can be biased in inversion, which have been only rarely considered in the literature so far.

6.1. Introduction

Heavy ions are known to plague the operation of space electronics, causing both soft and hard errors. Soft effects like single event upsets or single event transients may lead to a loss of information but no permanent damage is caused to the electronic circuit [Irom07]. Concerning hard errors, many issues are linked to the integrity of the gate oxide, which may subjected to several phenomena, which are, from the most to the less severe: Single Event Gate Rupture (SEGR) [Sexton03], Radiation Soft Breakdown (RSB) [Massengill01], [Conley01], and Radiation Induced Leakage Current (RILC) [Larcher99]. Microdose effects [Poivey94] responsible for stuck bits in SRAM cells irradiated with heavy ions are also possible, even though the thinning of the gate oxide seems to have relieved this problem [Oldhm93]. All of these phenomena may permanently damage circuits in radiation harsh environments and possibly affect their functionality, raising serious reliability problems, especially in

spacecrafts and satellites where maintenance is unfeasible.

In addition to the effects which are observable immediately after the exposure, long-term reliability of irradiated devices is also an interesting field of study. Indeed, a large amount of data have been published about the interplay between heavy-ion strikes and electrical stress [Cester03], [Choi02]. The latent damage produced by radiation may act as a seed for subsequent degradation, and accelerate device ageing. This is an issue both for deep space missions and high-energy physics experiments, which are expected to operate for several years.

SEGR has been traditionally studied in power electronics, due to the catastrophic nature of the failure [Sexton03], [Allen96], [Selva03], [Titus03]. Yet, since the scaling of CMOS technology has led to ever-increasing electric fields, SEGR has become a concern also in low-voltage circuits. Several papers and models have appeared over the years, accounting for the influence of temperature, Linear Energy Transfer (LET), incidence angle, gate oxide thickness, and electric field, recently reviewed by Sexton [Sexton03]. Despite the large amount of work carried out, there are some issues which have not been completely addressed. RSB, RILC, and heavy-ion induced early breakdown have been traditionally studied with large area capacitors, which may not exactly reproduce the sensitivity of real circuits. The same consideration applies to SEGR, which has been often investigated with bias conditions (accumulation) and structures (capacitors), which do not straightforwardly correlate to actual devices. In addition early breakdown was investigated only on devices left floating during irradiation.

6.2. Experimental and Devices

The samples used in these experiments were n- and p- MOS capacitors manufactured by Numonyx with gate oxide thickness of 1.8 nm and surrounded by n- or p- rings to make it possible to bring the devices in inversion. The capacitors, sketched in Fig. 6.1, belong to two groups having the same total area of $1 \cdot 10^{-4}$ cm^2, but different layout in order to investigate possible edge effects:

- Area Self Aligned (ASA): standard square capacitors with side length equal to 100 μm;
- Perimeter Self Aligned (PSA): transistor-like capacitors designed with multiple fingers with length 0.13 μm connected together, in order to maximize the length of the self-aligned border for a given sample area.

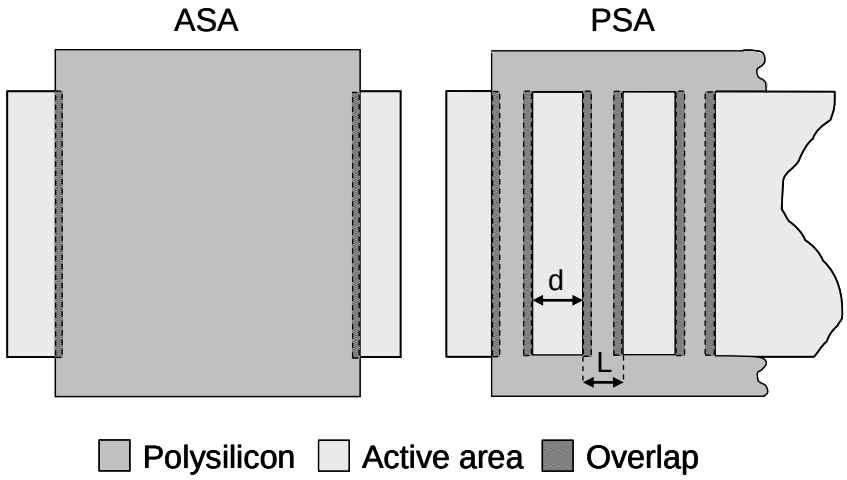


Fig. 6.1 Schematic top-view (not to scale) of ASA capacitor (left side) and PSA capacitor (right side).

Irradiation was performed at the SIRAD facility of the Tandem Van Der Graaf accelerator at the INFN, Laboratori Nazionali di Legnaro (LNL), Italy [Wyss01] with 212-MeV Nickel ions (LET = 28.2 MeV cm^2 mg^{-1}) and 256-MeV Iodine ions (LET = 58 MeV cm^2 mg^{-1}) at different fluxes. During irradiation a staircase voltage was applied at the gate contact keeping the other terminals grounded, to maintain the samples in accumulation or inversion. The gate voltage was raised from ± 1.5 V with steps of 100 mV, each lasting 25 s, until gate-oxide breakdown (BD) occurred. During irradiation we monitored the gate current at the stress voltage ($V_{g\text{-}HV} = V_{gate}$) and at low voltage ($V_{g\text{-}LV}$ = ± 500 mV) in order to maximize the possibility of detecting events in the gate current. All measures were performed with a semiconductor parameter analyzer HP4156B. The data points presented in this work are averaged on at least three samples. The error bars are calculated as the standard deviation of the mean, $\sigma/\sqrt{N}$, with N the number of samples. When not visible in the graphs, the error bars fall within the symbols (smaller than 1-2 %).

6.3. Experimental Results

6.3.1. n-channel MOS Capacitors

Fig. 6.2 shows the low-sense gate current (I_g @ $V_{g\text{-}LV}$ = 500 mV) normalized to the pre-irradiation value, for three different ASA n-MOS capacitors biased in inversion:

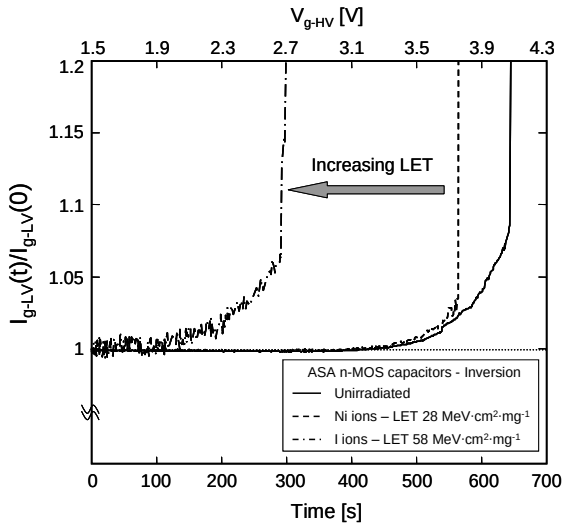


Fig. 6.2 Low sense current ($V_{g\text{-}LV}$ = 500 mV) normalized at the stress beginning as a function of stress-time for ASA n-MOS samples unirradiated and under irradiation with different ions. The staircase gate voltage applied to the gate during stress/irradiation is reported in the upper axis.

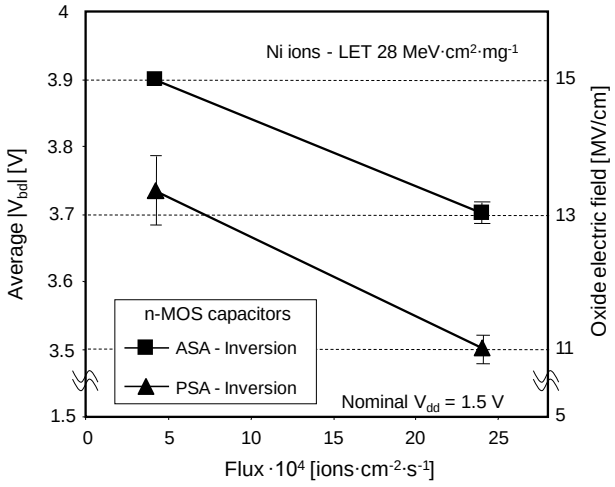


Fig. 6.3 Average voltage to breakdown and oxide electric field as a function of Nickel ions flux for both ASA and PSA n-MOS capacitors biased in inversion.

one was irradiated with Nickel, another with Iodine, and the unirradiated third was electrically stressed as a reference outside of the beam. Each run was performed with the same ion flux 2.4x10^5 ions cm^{-2} s^{-1}.

This behavior is representative of all the samples we tested: the gate clearly breaks

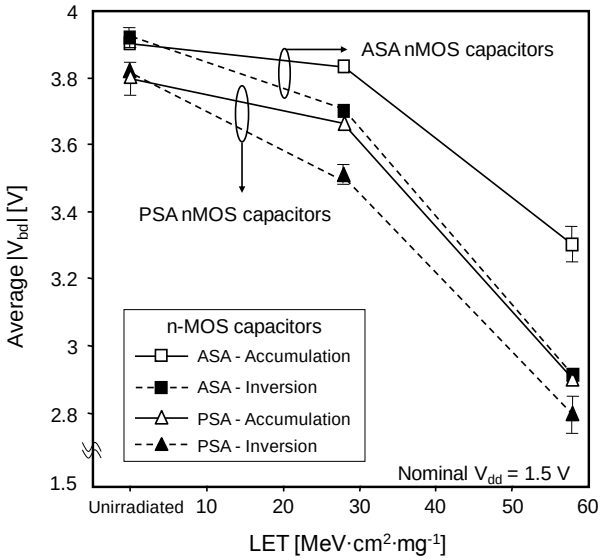


Fig. 6.4 Average voltage to breakdown as a function of LET for both ASA and PSA n-MOS capacitors biased in inversion and accumulation.

down earlier in irradiated samples and a LET dependence is noticeable: the higher the LET, the earlier the breakdown. In fact BD in irradiated samples occur for Iodine and Nickel with a 50 % and 5 % smaller $V_{g\text{-}HV}$ than in unirradiated devices, respectively.

In both irradiated and unirradiated devices, breakdowns are preceded by a substantial increase of the gate leakage current. Concerning the irradiated devices the leakage current grows sooner than in unirradiated samples. Moreover, devices under heavy ion exposure (especially at high LET) exhibit a noisy degradation since the stress start.

Fig. 6.3 reports the dependence of the average breakdown voltage $|\langle V_{BD}\rangle|$ and oxide electric field on the Nickel ion flux for both ASA and PSA capacitors biased in inversion. To calculate the $|\langle V_{BD}\rangle|$ we adopted as breakdown criterion the sudden growth of the low-voltage-sense current. The difference in $|\langle V_{BD}\rangle|$ between low ($4.5\cdot10^4$ ions cm^{-2} s^{-1}) and high ($2.4\cdot10^5$ ions cm^{-2} s^{-1}) flux and between the two kinds of samples is about 200 mV.

Fig. 6.4 shows $|\langle V_{BD}\rangle|$ as a function of LET (for a given flux) for ASA and PSA n-MOS capacitors, biased in inversion (positive voltage) and accumulation (negative voltage). Concerning unirradiated devices, there is negligible dependence on the bias polarity, and PSA samples have a $|\langle V_{BD}\rangle|$ about 100 mV smaller than ASA ones.

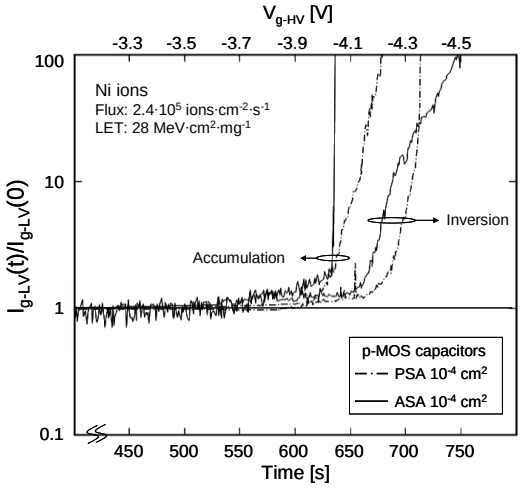


Fig. 6.5 Low sense current ($V_{g\text{-}LV}$ = 500 mV) normalized at the stress beginning as a function of stress-time for p-MOS samples irradiated with Nickel ions. The staircase gate voltage applied to the gate during stress/irradiation is reported in the upper axis.

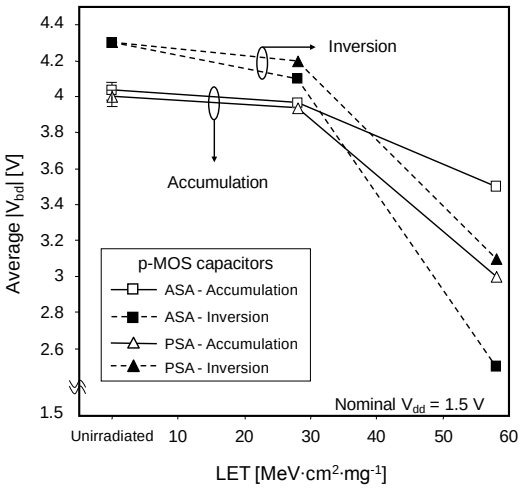


Fig. 6.6 Average voltage to breakdown as a function of LET for both ASA and PSA p-MOS capacitors biased in inversion and accumulation.

On the contrary, under radiation, the bias polarity plays an important role especially at very high LET. In fact, both ASA and PSA devices biased in inversion show a 200-mV smaller $|\langle V_{BD}\rangle|$ than their counterparts biased in accumulation at

LET = 28.2 MeV cm^2 mg^{-1}. At higher LET (58 MeV cm^2 mg^{-1}), ASA capacitors show a very large difference in $|<V_{BD}>|$ (about 400 mV), depending on the irradiation bias polarity, whereas PSA do not change appreciably.

6.3.2. p-channel MOS Capacitors

Fig. 6.5 reports the low-sense gate current ($V_{g\text{-}LV}$ = ±500 mV) normalized to the pre-irradiation value of ASA and PSA p-MOS capacitors, biased in inversion and accumulation during irradiation with Nickel ions. Biasing p-MOS samples in inversion is less severe than in accumulation (for a given applied bias in absolute value) concerning breakdown. Again, the noisiest curve is related to the ASA capacitor (compare Figs. 6.2 and 6.5).

Fig. 6.6 shows $|<V_{BD}>|$ as a function of LET for p-MOS capacitors biased with different polarities. The results on unirradiated devices do not depend on the layout, with ASA and PSA capacitors having the same $|<V_{BD}>|$, whereas especially with Iodine (58 MeV cm^2 mg^{-1}), ASA in inversion and, by a slight margin, PSA in accumulation tend to break down before.

To summarize the results Fig. 6.7 shows the amount of $<V_{BD}>$ change induced by radiation for all the different kinds of devices we analyzed. As shown, the effect of

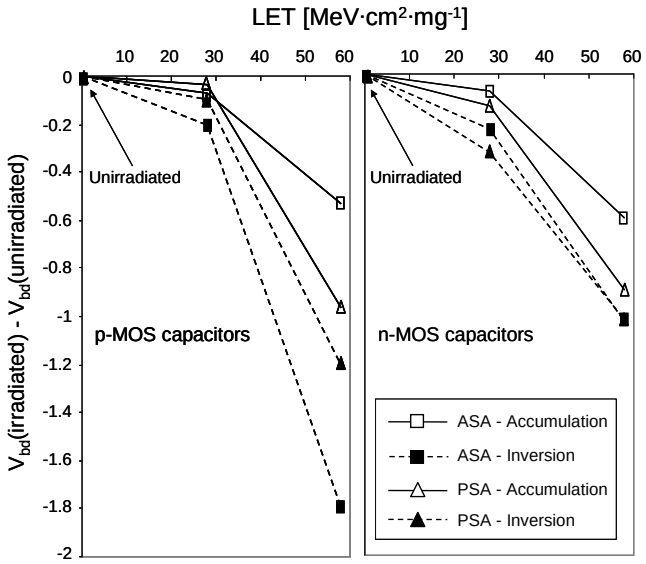


Fig. 6.7 Amount of average voltage to breakdown change induced by heavy ion irradiation for ASA and PSA capacitors kept in inversion and accumulation.

heavy ion irradiation is maximized in devices biased in inversion. Moreover a layout dependence is present in p-MOS capacitors and to a lesser extent in n-MOS ones.

6.4. Discussion and Simulations

6.4.1. Flux Dependence

The flux dependence (Fig. 6.3) is the first striking feature of our results. Johnston et al. [Johnston98], proposed that the impact of fluence on SEGR experiments could be interpreted either in terms of the probability that an ion intercepts a pre-existing damaged area in the gate oxide, or of the gradual oxide weakening due to ion strikes.

When working with ultra-thin gate oxides, one must also consider that the applied voltage itself can generate defects (if the field across the oxide is high enough), which could add up to those created by the impinging ions. As shown in the previous section, the difference between $<V_{BD}>$ in irradiated and unirradiated samples may be quite low, implying that defect generation due to electrical stress is certainly not negligible in both cases.

Yet, in principle this should not give rise to a flux dependence, unless we assume that electrically-stressed defects are not uniformly created in the gate oxide area. In fact, it is well known that gate oxide BD is triggered after a critical defect density, d_{crit}, is reached. Both electrical stress and heavy ions contribute to reach d_{crit}, even though defect generation by electrical stress is usually spread across the whole gate area, whereas the one induced by heavy-ions is limited to the struck positions.

If we assume that no overlapping strikes take place in the gate oxide during irradiation, the defects created by heavy ions are distributed without cumulative effects in the same struck location. At the same time, if the electrical stress creates local regions with higher-than-average defect density, the BD under irradiation could be triggered by a strike in those regions. In turn, the regions where electrical stress has generated more defects could be those which were originally weaker. As a consequence the flux dependence can arise because the larger number of ion strikes, the higher the probability to hit an oxide weak point.

In our experiments overlapping strikes cannot be excluded. The defects generated by a second ion impinging on a region already damaged by a previous particle could trigger the gate oxide rupture, and this process is certainly driven by fluence. The number of ions that impinge on our capacitors during every step (i.e., every 25 s) is about 100 and 600 at Low Flux (LF) and High Flux (HF), respectively. On average

about 2400 Ni ions hit a device at LF before the onset of BD, and this should give rise to about 36 pairs of strikes which are closer than 100 nm. On the other hand, at HF about 13200 Ni ions, corresponding to 1000 double strikes, hit the capacitors.

Another interesting point is that well before the onset of breakdown, increase in leakage current occurs in devices under irradiation at voltages much lower than in unirradiated samples, especially with Iodine. This is probably due to multiple percolation paths, created on the struck positions. The conductivity of these micro spots is modest, much lower than that associated with BD and similar to RILC.

These results may be compared with the early BD observed in similar ultra-thin gate oxides [Cester03], but with an important difference: in the present experiments, the devices were kept under bias during irradiation. This is expected to have a major influence on the radiation-induced defect generation, since the charge yield of heavy ions is greatly influenced by the electric field.

6.4.2. Impact of Bias Polarity

As we discussed in the previous section, the effects of electrical stress add up to those caused by heavy-ion irradiation, at least when the bias voltage is high enough to cause a significant injection of energetic carriers into the oxide. The critical defect density, d_{crit}, necessary to trigger a BD event under heavy-ion irradiation, can be expressed as the sum of two contributions: $d_{crit} = d_{crit,HI} + d_{crit,el.stress}$.

Our results (Fig. 6.7) show that heavy-ion strikes are more effective at creating damage when the devices are biased in inversion during the exposure (i.e., a larger reduction in the average voltage to breakdown occurs in this condition). In other words, the term $d_{crit,HI}$ weighs more in inversion than in accumulation. This behavior is in agreement with [Gerardin05], where deep depletion and accumulation were compared, leading to the conclusion that the carriers heated in the depletion region play a significant role in the breakdown event.

The amplification of the effects of the heavy ion strike in inversion causes the symmetry, which exists in unirradiated NMOS devices between negative and positive bias, to be broken (under no exposure the absolute value of the average voltage to breakdown is the same in accumulation and inversion, Fig. 6.4).

Apparently the electric field associated with the depletion region is not enough to give rise to a substantial generation of energetic carriers. Yet, an ion striking a device in strong inversion perturbs the electric field, extending the depletion region into the silicon substrate, causing the well known funnel effect [Messenger82], [McLain82]. As a consequence, carriers (electrons in n-MOS and holes in p-MOS) could be

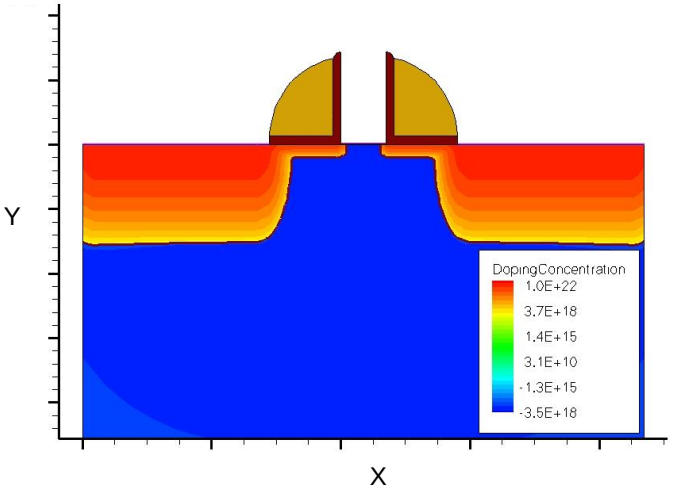


Fig. 6.8 2D structure used to simulate PSA samples.

accelerated in the extended depletion region [Gerardin05], and gain sufficient energy to be injected into the gate-oxide, where they can create defects in addition to the ones possibly generated by the ion itself [Beck08].

According to the model presented by Brews [Brews93], during the passage of a heavy ion the electric field across the oxide splits the electron hole pairs pushing the holes toward the substrate and the electron toward the gate contact (for a positive gate voltage). The swift accumulation of positive charge at the interface (and its counterpart image charge at gate electrode) leads to a fast increase of the local oxide electric field, eventually bringing the device to the breakdown field region few picoseconds after the strike. Although this phenomenon cannot be excluded, the model was applied to vertical power MOSFETs and the correlation with modern shrunk digital devices may not be straightforward (at least for PSA samples).

We can better elucidate the funnel injection mechanism through 2-D TCAD physical simulations. Fig. 6.8 reports the short-channel n-MOS transistor used in our simulations to reproduce PSA capacitors. An identical one in terms of doping profile, but with a longer gate length, was used to simulate ASA capacitors. The heavy ion was modeled according to [Dodd98] with a Gaussian radial track structure. Moreover the strike position was varied from the middle of the channel to the overlap region.

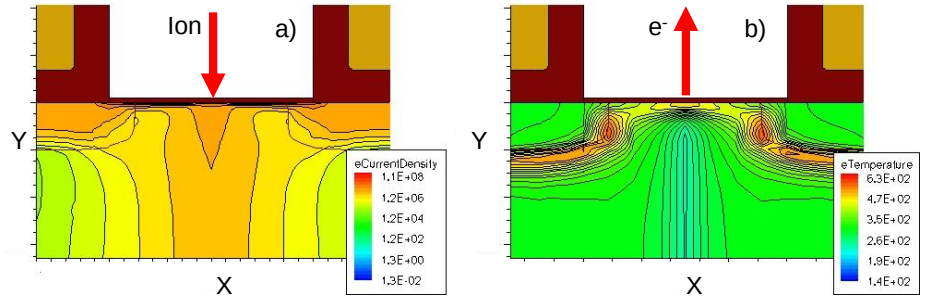


Fig. 6.9 Simulated electron current density (eCurrentDensity [A·cm^{-2}]) and electron temperature (eTemperature [K]) in an inverted n-MOS transistor (V_{gb} = 3.8 V with the other terminals grounded) during a Nickel ion strike. Tunneling could be enhanced because electrons gain energy at the silicon oxide interface.

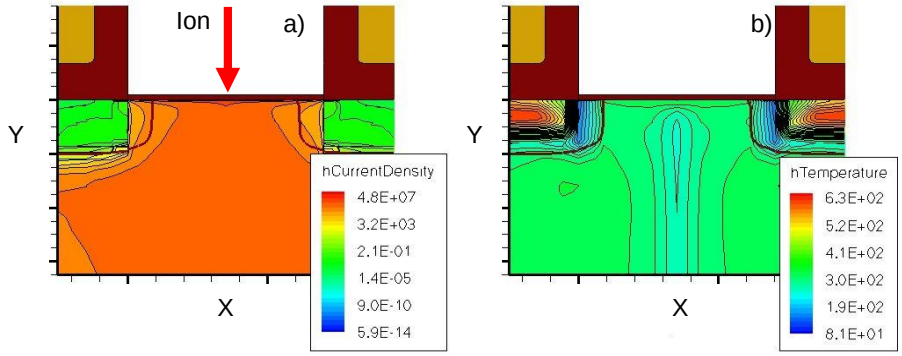


Fig. 6.10 Simulated hole current density (hCurrentDensity [A·cm^{-2}]) and hole temperature (hTemperature [K]) in an accumulated n-MOS transistor (V_{gb} = 3.8V with the other terminals grounded) during a Nickel ion strike. Tunneling is not enhanced because neither electrons nor holes gain energy at the silicon oxide interface.

Fig. 6.9 shows the electron current density and electron temperature in a n-MOS transistor biased in inversion (V_{gb} = 3.8 V, other terminals grounded), when an ion (LET = 28 MeV cm^2 mg^{-1}) hits the middle of the channel.

The drift current is directed toward the gate oxide due to the electric field (Fig. 6.9a). Moreover the energy of the electrons rises at the silicon-oxide interface, as shown in Fig. 6.9b, enhancing the tunnel probability through the gate oxide and the subsequent

damage. For comparison, Fig. 6.10 displays the hole current density and hole temperature in the same transistor as in Fig. 6.9, but now biased in accumulation (V_{gb} = - 3.8 V). Due to the lack of the funnel neither holes nor electrons gain energy at the silicon-oxide interface as shown in Fig. 6.10b. Consequently less carrier-injection-induced damage is produced in the gate oxide when devices are biased in accumulation. The magnitude of this effect is similar in both n-MOS and p-MOS, even though different electric fields and injected species may give rise to variations in the device response.

6.4.3. Impact of Device Layout

The two structures we examine in this chapter differ for the ratio between the overlap and the total gate oxide area. A larger border region is present in PSA samples because of their fingered structure. PSA capacitors are manufactured with minimum-size polysilicon depositions repeated at fixed distance (*L* and *d* in Fig. 6.1, respectively), to have the same area as ASA devices, which are designed with a square polysilicon deposition over an active region. PSA capacitors resemble real transistors more closely than ASA samples, and should be therefore more adapt to estimating gate rupture issues in real integrated circuits. Of course, the different layout causes a much larger number of strikes to occur in border regions in PSA than in ASA devices during heavy-ion exposure.

As shown in Fig. 6.7 the dependence on the layout is quite complex and is possibly due to a combination of different factors which may vary from the channel to the overlap region:

a) Oxide electric field in the overlap region vs. channel
b) Carrier heating in inversion due to heavy-ion strikes (see previous section) in the channel vs. overlap region
c) Pre-existing defects in the channel vs. overlap region

The electric field is the most straightforward element to analyze. The gate oxide of PSA and ASA devices is nominally identical and theoretically the capacitance is the same for high enough voltages. Our TCAD simulations confirm that the oxide field is equal in the two different layouts, but they highlight one important feature. Fig. 6.11 shows the simulated gate oxide electric field in the overlap region normalized to the one in the middle of the channel (slices 1 and 2 in the inset of Fig. 6.11, respectively) as a function of gate voltage for a PSA. The overlap regions display a ~ 3 % larger electric field compared to the middle of the channel in inversion.

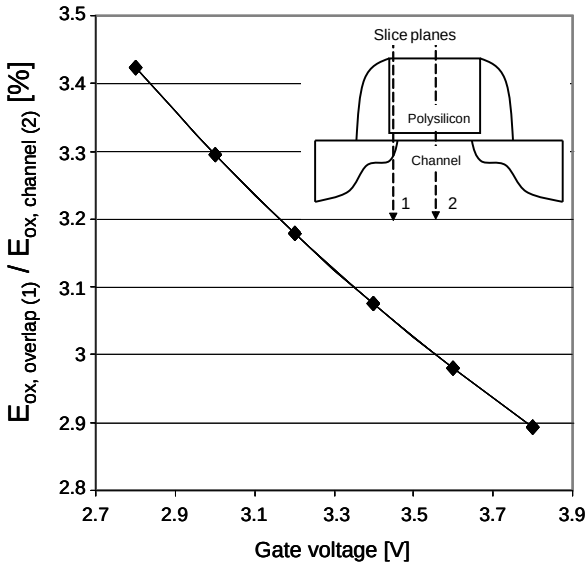


Fig. 6.11 Gate oxide electric field in the middle of the overlap region (1) normalized to the one over the channel (2) as a function of the gate voltage.

The area occupied by the overlap regions is almost negligible in ASA, whereas it is a large part of PSA. As a result, the ~ 3 % less $<V_{BD}>$ exhibited by unirradiated nMOS PSA compared to ASA capacitors (Fig. 6.4) could be attributed to the higher electric field in the large overlap area.

The same relationship between the electric field at the border and in the middle of the channel holds for accumulation as well. A higher electric field in the overlap region means that a strike there will have a larger charge yield and higher probability of inducing damage in the oxide. This correlates very well with the experimental behavior (Fig. 6.7), which shows that the reduction in the average breakdown voltage of PSA is larger than that of ASA.

Moreover hits (or double hits) in the gate area over the channel may create more defects than those occurring on the overlap regions in inversion. The reason is shown in Fig. 6.12a: a strike in the middle of the channel of a pMOS structure generates a substantial number of energetic holes, which can be injected into the oxide by the electric field and create defects. On the contrary, a strike in the overlap does not cause holes to significantly gain energy as illustrated in Fig. 6.12b. This fact causes ASA

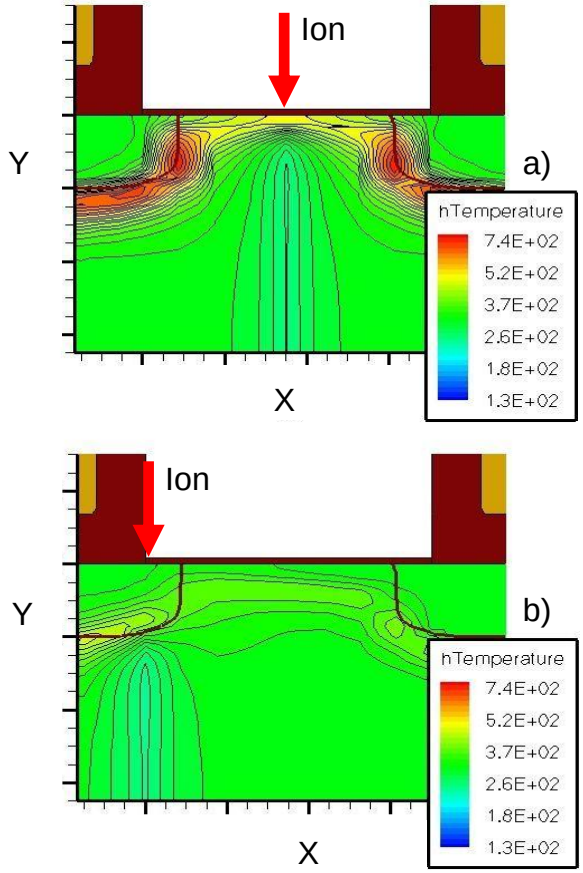


Fig. 6.12 Simulated hole temperature (hTemperature [K]) in an inverted p-MOS transistor (V_{gs} = -3.8 V other terminals grounded) during a Nickel ion strike a) in the middle of the channel b) in the overlap. Tunneling through gate oxide is not enhanced when the ion hits the overlap because the funnel is distorted by the LDD.

capacitors to have a stronger reduction in $<V_{BD}>$ due to heavy ions than PSA devices (Fig. 6.7).

The final factor is the presence of pre-existing process-related defects, which may explain some weak dependences observed in our data. For instance, halo implantation involves only the regions close to the source and drain junctions and may give rise to some defectiveness in those regions.

6.5. Conclusions

In this chapter the influence of bias regime and device layout have been analyzed. Two different capacitors layout have been designed in order to study the impact of the borders, characteristics of shrunk devices.

The gate oxide during heavy-ion irradiation breaks down earlier as compared to unirradiated devices. Moreover the higher the LET, the earlier the breakdown. In fact breakdown occurs respectively for Iodine and Nickel ions with a 50 % and 5 % smaller gate voltage as compared to unirradiated devices stressed outside of the beam for reference.

Under heavy ions, the bias polarity becomes a key point. In fact, both device layouts biased in inversion show a smaller voltage to breakdown (more closed to operative voltage) than the others biased in accumulation. Moreover, this behavior is enhanced when the LET is increased. This behavior, confirmed by TCAD simulations, is attributed to the carriers that can be heated in the channel region accelerated by the distorted field (funnel) immediately after the ion strike.

The dependence on the layout has been found to be complex and dependent on several factors. Our simulations indicate that the gate oxide electric field is about 3-4 % larger in the overlap regions than above the channel. As a consequence, more damage can be produced in that zone of the gate oxide in addition to the intrinsic ones. On the other hand, an ion strike in the overlap region cannot enhances the mean energy of the electrons due to the presence of the LDDs but, in contrast, the presence of pre-existing defects can weak the gate oxide leading to premature breakdown.

Chapter 7

Single Event Gate Rupture: Impact of X-ray exposure

In this chapter a study of the influence of precursor damage, produced by 10-KeV X rays up to very high TID levels, on single event gate rupture in 130-nm CMOS transistors is presented. Through the use of dedicated test structures, the impact of heavy-ion irradiation, TID, and high bias on gate oxide integrity is evaluated.

7.1. Introduction

Single event effects (SEE) induced by heavy ions present a continual reliability challenge to the operation of the electronic devices used in radiation harsh environments, such as space and HEP experiments. The effects produced by heavy ions hitting a sensitive part of an integrated circuit can be complicated, and depend on several factors related to the ion (LET, energy, incident angle) and to the characteristics of sensitive devices. Non-destructive phenomena have been observed such as a bit-flips in an SRAM cell, charge loss from flash memory floating gate, stuck bits, microdose effects, Single Event Functional Interrupt (SEFI) [Cellere04]. However, heavy ions can induce also destructive events such as burn-out of a power MOSFET, and gate rupture [Allen96], [Johnston98], [Selva03]. The probability of

catastrophic events, such as Single Event Gate Rupture (SEGR) must be carefully assessed, especially when maintenance is unfeasible, like in spacecrafts and satellites, or quite problematic, like in HEP experiments. In the latter case, thousands to millions of electronics channels operate in tracker detectors very close to the collision point, and reliability must be ensured for many years under extremely high levels of radiation [Candel05].

The use of modern CMOS devices even below the 130-nm technological node in radiation-harsh environments rises concerns about the long-term reliability due to the continuous increase of the operative electric fields [Dennard07]. Concerning total ionizing dose effects, even if the lateral isolation (STI) still represent the Achilles' heel of modern CMOS devices [Barnaby06], the very thin gate oxides used nowadays are much less sensitive. Considering SEGR, the sensitivity of modern scaled devices is reduced as well (in spite of the higher electric field) as compared to thicker and older oxides [Sexton03], even when new high-κ dielectrics are used [Massengill01].

Besides the large amount of TID accumulated in the front-end electronics of future HEP experiments, Single Event Effects (SEE) are expected due to the large number of fast hadrons produced by particle collisions at the center of the experiments. Secondary ions generated by nuclear reactions of fast hadrons with chip and transistors materials [Beck08], may pose a serious threat to the gate oxide of the front-end electronics.

Past works demonstrated that irradiation with γ-rays below 1 Mrad(SiO_2) do not impact SEGR occurrence in MOS capacitors [Lum04] and power MOSFETs [Titus96]. Similarly, precursor damage generated by heavy ions was found to have minor influence on SEGR [Sexton98], but was shown to contribute to the lifetime reduction of the devices [Cester03], [Choi02]. In contrast, proton irradiation was found to reduce the SEGR critical voltage of power MOSFETs subsequently subjected to heavy ion irradiation [Scheick07]. However, tests have never been performed with the high TID levels expected in the SLHC in deep submicron devices, as carried out in this work.

7.2. Experiments and Devices

We performed our experiments with a dedicated test chip defined and designed to asses SEGR on realistic CMOS transistors. Three transistor arrays have been integrated in the chip, each made up of MOSFETs with gate oxide thickness of 2.2 nm, whose source, drain, and bulk were short-circuited, while all the gates were

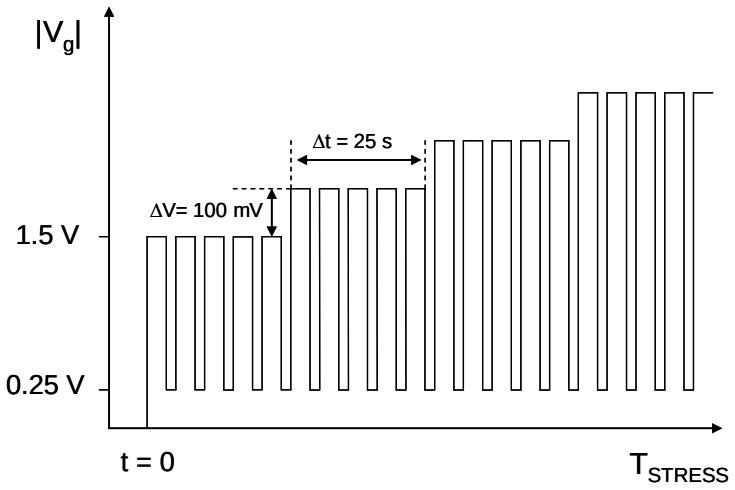


Fig. 7.1. Simplified representation of the staircase voltage used in our experiments (not to scale). It starts from 1.5 V and is updated by 100 mV every 25 s until breakdown occurs. Periodically we sample the current at 250 mV in order to detect soft breakdown events.

connected in parallel by metal interconnects. Each array is designed to have one bonding pad for source, drain, and gate. Close to the gate bonding pad, a double diode protects the structure from plasma damage and electrostatic discharge events.

The three arrays were designed as follows:

1. NMOS-A: NMOSFET array composed of large elements (limits are imposed by design rules in the used technology). The individual element size has been chosen to be 15x15 μm^2. 354 such elements are connected in parallel, for a total gate area of 79650 μm^2. Each individual gate is connected to a protection diode (n+ in p-substrate) to prevent plasma damage during manufacturing.
2. NMOS-B: This capacitor has the same total gate area of NMOS-A, but has been designed with a larger number of elements (318600), each with a much smaller gate area of 0.5x0.5 μm^2. These basic elements are grouped in building blocks of 900, so that the gate area of each is the same as the individual element in NMOS-A (225 μm^2). Each such block has ten protection diodes (n+ in p-substrate).
3. PMOS-A: This capacitor is geometrically identical to NMOS-A, but in this case the basic transistor is a p-MOS instead of an n-MOS. All protection diodes are the same.

The LHC and SLHC inner tracker radiation environment is mainly characterized by the presence of protons. According to [Paillet02], charge yield of 10-keV X rays more closely matches that of protons than ^{60}Co gamma rays. Moreover, the need to accumulate very high doses in a reasonable amount of time led us to choose the CERN 10-keV X-ray facility. We irradiated the samples with a fixed dose rate of 25 krad(SiO_2)/min, keeping the devices in the worst-case bias condition during irradiation (all terminals grounded except the gate of the NMOS transistors, kept at V_{dd}). We measured the I_g-V_{gs} before and after the exposure. While some samples were exposed to 30-100 Mrad(SiO_2), doses of interest for SLHC applications, others were irradiated to 3 Mrad(SiO_2), a level of TID known to produce the worst-case response for lateral source-drain leakage current [Faccio05].

Both X-ray pre-irradiated and unirradiated samples were then subjected to heavy-ion irradiation at the Cyclone Heavy Ion Facility (HIF), Louvain-la-Neuve, Belgium, with 756-MeV Krypton ions (LET = 32.4 MeV cm^2 mg^{-1}) at a fixed flux of 2 x 10^4 s^{-1} cm^{-2}. During heavy ions experiments the staircase voltage shown in Fig. 7.1 (with sampling at low gate voltage) was applied at the gate contact [Cester03], [Silvestri09], [Gerardin05], keeping the other terminals grounded in order to maintain the samples in inversion. The gate voltage was raised from ± 1.5 V with steps of 100 mV, each lasting 25 s (voltage ramp rate 4 mV s^{-1}), until gate-oxide breakdown (BD) occurred. The breakdown voltage V_{BD} in these tests is taken as the voltage at which $I_{g\text{-}LV}$ suddenly increases (remaining stable) more than one order of magnitude. After the event, a conductive path through the gate dielectric of (at least) one of the transistors in the array is present. During irradiation we monitored the gate current at the stress voltage ($V_{g\text{-}HV}$) and periodically (every second) we sampled the gate current at low gate voltage ($V_{g\text{-}LV}$ = ± 250 mV) in order to detect soft breakdown events [Conley01]. The $V_{g\text{-}LV}$ sense voltage does not stress at all the gate oxide, but it is useful to control the low leakage current otherwise masked by the high tunneling current measured at stress voltage ($V_{g\text{-}HV}$).

7.3. X-ray Irradiation Results

Fig. 7.2 shows the gate current as a function of the gate voltage (I_g-V_{gs}) for unirradiated and for X-ray irradiated NMOS-A and NMOS-B samples at different total ionizing doses. We show the curve mainly in inversion, because we cannot apply a large negative voltage (V_{gs} < ~ -0.5 V) to the gate, in order not to turn on the protection diode.

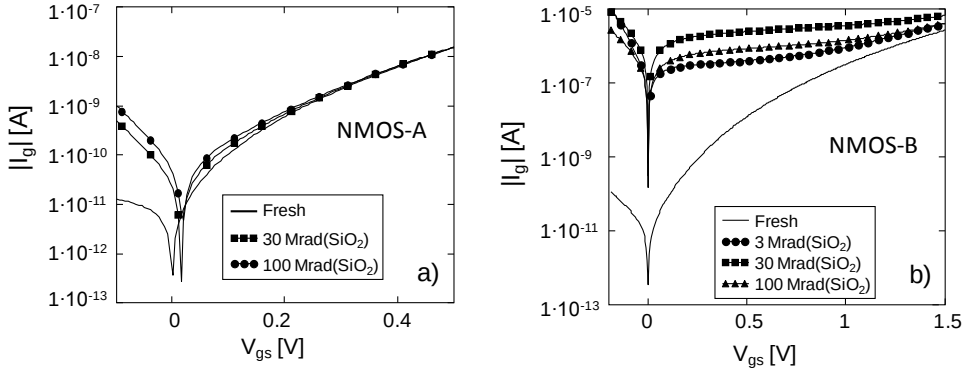


Fig. 7.2 Gate leakage current as a function of the gate voltage for different amount of X-ray exposure in a) NMOS-A and b) NMOS-B samples

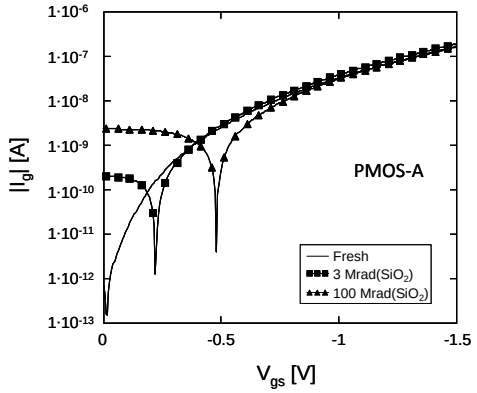


Fig. 7.3 Gate leakage current as a function of the gate voltage for different amount of X-ray exposure in PMOS-A samples.

NMOS-A arrays, presented in Fig. 7.2a, exhibit only a slight increment in the leakage current with dose up to 100 Mrad(SiO_2), visible at very low gate voltages (100-200 mV). As for NMOS-B (Fig. 7.2b) the current of the irradiated samples overlaps the one of the unirradiated ones for higher gate voltages (above 0.4 V).

In contrast NMOS-B arrays presented in Fig. 7.2b display a large increment in the gate leakage current of about three orders of magnitude at 250 mV after 30 Mrad(SiO_2). The leakage current measured after 100 Mrad(SiO_2) is almost one order of magnitude below the one taken after 30 Mrad(SiO_2), and close to that after

3 Mrad(SiO_2). Moreover at low voltage the leakage current changes sign, and the voltage at which this occurs moves toward more positive gate voltage values (about 15 mV) after irradiation. A larger shift of that voltage (current inversion) is observed in the I_g-V_{gs} of PMOS-A devices as a function of TID, as shown in Fig. 7.3. We found about 250 mV and 500 mV after 3 and 100 Mrad(SiO_2), respectively. Again the current exhibited by irradiated samples rejoins the one related to unirradiated ones at higher gate voltages. We want to remark that for large enough gate voltages, no radiation induced leakage current is visible. This behavior is representative of at least three samples for each dose level and array structure.

7.4. Heavy-Ion Irradiation Results

7.4.1. Samples not Irradiated with X rays

Fig. 7.4a shows the gate leakage current taken at low sense voltage ($I_{g\text{-}LV}$ at 250 mV) as a function of stress time for an NMOS-A device measured outside of the beam and one under heavy-ions beam. Correspondingly in Fig. 7.4b the $I_{g\text{-}LV}$ is reported for NMOS-B devices. In both plots the transistor arrays were not previously irradiated with X-rays.

The breakdown event occurs earlier under heavy ion irradiation, displaying 100-mV reduction in the rupture voltage (V_{BD}) for both structures. Neither progressive breakdown (PBD) nor leakage current increase were detected, and both NMOS-A and NMOS-B exhibited a soft breakdown (~ 10^{-6} A) followed by a hard one (~ 10^{-3} A). On the contrary, there is a slight increase (< 10 %) in the gate current in the devices stressed outside of the beam that starts when the gate ramp has reached 4 V.

Unlike the NMOS devices, PMOS samples exhibit a leakage current increase before breakdown during stress both outside and inside the heavy-ion beam without any relevant effect. Moreover, heavy ions do not influence the V_{BD} significantly.

7.4.2. X-ray Irradiated Samples

Fig. 7.5 shows the $I_{g\text{-}LV}$ during heavy ion exposure of unirradiated samples reported with dotted lines (solid line in Fig. 7.4) and previously X-ray irradiated ones up to 100 Mrad(SiO_2), NMOS-A (Fig. 7.5a) and NMOS-B (Fig. 7.5b) samples.

As shown in Fig. 7.2 the effect of total dose on the gate leakage is remarkable only in NMOS-B arrays featuring a leakage current of 10^{-7} A instead of 10^{-9} A (taken at 250 mV) exhibited by fresh devices.

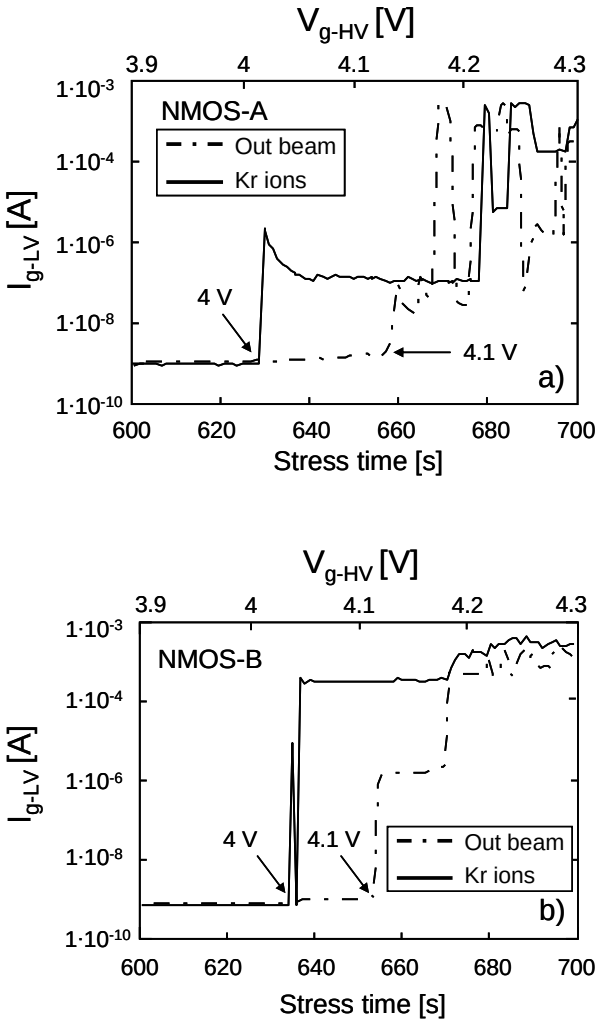


Fig. 7.4 Gate leakage current (taken @ 250 mV) as a function of stress time and gate voltage for devices stressed outside and under Kr ion beam not previously irradiated with X-rays. a) NMOS-A samples, b) NMOS-B samples.

On the other hand X-ray irradiated NMOS-A devices (Fig. 7.5a) display only about $1{\cdot}10^{-9}$ A more leakage current as compared to unirradiated ones. Although the TID effects are visible and not negligible (at low voltage) they do not influence the breakdown occurrence even after 100 Mrad(SiO_2). In fact we found the same V_{BD} (4 V) under heavy ions with and without previous X-ray irradiation, with a difference in time between the ruptures of few seconds.

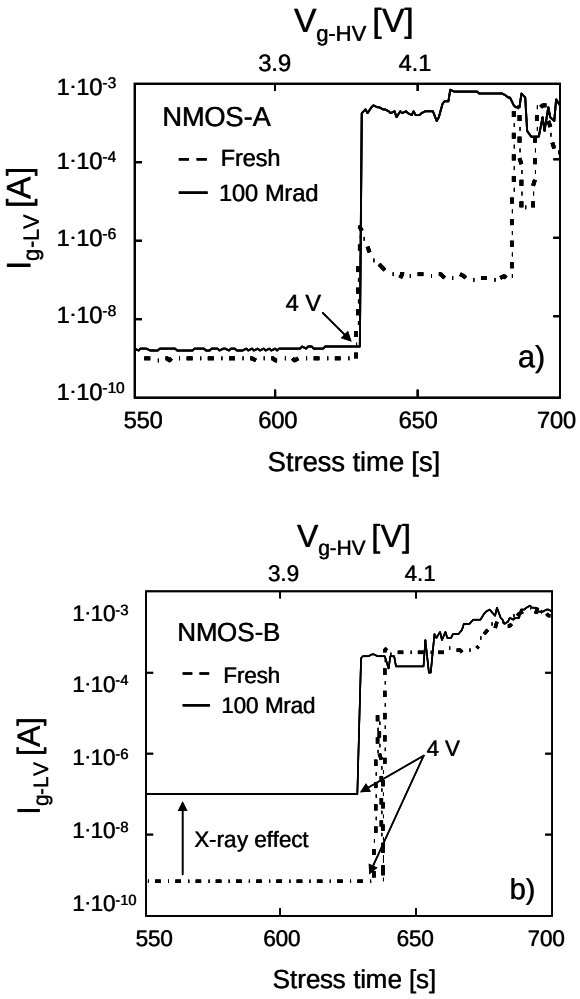


Fig. 7.5 Gate leakage current (taken @ 250 mV) as a function of stress time and gate voltage for unirradiated and previously irradiated with X-rays up to 100 Mrad(SiO2) stressed under heavy ion beam. a) NMOS-A samples, b) NMOS-B samples.

Fig. 7.6 reports the results for NMOS-B samples previously irradiated with X-rays up to 3 Mrad(SiO_2). As opposed to the 100 Mrad(SiO_2) X-ray irradiation shown in Fig. 7.5b, the 3 Mrad(SiO_2) exposure leads to an earlier degradation under heavy ions. The hard rupture in X-ray irradiated samples happens between 3.8 V and 3.9 V, about 100 – 200 mV before the rupture of the device irradiated with heavy ions but with no previous TID exposure. The sudden current drop visible with the long dashed line around 620 s is due to melting of the gate interconnection (which is not designed to

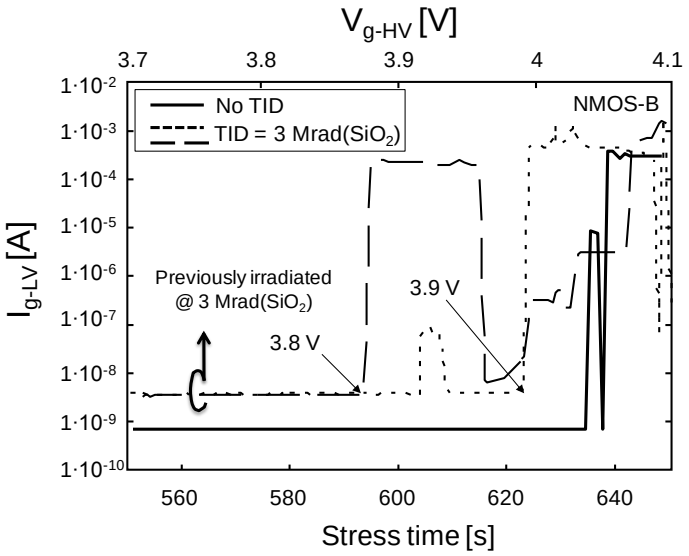


Fig. 7.6 Gate leakage current (taken @ 250 mV) as a function of stress time and gate voltage for NMOS-B arrays unirradiated and previously irradiated with X-rays up to 3 Mrad(SiO_2) subsequently stressed under heavy ion beam.

carry high currents) that changes the series resistance and consequently the current. On the contrary, the temporary increase exhibited by the other sample (short dashed line) is a transient conduction through the gate dielectric probably due to unstable defects, often observed before breakdown [Degraeve98].

X-rays irradiated PMOS arrays do not display appreciable influence on V_{BD} neither at 3 Mrad(SiO_2) nor after 100 Mrad(SiO_2).

We want to point out that the results presented in the previous sections are representative of all the samples we tested. The slight V_{BD} differences we found (5-7 %) may grow with higher ion LET according to previous data reported on similar 130-nm CMOS technology [Silvestri09]. However, even if we are confident about our conclusions, the experimental uncertainty is comparable to the observed differences.

7.5. Discussion

The use of test structures as close as possible to real CMOS transistors was recommended to have a realistic assessment of SEGR issues in submicron CMOS

technology [Silvestri09]. However, the structure presented in the previous chapter was still different from real transistors because the polysilicon fingered capacitors were shrunk only in one dimension (the "channel" length was 130 nm) while the width was 100 μm. In this work we used transistor arrays designed with a large number of 130-nm CMOS transistors close together with source and drain shorted by design and with the gates connected in parallel. These structures allows us to perform a SEGR test on a large number of theoretically identical devices at the same time, increasing in this way the probability of an ion strike in the gate region.

We have shown in Fig. 7.4 the comparison between NMOS-A and NMOS-B samples (without previous X-rays) stressed outside and under the heavy ion beam. The small difference between the V_{BD} obtained with and without Kr ions may suggests that we are dealing with Time-Dependent Dielectric Breakdown phenomenon [Stathis01] rather than a single effect induced by a heavy ion. Indeed, the high applied voltage at the gate contact leads to injection of energetic carriers through the gate oxide due to the well known Fowler-Nordheim tunneling mechanisms. The energy released by the interaction between those carriers and the lattice generates defects [Stathis01], which could add up to those created by the impinging ions. However, the degradation observed in these experiments is different from previous tests [Silvestri09], [Gerardin05], where a clear increase in the leakage current was observed before the hard breakdown due to potential synergism between damage induced by ions and the stress voltage.

In order to understand the influence of the rate at which the gate voltage increases during these SEGR tests we used two different rates: the Slow Ramp (SR) was 1 mV/s (100 mV every 100 s) and the Fast Ramp (FR) was 4 mV/s (100 mV every 25 s).

The number of ions that struck the whole array area (including source and drain overlaps of each transistor in the array) during every SR-step (i.e., every 100 s) is about 1600. On average about 4×10^4 Kr ions hit the array before the onset of the breakdown. The number of ions that strike the entire available gate area (including source and drain overlaps of each transistor in the array) during every FR-step (i.e., every 25 s) is about 400; and on average about 9600 Kr ions hit the entire array before breakdown.

Multiple hits in the single MOSFET gate area cannot be excluded, especially for NMOS-A arrays designed with 15x15 μm^2 MOSFETs. Considering a track radius of 100 nm [Dodd05], 400 and 1600 strikes per step lead to zero and about one couple of strikes closer than 100 nm, respectively. As a consequence, overlapping hits can occur mainly when SR-stress rather than FR-stress is used.

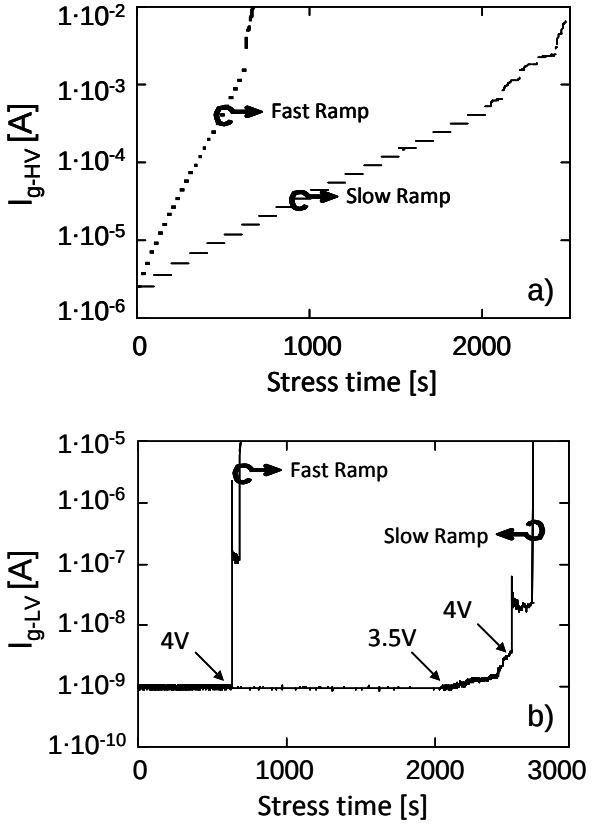


Fig. 7.7 Gate leakage current as a function of stress time for a NMOS-A stressed with two different gate ramp rates under heavy ions: a) taken at stress voltage, b) taken at 250 mV (see Fig. 1).

The comparison presented in Fig. 7.7 shows a different behavior when we applied the SR as opposed to the FR during heavy ions exposure. While the breakdown is abrupt with the FR, in the case of the SR the low voltage leakage current $I_{g\text{-}LV}$ as well as the stress current $I_{g\text{-}HV}$ increase progressively before the final rupture, starting from 3.5 V (2000 s).

In Fig. 7.8 we report in detail the comparison between two SR experiments performed with one device under Kr ions (Fig. 7.7) and another one out of the beam for reference. No increase in $I_{g\text{-}LV}$ is detected until 2000 s (3.5 V) for both devices suggesting that the density of ions-induced and stress-induced defects is not enough to affect the integrity of the gate oxide. However, something happens around 2040 s (3.5 V) and the device under heavy ions starts to degrade progressively until the soft

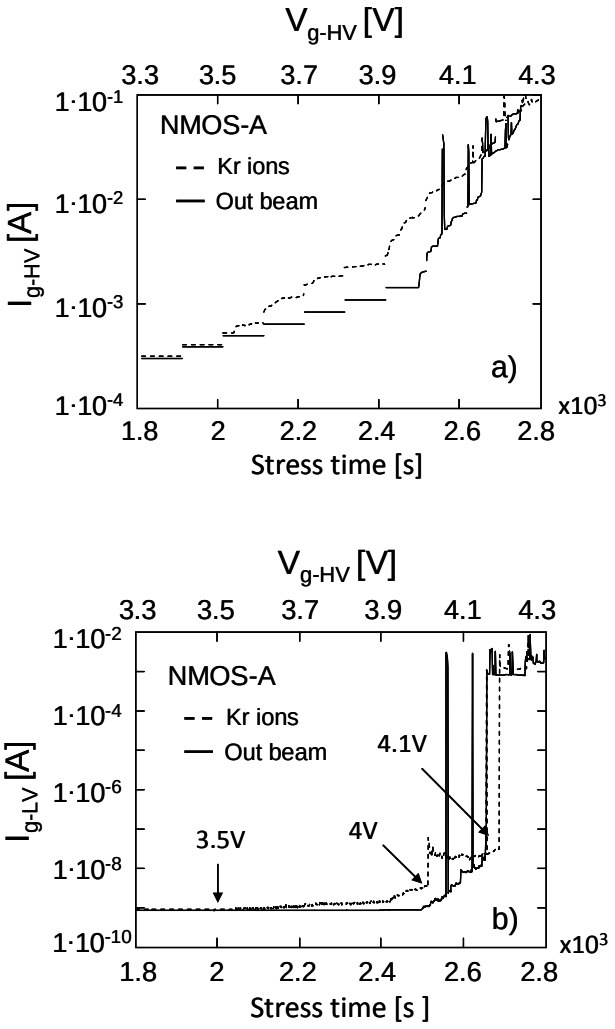


Fig. 7.8 Gate leakage current as a function of stress time and gate voltage for a NMOS-A stressed outside of the beam and under Kr ions during slow ramp (SR) experiments: a) taken at stress voltage, b) taken at 250 mV (see Fig. 7.1).

breakdown (SBD) and the hard breakdown (HBD) occur around 2500 s (4 V) and 2680 s (4.1 V), respectively.

In the meantime, the sample stressed outside of the beam reaches about 2500 s (4 V) with no gate current increase, then it breaks down progressively accordingly to what has been found in similar ultra-thin oxides [Monsieur01], until 2650 s (4.1 V) when

the intrinsic HBD occurs (a similar behavior is found, to a lesser extent, in the NMOS-B samples where the degradation starts from 3.6 V).

Similarly, the devices tested outside of the beam during FR stresses show the $I_{g\text{-}LV}$ increase (less than 10 %) only after 4 V reaching the intrinsic HB at 4.1 V (see Fig. 7.4). However, we want to emphasize that all the FR experiments under heavy ions exhibit a sudden rupture of the gate dielectric with no leakage current progression. As a consequence, from the electrical stress point of view the comparison between the two procedures suggests that these two different ramp rates do not influence appreciably the SEGR occurrence, since the reference devices (stressed outside of the beam) starts to degrade only after ~ 4 V regardless of the $V_{g\text{-}HV}$ rate (compare Figs 7.4 and 7.8).

In contrast, the longer the stress step (slow ramp) the larger the cumulative damage produced by ions as demonstrated in Fig. 7.8 (higher fluence and double hits per step). These results lead us to assume that the FR-stress limits the influence of cumulative damage produced by the passage of the heavy ions helping us to better discriminate the influence of pre-existing X-ray-induced defect on SEGR incidence.

As shown in Figs. 7.2 and 7.3 we can definitely observe that X-ray irradiation has affected the arrays. In fact, the gate leakage current increases due to the presence of traps in the SiO_2 band gap that favor the carrier tunneling through the gate oxide, deeply investigated and known as Radiation Induced Leakage Current (RILC) [Ceschia99], [Larcher99].

However, it is worth highlighting how the amount of leakage current exhibited by NMOS-B samples in Fig. 7.2b is larger than what has been previously published for irradiated capacitors with thicker oxides [Ceschia99]. Also the rebound in the gate leakage current is in contrast with previous results, where a monotonic degradation with TID was reported. This rebound, though, reflects the behavior of the drain-source leakage current (I_{off}) that was found especially in narrow transistors [Faccio05].

This inconsistency with previous data can be justified by the difference in the test structures: whilst in [Ceschia99] large area CMOS capacitors were used (gate area 10^{-2} cm^2), this work uses arrays of real deep-submicron CMOS transistors, each surrounded by lateral oxide isolation (STI) that after X-ray irradiation, traps charge and develops interfaces states that influence the electrostatics of the transistors. In fact, for the same 130-nm technology, the threshold voltage shift induced by X-ray irradiation was found to be maximized around 1-3 Mrad(SiO_2) [Faccio05].

The comparison between NMOS-A and NMOS-B reported in Fig. 7.2 as well as PMOS-A reported in Fig. 7.3, suggests the presence of a parasitic leakage path

through the NMOS-B and PMOS-A arrays. However, all the X-ray irradiated devices exhibit the behavior reported in Figs. 7.2 and 7.3, hence we are dealing with a systematic degradation of the arrays. As a consequence, the current exhibited after irradiation (at low voltage) is a sum of RILC and parasitic leakage that however has not a significant impact on single event gate rupture, since at the stress voltage (V_{gs} > 1.5 V) the gate current is the same regardless of the previous irradiation.

It is interesting to point out that at the very high dose of 100 Mrad(SiO_2) we do not observe remarkable effects during Kr ion experiments (see Fig. 7.5). There is no leakage current increase before breakdown and the V_{BD} is 4 V as for the arrays not previously irradiated with X-rays. We only found an earlier breakdown (few seconds) but we cannot attribute it to the X-ray-induced defects.

Concerning the 3 Mrad(SiO_2) irradiated samples, whose results are reported in Fig. 7.6, we found a more clear earlier breakdown around 3.8 V and 3.9 V. Even if the breakdown definitely occurred at lower V_{gs}, the 5-7 % V_{BD} difference exhibited at this LET, as compared to devices stressed outside of the beam, may fall within the experimental error. However, 200-300 mV lower V_{BD} is in agreement with the results obtained with 212-MeV Nickel ions (LET = 28.2 MeV cm^2 mg^{-1}) in a similar 130-nm technology [Silvestri09]. Since the gate current measured at stress voltage (V_{gs} > 1.5 V) is not affected by X-ray irradiation as seen in Figs. 7.2 and 7.3 we cannot ascribe the observed V_{BD} differences to the stress current itself. In fact, a different injection rate of charge during stress can lead to a later or earlier breakdown [Martin96]. In this case, the reason for this earlier BD may be attributed to the different concentration of positive trapped charge and interface states present in the structures before heavy ion exposure, as pointed out in [Lum04], [Scheick07]. The presence or absence of a spatial distribution of charge induced by X-ray irradiation in the device can lead to a different local electric field in the oxide, in particular close to the transistors edges. In fact, at this dose rate, a high level of TID in CMOS MOSFETs is mainly characterized by the presence of interface states while positive trapped charge is the main phenomenon at low doses, even if the concentration is low for gate oxide thickness below 3 nm [Barnaby06].

The critical defect density to onset the breakdown $d_{crit\text{-}BD}$ is given by the sum of ion-induced defects $d_{heavy\text{-}ions}$ and applied bias induced ones d_{bias}. When $d_{crit\text{-}BD}$ is reached, a conductive path through the gate oxide is formed, and the current is then able to flow inducing the thermal runaway and finally the breakdown [Stathis01]. With previous X-ray exposure, the defect generation rate is possibly modulated by the presence of positive trapped charge and interface states (generated by X rays) that locally change

the net oxide electric field. As a consequence, the electric field enhancement generated by positive charge trapping may cause the breakdown voltage to slightly decrease at 3 Mrad(SiO_2). On the contrary, after 100 Mrad(SiO_2), the larger number of negatively charged interface states compensate the positive trapped charge at the bulk-oxide and bulk-STIs interfaces, possibly reducing the local oxide electric field and consequently the impact on V_{BD}.

7.6. Conclusions

In this chapter the TID influence on SEGR critical voltage (V_{BD}) has been studied for the first time in real advanced CMOS transistors.

After X-ray exposure I-V curves have been affected by damage induced by radiation but only a slight impact on SEGR critical voltage is found.

Krypton-ion irradiation does not affect dramatically the SEGR critical voltage of these transistor arrays, in fact the voltage to breakdown (around 3.9 V) lies far above the nominal operative bias (1.5 V).

Previous X-ray irradiation has a small but interesting influence on the SEGR critical voltage during subsequent heavy-ion exposure due to a possible interplay between X-ray induced defects and heavy ion strikes.

Low doses such as 3 Mrad(SiO_2) can introduce a V_{BD} variability especially in shrunk devices due to the influence of the positive charge especially at the gate oxide edges (near the overlap regions) that can locally enhance the oxide electric field.

In contrast, very high doses such as 100 Mrad(SiO_2) do not influence V_{BD} possibly due to the screening effect induced by the negatively charged interface traps at the interfaces with gate oxide and STIs. This negative charge can in fact relax the electric field reducing the occurrence of SEGR.

Finally, the influence of the stress procedure has been analyzed showing that the breakdown exhibited by slow-ramp-rate tests is not due to a single ion strike but, on the contrary, to an accumulation of ion-induced defects produced by multiple strikes.

Chapter 8

Conclusions and Future Work

A synergy between lifetime and ionizing irradiation tests exists in the 130-nm technology node examined in this manuscript. In this framework, long-term degradation is the most affected reliability aspect to consider for the assessment of a real mission scenario. In fact, from the electrical ageing point of view, the common worst-case bias condition during irradiation may become the best one for the subsequent electrical stress and vice versa. Moreover, with the continuous CMOS scaling these effects are going to become more and more important and an extra care must be taken into account in the foreseen long-lifetime missions.

8.1. Conclusions

In this thesis, two major challenges for scaled devices implemented in harsh radiation environments have been addressed. Firstly, the interaction between X-ray-induced defects and electrical stress has been analyzed for both open and enclosed layout MOSFETs. A large influence of TID on subsequent CHC and TDDB ageing tests has been found as a function of irradiation bias, oxide thickness, and device geometry. The influence of the back-end (metal layers) on the TID response has been analyzed as well showing that scaled technologies can have different sources of interplay. Secondly, new experimental results have been provided for the assessment of more realistic SEGR experiments in scaled devices. The influence of the indispensable high bias applied to the transistor gates, as well as TID and device geometry has been studied and some recommendations provided for future works.

In Chapter 2 we found that previous irradiation worsens the behavior of MOSFETs during hot carrier stresses in small-width core transistors. In addition, grounding the gate produces less trapped charge and interface states during irradiation, but negatively impacts the resilience to subsequent hot carriers degradation. With the help of physical device simulations we attributed these phenomena to differences in the impact ionization rate and enhanced defect generation at the bulk-STI interfaces.

As a result, extra care must be taken when evaluating the suitability of circuits (especially those having small-width MOSFETs) for harsh-radiation environments, since hot-carrier lifetime can decrease due to irradiation. In addition, these results raise some issues on how the spare devices must be biased during the operation under ionizing radiation, in order to maximize their lifetime.

In Chapter 3 we demonstrated that the parametric degradation of enclosed layout transistors under Channel Hot Carrier stresses features a time exponent higher than the one of conventional open layout devices. For short stress times, OLTs degrade more than ELTs, in spite of the smaller time exponent. We attributed this behavior to a different geometry of hydrogen diffusion after the creation of interface traps, and confirmed this possibility with TCAD simulations. Furthermore, we showed that interplay exists between radiation and hot carriers damage in ELTs, more noticeably for 5.2-nm gate oxides and to a lesser extent for 2.2-nm oxides. Radiation-induced defects cause an enhancement of the barrier for hot carrier injection, thus slightly reducing CHC degradation. Finally, temperature dependence of CHC damage is not affected by previous irradiation, but subsequent annealing steps at high temperature yield very different results on irradiated and unirradiated devices.

The results presented in this chapter might be difficult to extrapolate directly to very advanced CMOS technologies, in the 65 nm and below, where design rules imposed by novel manufacturing techniques forbid the integration of enclosed layouts. Nevertheless, the results concerning the response of irradiated gate oxides to CHC injection and the dynamics of hydrogen diffusion are of general applicability as long as fundamental changes on the transistor manufacture are not introduced (gate and isolation materials, 3D structures, etc.).

In Chapter 4 we have found that the irradiation bias conditions affect the TDDB of the examined 130-nm CMOS transistors. For the devices and irradiation conditions employed here, an interplay exists between X-ray irradiation and Fowler-Nordheim stress, producing a longer TDDB lifetime after irradiation. We attribute this behavior to the effect of radiation-induced traps that reduce the injected charge during

subsequent stress. Moreover, there is a large bias dependence in PMOS devices, possibly due to the drift of hydrogen from the bulk during irradiation, as opposed to NMOS samples where hydrogen comes from the gate oxide (or polysilicon), where it is less abundant.

These results show that careful choice of bias conditions during irradiation is necessary not only to lead to correct prediction of radiation effects, but also for the assessment of device reliability following radiation exposure.

In chapter 5 we demonstrated that the presence of metal-1 tracks in the proximity of the device active areas may significantly modify the response to X-rays of deep-submicron CMOS technologies. The impact of the secondary electron emission from metal-1 layers is strongly dependent on the relative position to the transistor lateral isolation, LDD spacers, and gate oxide. In particular, secondary electrons generated over source/drain junctions cause significant dose-enhancement effects in the LDD spacers, which are the main responsible of series resistance degradation in these devices.

These data suggest that dose enhancement in deep-submicron devices must be carefully considered when X-ray facilities are used to perform total-dose tests, due to the strong impact that metal-1 interconnects, especially when made of copper, can have on the final results.

In Chapter 6 we experimentally demonstrated that, in addition to the usual parameters considered in gate rupture induced by heavy-ions (ion flux and LET), also the bias polarity and gate oxide overlap regions are of primary importance to determine the critical voltage to breakdown in ultra-thin oxides. Inversion regime is worse than accumulation. due to the generation of energetic carriers in the conductive channel close to the gate after the passage of the heavy-ion. TCAD simulations confirm this hypothesis, showing that the funnel effect plays an important role in carrier heating. The dependence on the layout is quite complex and driven by different factors. As shown by TCAD simulations, on one hand the electric field in the oxide is higher in the overlap region, on the other hand carrier heating is reduced when strikes occur in the overlap areas of inverted devices. As a consequence, transistor-like structures, such as those we used in this work, can have a different breakdown voltage than the large area capacitors commonly used for SEGR tests.

These findings strongly advocate the use of test structures as close as possible to real transistors and biasing in inversion to have a truthful assessment of gate rupture issues in modern CMOS technologies.

In Chapter 7 the influence of previous X-ray irradiation on SEGR critical voltage has been analyzed. We found only a slight impact on gate rupture critical voltage at a LET of 32 MeV cm^2 mg^{-1} for devices previously irradiated up to 3 Mrad(SiO_2), and practically no change for 100 Mrad(SiO_2) irradiation, which simulates ten years of operation in the future super large hadron collider. We attribute this effect to possible interplay between trapped charge, and defects introduced by X rays, heavy ions, and electrical stress.

The rupture voltage lies far from operative conditions even when the devices were subjected to extremely high TID. The results presented in this chapter, related to the role of border regions, advocate the use of test structures based on MOSFETs arrays, rather than large area capacitors usually used in similar assessments.

8.2. Future Work and Perspective

The work performed during this Ph.D. lays the foundations for the next long-term reliability studies of advanced CMOS devices implemented in harsh radiation environments. From this point of view the 130-nm CMOS technology can be considered the borderline technology for this kind of interactions.

Below this feature size even localized defects will become source of degradation due to the very small device dimensions. Moreover, the need to reduce the dopant atoms to prevent fluctuations of the doping among the devices, the use of different materials such as high-κ dielectrics or MUltiple Gate Transistors (MUGFET), to continue with the CMOS scaling, will introduce new challenges for the long-term reliability.

Space-IC designers will have to deal with these issues since the next deep-space missions will need of high memory and data handling capability without extra silicon area consumption. A lot of work will have to be done at the device level especially when new materials are used such as high-κ dielectrics in order to deeply understand the basic degradation mechanisms. However, in the meantime, will be important also to move to a higher level of abstraction and try to study these phenomena at the circuit level. In fact, not only the synergetic effects between reliability and ionizing radiation will be heavily present but even the device-to-device variability will play an important role. The phenomena observed at the device level can assume a totally different perspective at the circuit level. Moreover, large campaigns of heavy-ion experiments should be performed in real CMOS transistors, like the ones used in this work, in order to statistically understand if SEGR is a real issue for space electronics and how the different processes and manufacturer can impact this occurrence. New models should

be provided for ultra-thin oxides since the ones proposed in state-of-the-art literature are not conclusive and especially built for power devices. Unfortunately, or fortunately for who works in this field, there are a plethora of degradation mechanisms that can play in different ways leading to different results.

Other exciting new devices like FinFETs, MUGFETs, gate all-around transistors, Carbon Nano Tubes (CNT), III-V-based electronics like GaN High Electron Mobility Transistors (HEMT), Micro Electro Mechanical Systems (MEMS), must be explored and studied under radiation and accelerated electrical stress, providing new models and degradation mechanisms.

Even if the space market will be always far from state-of-the-art technologies, it is important to compare these new technologies with the well established old ones in order to understand how and where emerging effects play a role. Only with continuous research effort we can win the next technological challenges on Earth and in the outer space.

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Biography

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His research activity has covered physical simulations, electrical characterization, impact-ionization effects, ultra-thin dielectric reliability, ionizing radiation effects in advanced CMOS transistors as well as defect-related effects and Monte Carlo transport simulations in GaN-based devices.