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TESI DI DOTTORATO

Reliability and dynamic properties of GaN devices

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Contents

Abstract

Nowadays power electronics market is increasingly having the need for high efficiency power conversion systems. Due to its outstanding properties in terms of high temperature, high voltage and high frequency capability, GaN material seems to be a valid candidate to provide the solution to the market requirements. In particular, GaN High Electron Mobility Transistors (GaN HEMTs) are promising devices suitable for high voltage and high power applications. In the last years, many works about GaN power HEMTs devices have been published and this confirms the huge interest in this emerging technology. Despite the outstanding performance already demonstrated of GaN HEMTs, market is still wary of this technology due to some still open reliability issues. In particular, many works have been published regarding the reliability of such devices but only few are able to predict the lifetime of such devices working in the final real application with reasonable accuracy. Many failure modes have been investigated in laboratory direct current (DC) and pulsed conditions but only few works try to analyze the behavior of GaN HEMTs transistors in the real application environment. The main goal of this thesis is to investigate reliability of GaN power HEMT devices during dynamic operation in real life conditions. This thesis try to identify the most important aspects that limit reliability of GaN HEMT devices in real life conditions and try to identify the failure modes during real switching operation. Many test concepts to assess performance and reliability of GaN HEMTs working in application conditions are also reported. The thesis starts by explaining the traditional state-of-the art approach used until now to assess HEMTs reliability, then introduce novel measurement concepts that are used to test devices in real switching operation close to the operative conditions of a real power converter. First of all, a novel measurement system able to assess dynamic performance and reliability of GaN devices is presented. As a result, some novel measurements concepts and the related results are reported showing that testing GaN HEMTs in real life conditions is of fundamental importance

to assess performance and reliability of such devices. At the end of the thesis a methodology capable to carry out accelerated stress test in dynamic operation conditions has been found, using an external additional capacitor in parallel with the HEMT under test. We think that the concepts introduced in this thesis enable a novel test approach that can lead to the definition of a lifetime model for GaN power HEMTs able to predict the time to failure of devices working in real life conditions.

Sommario

Attualmente il mercato dell'elettronica di potenza sta avendo sempre maggiore bisogno di sistemi di conversione dell'energia ad alta efficienza. Il nitruro di gallio, grazie alle sue eccellenti proprietà in termini di capacità di funzionamento ad alta temperatura, alta tensione e alta frequenza, sembra essere un valido materiale utilizzabile per sopperire alle richieste del mercato. In particolare, i transistor ad alta mobilità al nitruro di gallio (GaN HEMT) sono dispositivi promettenti che possono essere usati in applicazioni di potenza ad alta tensione e alta frequenza operativa. Negli ultimi anni sono stati pubblicati molti lavori sui GaN HEMT e questo conferma il grande interesse riguardo questa tecnologia emergente. Nonostante siano già state dimostrate le eccellenti prestazioni di questi dispositivi, il mercato attualmente sta ancora dubitando di questa tecnologia a causa di alcuni problemi ancora aperti riguardo l'affidabilità. In particolare, sebbene siano stati pubblicati molti lavori sull'affidabilità di questi dispositivi, solo pochi cercano di fornire una stima accurata del tempo di vita dei dispositivi funzionanti in un convertitore reale. Molte modalità di rottura sono state studiate in laboratorio sia in condizioni DC sia in condizioni impulsate ma solo pochi lavori hanno provato ad analizzare il comportamento dei GaN HEMT nell'effettiva applicazione finale. Lo scopo principale di questa tesi è investigare l'affidabilità di dispositivi GaN HEMT di potenza durante il funzionamento in condizioni reali. Questa tesi cerca di identificare gli aspetti più importanti che limitano l'affidabilità di GaN HEMT in condizioni effettive di funzionamento e cerca di identificare i modi di rottura durante il reale funzionamento di commutazione tipico dei dispositivi di potenza. Nella tesi vengono riportati molti concetti di test per valutare le prestazioni e l'affidabilità di dispositivi GaN HEMT funzionanti in condizioni applicative. La tesi parte spiegando lo stato dell'arte nell'analisi dell'affidabilità degli HEMT, quindi introduce nuovi concetti di misura che sono usati per testare i dispositivi in condizioni operative molto vicine a quelle di un effettivo convertitore di potenza. Prima di tutto viene presentato un nuovo sistema di misura in grado

di valutare le proprietà dinamiche di questi dispositivi funzionanti in un convertitore DC-DC. In seguito vengono illustrati alcuni nuovi concetti di misura e i relativi risultati, confermando che testare questi dispositivi in condizioni reali di commutazione è di vitale importanza per valutarne le prestazioni e l'affidabilità. Infine viene presentata una metodologia in grado di eseguire stress accelerati in condizioni dinamiche, usando un condensatore connesso in parallelo al dispositivo testato. I concetti mostrati in questa tesi introducono un nuovo approccio di test che può portare alla definizione di un modello di vita per dispositivi GaN HEMT di potenza in grado di stimare il tempo di vita dei dispositivi funzionanti in condizioni reali di commutazione.

Chapter 1

GaN HEMTs overview and Thesis motivation

1.1 GaN properties and GaN HEMT theory. From normally ON to normally OFF devices

Due to its outstanding performance, GaN is an attractive material to be used in power application devices. In particular the most important characteristics can be summarized as follows:

- Wide Bandgap (E_G). GaN is a binary III/V direct bandgap semiconductor and has a wide energy gap (E_G = 3.47 eV). It is well known that the impact ionization energy is higher for wider E_G semiconductors. Thanks to this important property GaN is able to withstand high breakdown electric field (E_{BK}) and thus is able to operate at very high voltage. This leads to the possibility to decrease the Gate-Drain distance where the highest electric field appears and thus it is possible to obtain smaller devices able to withstand the same breakdown voltage level. A wide E_G leads also to a low value of intrinsic carriers (n_i). Since hole-electron generation probability increases with temperature due to thermal excitation, the intrinsic carrier density increases with temperature in a semiconductor. GaN starts with low value of n_i thus it has the possibility to operate at very high temperature in comparison with other semiconductors.

- High mobility (μ). Another important benefit of GaN is the opportunity to

create the transistor channel in an intrinsic GaN semiconductor thus the mobility (μ) is not reduced by impurities. Thanks to this property, it is possible to obtain transistors with high value of μ and carriers saturation speed (V_{SAT}). Due to this important result, GaN devices are able to work at very high values of current density and can withstand very high power.

Due to these important properties, GaN can be used to grow outstanding devices able to withstand high voltage and high temperature and able to work at very high frequency with a very low drain to source on-resistance (R_{DSON}). All these features lead to power devices that can be used in power applications with excellent performance in terms of power saving. The core of a GaN HEMT device is the heterostructure between AlGaN and GaN, i.e. the junction between two semiconductors with differen energy gap (see fig. 1.1). The AlGaN semiconductor is the barrier layer and works as a barrier which confines the electrons. The intrinsic GaN layer is the buffer and provides the charge to the conduction channel. When these two materials are combined together in well controlled thickness and composition conditions, a bi-dimensional electron gas (2DEG) appears in the buffer layer due to the lowering of the conduction band under the fermi level (see fig. 1.1). This creates the conduction channel between the drain and source terminals. It is worth noticing that the channel appears in an intrinsic semiconductor. This is one of the most important feature of GaN HEMT devices since the mobility is not affected by impurities. Moreover, it can be noticed that the channel appears even with no gate bias applied, thus normally ON devices are achieved with this structure type. Recently, a high effort has been put to achieve normally

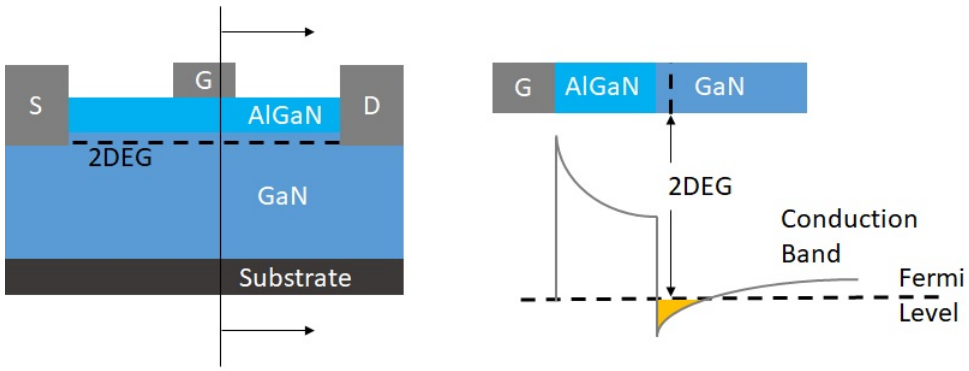

Figure 1.1: Normally ON HEMT structure and simplified band diagram

OFF devices due to (i) their self-protection in case of gate driver failure and (ii)

the need of enabling an half-bridge circuit diagram in a traditional configuration with normally OFF driving [1] [2] [3] [4]. Many techniques have been proposed to obtain enhanced mode GaN HEMT power devices. In this thesis we focus on the p-type technology since the devices tested use this configuration. In order to obtain positive threshold voltage a p-type semiconductor is grown above the barrier layer. In this way, the p-type semiconductor raises up the band diagram respect to the fermi level and allows obtaining enhanced mode HEMT devices. Fig. 1.2 shows this concept: the most commonly used p-type semiconductor is p-GaN. As can be noticed, the p-GaN layer raises up the conduction band and causes the pinch off of the channel when no bias is applied to the gate. When a positive voltage is applied to the gate the band diagram lowers and the 2-DEG appears (not shown). In this way, a positive threshold voltage is achieved.

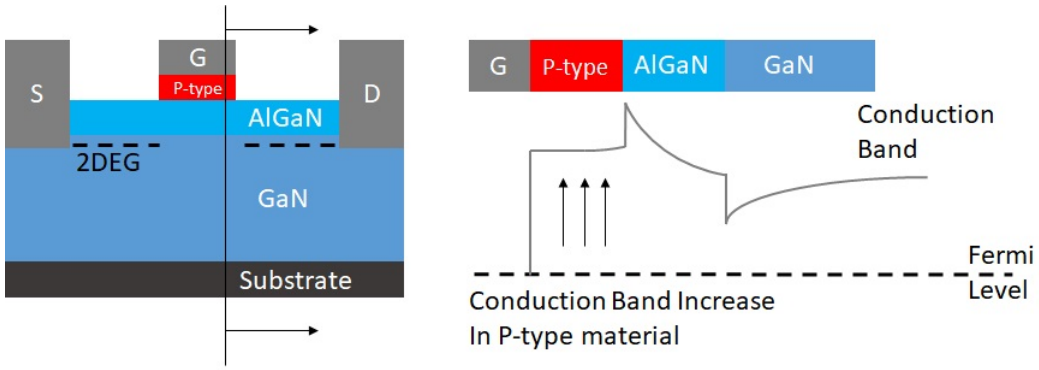

Figure 1.2: Normally OFF p-type HEMT structure and simplified band diagram

1.2 GaN HEMT dynamic R_{DSON} and GaN mobility temperature dependence

One of the main problem of GaN HEMTs is the well known dynamic R_{DSON} - i.e. the increase of the R_{DSON} due to charge trapping at high voltage [5, 6]. The main cause of the dynamic R_{DSON} is the presence of charge trapping states which can trap electrons or holes as illustrated in fig. 1.3 for a normally OFF device ($V_{TH} > 0V$). When the device is subjected to high voltage in OFF state, due to the high electric field, charges can be trapped within the structure of the device both in the buffer and in the surface under the gate or in the assess region (region between the gate and drain). After the charge has been trapped,

when the HEMT is turned ON, the trapped charge can have a significant de-trapping time constant and thus it can remain trapped within the structure of the transistor. This phenomenon changes the band diagram of the HEMT causing a residual pinch off of the channel i.e. an increase in the R_{DSON}. Fig. 1.4 reports a

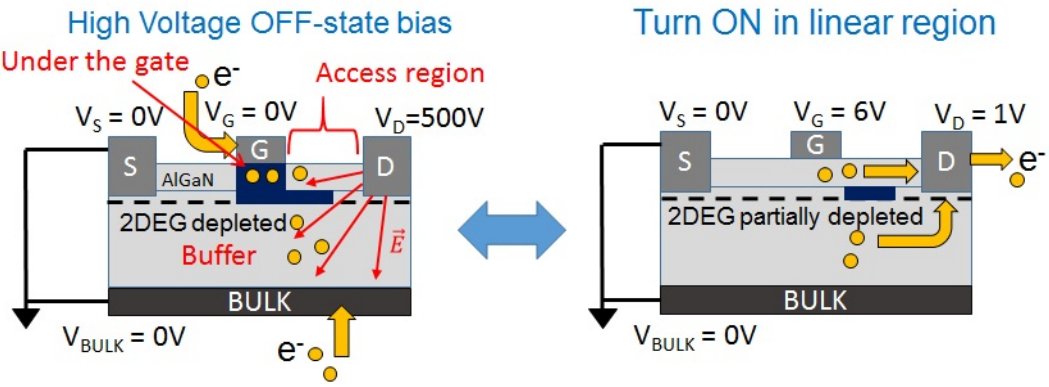

Figure 1.3: Charge trapping mechanisms in OFF-state

R_{DSON} transient for a normally ON device ($V_{TH} < 0V$) which suffer from charge trapping. The device is subjected to a very short OFF state bias (1s at V_G = -5V, V_D = 500V) and then is turned ON for 100s in linear region (100s at V_G = 0V, $V_D < 1V$). As can be noticed, the R_{DSON} of the transistor starts from about 75 Ω immediately after the turn ON (at about 15 μs) and reaches 65 Ω after 100s. This plot shows a typical dynamic R_{DSON} transient of a power device. The de-trapping time constant can change depending on the nature of the trapping state. In the last years, many works have reported the dynamic R_{DSON} issue. This phenomenon has been atributed mainly to the high voltage charge trapping due to the high electric field involved in OFF-state. Recently, other causes have been found to be relevant: some works reported also the charge trapping due to hot electrons created during hard-switching transients [7] and, the increase of the junction temperature (Tj) due to self-heating [8] as physical causes of the R_{DSON} increase.

As far as hot electrons is concerned, similar consideration of the OFF state trapping are valid. When the device is subjected to the simultaneous presence of high electric field and high current typical in hard switching conditions, electrons can be accelerated within the structure of the device and can be trapped in defect energy states. Also in this case the de-trapping process can occur in a finite time thus the trapped charge can modify the band diagram and changes the conduction properties of the device causing an increase of the dynamic R_{DSON}. As far as

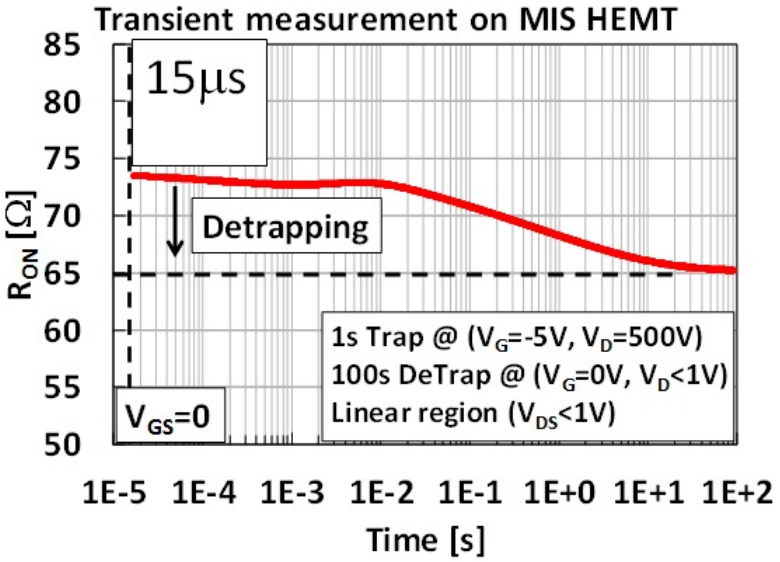

Figure 1.4: R_{DSON} transient due to charge trapping in OFF-state

the temperature is concerned, it is well known the relationship between mobility (μ) and temperature in a semiconductor. Fig. 1.5 is taken from [9] and reports the relationship between μ and temperature for two typical GaN crystals. Two

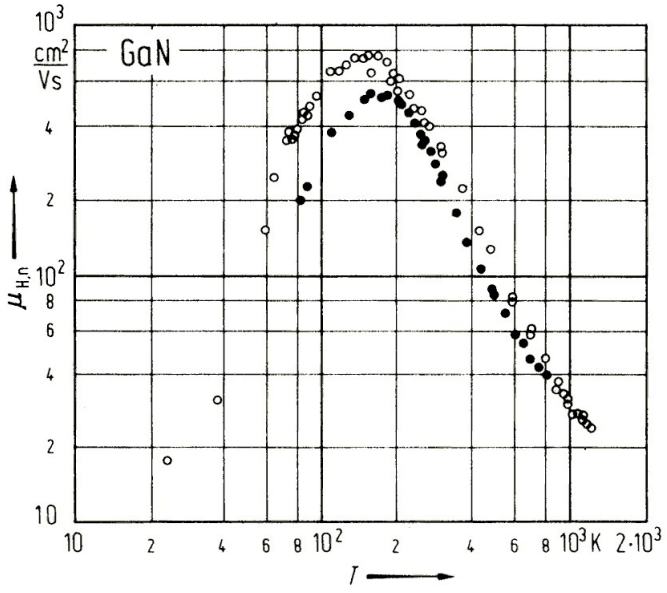

Figure 1.5: The electron mobility, μ as a function of temperature. Image taken from [9]. Two clear scattering mechanisms are present: (i) at low temperatures scattering with ionized impurities and (ii) at high temperatures scattering with lattice

mechanisms are responsible for the variation of (μ) with temperature: (i) the scattering of carriers with ionized impurities and (ii) the scattering with the lattice. The scattering with ionized impurities decreases at higher temperature because the thermal excitement promotes carriers release from the electric field of impurities. On the contrary, the scattering with the lattice increases with temperature due to the higher vibration thus the interaction probability between carriers and the lattice increases at higher temperature. At ambient temperature the second mechanism dominates thus the mobility decreases with the temperature increase and thus the R_{DSON} increases with the temperature increase.

1.3 State of the art GaN HEMT performance and reliability assessment

Until now, GaN HEMTs reliability assessment was based mainly on DC tests and pulsed tests. In the DC tests, the devices are characterized or stressed in stable fixed conditions and the time measurement can change between a few ms for the DC characterizations and hundreds or thousands of seconds for the stresses. In order to explain this test regime fig. 1.6 and fig. 1.7 report respectively an output DC characterization (I_D-V_D) and a DC step stress carried out on two devices. During the I_D-V_D characteristic measurement the gate voltage is fixed, the V_D voltage is swept from 0V to 5V and the I_D and I_G are measured. Each measurement point lasts for tens of ms thus the performance of the device in a steady state condition is assessed. Fig. 1.6 shows that the device reaches about 0.3A/mm which is a typical value for power HEMT devices. In the step-stress

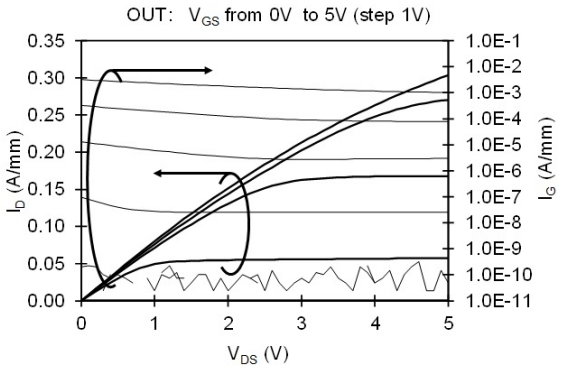

Figure 1.6: Output DC characteristic of a power HEMT device

reported in fig. 1.7 the device is tested with a fixed drain bias (50V) and the

gate voltage is stepped up until the failure of the device; each bias step lasts for 120s. Also in this type of measurement, the device is tested in a steady state condition and the robustness to high continuous gate voltage and current can be assessed. As can be noticed, when the gate voltage (V_G) is higher then 7.5 V the gate current is unstable until the catastrophic failure at V_G = 19.5 V. Usually

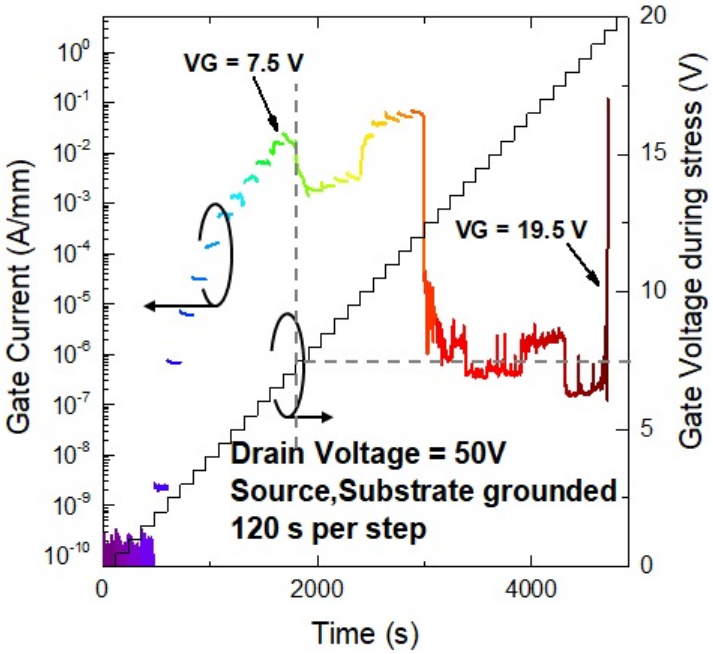

Figure 1.7: Gate step stress on a power HEMT device

DC tests are carried out with parameters analyzers which are instruments able to provide proper electrical bias to the device terminals and measure the current and/or voltage with minimum time in the order of few ms. Since GaN HEMT power devices are expected to work at very high frequency (> 1MHz) in high power converters [10, 11], this type of measurements are not able to test the devices close to the real frequency where the transistors are expected to work. In order to assess the performance of GaN HEMTs at higher frequency one of the most widespread measurement technique used so far is the so-called double pulse measurement. Fig. 1.8 shows the typical waveforms (I_{DS}, V_{DS}, V_{GS}) of a double pulse measurement: in the double pulse characterization, the device is kept in OFF state with V_{GS} = 0 V and fixed V_{DS} voltage (V_{DSOFF}). Starting from this bias condition (called base line), two properly synchronized voltage

pulses are applied on the Gate and Drain terminals for a very short time (i.e. 20 μs) in order to acquire the device output pulsed characteristic (I_{DS}-V_{DS} at fixed pulsed V_{GS}). From the I_{DS}-V_{DS} output characteristic, the transistor R_{DSON} can be extrapolated. By varying the V_{DSOFF} voltage, the impact of the high electric field induced in OFF state on the R_{DSON} of the transistor can be investigated. Note that in this case, the measurement assesses the performance in a pulsed regime thus this type of measurement is useful to evaluate devices characteristics closer to the real operation frequency they are expected to work. It is worth noticing that, with this kind of measurement, the device is tested in a "soft" pulsed operation regime. In fact, primarily the V_{DS} imposed by external electronics is lowered and then the transistor is turned ON with the gate signal. Moreover, the device does not suffer from self-heating during the measurement due to the very low duty cycle (1%) and the very short ON time used (pulse width typical $<$ 20 μs). Fig. 1.9 reports the double pulse output characteristics and the related

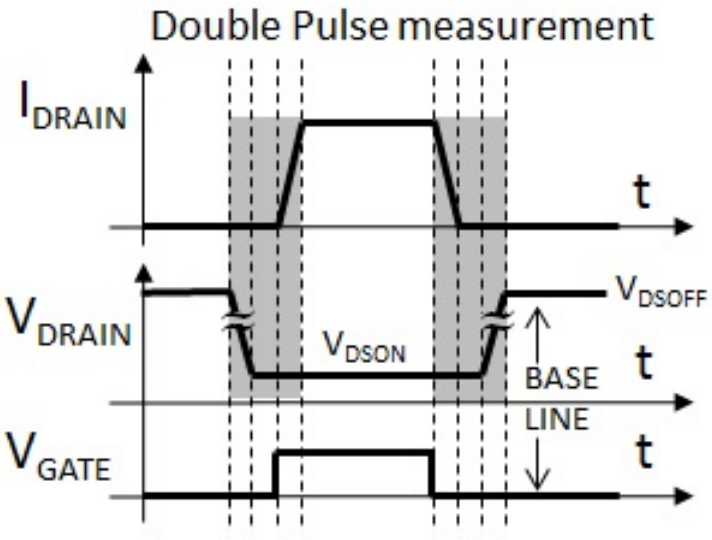

Figure 1.8: Typical waveforms during a double pulse measurement with base line in OFF state

R_{DSON} values obtained with different base lines (V_{DSOFF} from 0 V to 600V, step 100V) for a device which suffers from dynamic R_{DSON}. As can be noticed, the R_{DSON} shows a non monotonic increase with the increasing of the base line drain voltage. This behavior can be ascribed to the impact of charge trapping due to the high electric field in OFF state. It is known in literature that the R_{DSON} increases for increasing V_{DS}, due to the ionization of buffer acceptors [12]. On the other hand, at very high voltage ($>$ 250 V) the electric field within the vertical epitaxial

structure of the device favors charge de-trapping, and the corresponding decrease in R_{DSON} [12]. As a result of this, at first the R_{DSON} increases with V_{DSOFF} and then it decreases. From this sample measurement, it is clear that the double pulse technique is useful to investigate performance of GaN HEMT devices at high frequency. It is worth mentioning now that the double pulse measurement technique tests devices closer to the real operation conditions respect to the DC tests. In fact, the transistor works in pulsed mode which is the operation regime where a power device is expected to work. The main limitation of this approach is that double pulse tests the device in a soft switching operation mode which is not the real application case; this will be the main topic of the next section.

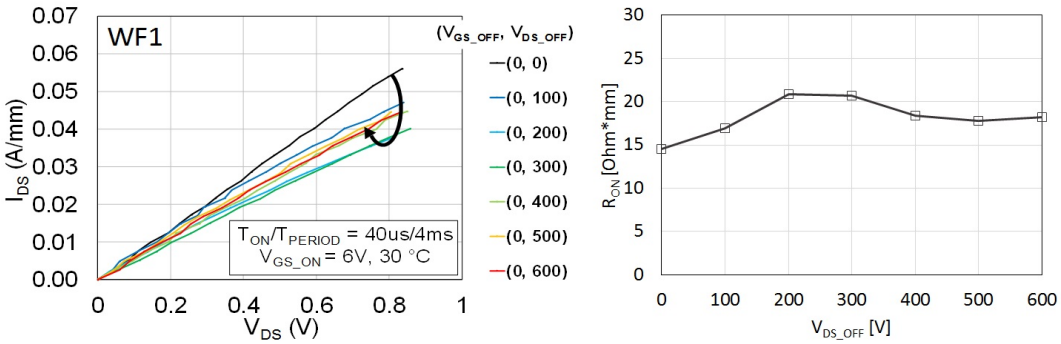

Figure 1.9: OFF state double pulse measurement: output characteristic and related R_{DSON} extrapolation

In conclusion, to date the state of the art approach tested GaN HEMT devices with DC tests and with pulsed measurements. This approach is able to provide important and useful information regarding performance and reliability of GaN HEMT devices but there still exists a gap to assess such devices working in real life conditions.

1.4 The hard switching application related issue

GaN power HEMTs are expected to work in power converters at very high frequency [10, 11]. When a transistor works inside a power converter it continuously switches between ON state (in linear region) and OFF state as indicated in fig. 1.10. The most important difference between the real operation and the state of the art tests explained in section 1.3 is that in the real application usually

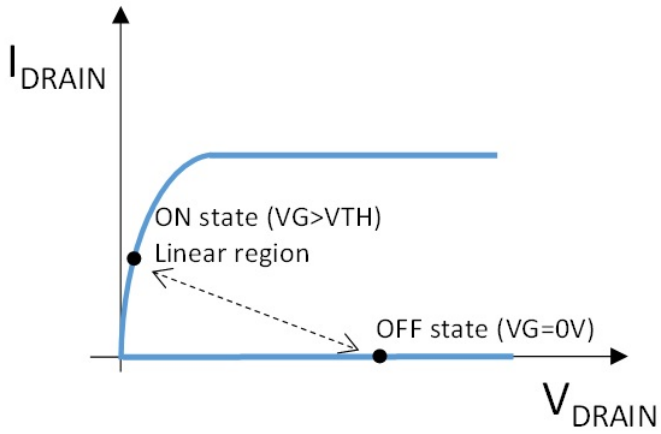

Figure 1.10: Typical operation states of a power transistor

the transistor works with an inductive load instead in the DC and pulsed tests usually a resistive load is adopted. When the device switches with an inductive load, it works very differently respect to the DC tests and the double pulse tests previously reported. In fact, when the load is inductive and no resonant configuration is used in the power converter, the device switches in hard switching mode as reporter in fig. 1.11. When the device turns ON and OFF there are transients where V_{DS} and I_{DS} are simultaneously high thus the device is subjected to transient high instantaneous power. This condition has not been well

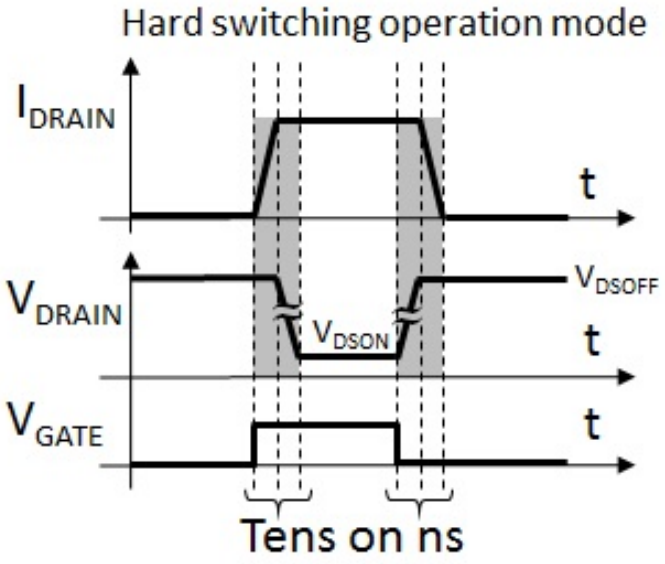

Figure 1.11: Hard switching operation mode

investigated until now in literature for GaN power HEMTs. [7] shows that during hard switching hot-electrons can appear and the dynamic R_{DSON} increases due to charge trapping. In fact, due to the high electric field and the high current involved during hard switching transients, carriers reach high energy level and can be trapped within the structure of the device causing the worsening of the transistor performance. To conclude this section, it is worth pointing out that the arise of hot electrons can lead to the GaN HEMTs degradation [13] thus the study of hard switching conditions is of fundamental importance to assess reliability of such devices.

1.5 Thesis motivation

Section 1.2 and 1.3 explained the main issue of GaN HEMTs and the state of the art performance and reliability assessment approach. We showed that, until now, devices were tested in DC and soft switching regime. Section 1.4 introduced a new issue that GaN devices can face, i.e. the capability of working in hard switching conditions. This mode of operation was not well investigated until now in literature and some works have already shown that it can affect the performance in terms of R_{DSON} increase [7]. As a result, it is easily clear that performance and reliability of GaN HEMTs in real life conditions are not fully assessed with the state of the art approach. In other words, a gap exists between the current test approach and the real operation mode where the devices are expected to work. The goal of the thesis can be summarized as follows:

- To investigate GaN HEMTs characteristics in real-life conditions
- To identify new failure modes/mechanisms of power GaN HEMTs in real application conditions
- Mimic application conditions in laboratory test procedures
- Study the impact of switching conditions on trapping/detrapping behavior as well as degradation over time.
- Define test methodologies (including equipment, software routines, and data assessment procedures) to investigate the impact of switching conditions on performance and reliability of GaN HEMTs.

1.6 Chapter summary

In this chapter the GaN HEMT normally OFF technology based on p-type gate has been presented. We showed that by growing a p-type material under the gate contact the band diagram increases and normally OFF operation can be achieved. Moreover, the dynamic R_{DSON} issue was presented, showing that the R_{DSON} can be unstable and can change depending on the filling and emptying of the charge trapping states. Then, the state of the art approach to study such problem was shown. In particular, the double pulse measurement technique was reported showing that the R_{DSON} can change depending on the OFF state bias. Then, the hard-switching issue has been introduced showing that this operation mode is potentially detrimental for GaN HEMT devices in terms of reliability. Finally, in the last section the thesis motivation has been presented.

Chapter 2

High voltage and high speed dynamic measurement techniques

This chapter reports in detail the measurement techniques used to assess the dynamic performance of GaN HEMTs devices. Starting with the state of the art techniques (section 2.1), the analysis is enlarged with a novel measurement technique proposed to study GaN HEMT devices in real application conditions (section 2.2).

2.1 State of the art approach

This section reports some state of the art measurement techniques useful to study performance and reliability of GaN HEMT devices. In particular the following techniques are analyzed:

- Double Pulse (DP): used to study the dynamic R_{DSON} and V_{TH} shift problems due both to the drain and gate charge trapping.
- Fast backgating: used to study charge trapping related to the buffer states.
- Drain Current Transient (DCT): used to extrapolate the activation energy of the charge trapping process.
- Transmission Line Pulse (TLP): used to test devices at very high speed (100ns).

2.1.1 Double pulse measurement

As already reported in chapter 1, one of the most important technique to study pulsed characteristics of GaN HEMTs is the double pulse system. Fig. 2.1 reports the block diagram of the system used for the measurements in this thesis. As can be noticed, in order to measure the I_{DSON} (the ON current of the transistor), a resistive load is connected to the drain node of the device under test (DUT) and a differential voltage probe is used to acquire the load resistor voltage. A voltage probe is used to measure the V_{DSON}, i.e. the drain voltage of the transistor when it is in ON state. The V_{DSON} and I_{DSON} are acquired with an oscilloscope. Two voltage pulsers provide the proper V_{DS} and V_{GS} voltage waveforms. The entire system is automatically controlled via Labview with a PC.

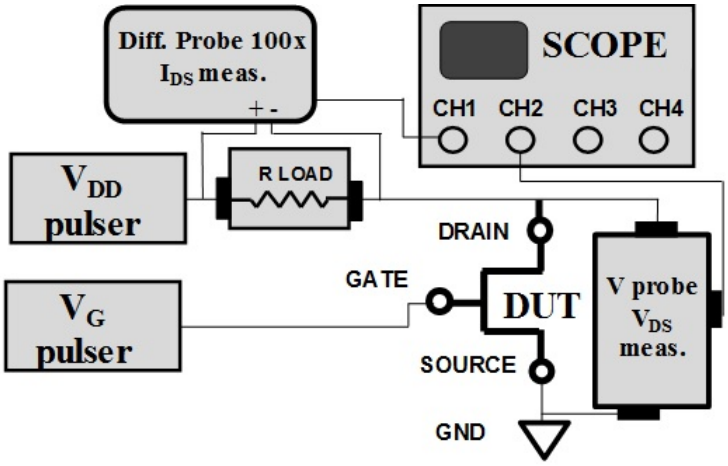

Figure 2.1: Block diagram of the double pulse system

Fig. 2.2(A) shows the typical waveforms of an OFF state base-line double pulse output characteristic measurement for a normally OFF device. In the double pulse measurement there are two main phases. In the first phase (base line or filling state), the device is biased in OFF state condition with a high V_{DSOFF} voltage (up to 600 V) and V_{GS} = 0 V (in the following the voltage during the base line will be named V_{XBL} where X is ether DS or GS). In this condition, the main goal is to fill trapping states due to the high electric field present within the structure of the device. In the second phase, the device is turned ON and the V_{DSON} and the I_{DSON} are measured. Starting from the base line two properly synchronized pulses are applied to the gate and drain of the DUT. In particular, in order to obtain soft switching conditions, first of all the V_{DS} is lowered and then the gate is raised to turn ON the device. The pulse width is typical in the

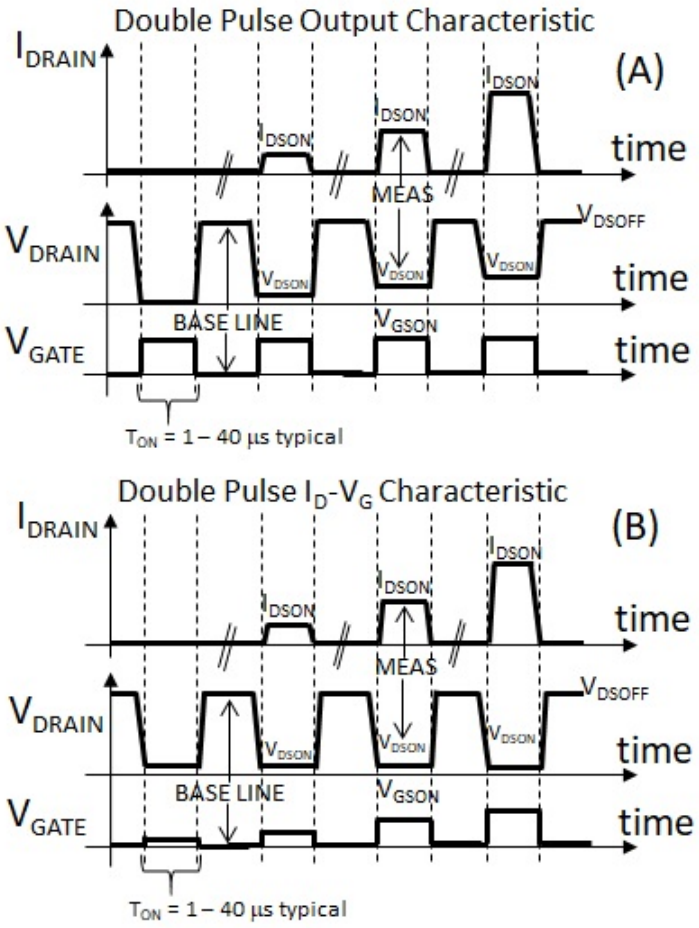

Figure 2.2: Double pulse output (A) and I_D-V_G (B) characteristic measurements in drain lag condition

range of 1 - 40 µs. By changing the V_{DSON} value and keeping V_{GSON} constant, it is possible to extrapolate the output pulsed characteristic of the DUT. Moreover, by changing the base line (for example V_{GSBL} = 0 V in all cases and V_{DSBL} = 0 V, 100 V, 200 V, 300 V, 400 V, 500 V, 600 V) the impact of the OFF state high voltage charge trapping phenomenon can be studied. Similar considerations are also valid for the I_{DS}-V_{GS} waveforms (fig. 2.2(B)). By changing - during the measurement - the V_{GSON} pulse level and keeping the V_{DSON} pulse constant, the pulsed I_{DS}-V_{GS} (at fixed V_{DSON}) curve can be measured and the the threshold voltage (V_{TH}) in pulsed regime can be extrapolated. Fig. 2.3 explains the base line condition and the measurement bias for an I_{DS}-V_{GS} double pulse measurement. As can be noticed, during the filling bias point (Base Line) the high electric field induced both in the surface and in the buffer fills the trapping states. Then

the device is switched to the measurement condition. The V_{GS} voltage is pulsed from 0 V to 5 V, whereas V_{DS} pulse is fixed to 2 V. When the device turns ON the residual trapped charge can modify the properties of the device thus worsening both the R_{DSON} and the V_{TH}.

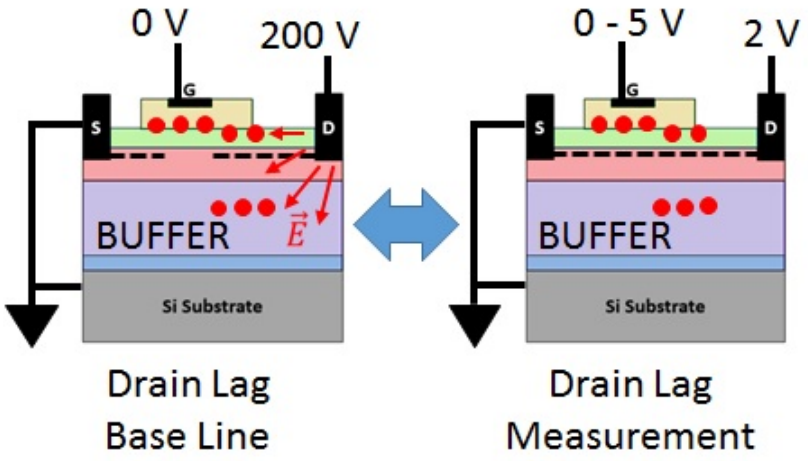

Figure 2.3: Drain Lag I_{DS}-V_{GS} Double pulse filling and measurement bias points

It is worth mentioning that the double pulse measurement can be carried out not only in OFF state with high V_{DSOFF} voltage (drain lag condition) but also with other filling bias points. For example, in order to investigate the gate bias charge trapping (gate lag), a base line set similar to [(V_{GSBL}, V_{DSBL}) = (0 V, 0 V); (1 V, 0 V); (2 V, 0 V); (3 V, 0 V); (4 V, 0 V); (5 V, 0 V)] can be used. With such a bias set the impact of the gate charge trapping is assessed since, during the base line, the device is kept at zero drain current (I_{DSBL} = 0 A) with V_{DSBL} = 0 V and an increasing gate voltage (V_{GSBL}) is applied.

Note that, in order to avoid the self-heating of the DUT, in the double pulse measurement, the typical duty cycle is 1% and the T_{ON} time can change in the range of 1 - 40 µs. In this way, the contribution of the self heating on the pulsed characteristics can be considered negligible and only the charge trapping contribution is assessed.

2.1.2 Fast backgating measurement

In order to better identify whether the trapping occurs in the surface or in the buffer, a new type of measurement (called fast backgating measurement) has been studied. The main concept consists in using a different filling bias point in

which charge trapping is induced mainly in the buffer and slightly in the surface as shown in fig. 2.4.

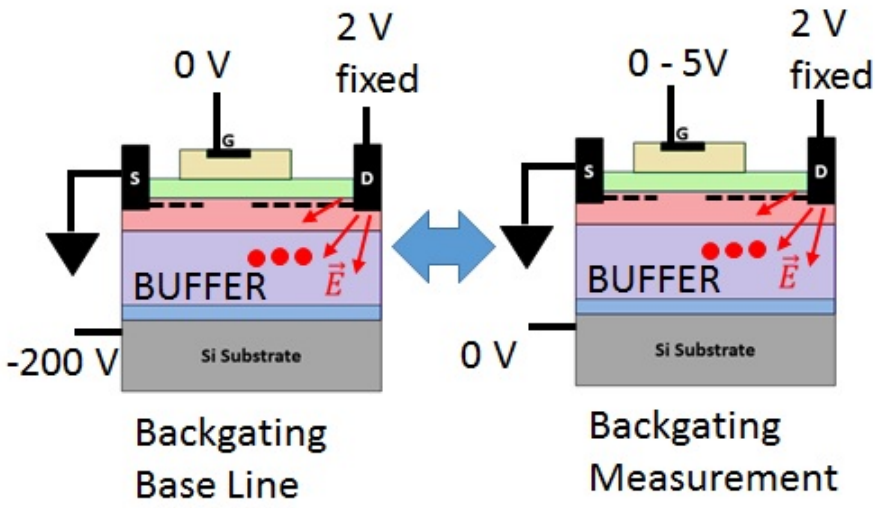

Figure 2.4: Backgating filling and measurement bias points during the I_{DS}-V_{GS} measurement

In order to obtain this condition, a negative voltage is applied to the substrate of the device, the gate and the source are grounded and the drain is kept fixed at low voltage (2 V). During this base line, an high electric field is induced on the buffer thus we expect that charge trapping occurs mainly in this region. In order to measure for example the I_{DS}-V_{GS} characteristic of the DUT, the device is switched to the measurement state as reported in fig. 2.4. The substrate voltage is rapidly pulsed at 0V, then the transistor is turned ON with an increasing positive gate voltage and the related pulsed I_{DS} is acquired. This measurement technique is useful to investigate buffer charge trapping and separate the effects of the surface.

Fig. 2.5 shows the system used to carry out the fast backgating measurement. As can be noticed, there are two pulsers connected respectively to the gate and the substrate nodes. The drain node is kept at fixed voltage and a current probe is used to measure the I_{DS}. The need of using a current probe to measure the I_{DS} is recommended since the V_{DS} has to be fixed in the I_{DS}-V_{GS} characteristic and using a resistive load the V_{DS} will changes as a function of the drain current and V_{GS}. It is worth mentioning that this technique can have tighten timing constraints respect to the double pulse measurement previously explained. In fact, usually the substrate of the device is connected to the substrate of the

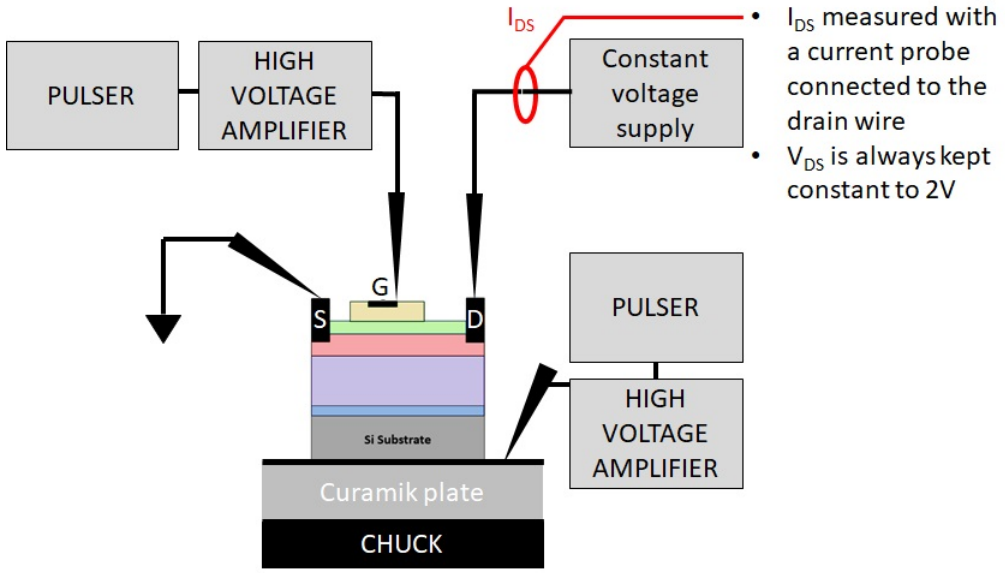

Figure 2.5: backgating measurement system

entire wafer thus the substrate node behaves like a capacitor plane. This leads to slower dV/dt on the substrate node respect to the standard drain - gate double pulse measurement described in section 2.1.1.

2.1.3 Drain current transient (DCT) measurement and Arrhenius plot method

The double pulse and backgating measurement techniques are useful to identify the location of the charge trapping within the structure of the HEMT. In particular, as already explained, these measurements allow to separate surface and buffer charge trapping contributions. No information about the physical nature of the traps is provided. The drain current transient (DCT) measurement is a useful technique able to identify the chemical species responsible for the trapping/de-trapping phenomena. During the DCT measurement the device is biased in a trapping condition for a certain filling time and then is turned ON for a long time (usually 100 s) in order to induce a complete detrapping phase. The current I_{DS} and the voltage V_{DS} during the de-trapping phase are acquired and the R_{DSON} is calculated. Previously reported fig. 1.3 shows a typical DCT for a normally ON device. As can be noticed, the device is biased for 1s in OFF state with very high V_{DS} (the filling bias point is: V_{GS} = -5 V, V_{DS} = 500 V) and then is turned ON in linear region (the measurement bias point is: $V_{GS} = 0$

V, V_{DS} = < 1 V). The evolution of the R_{DSON} during the ON phase is reported.

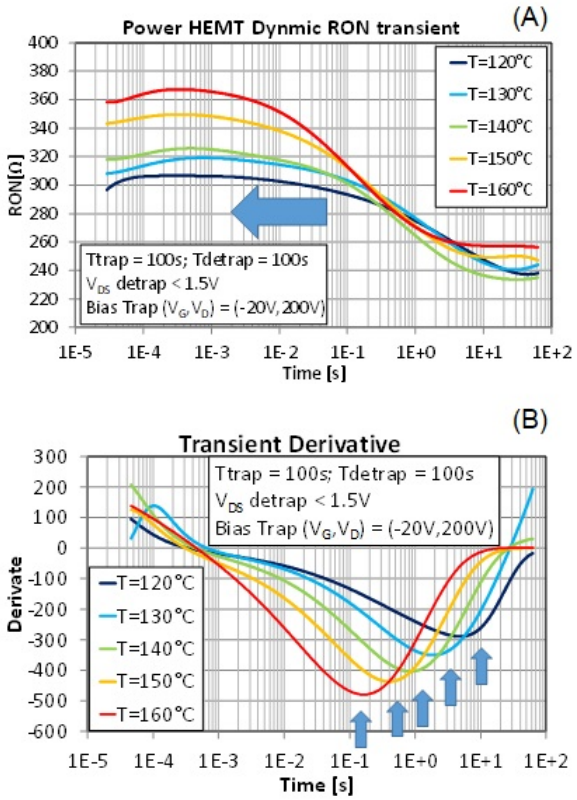

Figure 2.6: DCT measurements thermally activated. (A) R_{DSON} evolution at different temperature, (B) derivative of the R_{DSON} waveforms

As can be noted, due to charge de-trapping, the R_{DSON} starts from a higher value and then it drops down to its steady state value in about 100s. In case the charge detrapping phenomenon is affected by temperature (T), by repeating the DCT measurement at different temperatures the activation energy (E_A) of the process can be extracted. Fig. 2.6(A) shows the DCT measurement at different temperatures of a normally ON power HEMT device. As can be noticed, the R_{DSON} detrapping time constant decreases with the increasing of the temperature. By taking the derivative of the R_{DSON} transients (fig. 2.6(B)) and calculating the times of the different minimum values, the time constants (τ_{peak}) for each temperature can be calculated.

By plotting the points ($\ln(\tau_{peak}*T^2)$, q/KT) for each temperature, the Arrhenius plot is obtained, where τ_{peak} is the time constant of the R_{DSON} transient, q is the elementary charge, K is the Boltzman constant and T is the temperature in Kelvin degrees. Fig. 2.7 reports the Arrhenius plot obtained from the data of

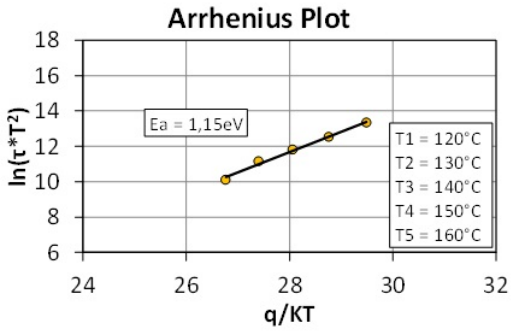

Figure 2.7: Arrhenius plot related to the DCT of fig. 2.6

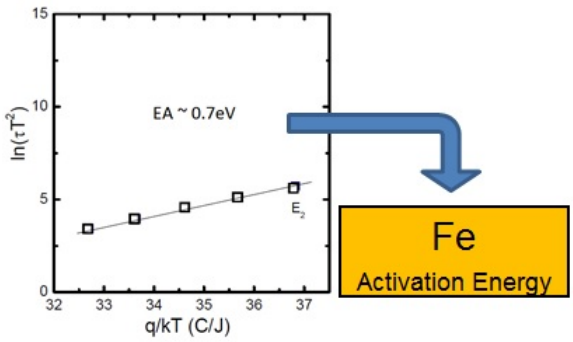

Figure 2.8: In [14] buffer Iron doping causes trapping with activation Energy about 0.7 eV

fig. 2.6. The activation energy (E_A) of the detrapping process is the slope of the linear fitting of the Arrhenius curve. The Arrhenius method is a useful technique to identify the number of trapping / de-trapping processes involved. In fact, there can exist cases where the Arrhenius plot provides multiple activation energies. Moreover, due to the fact that different contaminants species exhibit different activation energies, the Arrhenius plot is useful to identify the chemical species responsible for the trapping/de-trapping phenomena. For example fig. 2.8 shows the Arrhenius plot of devices doped with iron reported in [14]. An activation energy of about 0.7eV is obtained and this signature closely matches with those reported in previous papers [15, 16], based on different techniques.

2.1.4 TLP measurement

The transmission line pulse (TLP) system is a dedicated measurement setup able to provide very short pulses (100 ns) and measure the voltage and the current during the pulse.

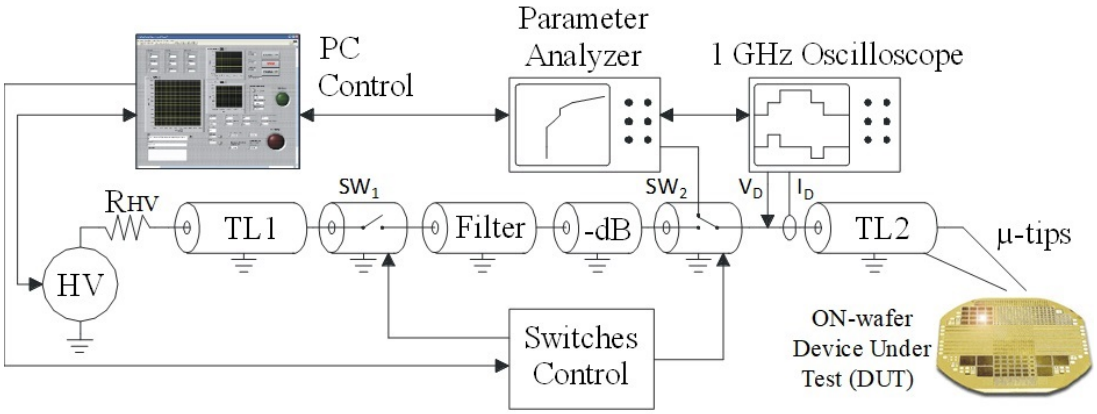

Figure 2.9: The TLP system

Fig. 2.9 shows the schematic of the TLP system used within this thesis: a high voltage power supply (HV) charges a transmission line (TL1) with a resistor (R_{HV}). Once the transmission line is charged, it can be discharged toward the device through a relay (SW_1). An attenuator (-dB) is used to soften the oscillations of the line. The system uses a 1GHz oscilloscope to measure the voltage and current pulses provided to the device. Moreover, the system is able to carry out off line measurements between the pulses by connecting the load to a Parameter Analyzer (through the switch SW_2). The entire TPL setup is controlled by a control PC with a Labview program. The width of the pulse provided to the load can be changed by adjusting the transmission line length. The TLP measurement is important since it enables to assess device performance at very short time (100 ns). This timing is perfectly comparable with that of real operation since GaN HEMTs are expected to work at very high frequency (in the MHz range). Due to these features, the TLP measurement technique is useful to investigate the device behavior at timings close to the real application ones even if the device is biased in a very different condition respect to the real operation. In fact, during the TLP measurement the device is subjected to short pulses only in ON-state, instead in the real application the power device switches continuously between ON and OFF state and is subjected also to high OFF state voltage.

Fig. 2.10 shows a typical measurement carried out with the TLP system. The DUT is biased with a fixed $V_{GS} > V_{TH}$ and the TLP system provides pulses to the drain node until failure. As can be noticed, the output characteristic at 100 ns is achieved and when V_{DS} is close to 650 V the device breaks. A short circuit failure mode occurs since the V_{DS} goes to a very low value and the current

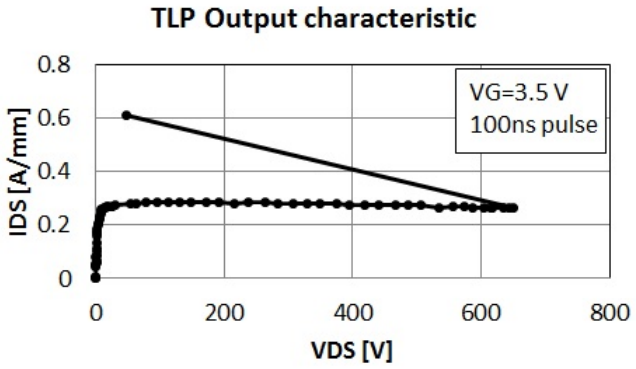

Figure 2.10: TLP output characteristic until failure

increases. This preliminary measurement shows that this technique is useful to explore the device operation limits at very short time avoiding the transistor self-heating.

2.2 A novel real application like measurement approach

In this section a novel measurement approach to test GaN HEMT devices in hard-switching conditions is presented. Within this thesis, a novel system to investigate the dynamic properties of GaN-based power transistors in realistic application conditions was developed. The system is able to analyze on-wafer test devices with an ON-resistance in the range from few Ohms to hundreds of Ohms and is useful to improve the development process of GaN HEMTs power devices. Contrary to the conventional double pulse setup where a resistive load is usually used in combination with a very low duty cycle, the dynamic R_{DSON} is acquired during realistic operating conditions, in a boost power converter. As a consequence, the system is able to study not only the field-activated trapping processes (evaluated by the conventional DP and DCT systems), but also those induced by hard switching conditions, i.e. promoted by hot-electrons and self-heating. The maximum working voltage (600 V) and the minimum measurement time (2 µs) allow to evaluate the operation limits of the devices in a voltage/frequency range close to real switching condition. Summarizing, the main benefit of this system is to assess the R_{DSON} of on-wafer normally-off GaN HEMTs in a real environment with all the contributions responsible for the R_{DSON} increase applied, thus allow-

ing a more realistic assessment of the dynamic R_{DSON} behavior, which cannot be studied until now, with the state of the art approach.

2.2.1 The novel system description

The system developed within this work consists of a boost DC-DC converter where the switching transistor is an on-wafer device. The boost converter electronic board is directly mounted on a microscope-based probe station to allow the user to contact the power HEMT with micro tips. Moreover, the system is equipped with the measurement instrumentation which allows studying the HEMT transistor during the real switching operation in the DC-DC converter. The system meets two main requirements: (i) the need for the converter working with an on-wafer device and (ii) the need for measuring the R_{DSON} during operation, starting from 2 µs after the turn on of the device.

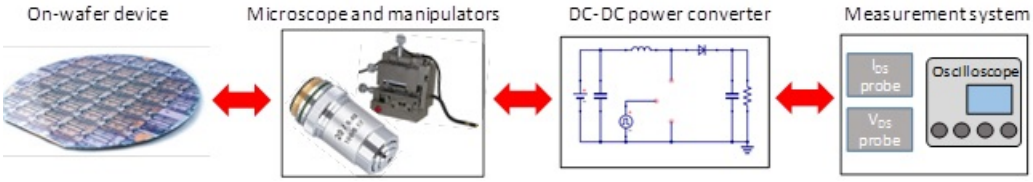

Figure 2.11: Schematic representation of the system. There are three main blocks: (i) the equipment used to contact the device including the microscope and the manipulators, (ii) the DC-DC boost power converter and, (iii) the measurement system.

Therefore, the system can be divided in three main blocks (see fig. 2.11): (i) the equipment used to contact the on-wafer device including the microscope and the micro manipulators; (ii) the power converter board which emulates the real application; (iii) the R_{DSON} measurement equipment including probes for the measurement of the voltage and the current during the transistor operation and an oscilloscope. Fig. 2.12 shows some photos of the setup. As can be noticed, the converter board is directly mounted on the microscope, and three wires connect the power converter board and the three tips of the manipulators (respectively gate (G), drain (D) and, source (S)). The converter board and the entire arrangement have been studied in order to minimize the length of these interconnections to minimize parasitic effects. In the following, the two most important blocks of the setup are described: the power converter board and the R_{DSON} measurement system.

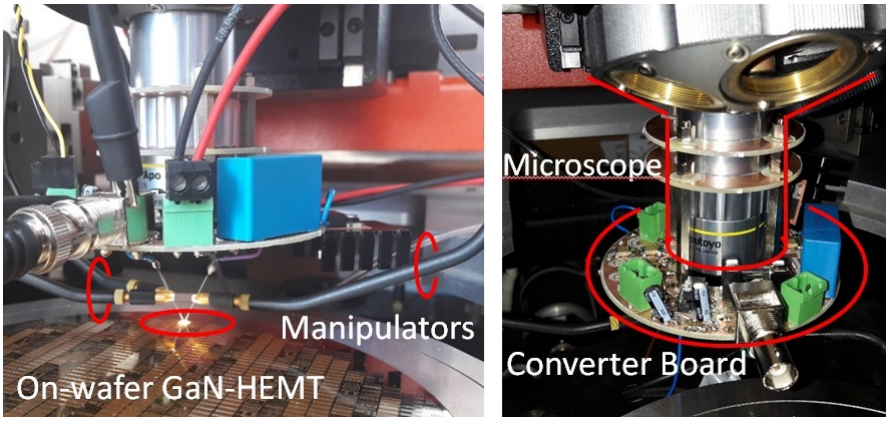

Figure 2.12: Pictures of the system. The power converter board, the microscope, the manipulators and, the wafer are clearly visible.

The power converter board

The power converter board consists of a diode based DC-DC boost converter topology. The board is equipped with all the components except for the switching transistor which is located on the wafer and has to be connected through the three manipulators previously described (respectively gate, drain and source connectors). Fig. 2.13 shows the schematic of the board. In order to guarantee the continuous mode operation (CCM) in the entire range of measurements, a 20 mH inductor (L) was adopted. The diode (D) is a zero recovery silicon carbide 600 V device. The gate driving is of crucial importance in switching power converters. In fact, driving large-area power transistors requires high-pulsed gate currents and oscillations have to be avoided in order to fully exploit the performance of GaN HEMTs [17]. The high-speed integrated circuit gate driver MIC4452YN by Micrel® has been used .This driver has a half bridge output stage which is able to provide high peak current (12 A) with a very low output resistance ($<$ 1.5 Ω) and it is able to provide pulses with very short rise and fall times (0.75 V/ns). Moreover, in order to prevent the gate voltage oscillation, an external gate series resistor of 22 Ω has been added. In turn, an external pulse generator drives the gate driver and provides the proper switching frequency and duty cycle. The power converter board is equipped with connectors in order to connect the voltage and current probes used to measure the transistor V_{DSON} and I_{DSON}.

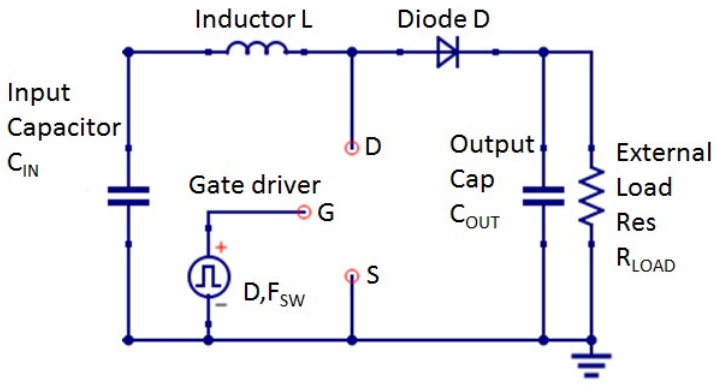

Figure 2.13: Schematic of the boost converter used for the power converter board.

The measurement equipment

In order to measure the R_{DSON} of the GaN HEMT under test, the ON-STATE drain to source voltage (V_{DSON}) and the ON-STATE drain to source current (I_{DSON}) are measured with a Tektronix DPO4104B oscilloscope (see fig. 2.14(a)). For the current measurement, a DC - 100 MHz bandwidth range current probe connected to the drain wire has been used. The sensitivity of the current probe is 1mA.

On the other hand, the measurement of the voltage is more complicated. In fact, the high voltage involved leads to the oscilloscope input channel saturation [18] - i.e. the distortion of the measured voltage due to the high voltage applied to the oscilloscope channel when the V_{DS} drops down from the value in OFF-STATE (100-600 V) to the ON-STATE one in linear region (< 2 V). To better understand the problem, fig. 2.15 shows a preliminary result obtained with the system: the inductor current (I_L) and the V_{DS} of the converter are depicted in the case of $V_{OUT} = 400$ V and load resistor $R_{LOAD} = 150$ kΩ. As can be noticed, the V_{DS} has a rectangular shape and swings between a few volts during the ON-STATE of the transistor and hundreds of volts (up to 600 V as maximum rating) during the OFF-STATE. In order to calculate the R_{DSON} with enough resolution, the vertical scale of the oscilloscope has to be reduced to at least 1 V/div. With such a low vertical scale setting and the high voltage applied at the same time, usually oscilloscopes suffer from saturation effects resulting in the distortion of the measured voltage signal due to the overdrive of the oscilloscope input stage. In literature, many solutions have been proposed to solve this problem (see for instance [18] and [19]). In this work, the clamp circuit described in [19] was adopted. The circuit is based on a high voltage MOSFET (M1) and a Zener

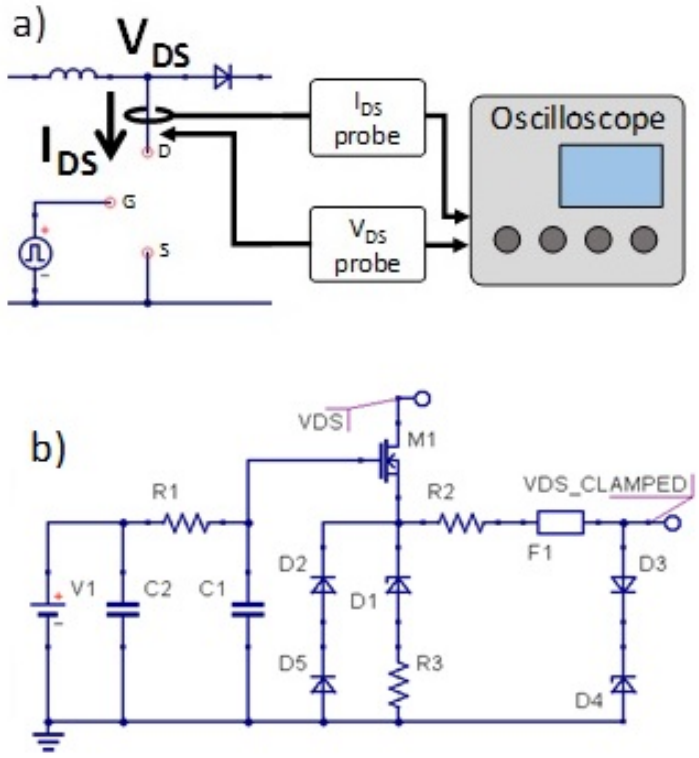

Figure 2.14: Schematic of the R_{DSON} measurement hardware. A current probe and a voltage probe measure the I_{DSON} and V_{DSON} respectively (a). The current probe is a high sensitivity 100 MHz current probe. The voltage probe is a custom voltage probe equipped with a voltage clamp circuit (b).

diode (D1) as depicted in fig. 2.14(b). The power supply V1 provides a voltage (9 V) to the gate of M1 higher than its threshold voltage ($\sim$ 1.5 V) and keeps it ON when the voltage to be measured (V_{DS}) is low (less than V1 - V_{TH} $\sim$ 7.5 V). In fact, when V_{DS} < (V1 - V_{TH}), the source voltage of M1 is less than (V1 - V_{TH}), and the condition $V_{GS} > V_{TH}$ is met. When V_{DS} to be measured drops down to typically hundreds of mV, a low current flows thorough M1 (I_{DSM1}) because the zener D1 is turned off and a very low current flows thorough R2 due to the very high input impedance of the oscilloscope probe. In this condition, M1 is turned ON in linear region with a very low I_{DSM1} thus we can neglect its drain to source ON voltage (V_{DSM1}), and the V_{DSON} of the GaN HEMT under test can be measured on the cathode of D1. On the other hand, if $V_{DS} >$ (V1 - V_{TH}), the current flowing through M1, D1, and, R3 raises, the source voltage of M1 increases, thus the V_{GS} of M1 decreases. This causes the MOSFET M1 to

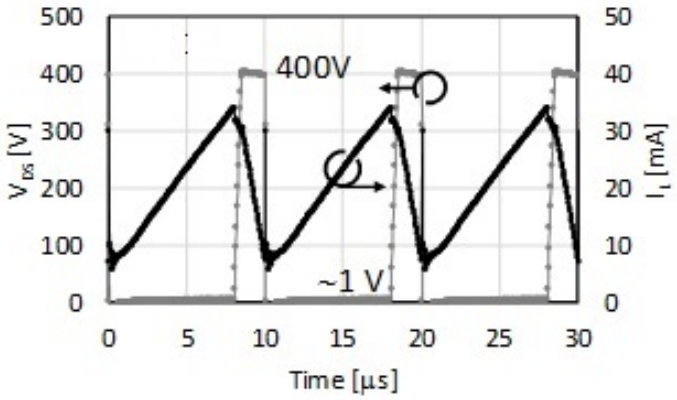

Figure 2.15: Inductor current I_L and V_{DS} voltage of the GaN HEMT under test during operation with switching frequency of 100 kHz, $V_{IN} = 72.5$ V, $V_{OUT} = 400$ V, load resistor $R_{LOAD} = 150$ kΩ . Related clamped V_{DS} waveform is reported in Fig. 2.17.

shut down when the condition $V_{GS} < V_{TH}$ is met. The voltage on the cathode of D1 is clamped to its Zener reverse voltage (V_Z) and the high voltage reached by V_{DS} is not applied to the oscilloscope input, thus avoiding the saturation of the oscilloscope channel. Referring to fig. 2.14(b) the components resistor R2, fuse F1, diodes D3 and, D4 are auxiliary and act as a safety circuit to prevent over-voltage on the input of the oscilloscope in the case of M1 failure. By using this circuit, good results in terms of bandwidth have been obtained.

Fig. 2.16 shows a PSPICE simulation of the clamp circuit. A 300V (High

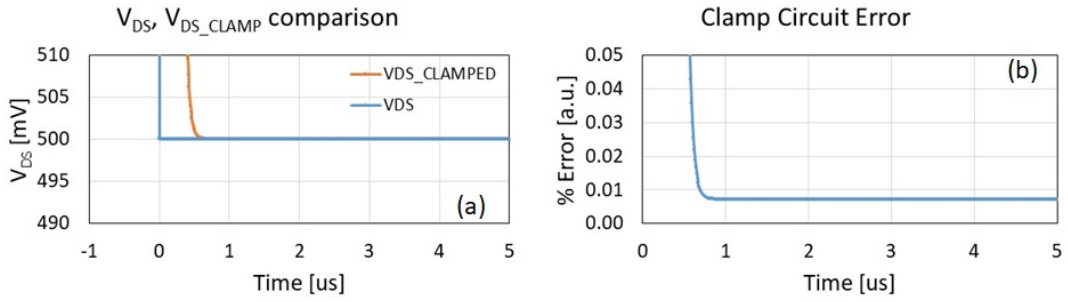

Figure 2.16: PSPICE simulation of the clamp circuit: (a)V_{DS} and $V_{DSCLAMPED}$ comparison, (b) error between the two waveforms.

level) - 500mV (Low level) square waveform is applied to the input (V_{DS}) of the clamp circuit of fig.2.14(b) and the related $V_{DSCLAMPED}$ is reported (see fig.

2.16(a)). As can be noticed the clamped waveform fits well the square waveform after an initial delay due to bandwidth limitation of the circuit. Fig. 2.14(b) shows that the percentage error between the two curves is less than 0.01 % after 1 µs. It will be clear soon that a measurement at 1 µs is a challenge in the real case due to oscillations introduced by parasitics. A reasonable minimum measurement sampling time will be 2 µs.

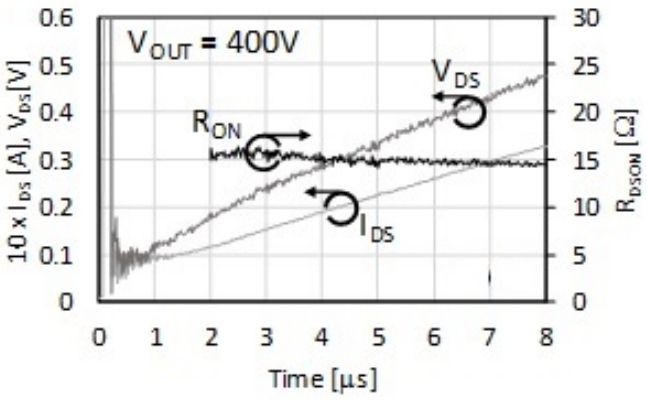

Figure 2.17: R_{DSON} measurement of the GaN HEMT under test during operation in the boost converter. V_{DS} is measured with the clamp circuit and can be considered valid after 2 µs from the turn on gate commutation. R_{DSON} is calculated as the ratio between V_{DS} and I_{DS} during the ON-STATE.

Fig. 2.17 shows the measurement results obtained with V_{OUT} = 400 V. The V_{DSON} and I_{DSON} waveforms during the ON-STATE of the transistor are reported. The two curves are triggered with the rising edge of the gate signal - i.e. the turn on commutation of the gate signal. As can be noticed, the V_{DS} and I_{DS} waveforms have a little ringing immediately after the drop of the V_{DS} from 400 V to hundreds of mV due to the parasitics of the connection wires and the circuit. After 2 µs from the turn on gate transition, the V_{DSON} signal can be considered valid and the R_{DSON} can be calculated as the ratio of the voltage and the current during the ON-STATE. This timing is perfectly suitable for the assessment of the dynamic behavior of state-of-the-art GaN HEMTs, which are supposed to work up to 600 V and close to 1 MHz frequency range. Considering the noise in the V_{DS} measurement, the sensitivity of the current probe and, the 8 bits resolution and the average mode of the oscilloscope, an error in the R_{DSON} measurement of 0.5 Ω in typical measurements (V_{OUT} = 200 V) has been estimated. This value is perfectly suitable to measure the R_{DSON} of on-wafer devices which is in the

range between 5 Ω to 100 Ω.

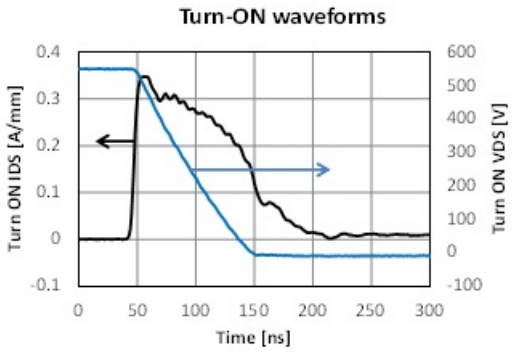

Figure 2.18: Typical turn ON waveforms during operation in the boost DC-DC converter at 550V

Finally, it is worth noticing that the system is also able to measure the transients waveforms during the turn ON and turn OFF switching events. This is an important feature since it allows (i) to identify the amount of instantaneous current and power that the device has to withstand during hard switching operation and (ii) to study the mode of operation of the devices during hard switching. Fig. 2.18 reports the typical I_{DS} and V_{DS} turn ON waveforms of the device during operation in the boost DC-DC converter. As can be noticed, the turn ON I_{DS} and V_{DS} waveforms are overlapped and this demonstrate that the turn ON occurs in a hard switching mode since the device is subjected to simultaneous high current and high voltage. From the transient current and voltage waveforms the instantaneous power during the hard switching event can be calculated as reported in fig 2.19.

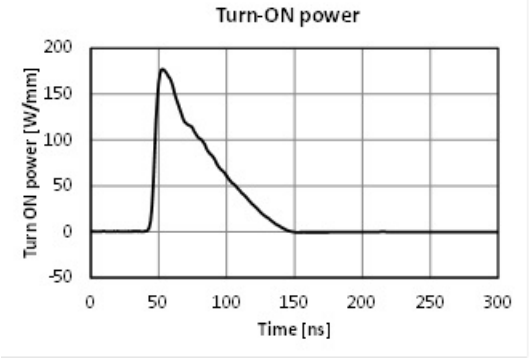

Figure 2.19: Typical turn ON instantaneous power during operation in the boost DC-DC converter at 550V

2.2.2 The novel measurement concept description

In this section some novel in-circuit measurement techniques based on the novel on-wafer hard-switching system are described. Both performance and reliability measurements can be achieved using the system.

Performance assessment: voltage sweep measurement

The novel system developed within this thesis emulates the switching application conditions and it is able to study all the mechanisms responsible for the R_{DSON} variation: (i) the change of the junction temperature (T_J), (ii) the charge trapping due to hot electrons formation during hard switching and, (iii) the charge trapping due to the high electric field induced during high voltage operation. With such a system, a real performance assessment of on-wafer GaN power HEMTs is now available, thus shortening the loop in the development process of such technology. In fact, the operation in a power converter is typically evaluated only after the device packaging at the end of the production process. The novel system of this thesis allows assessing the switching performance of devices at wafer level and therefore if enables also studying in detail the physical processes and failure mechanisms that can occur during real application operation.

In order to investigate the GaN HEMT R_{DSON} variation during operation in the wafer-level boost power converter as a function of the output voltage (V_{OUT}), measurements with increasing output voltage from $\sim$ 60 V to $\sim$ 600 V have been carried out. The main parameters (duty cycle D, switching frequency F_{SW}, and load resistor R_{LOAD}) of the converter are kept fixed. It is worth noticing that with this approach also the impact of the junction temperature T_J on the R_{DSON} is taken into account since the load is fixed and the output current and power increase with the rising V_{OUT}. Table 2.1 summarizes the typical boost converter settings used for the analysis of the GaN HEMTs R_{DSON}. In order to obtain the

Table 2.1: Typical boost converter settings

Symbol	Quantity	Value
D	Duty cycle	80%
F_{SW}	Switching frequency	100 kHz
R_{LOAD}	Load resistor	150 kΩ
V_{IN}	Input voltage	from $\sim$ 12 V to $\sim$ 120 V
V_{OUT}	Output voltage	from $\sim$ 60 V to $\sim$ 600 V

output voltage in the range from ∼60 V to ∼600 V, the input voltage (V_{IN}) was adjusted between ∼12 V and ∼120 V. For each V_{OUT}, the R_{DSON} of the GaN HEMT is measured. Note that, in a boost DC-DC converter, the output voltage is equal to the drain to source voltage of the GaN HEMT when it is in OFF-STATE ($V_{OUT} = V_{DSOFF}$) thus with this kind of measurement, the overall impact of the high voltage, temperature and, hot-electrons on R_{DSON} was investigated.

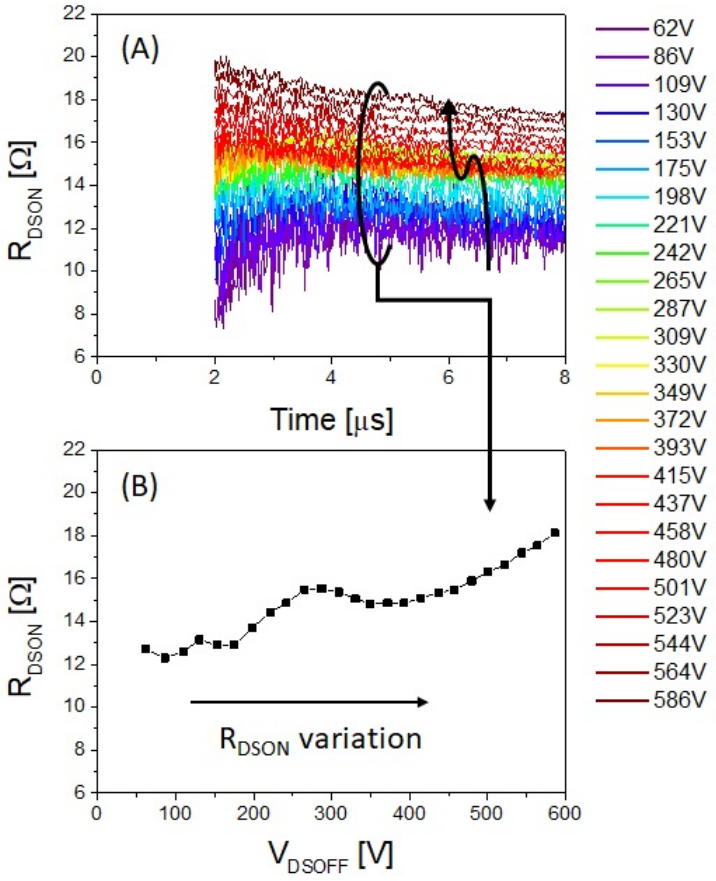

Figure 2.20: R_{DSON} measurement during operation for a device which suffer from dynamic R_{DSON} due to charge trapping, V_{OUT} from 62 V to 586 V.

Fig. 2.20(A) reports the R_{DSON} waveforms as a function of the ON time for V_{OUT} varying from 62 V to 586 V for a typical device which suffers from high voltage charge trapping issues. From this plot the R_{DSON} values as a function of the V_{DSOFF} con be extracted (see fig. 2.20(B)). The R_{DSON} values are calculated 5 µs after the turn on of the transistor (see black circle in fig. 2.20(A)). As can be noticed, the R_{DSON} changes as a function of V_{OUT}, due to (i) the increase of the device temperature, which is not considered in conventional double-pulse

measurements and (ii) the increase of the trapping mechanisms (due both to the high voltage and the hard switching trapping). It is worth noticing that, with increasing V_{OUT}, also an increase of the junction temperature is expected due to the fixed load.

Reliability assessment: stress measurement

As far as the reliability assessment is concerned, the real application system can be used to stress devices in hard switching conditions. In particular the evolution of the R_{DSON} during the stress can be monitored. It should be noted that the typical DC link voltage in 230 V AC/DC converter is at around 400 V, so the maximum output voltage of the system (600 V) allows for highly accelerated stress testing of the devices. The stress consists in making the on wafer GaN HEMT device working in the boost DC-DC converter at high voltage (i.e. 550V) and monitor the R_{DSON} and the switching waveforms during operation until the device failure. Fig. 2.21 reports a typical R_{DSON} evolution of an on-wafer GaN HEMT during operation in the boost DC-DC converter. Results show that the R_{DSON} increases up to 25% during the stress and a time to failure (TTF) of ∼6.8 hours is observed. This preliminary measurement demonstrates the capability of the novel system to stress GaN HEMTs in hard-switching conditions.

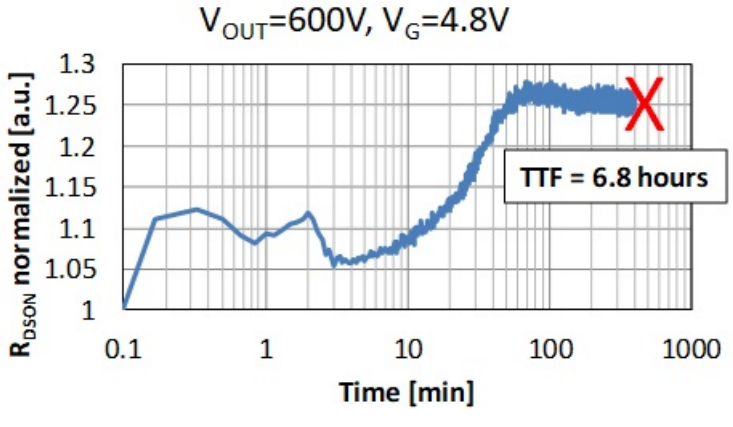

Figure 2.21: R_{DSON} evolution during stress test at 600 V for a sample device until failure

Limitations of the system

Parasitics represent the main limiting factor for our proposed system. Fig. 2.22 shows a schematic representation of the parasitics introduced by the connection wires of the Drain, Gate and Source of the transistor. The three wires have a parasitic series inductance (L_{PG}, L_{PD} and, L_{PS} respectively) of about 30 nH.

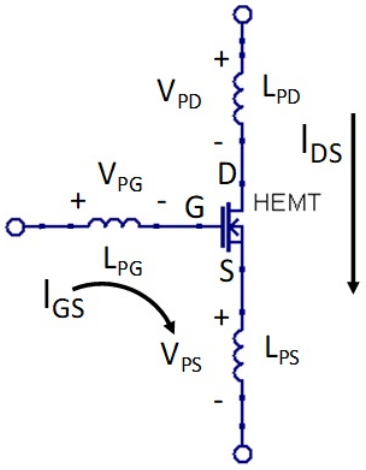

Figure 2.22: Parasitics of the system due to connections

Due to the change over time of the current flowing through the transistor's terminals during switching operation, these inductors can cause parasitic voltage drops (V_{PD}, V_{PG} and, V_{PS} respectively), which can modify the V_{GS} and V_{DS} of the HEMT. $V_{P(D/G/S)}$ can be calculated as follows:

$$V_{PD} = L_{PD}\frac{dI_{DS}}{dt} \tag{2.1}$$

$$V_{PG} = L_{PG}\frac{dI_{GS}}{dt} \tag{2.2}$$

$$V_{PS} = L_{PS}\frac{d(I_{DS} + I_{GS})}{dt} \tag{2.3}$$

where $V_{P(D,G,S)}$ are the parasitic voltage drops through the parasitic inductance respectively of the Drain, Gate and Source terminals and $L_{P(D,G,S)}$ are the parasitic inductance respectively of the Drain, Gate and Source terminals.

The parasitics analysis can be divided in two parts: (i) the effects of parasitics on the V_{DSON} and (ii) the effects on the V_{GS}. As far as the V_{DSON} is concerned, L_{PD} and L_{PS} affect the V_{DSON} measured by the system due to the parasitics

voltage drops V_{PD} and V_{PS} (see fig. 2.22). However, due to the low working currents ($\sim$ 50 mA) and the low dI_{DS}/dt, the parasitics have a negligible effect on the V_{DS}. In fact, by considering the maximum current ($\sim$ 50 mA), the parameters reported in table 2.1 and by calculating the T_{ON} as follows

$$T_{ON} = T_{PERIOD} * D = 10\mu s * 0.8 = 8\mu s \tag{2.4}$$

we obtain

$$V_{PD} + V_{PS} < 0.5mV \tag{2.5}$$

This voltage level is negligible compared to the measured V_{DSON}, which is in the range of hundreds of mV. As far as the V_{GS} is concerned, we have to consider the effects of L_{PG} and L_{PS} on the gate drive circuit. These inductors can lead to the ringing of the gate signal and to the slowdown of the switching speed [20]. In order to limit these effects, a series-dumping resistor on the gate and/or a slowdown circuit for the gate signal can be adopted. In the system proposed in this work, a series resistance of 22 Ω was adopted: this prevents the gate ringing but slows down the maximum dV_{DS}/dt reachable and increases the switching losses. Despite of parasitics introduced by the connection wires, we were able to mimic hard-switching application conditions with the on wafer device obtaining good results in terms of accuracy on the R_{DSON} measurement and in terms of minimum measurement time (2 μs). Such time-frame is comparable with those reported in previous studies on conventional setups, see for instance [21] and references therein.

It is worth noting that one of the main critical issues of our proposed system is that during operation it is difficult to discriminate the impact of temperature on the R_{DSON} increase. In fact, it will be clear on section 4.1 (by comparing results of the R_{DSON} variation obtained in the boost DC-DC converter respect to the double pulse system) that the in-circuit system proposed is able to discriminate the effects of the high voltage electric field respect to that induced by hard switching and temperature together. It is not able to separate the effects of temperature and hard switching on R_{DSON}. Finally, it is worth mentioning that our system cannot reproduce perfectly the hard switching regime of a package level device. In fact, parasitics introduced by connections of our system cannot match the parasitics introduced by the package of a real device. In particular, due to the long connections and the tip contacts, our system can be considered as a worst case of parasitics level and it is useful to test devices in a detrimental hard

switching regime. At last, it is important to clarify that usually GaN HEMTs real applications use a half-bridge configuration; namely the freewheeling diode, used in the boost converter of this work, is replaced with a high side device connected to the power supply. The choice of a freewheeling diode in the system was due to its ease of operation and because it would be very complicated to connect another on-wafer device for the high side transistor.

2.3 Chapter summary

The first part of this chapter presented the most important state of the art dynamic measurement techniques used to investigate performance and reliability of GaN HEMT devices. In particular the double pulse, fast backgating, DCT and TLP measurement techniques were presented. Table 2.2 summarizes the aim of each measurement technique.

Table 2.2: State of the art dynamic measurement techniques

Measurement	Aim
Double Pulse	Investigate the dynamic R_{DSON} or the V_{TH} shift as a function of the drain or the gate voltage in soft switching conditions
Fast backgating	Investigate the location of the traps, whether they are located in the buffer or in the surface
Drain Current Transient	Find the activation energy of the trapping process and correlate it with the chemical species responsible for the charge trapping states
TLP	Investigate pulsed behavior at very short time (100ns) and measure the safe operation area (SOA) of devices

The second part of this chapter presented a novel measurement system able to test the device in real life conditions and to measure the dynamic R_{DSON} during operation. Preliminary measurements showed that (i) the device is tested in hard-switching conditions with high transient power, (ii) the system is able to measure the dynamic R_{DSON} during operation starting from 2 μs respect to the turn on of the gate voltage. Finally, preliminary measurements demonstrated that both the dynamic R_{DSON} and the reliability of the device under test (DUT)

are affected by hard switching operation conditions and the system is able to study these phenomena.

Chapter 3

The on-wafer hard-switching novel test system. Detailed analysis

In this chapter a detailed analysis of the novel system to test on-wafer GaN HEMT devices in hard-switching conditions is reported. At first, a detailed analysis of the hard-switching operation mode occurring in the boost DC-DC converter is reported. In particular, the switching transients during the turn ON and turn OFF events are analyzed. Using the results obtained, a simplified version of the system is proposed which has several advantages: (i) low parasitics, (ii) simplicity in testing concept, (iii) self limiting failure current, (iv) ease in settings tests parameters such as hard switching energy, current and voltage levels.

3.1 Boost converter basics

Fig. 3.1 shows the circuit diagram of the diode based boost DC-DC converter used in the system developed within this thesis. In order to limit parasitics at the drain node, a zero recovery SiC high voltage diode has been used. A proper inductance value for the inductor was chosen in order to obtain continuous or discontinuous conduction mode of operation (CCM and DCM) depending on the type of measurement. The main advantage of using a boost DC-DC converter is that no high voltage power supply is needed to test devices since the very high voltage (up to 600 V) is obtained with the converter itself. As can be noticed, in the boost DC-DC converter the drain switching transistor is connected to an inductive load (L) and no snubber circuits or resonant topology are used,

thus this circuit can be used to test the HEMT transistor in real hard switching operation conditions.

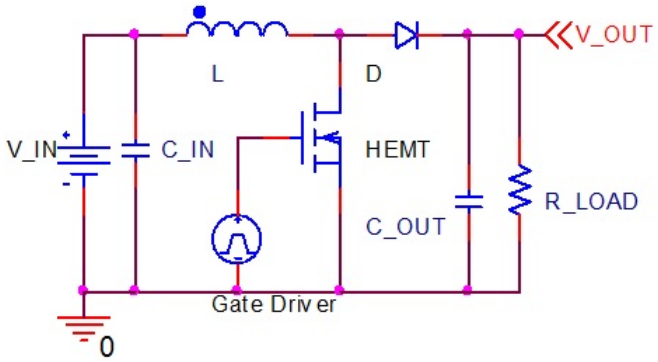

Figure 3.1: DC-DC boost converter circuit diagram

In order to better understand the behavior of the switching transistor working in the DC-DC converter of fig. 3.1, a brief recall of the boost converter operation modes are here reported. Figs. 3.2 and 3.3 show the typical transistor drain to source voltage (V_{DS}), gate to source voltage (V_{GS}) and inductor current (I_L) waveforms of a DC-DC boost converter working in continuous (CCM) and discontinuous (DCM) modes. The main difference between the two modes is that in CCM I_L is always grater than 0, instead in DCM I_L drops to 0 for a finite amount of time after the freewheeling phase (i.e. when the diode is ON and the HEMT is OFF).

3.1.1 CCM mode analysis

In CCM mode the condition $I_L > 0$ is always met thus, since the current has to find a recirculation path, the converter works alternating two states: (i) HEMT ON diode OFF and (ii) HEMT OFF diode ON. In this mode of operation the voltage gain can be written as follows:

$$M = \frac{U_{out}}{U_{in}} = \frac{1}{1-d} \tag{3.1}$$

with

$$d = \frac{T_{ON}}{T_{PERIOD}} \tag{3.2}$$

and

$$T_{PERIOD} = \frac{1}{F} \tag{3.3}$$

where U_{out} is the output voltage, U_{in} is the input voltage, d is the duty cycle, T_{ON} is the ON time of the switching transistor, T_{PERIOD} is the switching period and F is the switching frequency. It is worth noticing that, when the transistor is OFF, the drain voltage is equal to U_{out}, i.e. $V_{DSOFF} = U_{out}$. As a result, by changing the converter output voltage (i.e. by changing U_{in} or d) the device under test is subjected to different OFF state voltage. This concept will be used in the next chapter to test the devices increasing the drain OFF voltage. Finally, we will see in the next sections that it is important to focus on the turn ON transient waveforms. In fig. 3.2 (red square), the power converter conditions immediately before the transistor turn ON are visible: $V_{DS} = V_{OUT} >> 0$ V and $I_L > 0$ A. Whit these starting conditions the transistor switches in hard switching mode and is subjected to the simultaneous presence of high voltage and high current.

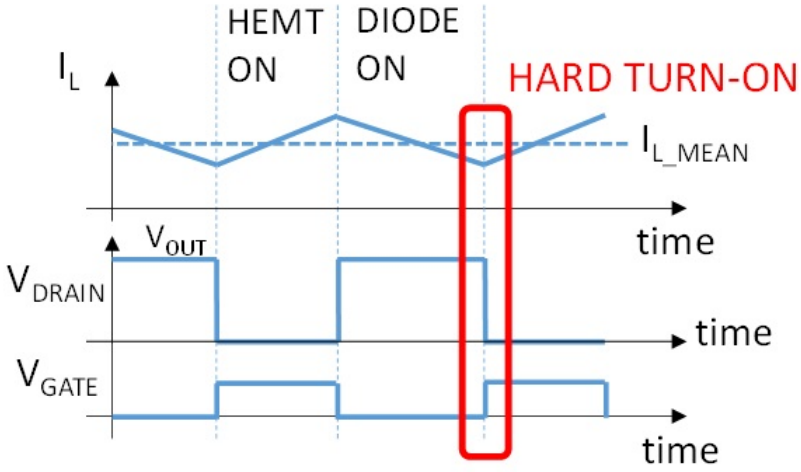

Figure 3.2: Boost converter continuous mode of operation (CCM) waveforms

3.1.2 DCM mode analysis

In DCM mode the condition $I_L = 0$ is verified for a finite amount of time thus an additional state occurs during operation: (i) HEMT ON diode OFF, (ii) HEMT OFF diode ON and (iii) HEMT OFF diode OFF. In this mode of operation the voltage gain can be written as follows:

$$M = \frac{U_{out}}{U_{in}} = 1 + d^2 \cdot \frac{U_{in}}{2 \cdot F \cdot L \cdot I_{out}} \tag{3.4}$$

where I_{out} is the load current. It is worth noticing that in DCM mode the inductor current drops to zero naturally during the transistor OFF phase. During the

subsequent turn ON the device switches in zero current switching (ZCS) mode in soft switching regime since the inductor current is zero (see fig. 3.3 red square). This demonstrates that DCM operation is less demanding respect to CCM in terms of hard switching stress. As a result of this, in order to test devices in hard-switching conditions, CCM mode has to be guaranteed during operation.

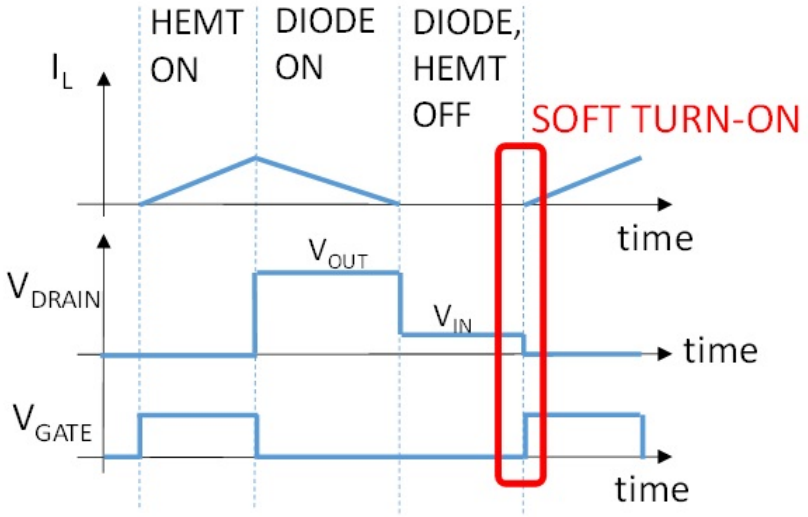

Figure 3.3: Boost converter discontinuous mode of operation (DCM) waveforms

3.2 MOSFET hard switching basics

In order to understand the basics concerning the switching transients of a device working with an inductive load, in this section we look in detail inside the switching waveforms during hard switching operation for a MOSFET device. The analysis is a summary of chapter 3 reported in [22]. Fig. 3.4 reports the simple equivalent circuit diagram that can be used to analyzed the behavior of a power transistor working with an inductive load. This circuit diagram can be used to analyze the device switching process in the general case of hard-switching turn ON and turn OFF in the ideal case. The switching device is replaced with an ideal switch (S). In order to focus only on the switching transients, the current ripple of the inductor current can be neglected, thus the inductor is replaced with a constant current generator (I_{on}) . An ideal voltage generator V_{off} apply the off state voltage to the switching device.

Fig. 3.5(a) reports the transients switching waveforms in the ideal case. In order to simplify the analysis, a linear behavior of voltage and current is assumed.

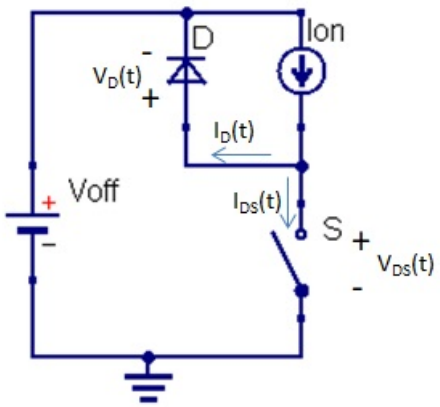

Figure 3.4: Inductive load simplified circuit diagram: ideal case

It is worth noticing that device voltages and currents are constrained by Kirchhoff laws as follows:

$$\begin{aligned} I_{on} &= I_D(t) + I_{DS}(t) \\ V_{off} &= V_{DS}(t) - V_D(t) \end{aligned} \tag{3.5}$$

Due to these constrains, during turn-ON the switch (S) voltage ($V_{DS}(t)$) cannot drops down until the diode turns off, namely when its current reaches zero (i.e. when $I_{DS}(t) = I_{on}$). As a consequence, during the t_{ri} interval (see fig. 3.5) the $V_{DS}(t)$ is clamped to V_{off} and only after the $I_{DS}(t)$ reaches I_{on} the $V_{DS}(t)$ can decrease to zero during the t_{fv} interval. On the contrary, during turn-OFF the switch current cannot drops down until the diode turns ON (i.e. when $V_D(t) \geq 0$ V). As a consequence, during the t_{rv} interval the $V_{DS}(t)$ increases and the $I_{DS}(t)$ is fixed to I_{on} since the diode is still OFF. When $V_{DS}(t)$ reaches V_{off} the diode turns ON and the $I_{DS}(t)$ can drops down to zero during the t_{fi} interval. Fig. 3.5(b) reports the voltage/current trajectories in the device's output characteristic plane corresponding to the analyzed $V_{DS}(t)$ and $I_{DS}(t)$ waveforms. This plot is also called in literature as "locus" since it reports the set of bias points ($V_{DS}(t)$, $I_{DS}(t)$) which the device has to withstand during the hard switching transients. As can be noted in the ideal case the locus has a rectangular shape. Looking at fig. 3.5(a) one can easily see that, during turn-ON and turn-OFF transients, a not-negligible power dissipation occurs since there exist intervals where current and voltage are simultaneously present through the switching device. In fig. 3.5(a) the instantaneous power loss is reported ($p_{SW}(t)$): as can be noticed, in the ideal case, the instantaneous power has a triangular shape both during turn-ON and turn-OFF.

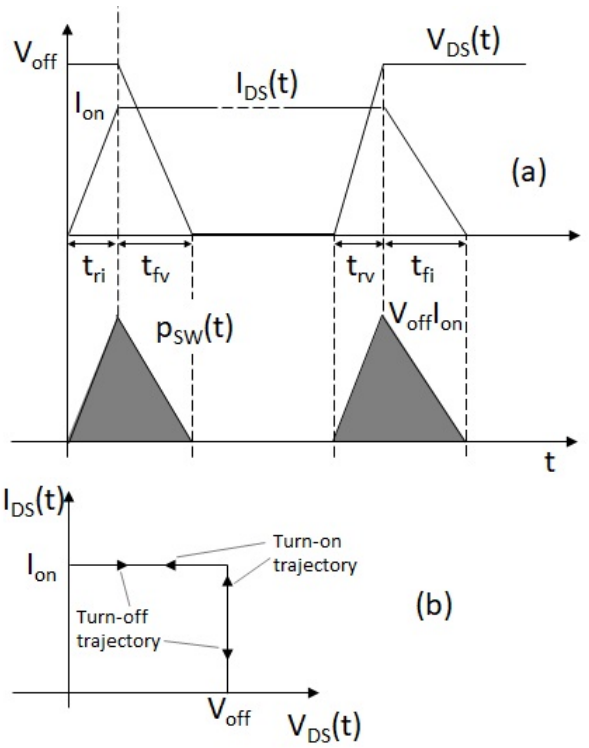

Figure 3.5: Inductive load hard switching waveforms in the ideal case. (a) V_{DS} and I_{DS} transients waveforms and (b) ideal locus i.e. the switching trajectories during turn-ON and turn-OFF intervals

Until now, the hard switching behavior was analyzed in the ideal case where the switching device is replaced by an ideal switch. In real life, the switching transients are affected (i) by the device behavior, (ii) by the gate driver and (iii) by the external parasitics. In order to analyze in detail the switching transients in a real case, in fig. 3.6 the ideal switch is replaced by a MOSFET and a gate resistor R_G is also added. R_G take into account for both the external resistor which usually is added to prevent oscillation in the gate loop and the internal finite output resistor of the gate driver.

Before analyzing in detail the switching transients in the case study of fig. 3.6 it is necessary to introduce the real equivalent model of the MOSFET reported in fig. 3.7. In the model, the three non-linear capacitances C_{GS}, C_{GD} and C_{DS} are reported. Moreover, the controlled current generator I_{DSsat} and the resistor R_{DSon} model the transistor respectively in saturation and linear regions. It is worth introduce here also other three quantities that are commonly found in MOSFET datasheets which are important in terms of switching behavior:

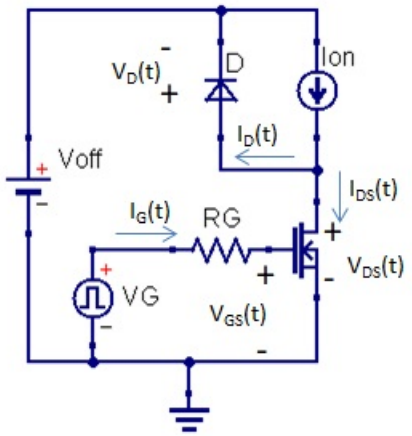

Figure 3.6: Inductive load simplified circuit diagram including the MOSFET power transistor and the simplified gate driver circuit

The input capacitance:

$$C_{ISS} = C_{GS} + C_{GD} \tag{3.6}$$

The Miller capacitance:

$$C_{RSS} = C_{GD} \tag{3.7}$$

The output capacitance:

$$C_{OSS} = C_{DS} + C_{GD} \tag{3.8}$$

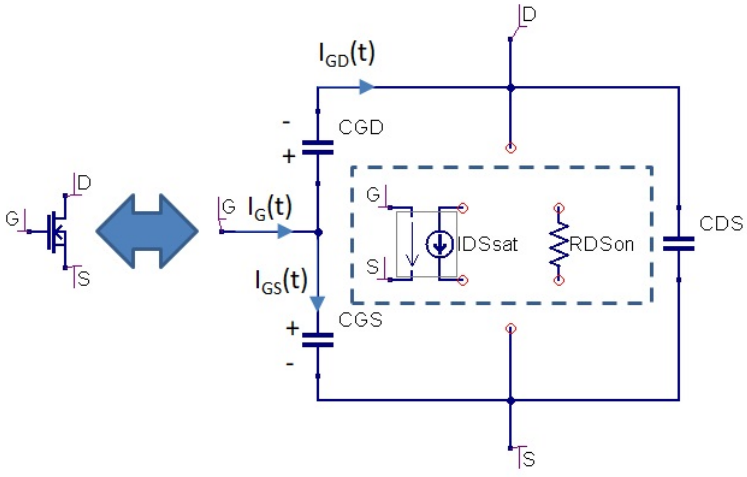

Figure 3.7: MOSFET equivalent model

In order to better understand the hard switching behavior of the MOSFET reported in fig. 3.6, a detailed analysis of the turn-ON switching transient is

reported in the next paragraph. In order not to broaden the discussion, the turn-OFF transient will be not analyzed here. Moreover, it will be clear later that, in the novel hard switching system proposed within this thesis the turn ON event is more important in terms of hard switching stress, thus it is important to focus the analysis on the turn ON event.

Fig. 3.8 show the typical turn-ON transient waveforms of a MOSFET working in the circuit of fig. 3.6.

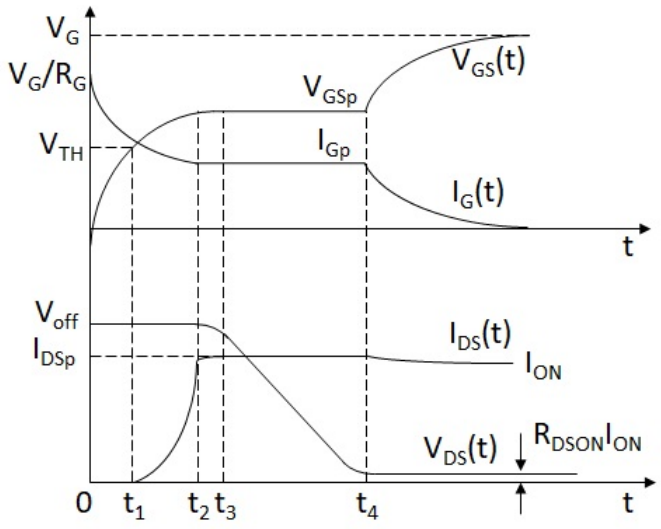

Figure 3.8: Main turn ON waveforms of a MOSFET working with an inductive load circuit

As can be noticed, the turn-ON transient can be divided into 5 intervals:

- $0 < t < t_1$:

  during this interval, the MOSFET is OFF and the current I_{on} is freewheeling through the diode D, which is in ON state. Being the $V_{DS}(t)$ constant to V_{off}, the C_{DS} current is zero and the other two remaining capacitors C_{GS} and C_{GD} act as they are connected in parallel. During this phase the MOSFET's input capacitance (C_{ISS}) is charged through the R_G resistor. This interval ends when $V_{GS}(t)$ reaches the MOSFET threshold voltage (V_{TH}).

- $t_1 < t < t_2$:

  When the $V_{GS}(t)$ reaches the threshold voltage the MOSFET drain current ($I_{DS}(t)$) starts to increases. Being the DIODE still on, the $V_{DS}(t)$ remains clamped at V_{off}. As a consequence, the MOSFET is in saturation since

the $V_{GS}(t)$ is above the threshold voltage and the $V_{DS}(t)$ is large. The gate-source voltage continues to rise causing the Drain current to increase until the current $I_{DS}(t)$ becomes equal to I_{on} with the consequent diode turn-OFF.

- $t_2 < t < t_3$:

  During this short interval the diode is OFF, the $V_{GS}(t)$ and $I_{DS}(t)$ continues to increase and the C_{DS} starts discharging. The decrease of the $V_{DS}(t)$ causes the changing of the gate current ($I_G(t)$). In fact, $I_G(t) = I_{GD}(t) + I_{GS}(t)$ where $I_{GD}(t)$ is the current flowing through the Miller capacitance and $I_{GS}(t)$ is the current flowing through the C_{GS} (see fig. 3.7). In particular, the decrease of the $V_{DS}(t)$ causes the increase of the $I_{GD}(t)$ and the decrease of the $I_{GS}(t)$. This phase ends when $I_{GS}(t)$ reaches zero. The MOSFET is in saturation region with constant $I_{DS}(t) \sim I_{on}$ thus $V_{GS}(t)$ and $I_G(t)$ remain constant causing a linear decrease of the $V_{DS}(t)$ voltage. At such equilibrium point the following equation can be written:

$$I_G(t_3) = I_{Gp} = \frac{V_G - V_{GSp}}{R_G} = C_{GD}\frac{dV_{GD}}{dt} = -C_{GD}\frac{dV_{DS}}{dt} = constant. \quad (3.9)$$

- $t_3 < t < t_4$:

  This interval is the so called "plateu" region. The $V_{GS}(t)$ is constant and using equation 3.9 the $V_{DS}(t)$ decrese speed can be calculated:

$$\frac{dV_{DS}}{dt} = -\frac{I_{Gp}}{C_{GD}} = \frac{V_G - V_{GSp}}{R_G C_{GD}} \quad (3.10)$$

  This equation shows that the turn-ON transient speed is dominated by the gate driver resistance and the Miller capacitance of the device. In particular, the more current the driver is able to provide (i.e. the lower is R_G) the faster is the transient. This phase ends when $V_{DS}(t)$ decreases to few volts and the MOSFET enter in linear region.

- $t > t_4$: This is the last interval where the transistor is in linear region and the $V_{GS}(t)$ starts to increase again exponentially up to the driver supply voltage (V_G) charging the input capacitance C_{ISS}. The MOSFET channel can be represented by a resistance (R_{DSon}) thus the $V_{DS}(t)$ reaches the value $I_{on}R_{DSon}$.

In order to summarize the MOSFET behavior in hard-switching operation it is important to focus on the $t_3 < t < t_4$ interval. In particular, the dV_{DS}/dt speed is totally dominated by the gate resistance and by the Miller capacitance. Moreover, in the gate waveform the so called "plateau" region is clearly visible. Similar consideration are also valid for the turn-OFF transient, i.e. the dV_{DS}/dt is totally affected by the gate resistance and by the Miller capacitance and a "plateau" region appears in the gate voltage waveform. As far as the turn-OFF is concerned, the equation 3.10 can be rewritten as follows:

$$\frac{dV_{DS}}{dt} = \frac{I_{Gp}}{C_{GD}} = \frac{V_{GSp}}{R_G C_{GD}} \tag{3.11}$$

3.3 HEMT saturation current limited switching mode

In this section a detailed analysis of the switching waveforms of GaN HEMTs is reported showing that the behavior is different respect to the MOSFET device. In order to start the analysis, a preliminary simulation in OrCAD PSpice was carried out. A MOSFET IRF820 and a HEMT GS66502B by GaNSystem were simulated in the circuit reported in fig. 3.6 and the related switching waveforms were compared. It is necessary to consider that these two devices are packaged and, respect to the on-wafer devices usually tested within this thesis, (i) they sink much more current and (ii) they have a much smaller R_{DSON}. Despite this, they behave very similar in terms of hard-switching transients. Fig. 3.9 shows the

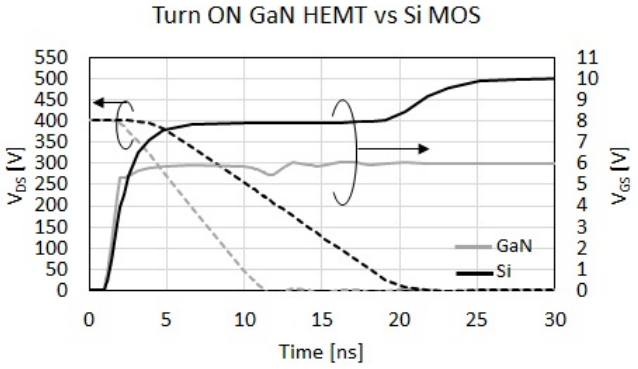

Figure 3.9: Turn ON simulated waveforms comparison: MOSFET vs GAN HEMT

obtained results. As can be noted, the GaN device is faster (see the dotted $V_{DS}(t)$

curves). Moreover, looking at the $V_{GS}(t)$ waveforms (full curves in the plot), the MOSFET shows the previously reported "plateau" region instead the HEMT device seems not to evince this phase. In order to conclude this introduction, it is clear that the GaN transistor is faster and it has a different transient behavior.

In order to analyze in detail the behavior of on-wafer GaN HEMT devices working in hard-switching conditions in the boost converter based system developed within this thesis, measurements with different gate resistance (R_G) and external drain capacitance (C_{DSADD}) were carried out (see fig. 3.10). Tested devices have a gate width (W_G) of 1.5mm and are tested with the system described in section 2.2.1. In order to understand the transient switching behavior of GaN HEMTs, the $V_{DS}(t)$, $V_{GS}(t)$ and $I_{DS}(t)$ transient waveforms during operation are acquired and compared for each condition.

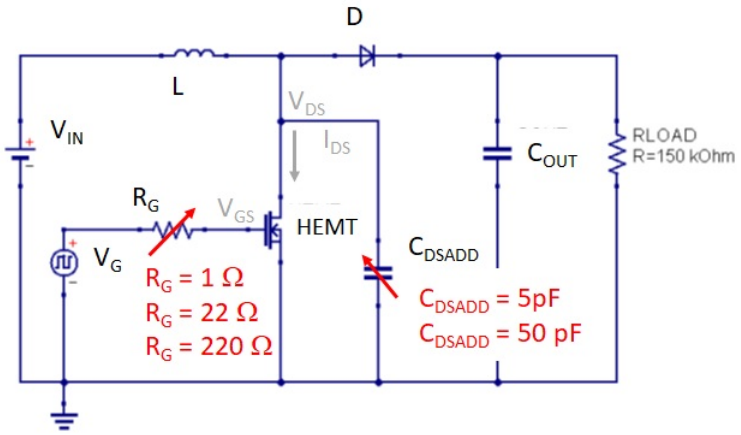

Figure 3.10: Experiment carried out in order to investigate hard switching behavior of GaN HEMTs

Fig. 3.11 and 3.12 show results obtained for the turn OFF analysis by changing respectively the gate resistance in the range of 1 Ω - 220 Ω and the drain capacitance in the range of 5 pF - 50 pF. As can be noticed in fig. 3.11, regardless of the R_G value, at first, the $V_{GS}(t)$ zeroes without showing any "plateau" region and then $V_{DS}(t)$ increases up to V_{OUT} = 100 V. As far as the drain current is concerned, the $I_{DS}(t)$ drops to almost zero during the increase phase of the drain voltage. This small amount of current charges the C_{OSS} of the transistor and the parasitics and does not flows through the HEMT, which has $V_{GS}(t) = 0$ V and is OFF. As a consequence, we can conclude that the turn-OFF switching transient occurs in soft-switching conditions i.e. there is not an overlapping in the $V_{DS}(t)$ and $I_{DS}(t)$ waveforms during the turn-OFF event. Also the results reported in

fig. 3.12 confirm this important result: as can be noticed by changing the C_{DSADD} also the $V_{DS}(t)$ rise time changes and still no "plateau" region appears in the gate voltage waveform. This behavior confirms the soft-switching operation mode during the turn-OFF transient since the $V_{DS}(t)$ rise time should not depend on the drain capacitance during hard-switching operation (see equation 3.11).

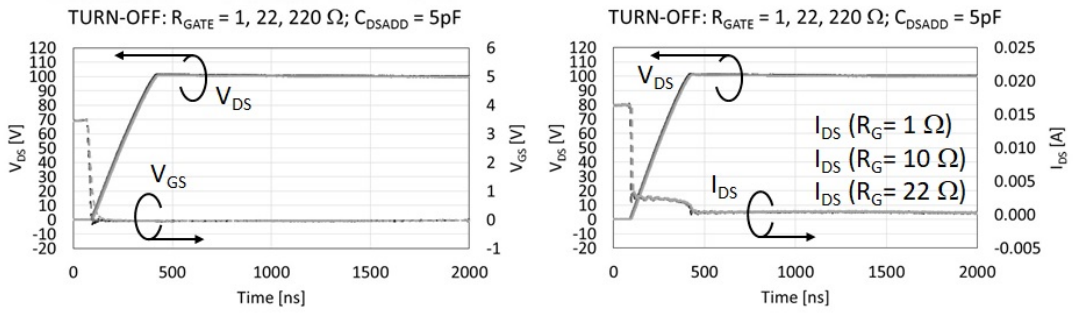

Figure 3.11: Turn OFF waveforms of a typical $W_G = 1.5$mm on-wafer device in the boost converter. $V_{OUT} = 100$ V, $C_{DSADD} = 5$ pF, $R_G = 1\ \Omega$, 10 Ω and, 22 Ω

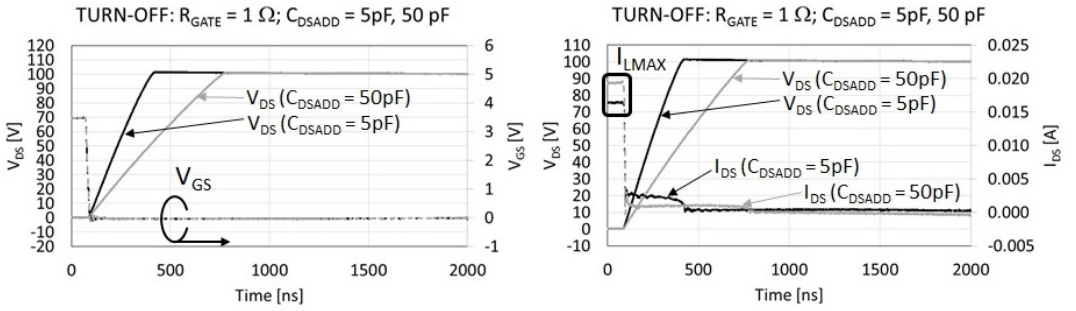

Figure 3.12: Turn OFF waveforms of a typical $W_G = 1.5$mm on-wafer device in the boost converter. $V_{OUT} = 100$ V, $C_{DSADD} = 5$ and 50 pF, $R_G = 1\ \Omega$

The important result obtained with the analysis reported in fig. 3.11 and 3.12 is that the GaN HEMT device, working in the boost DC-DC converter of fig. 3.10, switches in soft-switching mode during turn OFF. The inductor current reached during the ON phase (I_{LMAX} reported in fig.3.12) charges the total parasitic capacitance of the drain node at almost constant current. As a consequence, the following equation can be written:

$$I_{LMAX} = C_{DPARTOT}\frac{dV_{DS}}{dt} \tag{3.12}$$

where $C_{DPARTOT}$ is the total parasitic capacitance of the Drain node. From 3.12 the $C_{DPARTOT}$ can be calculated: in the case of C_{DSADD} = 50 pF, the $C_{DPARTOT}$ is equal to 117 pF.

In the next paragraph a detailed analysis of the turn ON transient is reported. Fig. 3.13 and 3.14 show the results obtained for the turn ON analysis by changing respectively the gate resistance and the drain capacitance.

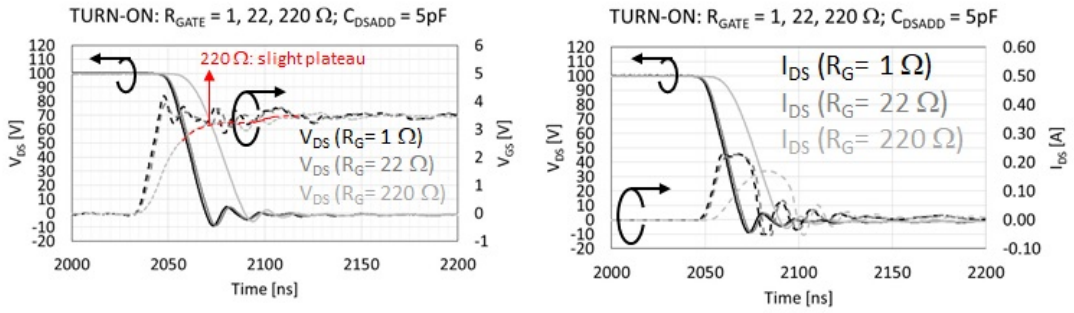

Figure 3.13: Turn ON waveforms of a typical W_G = 1.5mm on-wafer device in the boost converter. V_{OUT} = 100 V, C_{DSADD} = 5 pF, R_G = 1 Ω , 10 Ω and, 22 Ω

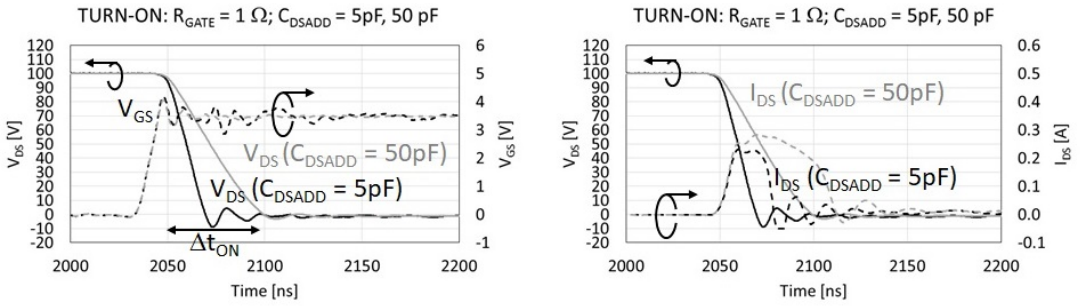

Figure 3.14: Turn ON waveforms of a typical W_G = 1.5mm on-wafer device in the boost converter. V_{OUT} = 100 V, C_{DSADD} = 5 and 50 pF, R_G = 1 Ω

As can be noticed in fig. 3.13 by changing the R_G value the $V_{DS}(t)$ fall time does not change significantly. Moreover, the gate voltage waveforms does not show a "plateau" region. For very high R_G value (220 Ω) there seems to be a little "plateau" but it is still negligible in comparison with the MOSFET waveforms. Note that, using R_G equal to 220 Ω, a slight delay in the turn ON occurs due to the slowing down of the gate signal. Looking at the $I_{DS}(t)$ waveforms, it can be noticed that current spikes are present simultaneously to the Drain voltage drop. Fig. 3.14 shows the results obtained by changing the C_{DSADD} value. As can

be noticed the $V_{DS}(t)$ fall time depends on the C_{DSADD} value and still the gate voltage waveforms do not show a "plateau" region. In this case, the dependency of the $V_{DS}(t)$ fall time with the C_{DSADD} value and the lack of "plateau" region seem to confirm that the turn-ON transient occurs in soft-switching condition. On the contrary, looking at the drain current waveforms, overlapping between the $V_{DS}(t)$ and $I_{DS}(t)$ waveforms occurs and this suggests a hard-switching mode of operation. In order to explain this discrepancy, a novel turn-ON hard switching concept was found for GaN power HEMTs. At first, from simple calculation it can be demonstrated that the turn-ON transient occurs in hard-switching and not in soft-switching mode. In fact, if the turn-ON occurred in soft-switching, the HEMT device would discharge the total drain capacitance with its R_{DSON} since the device should turn-ON directly in linear region without crossing the saturation region. From Fig. 3.14 the fall time Δt_{on} can be calculated: $\Delta t_{on} \sim 50$ ns in the case of $C_{DSADD} = 50$ pF. If it would be a soft-switching commutation we could write:

$$\Delta t_{on} = 2.2\tau = 2.2 C_{DPARTOT} R_{DSON} = 50ns \tag{3.13}$$

From the equation 3.13 the R_{DSON} can be calculated since we already have Δt_{on} and $C_{DPARTOT}$ (estimated from the turn OFF analysis). From simple calculation we obtain $R_{DSON} \sim 213\ \Omega$. This result differs a lot with the expected R_{DSON} which is in the range of 10 Ω (not shown). Due to this discrepancy, we can conclude that the switching cannot occur in soft-switching with the device already in linear region. In order to understand the type of hard-switching occurring for the GaN HEMT device, it is worth rewritten the equation 3.10 as follows:

$$V_G - V_{GSp} = \frac{dV_{DS}}{dt} R_G C_{GD} \qquad \rightarrow 0 \quad \text{for GaN HEMT} \tag{3.14}$$

Equation 3.14 $\rightarrow 0$ since C_{GD} is very low for GaN power transistors respect to MOSFET transistors. For example, comparing the two previously simulated devices, the IRF820 has a $C_{RSS} = 37$ pF instead the GS66502B has a $C_{RSS} = 0.5$ pF (data from datasheet). This result confirms that the "plateau" region is minimized for HEMT power transistors. It is worth noticing that such a small value of C_{RSS} leads to a bigger impact of the external parasitics (i.e. the parasitics introduced by the board and by other external components) on the switching transient. Moreover, looking at the fig. 3.14, it can be noticed that, at the beginning of the turn-ON transient, V_{DS} is high (100V) and V_{GS} is higher than the

threshold voltage ($V_{TH} \sim 1.5$ V). In this condition the HEMT transistor has to be in saturation region and it discharges the total drain parasitic capacitance at almost constant current with the maximum current it can provide in saturation depending on the overdrive (V_G-V_{TH}, where V_G is the external applied ON gate voltage and V_{TH} is the threshold voltage of the HEMT transistor). In this type of turn-ON transient the "plateau" region is minimized and it plays a less significant role in the switching speed. This transient behavior can be called saturation current limited switching mode in the sense that when the device turns ON it goes in saturation and it sinks the maximum saturation current it can provide depending on the overdrive and it discharges the total capacitance of the Drain node at almost constant current.

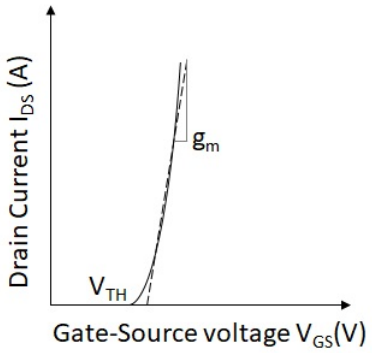

Figure 3.15: Linear approximation of the transfer characteristic

When the device is in saturation the transfer characteristic follows a quadratic law. However for small variation of the $V_{GS}(t)$ the transfer characteristic can be approximated by a straight line (see fig. 3.15) and the following approximated equation can be written:

$$I_{DSPEAK} \sim g_m(V_G - V_{TH}) \tag{3.15}$$

where I_{DSPEAK} is the current peak reached by the HEMT device during the turn-ON transient and g_m is the transconductance of the transistor. With the hypothesis that the HEMT transistor discharges the total Drain capacitance at constant current with its saturation current we obtain:

$$\frac{dV_{DS}}{dt} \sim \frac{I_{DSPEAK}}{C_{DPARTOT}} \tag{3.16}$$

This is an important result since from the equations 3.15 and 3.16 it can be noticed that, for a GaN HEMT transistor, the switching speed is affected by:

- $C_{DPARTOT}$: the more are the parasitics the lower is the switching speed.
- g_m: the more is the g_m the faster is the switching speed.
- V_G-V_{TH} (the overdrive): the more is the overdrive the faster is the switching transient and the more is the current peak reached by the device.

In order to validate this result a measurement with different overdrive was carried out in the system proposed in section 2.2.1. The V_G voltage is changed from 3.5 V to 5.5 V with step 0.2 V. For each step, the $I_{DS}(t)$ and the $V_{DS}(t)$ waveforms during the turn-ON and turn-OFF transients are acquired. Fig. 3.16 reports the obtained results. As can be noticed, the turn-OFF commutation occurs in soft-switching mode since first the $I_{DS}(t)$ zeroes, then the $V_{DS}(t)$ increases and the instantaneous power is negligible. On the contrary, the turn-ON commutation occurs in hard-switching saturation current limited mode. As can be noted, the peak of the $I_{DS}(t)$ (I_{DSpeak}) increases with the increase of the overdrive and the $V_{DS}(t)$ fall time decreases with the increase of the overdrive. The instantaneous power during the turn-ON event is not negligible and the more is the overdrive the more is the power peak.

Fig. 3.17 reports the dV_{DS}/dt extrapolated from the turn-OFF waveforms as a function of the V_G. As expected, since the I_{LMAX} is almost similar by changing the V_G (see fig. 3.16), the turn-OFF dV_{DS}/dt does not change with the V_G. This confirms that during the turn-OFF commutation the total parasitic Drain capacitance is charged by the inductor current. The $C_{DPARTOT}$ can be calculated using formula 3.12:

$$C_{DPARTOT}(\text{turn-off}) = \frac{I_{LMAX}}{\frac{dV_{DS}}{dt}(\text{turn-off})} \tag{3.17}$$

where dV_{DS}/dt (turn-off) is the dV_{DS}/dt extrapolated from the turn-OFF measurements and I_{LMAX} is the maximum inductor current reached during the ON phase (see fig. 3.16).

Fig. 3.18 reports the main parameters extrapolated for the turn-ON commutation. As can be noticed (fig. 3.18 (a) and (b)(black curve)) the I_{DSPEAK} and the dV_{DS}/dt linearly increase with V_G. This confirms equations 3.15 and 3.16. By using equation 3.16 and 3.17 the I_{DSPEAK} can be calculated as follows:

$$I_{DSPEAK}(\text{calculated}) = C_{DPARTOT}(\text{turn-off})\frac{dV_{DS}}{dt}(\text{turn-on}) \tag{3.18}$$

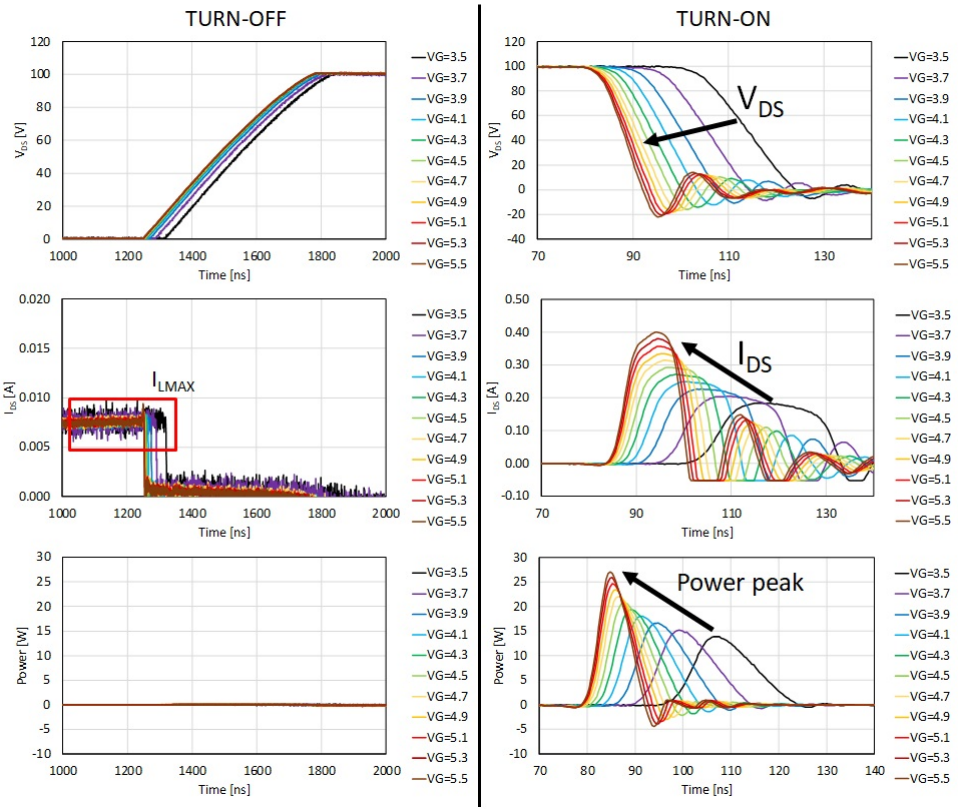

Figure 3.16: Turn ON and OFF transient waveforms of a typical W_G = 1.5mm on-wafer device in the boost converter with different overdrive. V_G from 3.5 V to 5.5 V

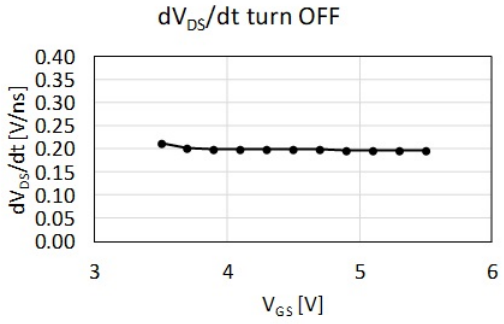

Figure 3.17: Turn OFF transient parameters extrapolation: dV_{DS}/dt vs. V_{GS}

where dV_{DS}/dt (turn-on) is the dV_{DS}/dt extrapolated from the turn-ON measured waveforms. The I_{DSPEAK} curve obtained is plotted in fig. 3.18 (b)(grey curve). As can be noted it is very similar to the measured curve and it confirms the hypothesis of saturation current limited hard switching mode. In fact,

since I_{DSPEAK}(calculated) $\sim$ I_{DSPEAK}(measured), the following equation can be written:

$$I_{DSPEAK}(\text{measured}) \sim C_{DPARTOT}(\text{turn-off})\frac{dV_{DS}}{dt}(\text{turn-on}) \tag{3.19}$$

The plot reported in fig. 3.18 (d) confirms equation 3.19 since the dV_{DS}/dt linearly increases with the increase of the I_{DSPEAK}. Moreover, fig. 3.18 (c) shows that the increase of the overdrive causes a linear increase of the instantaneous power peak that the device has to withstand during the switching transient.

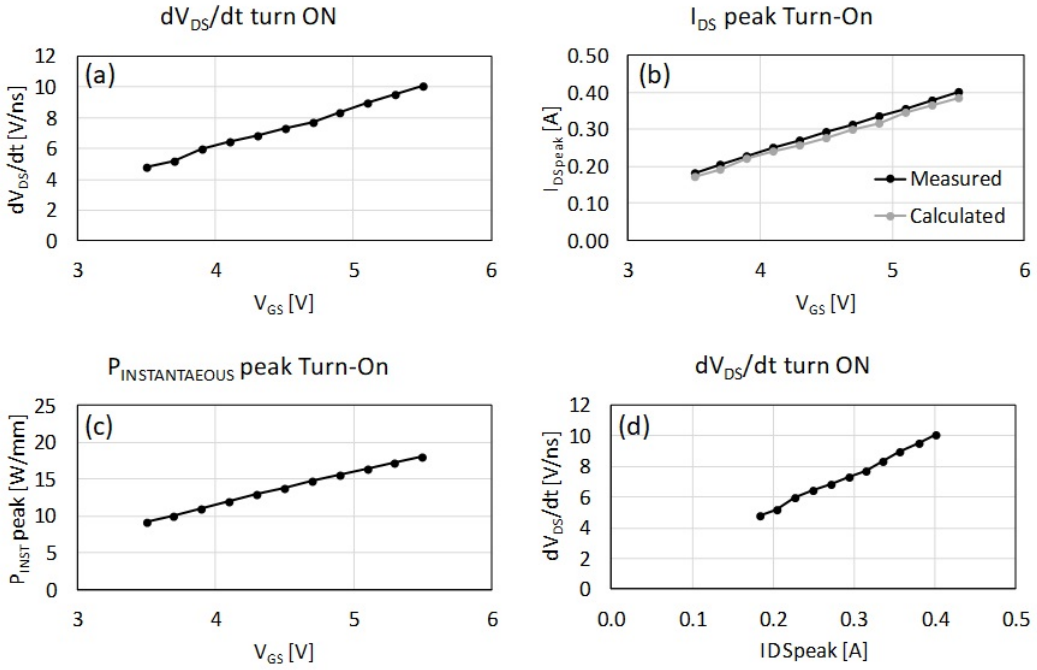

Figure 3.18: Turn ON transient parameters extrapolation: (a) dV_{DS}/dt vs. V_{GS}, (b) I_{DSPEAK} vs. V_{GS}, (c) Normalized instantaneous power peak vs. V_{GS}, (d) dV_{DS}/dt vs. I_{DSPEAK}

Finally, in order to conclude this section, it is worth summarize the behavior of the device working in the boost DC-DC converter developed within this thesis and underline other important concepts:

- the HEMT under test presents a soft-switching turn-OFF commutation
- the turn-ON commutation occurs in hard-switching saturation current limited mode.

- the more is the overdrive the higher are the I_{DSPEAK}, the dV_{DS}/dt and the instantaneous power peak during the turn-ON commutation.
- the overdrive can be used to adjust the I_{DSPEAK} during the turn-ON commutation, i.e. by changing the overdrive, the device can be stressed at different hard-switching current peak.
- if we compare different devices, we expect that, at the same gate ON voltage, the more is the g_m of the device the more is the I_{DSPEAK} and thus the dV_{DS}/dt during turn-ON - i.e. devices with higher g_m sink more current and are faster.

3.4 A simplified method to test GaN HEMT devices in hard switching conditions

Based on the results obtained in section 3.3, in this section an evolution of the novel hard-switching system based on the DC-DC boost converter is presented. In particular, it will be shown that the current saturation limited hard switching mode can be emulated with a resistive load circuit as reported in fig. 3.19. The resistive load has to be chosen in order (i) to maintain the device in linear region after turning ON (depending on the R_{DSON} of the device under test) and (ii) to obtain a V_{DSON} voltage in the order of few hundreds of mV to allows the R_{DSON} measurement. The main advantages of the proposed resistive load circuit diagram are:

- The parasitics of the drain node can be greatly reduced since the inductance and the freewheeling diode, connected to the drain node in the DC-DC boost converter, can be avoided. This enables the possibility to finely control the parasitics of the drain node (and thus to adjust the hard switching energy) by changing the external capacitance added (C_{ADD}).
- The current I_{DS} is automatically limited by the load resistor in case of device failure in short circuit mode. This is an important feature because it avoids the total destruction of the device after failure and it enhances the possibility to carry out failure analysis. On the contrary, in case of device failure in the boost DC-DC converter, the current is not limited and the short circuit current leads to the total destruction of the device and also of the contacting tips. In this case, the big short circuit current leads to

the burning of the device which is no longer available to carry out failure analysis after the failure.

- With the hypothesis that the V_{OFF} voltage and the R_{LOAD} are stable, the R_{DSON} of the device can be calculated only by measuring the V_{DSON}, avoiding the measurement of the I_{DSON} as follows:

$$R_{DSON} = \frac{V_{DSON} R_{LOAD}}{V_{OFF} - V_{DSON}} \tag{3.20}$$

- The resistive load system is much more easy to control in fact the V_{DSOFF} is fixed by an external power supply. On the contrary, the boost DC-DC converter presented in section 2.2.1 is controlled in open loop and the control of the output voltage is more complicated.

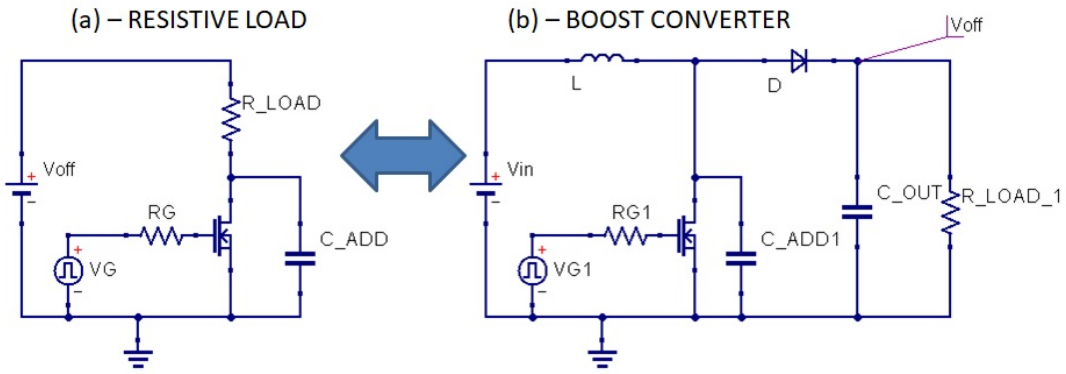

Figure 3.19: Emulation of current saturation limited hard-switching mode occurring in the boost DC-DC converter (b) with a resistive load circuit (a)

3.4.1 Resistive load system vs. DC-DC boost converter

In order to show that the two circuits presented in fig. 3.19 are similar in terms of hard switching transients behavior, in this section a Spice simulation of the GS66502B GaN HEMT device is presented. The device has been simulated in the two circuits shown in fig. 3.19 with voltage (V_{OFF}) of 250 V and gate voltage from 3.5 V to 5.5 V with 0.5 V step. The turn-ON waveforms are reported in fig. 3.20. The full curves refer to the boost DC-DC converter, instead the dotted ones refer to the resistive load circuit. As can be noticed from the plots (a), (b), (c) and (d) the turn-ON transients waveforms of the resistive load circuit

match the DC-DC boost converter. Moreover, looking at the plots of fig. 3.21 the extrapolated I_{DSpeak} and the instantaneous power peak increase linearly with the overdrive. This result is in agreement with the results obtained in section 3.3 and confirms that the two circuits reported in fig. 3.19 have the same behavior in terms of hard-switching transients. In particular, also in the resistive load circuit, during the turn ON transient, the GaN HEMT device discharges the total drain capacitance (parasitics included) at almost constant current with the maximum saturation current it can provide depending on the overdrive.

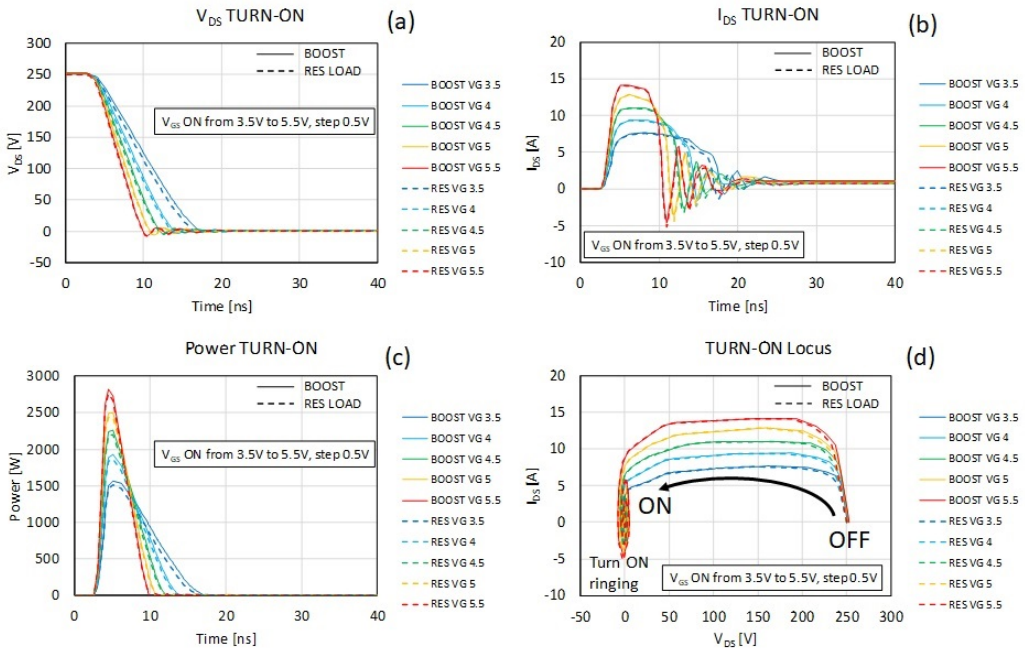

Figure 3.20: Comparison between resistive load circuit and DC-DC boost converter: simulation of GS66502B GaN HEMT device in the two circuits of fig. 3.19. (a) V_{DS} transient turn-ON waveforms, (b) I_{DS} transient turn-ON waveforms, (c) power transients turn-ON waveforms and (d) turn-ON trajectories. Full curves refer to the DC-DC boost converter, dotted curves refer to the resistive load circuit

3.4.2 The simplified novel resistive hard-switching system

After the analysis of the switching commutations, the system proposed in fig. 2.11, 2.12, 2.13 and 2.14 was modified in order to achieve hard-switching behavior with a resistive load circuit as explained in the previous sections. Fig. 3.22 reports the picture of the upgraded system (a) and the circuit diagram (b). The resistive

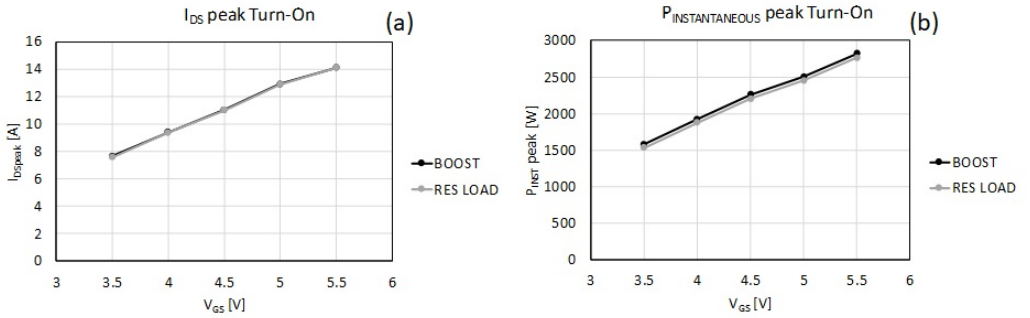

Figure 3.21: Comparison between resistive load circuit and DC-DC boost converter: simulation of GS66502B GaN HEMT device in the two circuits of fig. 3.19. (a) I_{DSpeak} versus V_{GS}, (b) Instantaneous turn-ON power peak versus V_{GS}. Black curves refer to the DC-DC boost converter, grey curves refer to the resistive load circuit

load R_{LOAD} and the added external capacitance C_{ADD} can be changed in order to adjust respectively the ON current and the turn-ON switching energy. R_{LOAD} was chosen in order to let the device working in linear region during the ON phase depending on the R_{DSON} of the device. A typical value of R_{LOAD} used to test the on-wafer devices analyzed within this work is 50kΩ. The gate driver and the clamp circuit for the drain voltage are the same presented in section 2.2.1. The V_{off} can be adjusted in order to investigate the hard-switching behavior at different voltage levels. As far as the measurement system is concerned three probes are used:

- a high voltage probe measures the voltage waveform in full range to acquire the $V_{DS}(t)$ transient.
- the high voltage clamp probe measures the $V_{DS}(t)$ voltage waveform only in the ON phase in order to calculate the $R_{DSON}(t)$
- a dedicated current probe measures the current during the switching transient $I_{DS}(t)$ in order to calculate the switching power.

The entire system is controlled by a Labview program and can carry out both V_{off} sweep measurements (i.e. V_{off} is changed from 100 V to 600 V and the related R_{DSON} is acquired) and constant voltage stress tests (i.e. the device works at a fixed frequency and voltage levels and the time evolution of the R_{DSON} is acquired). More details on the measurement concepts achievable with such a system will be reported and explained in the result sections.

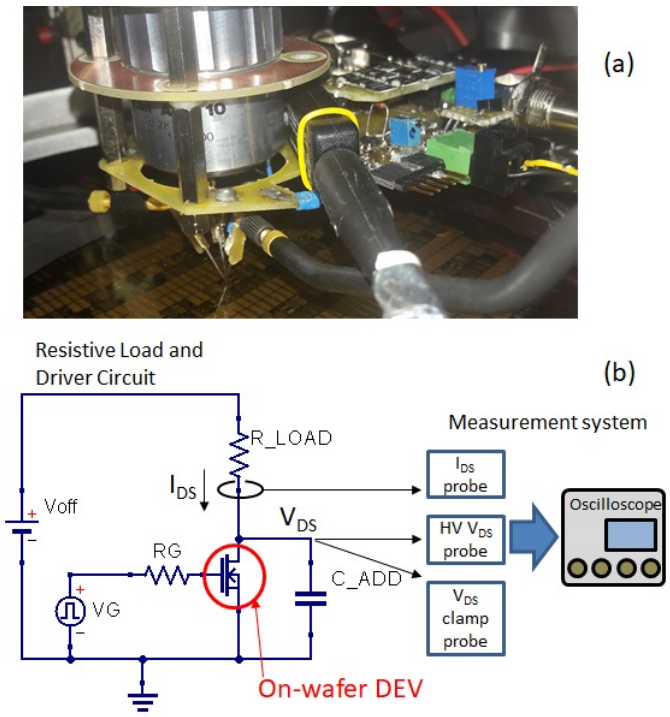

Figure 3.22: The simplified resistive load hard-switching system: (a) picture and (b) schematic of the system

3.4.3 Preliminary results obtained with the resistive load system

In order to test the effectiveness of the novel upgraded system with the resistive load, some preliminary measurements on a typical test device with $W_G = 1.5$ mm have been carried out. Table 3.1 shows the measurement settings used for the test.

Fig. 3.23, 3.24 and 3.25 show the obtained results: as can be noticed, the results are in agreement (i) with the simulations presented in section 3.4 and (ii) with the results obtained in the boost DC-DC converter presented in section 3.3. Note that the simulation have been carried out on devices with very high g_m and very low R_{DSON} thus the current and power levels are different respect to the on-wafer devices. Despite this, the behavior during the transient turn-ON commutation is very similar: the transient speed (i.e. the dV_{DS}/dt speed), the I_{DSpeak} and the instantaneous power power once again increase linearly with the overdrive. Results confirm the feasibility to test on-wafer GaN HEMT devices in hard-switching conditions close to real application operation mode using a

Table 3.1: Settings for the preliminary measurements in the resistive load hard-switching system

Symbol	Quantity	Value
D	Duty cycle	50%
F_{SW}	Switching frequency	100 kHz
R_{LOAD}	Load resistor	50 kΩ
V_{off}	OFF voltage	200 V
R_G	Gate resistor	22 Ω
V_G	Gate voltage	from 3.5 V to 5.5 V, step 0.5 V
C_{ADD}	External capacitance added	22 pF

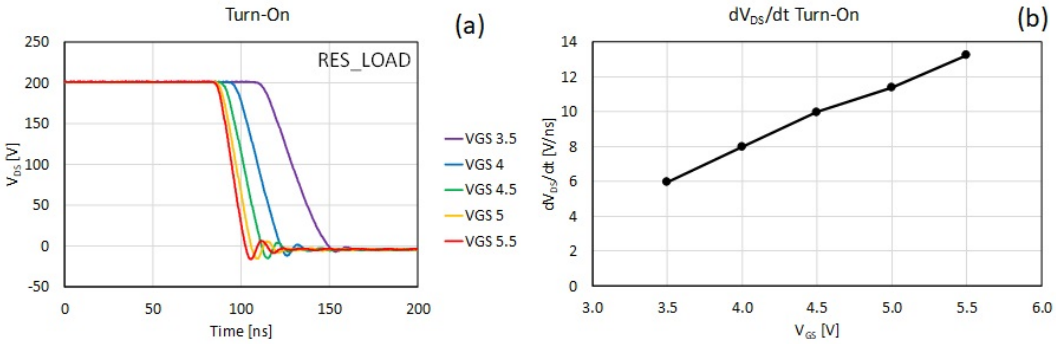

Figure 3.23: Results obtained with the resistive load circuit system on a typical 1.5mm on-wafer device. V_{DS} turn-ON waveforms for different V_G voltage (a) and dV_{DS}/dt versus V_G (b).

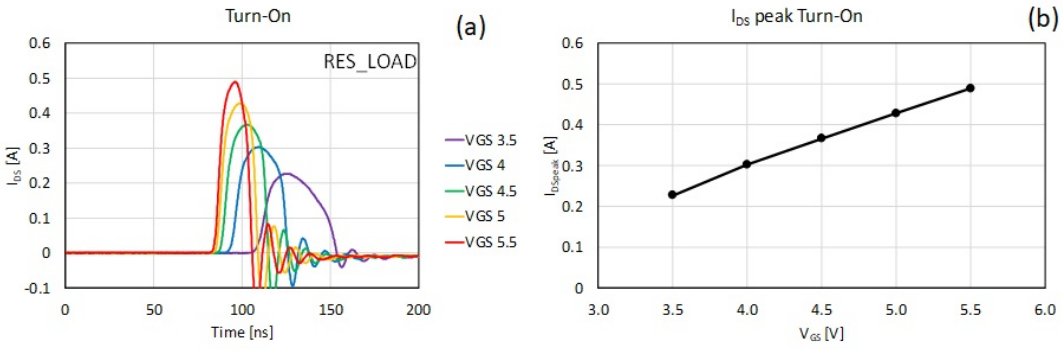

Figure 3.24: Results obtained with the resistive load circuit system on a typical 1.5mm on-wafer device. I_{DS} turn-ON waveforms for different V_G voltage (a) and I_{DSpeak} versus V_G (b).

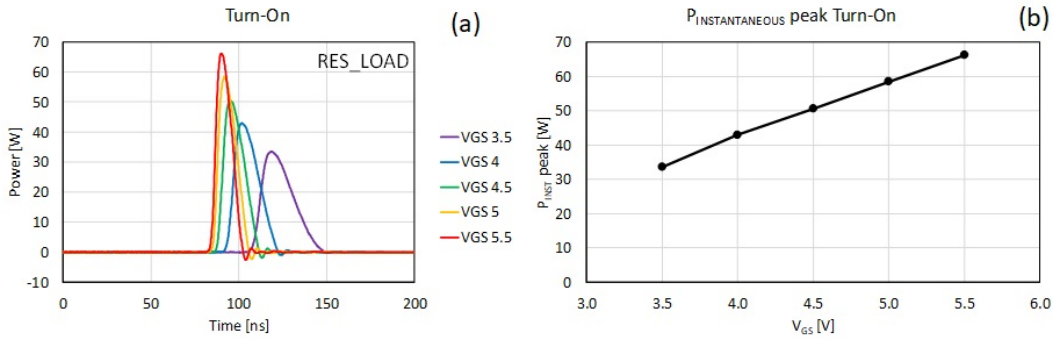

Figure 3.25: Results obtained with the resistive load circuit system on a typical 1.5mm on-wafer device. Instantaneous power turn-ON waveforms for different V_G voltage (a) and instantaneous power peak versus V_G (b).

resistive load circuit with an external capacitor connected in parallel to the DUT. This is an important result since it enables the opportunity to easily test on-wafer devices in real hard-switching conditions and investigate robustness of such devices in this detrimental operation mode, using a resistive load circuit.

3.5 Chapter summary

At the beginning of this chapter we presented the basics of the boost DC-DC converter used in the novel hard-switching test system developed within this thesis. Then we presented a theoretical analysis of the MOSFET behavior in hard-switching conditions showing that the transient speed is dominated by the Miller capacitance and the gate resistance. On the contrary, by testing the GaN HEMT devices on the boost DC-DC converter system, we demonstrated that such devices switch in saturation current limited mode: during the hard-switching transient, the device discharges the total drain parasitic capacitance at almost constant current with the maximum current it can provide in saturation (i.e. with $V_{GS} > V_{TH}$ and high V_{DS}). By using this concept, we developed a simplified resistive load circuit able to test GaN HEMT devices in hard-switching conditions and we demonstrated that such novel circuit is able to stress the DUT in dynamic operation very similarly to the real inductive switching operation.

Chapter 4

Hot-electrons charge trapping and temperature analysis

Many works in literature have investigated charge trapping in GaN HEMTs [6, 23, 7, 24, 12, 14, 15, 16]. One of the main problems of power GaN-HEMTs is the dynamic R_{DSON}, i.e. the recoverable increase of the ON-resistance during operation. This phenomenon is induced by (i) the charge trapping during high voltage off-state bias due to the high electric field [24], (ii) the charge trapping due to hot electrons created during hard-switching transients [7] and, (iii) the increase of the junction temperature (Tj) due to self-heating [8]. Until now, many works have investigated the impact of charge trapping due to the high electric field in soft switching conditions and only few have analyzed the behavior in hard switching operation mode. Moreover, very few works have tried to investigate the behavior of GaN power HEMT devices working in real life conditions. In this chapter, a comparison between the state-of-the art double pulse measurement approach and the novel in-circuit measurement technique proposed within this thesis is reported. It will be shown that hard-switching conditions can lead to additional R_{DSON} increase and thus the worsening of the device performance. In particular, in order to emphasize the potentiality of the novel in-application technique proposed in section 2.2, two wafers with different performance in terms of dynamic R_{DSON} have been analyzed - wafer 1 and wafer 2 respectively named WF1 and WF2 in the following. The analysis was carried out on devices with gate width $W_G = 1.5$ mm. The wafers come from two different production lots representing the evolution of the quality of the epitaxial layers and process maturity. WF2 is an updated version of WF1 with slight adjustment of both the AlGaN barrier and MOCVD deposition parameters. The devices are normally

off, with a threshold voltage of $\sim$ 1.2 V, and an ON-resistance of $\sim$ 15 Ωmm. It is worth noticing that the devices under test are on-wafer and are connected via external micro tips, which have current and contact resistance limitations. Moreover, by testing such prototypal devices, it is possible to assess the physical causes responsible for the dynamic R_{DSON}. The study of prototypal on wafer devices is fundamental to improve the design and production processes of GaN HEMTs, and to provide a rapid feedback at foundry level. The results of this analysis can be used to estimate the performance of the final on-package scaled device, which have R_{DSON} in the tens of mΩ range.

4.1 Hard-switching and Soft-switching impact on R_{DSON}

This section reports the measurement concept developed in order to compare the double pulse and the in-circuit measurement technique and the obtained results. In order to study the different charge trapping contributions to the dynamic R_{DSON}, at first double pulse measurements on the two wafers have been carried out. In the double pulse characterization, the device is kept in OFF-STATE with $V_{GS} = 0$ V and fixed V_{DS} voltage (V_{DS_OFF}). Starting from this bias condition, two properly synchronized voltage pulses are applied on the Gate and Drain terminals for a very short time (40 μs) in order to acquire the device output pulsed characteristic (I_{DS}-V_{DS} at fixed pulsed $V_{GS} = 6$ V). By varying the V_{DS_OFF} voltage, we investigate the impact of the high electric field induced in OFF-STATE on the R_{DSON} of the transistor. Fig. 4.1 shows the output double pulse characteristics of two typical devices of the two wafers.

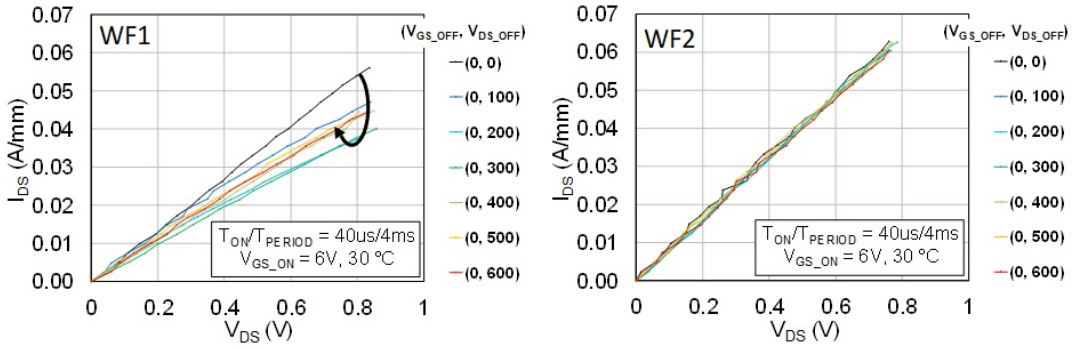

Figure 4.1: Typical pulsed output characteristics of devices of the two different wafers

As can be noticed WF1 suffers from dynamic R_{DSON} as a function of the OFF voltage applied instead the R_{DSON} of WF2 is not affected by the high voltage applied. The typical R_{DSON} curves as a function of the V_{DS_OFF} voltage were extracted from the curves of fig. 4.1 for the two wafers. Results are shown in fig. 4.2 (empty markers curves).

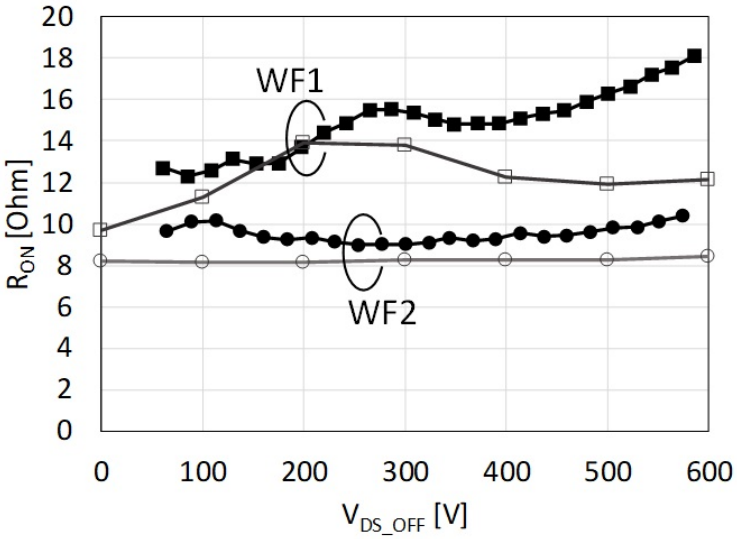

Figure 4.2: R_{DSON} measurement during operation in the boost converter (filled marker curves) and R_{DSON} measurement carried out with double pulse system (empty marker curves) for WF1 and WF2.

As can be noticed, WF1 has a strong dependence of the R_{DSON} on V_{DS_OFF}, with a maximum increase in the 200 V - 300 V range. On the contrary, WF2 shows good performance and the R_{DSON} is not affected by V_{DS_OFF} as desired. It is worth noticing that with this kind of measurement the device is tested in a "soft" regime condition. In fact, primarily the V_{DS} imposed by external electronics is lowered and then the transistor is turned ON with the gate signal. Moreover, the device does not suffer from self-heating during the R_{DSON} double pulse measurement due to the very low duty cycle (1%) and the very short on time (T_{ON} = 40 μs).

In order to investigate the GaN HEMT dynamic R_{DSON} variation during real operation in the wafer-level boost power converter (presented in section 2.1 and reported again as a reference in fig. 4.3) as a function of the output voltage (V_{OUT}), measurements with increasing output voltage from 60 V to 600 V were carried out. The main parameters (duty cycle D, switching frequency F_{SW}, and load resistor R_{LOAD}) of the converter were kept fixed during the measurement.

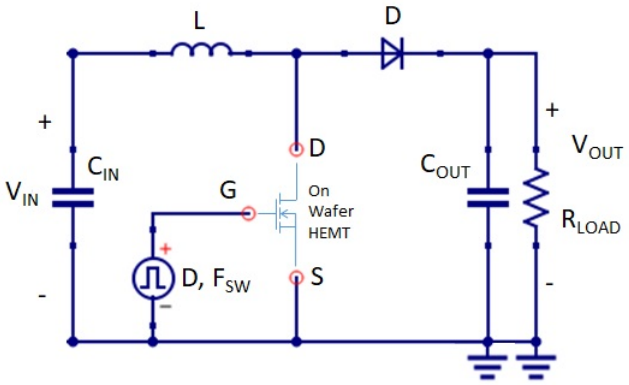

Figure 4.3: Boost converter used for the in-circuit tests

It is worth noticing that with this approach also the impact of the junction temperature T_j on the R_{DSON} is taken into account since the load is fixed and the output current and power increase with rising V_{OUT}. Table 3.1 summarizes the boost converter settings used for the analysis of the GaN HEMTs R_{DSON}. In order to obtain the output voltage in the range from ∼60 V to ∼600 V, the input voltage (V_{IN}) was adjusted between ∼12 V and ∼120 V. For each V_{OUT}, the R_{DSON} of the GaN HEMT is measured. Note that the output voltage is equal to the drain to source voltage of the GaN HEMT when it is in OFF-STATE ($V_{OUT} = V_{DS\_OFF}$) thus with this kind of measurement, the overall impact of the high voltage, temperature and, hot-electrons on the R_{DSON} was investigated. A typical result obtained on WF1 with this type of measurement was already reported in fig. 2.20. As can be noticed, by calculating the R_{DSON} for each V_{DS_OFF} after 5μs from the turn ON, the plot of the dynamic R_{DSON} as a function of the voltage can be drawn. This measurement was carried out both for WF1 and WF2 and the related R_{DSON} waveforms as a function of the V_{DS_OFF} are reported in fig. 4.2 (see filled marker curves). Results show that for WF1 the R_{DSON} increases with V_{OUT} whereas for WF2 the R_{DSON} does not increase with V_{OUT}. This different behavior of the two wafers can be ascribed to the combined effect of charge trapping and self-heating of the transistors on the R_{DSON} for the two different wafers. In particular, WF1 has a stronger dependence of the R_{DSON} on the high voltage trapping and temperature. On the contrary, WF2 has a better behavior and shows a much more stable R_{DSON}. During the measurement, the linear current density is expressly kept at low level (< 35mA/mm - not shown) to limit as much as possible the self heating of the device and study the charge trapping effects in more detail. Fig. 4.2 reports the waveforms obtained

with both the double pulse and the boost converter measurements. The double pulse system mimics soft switching conditions by using a resistive load. In order to prevent high power transients during turn on and turn off, the drain and gate pulses provided to the device are properly synchronized: first, the external drain voltage pulser lowers the drain voltage and then the gate pulser turns on the device by providing a positive gate signal. In this way, the switching losses are minimized. Moreover, the measurement is carried out with a very low duty cycle (1%) therefore the device does not suffer from self heating. With this approach, the double pulse measurement is able to investigate only the impact of the high OFF-STATE electric field on the R_{DSON}. It is worth noticing that the OFF-STATE time ($\sim$ 4 ms) of the double pulse measurement is much longer compared to the boost converter application: in fact, the GaN power transistors are expected to work in power converter applications in the hundreds of kHz frequency range with obviously shorter OFF STATE time [11]. On the contrary, the boost converter system of this study is able to mimic hard-switching operating conditions and to take into account the effects of switching losses, self-heating and high electric field on the R_{DSON}. As explained in section 3.3, due to the inductive load, after the gate turn ON transition, first the current raises and then the voltage lowers. This switching operation mode causes a high transient instantaneous power. The waveforms of WF1 (see square marker curves in fig. 4.2) show that there is a hump centered at about 270 V both in the curve of the double pulse and the boost on wafer measurement. This can be ascribed to the impact of charge trapping due to the high electric field in OFF-STATE. It is known in literature that the R_{DSON} increases for increasing drain voltage, due to the ionization of buffer acceptors [12]. On the other hand, at very high voltage ($>$ 250 V) the electric field within the vertical epitaxial structure of the device favors charge de-trapping, and the corresponding decrease in R_{DSON} [12]. Moreover, the R_{DSON} curve obtained with the hard-switching system increases more at high voltage respect to the double pulse measurement for WF1. This can be ascribed to the contribution of the hard switching charge trapping and temperature. The curves of WF2 (see circle indicators curves in fig. 4.2) show that this second wafer has a more stable behavior. In particular, the double pulse analysis confirms that this wafer only slightly suffer from charge trapping up to 600V. Moreover, the curve obtained with the boost converter shows that WF2 has better performance also in term of hard switching and temperature robustness. In order to better understand the R_{DSON} thermal dependency of the two wafers analyzed, two DC thermal maps have been carried out. Fig. 4.4

shows that WF1 has a slightly stronger dependency of the R_{DSON} respect to temperature and this is in agreement with the previous results. Moreover, the two thermal map curves do not differ so much to explain the results of fig. 4.2. This suggests that, in addition to self-heating, another mechanism is responsible for the R_{DSON} variation found in the real application measurements. We suppose that hot-electrons play a remarkable role and this will be demonstrated in the next section.

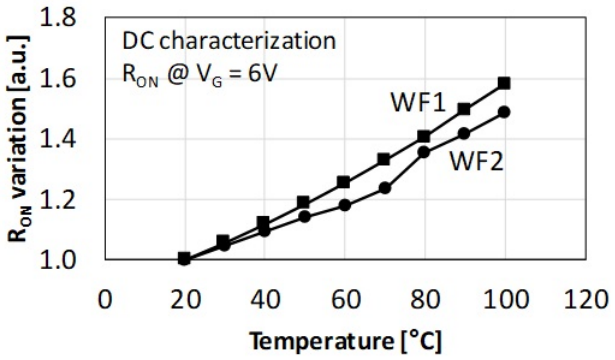

Figure 4.4: R_{DSON} DC typical thermal maps for the two wafers analyzed. WF2 shows better results in terms of R_{DSON} variation

4.2 Temperature and hot electrons trapping analysis during hard-switching operation

In this section an analysis of hot-electrons formation and temperature increase during the hard-switching transients is reported. First of all, it should be noted that the typical hard-switching transients timing during operation in the boost DC-DC converter is in the order of few tens of ns as previously reported in fig. 2.18. A typical dV_{DS}/dt value of an on-wafer 1.5mm device working in the DC-DC boost converter is about 5V/ns and is mainly limited by the drain node parasitics. In order to better understand the behavior of the device during the hard-switching turn ON event, a further analysis have been carried out and is here reported. In particular, it is important (i) to estimate how much is the temperature variation of a device subjected to very high instantaneous power and (ii) to study whether the transient power causes hot electrons trapping or not. These are two important aspects to be investigated before moving toward reliability aspects which will be presented in chapter 5. In fact, in this section it

is found that hot-electrons charge trapping can worsen device performance and reduce the switching current. Moreover, it is found that the switching transient speed is fundamental to avoid self-heating.

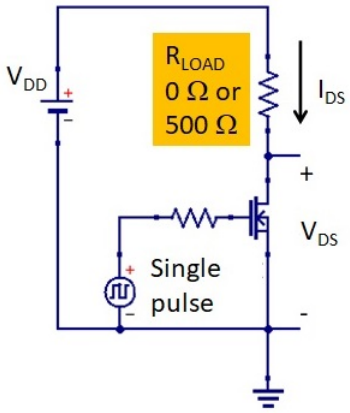

Figure 4.5: System used to carry out (i) high power and (ii) short circuit measurements

In order to test devices at (i) high voltage and (ii) high power a novel measurement technique was developed. The system described in section 3.4.2 was modified as shown in fig. 4.5. The external capacitance was removed and the resistive load was adjusted in order to obtain a high ON current. By pulsing the gate terminal, (i) high power and (ii) short circuits measurements have been carried out. Depending on the resistive load value, the device is turned ON (i) with high current and high V_{DS} in case of R_{LOAD} = 500 Ω and (ii) with high current and fixed $V_{DS} = V_{DD}$ in case of resistive load shorted. Such a technique is not used to emulate real hard-switching conditions but to study the device behavior in case of high instantaneous power applied. The current I_{DS} and the voltage V_{DS} during the pulse are acquired.

In order to understand the thermal behavior during high power transients, measurements with R_{LOAD} = 500 Ω and V_{DD} = 300 V have been carried out at different chuck temperatures from 30°C to 130°C, step 20°C. Results reported in fig. 4.6 show that during the gate pulse the device turns ON in saturation region with high current density and high voltage (V_{DS} >70 V). The current during the pulse is not constant due both to self-heating and hot electrons charge trapping which cause variation in the device current. Note that the temperature reported in fig. 4.6 is not the channel temperature of the device since the power loss during the measurement is large and self-heating is present. The reported temperature is the set chuck temperature. Looking at the waveforms at different

temperatures an estimation of the current drop due to the temperature increase can be extrapolated. The current peak drops down by 0.05 A/mm over 100°C (see black arrow in fig. 4.6).This result is in agreement with previous works found in literature [25]. Moreover, this result confirms that, in order to avoid huge device self heating, the high power hard-switching transients have to be reduced as much as possible. This can be achieved reducing the parasitics connected to the drain node of the device which are the main limiting factor for the switching speed as reported in section 3.3. In order to understand the hot electrons charge

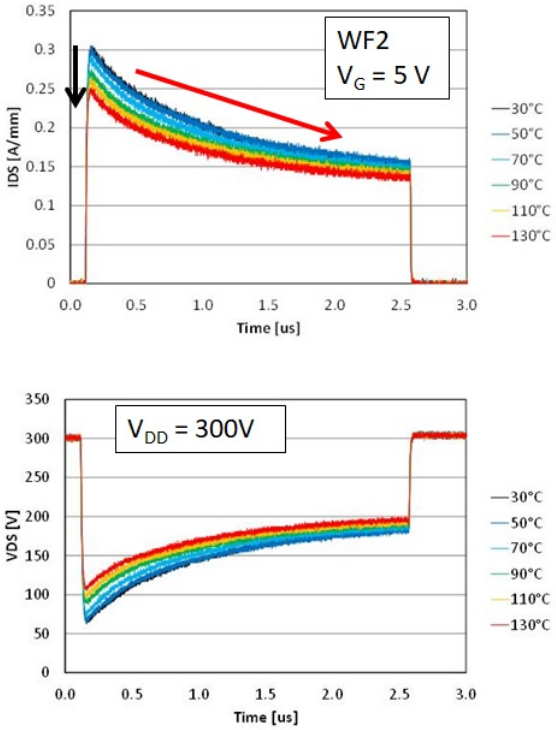

Figure 4.6: High power transients measurements at different temperatures, V_{DD} = 300 V

trapping phenomenon occurring during the high power transients, short circuit measurements with $R_{LOAD} = 0\ \Omega$ at room temperature have been carried out at different V_{DD} from 20 V to 250 V for both WF1 and WF2. The main benefit of this approach consists in having a constant $V_{DS} = V_{DD}$ and thus it is possible to control the instantaneous current and power during the pulse. In order to obtain a current peak density of $\sim$ 0.35A/mm, the gate voltages were adjusted to 6.1V and 4.5V respectively for the devices of WF1 and WF2. Obtained results are reported in figs. 4.7 and 4.8.

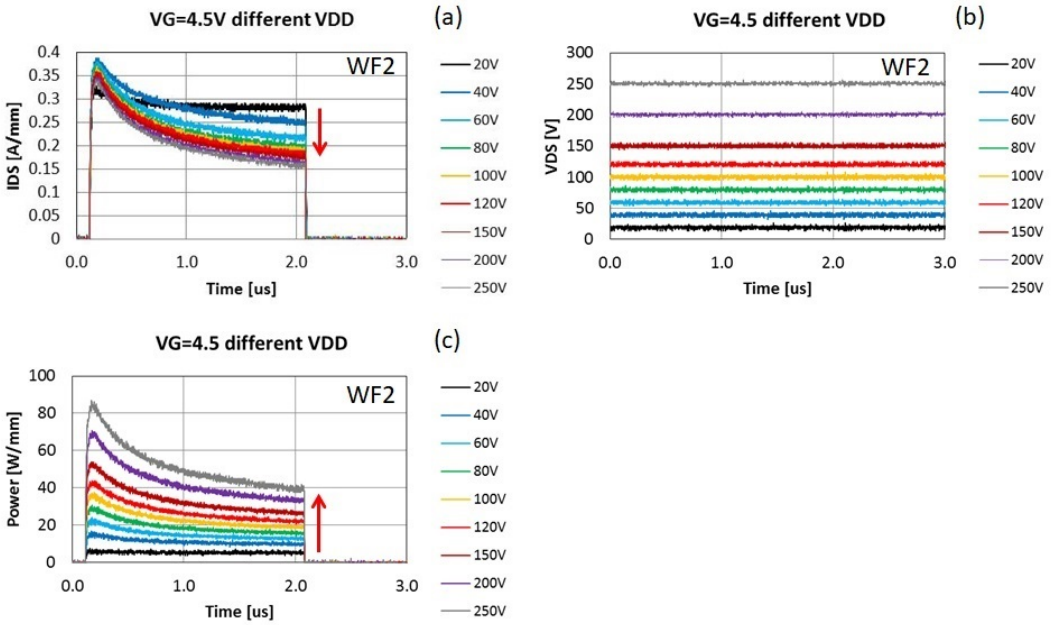

Figure 4.7: I_{DS}(a), V_{DS}(b) and Power (c) of a typical device of WF2 acquired in the short circuit high power measurement. The device is clearly in saturation.

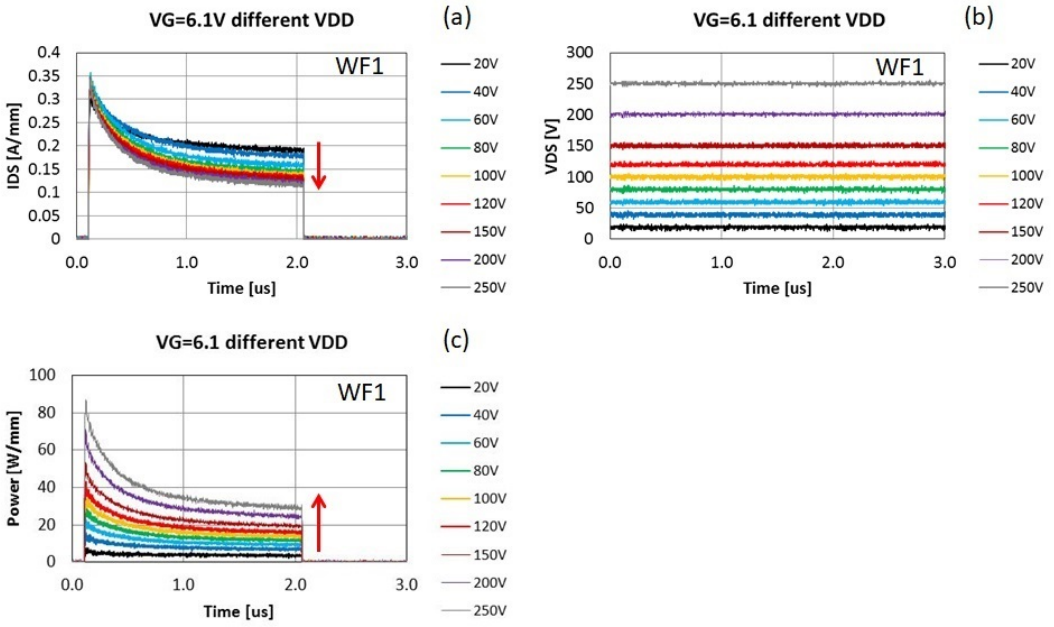

Figure 4.8: I_{DS}(a), V_{DS}(b) and Power (c) of a typical device of WF1 acquired in the short circuit high power measurement. The device is clearly in saturation.

Results show that the V_{DS} is constant to V_{DD} during the pulse ((b) plots). The current reaches a peak of about 0.35A/mm for both wafers and then it shows a transient during the pulse for both WF1 and WF2 (see (a) plots). Being the V_{DS} constant, the power waveforms are similar to the current ones but scaled with the V_{DS} (see (c) plots). The current plots show that the more is the power the more is the current decrease during the pulses (se red arrows in figs. 4.7 and 4.8). This can be ascribed to both self-heating and hot electrons charge trapping effects. Moreover, the current waveforms of WF1 are more collapsed - i.e. starting from similar current, voltage and power levels the $I_{DS}(t)$ transient is larger.

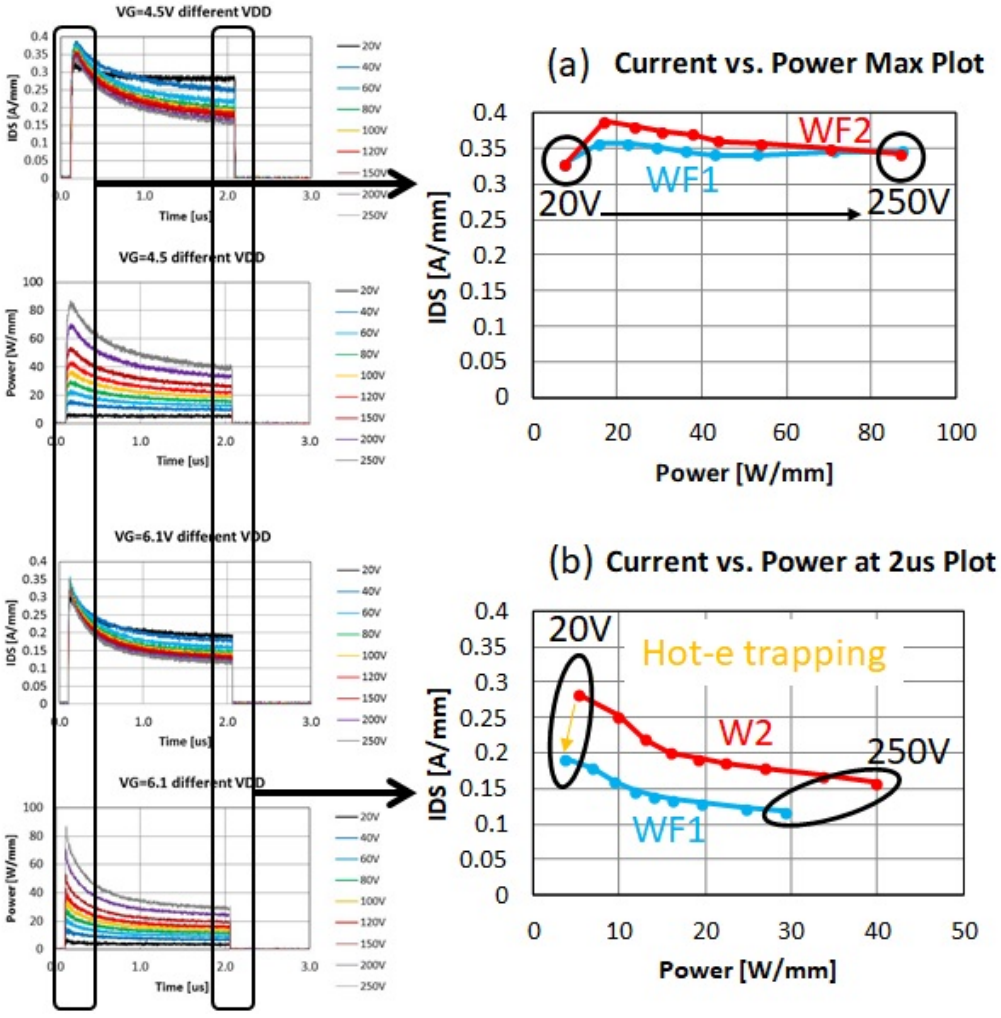

Figure 4.9: I_{DS} versus power at the beginning of the pulse (a) and at the end of the pulse (b) acquired during the short circuit measurement for the two different wafers. WF1 clearly shows more current collapse and suffers more from hot electrons charge trapping

In order to emphasize this result current vs. power plots at the beginning (a) and at the end (b) of the pulse have been reported in fig. 4.9. As can be noted, referring to the same voltage, the current and power levels at the beginning of the pulses are similar for the two wafers (see (a) plot). On the contrary, the current and power levels are more collapsed for WF1 at the end of the pulses (see (b) plot). Moreover, in the waveforms of plot (b) the lower is the voltage the lower is also the instantaneous power and thus the lower should be the self-heating of the device. Assuming that only the device self-heating has an impact on the current collapse, the two power-current curves of fig. 4.9(b) should be closer at low voltage. In fact, at low voltage and power also the self-heating should be low and the current collapse should disappear (see yellow arrow in fig. 4.9(b)). On the contrary, it is clearly visible that the curves of the two wafers show a constant shift and thus this demonstrates that another current collapse mechanism is present in addition to self-heating. Due to the simultaneous presence of high voltage (and thus high electric field) and current within the device structure during the measurement, the additional current collapse can be ascribed to hot electrons charge trapping occurring during the high power transients. Results demonstrate that this phenomenon is more pronounced in WF1.

4.3 Chapter summary

In this chapter we presented an extensive analysis of charge trapping in soft- and hard-switching conditions. We showed results on two different representative wafers. The former showed the dynamic R_{DSON} issue both in soft- and hard-switching conditions. We demonstrated that hard-switching operation can cause an additional increase of the R_{DSON} due to both temperature increase and hot-electrons charge trapping. The second wafer was an improved version with better performance both in terms of charge trapping immunity and self heating. In fact, WF2 showed a stable R_{DSON} as a function of the V_{DSOFF} stress. At the end of the chapter, an analysis of the hard-switching transients in terms of temperature increase and hot-electrons formation is presented. Also in this case the first wafer showed worst performance than the improved one. In fact, we found that WF1 shows an higher current collapse and suffers more from hot-electrons charge trapping during hard-switching operation. Finally, results demonstrate that hard-switching operation can cause (i) huge self-heating in case the switching transient time is longer than few tens of ns and (ii) hot electrons trapping formation. This

second phenomenon can cause both R_{DSON} increase and I_{DS} current collapse and thus limit the device performance.

Chapter 5

GaN HEMTs reliability in dynamic operation

Until now, GaN power HEMTs reliability in dynamic operation was not widely analyzed in literature. Only recently some works regarding GaN HEMTs working under hard-switching conditions have been presented [26]. In this chapter, an analysis of GaN transistor devices working in dynamic operation will be shown pointing out the importance of such topic. In fact, we found that hard-switching operation can lead to the formation of hot-electrons, which can affect reliability leading to the premature breaking of the device. At first, in order to assess devices robustness in pulsed mode at very short time (tens of ns timing range), the safe operation area (SOA) of such devices with 100ns width voltage pulses was carried out. Then, in order to assess the reliability statistics and to understand the physical phenomena occurring during the tests, some hard-switching tests and an electroluminescence analysis have been carried out.

5.1 TLP Safe Operation Area (SOA)

In order to assess the operation limits of GaN HEMTs at very short time, transmission line pulse (TLP) measurements were carried out on WF1 and WF2. The custom TLP system presented in section 2.1.4 was used. The measurement was carried out by keeping the gate voltage constant and pulsing the drain terminal increasing the pulsed V_{DS} voltage up to the device failure as depicted in fig. 5.1. Many devices with different gate voltage have been tested. The pulse width was fixed to 100ns. In the following, the V_{GS} sets for the two different wafers are reported (each V_{GS} corresponds to a broken device):

- WF1: V_{GS} = {2.5V, 3V, 3.5V, 4V, 5V, 6V, 6.6V, 7V}
- WF2: V_{GS} = {2.5V, 2.85V, 3V, 3.5V, 4V, 4.5V, 5V, 6V}

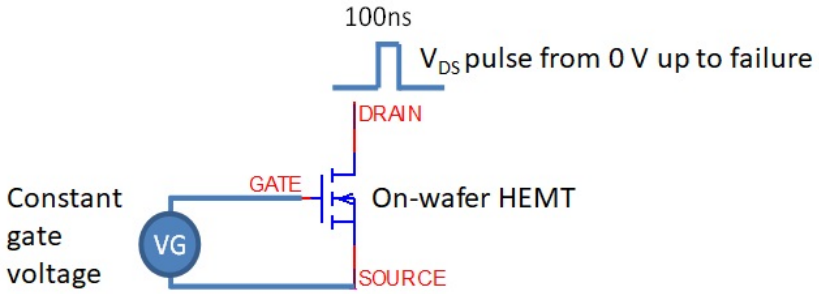

Figure 5.1: The TLP measurement concept: V_{GS} is fixed and the Drain terminal is pulsed up to device failure

By changing the V_{GS} for different devices, and by pulsing the V_{DS} voltage up to failure for each device, the devices' safe operation area was obtained. Fig. 5.2 shows the results obtained for the two wafers. As can be noticed, by pulsing the V_{DS} voltage we obtain the output characteristics of the transistor at fixed V_{GS}. Repeating the measurement for many devices with different fixed V_{GS}, we were able to obtain the SOAs of the two wafers.

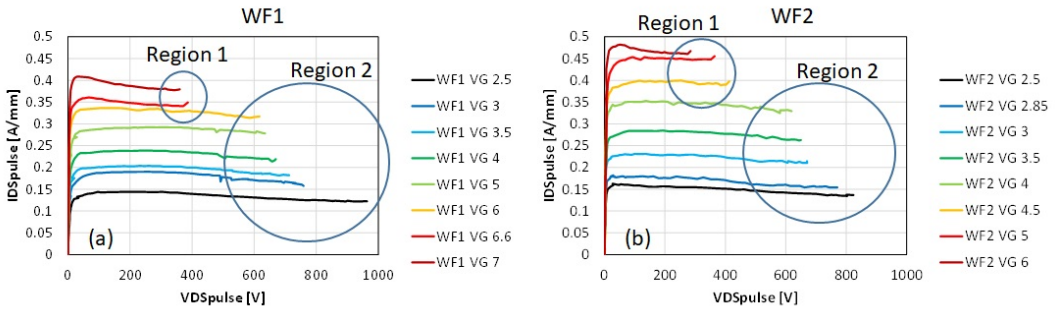

Figure 5.2: Safe operation area for WF1 and WF2. Devices are tested with pulses of 100ns

Fig. 5.3 shows the SOAs of the two wafers overlapped. In the plot, two main failure regions are clearly visible. In the first failure region the device is subjected to middle voltage level (in the range of 300V - 400V) and high current (>0.35A/mm). In the second region, the device is subjected to lower current levels (<0.35A/mm) and high voltage level (>600V). In the grey box the desired

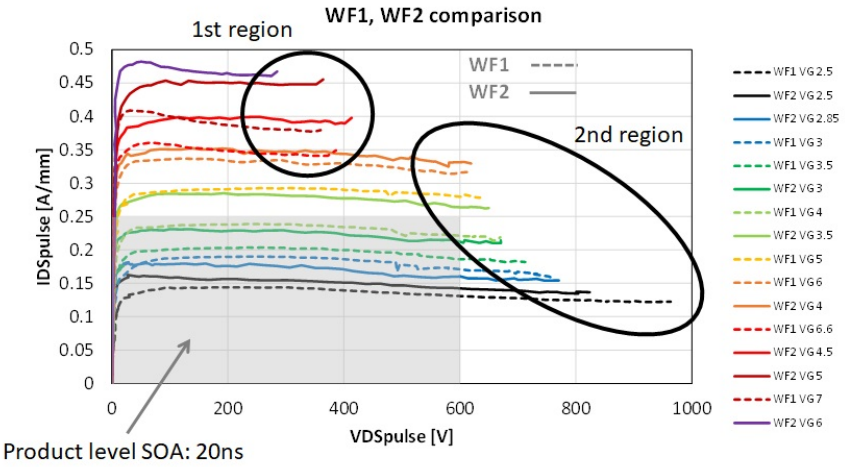

Figure 5.3: Safe operation area for WF1 and WF2 overlapped. Devices are tested with pulses of 100ns

production level SOA (at 20ns) is reported. It is clearly visible that the devices fulfill the product level SOA robustness also at 100ns. Looking at the broken devices with a microscope we were able to identify two different failure modes depending on the failure region. In fact, all the five broken devices of the first region break in the central part of the structure (see fig. 5.4). Instead, all the eleven broken devices of the second region break close to the final part of the drain finger where edges are present between the drain and source terminals (see fig. 5.5).

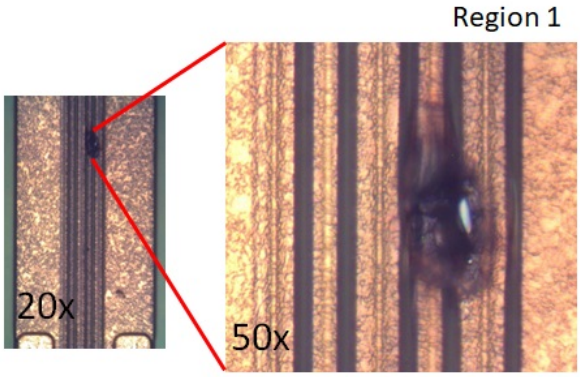

Figure 5.4: Failure mode of region 1: device breaks in the central part of the structure

Looking at the failure images and the pulsed characteristics, we supposed that in the first region a power related failure mode occurs. In this region, the device

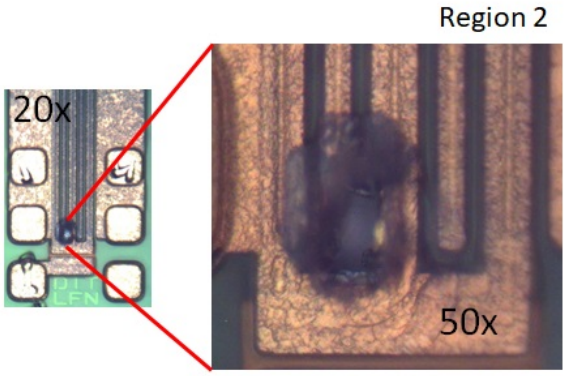

Figure 5.5: Failure mode of region 2: device breaks at the and of the Drain finger

is subjected to high power and the gate-drain reverse current can lead to the gate drain diode failure due to the local focusing of the current. In the second region, the failure seems to be related to the impact of the high electric field which is present between the drain and the other terminals. The high electric field can damage the dielectric between the drain and gate or between the gate and source terminals leading to the catastrophic failure of the device. Summing up, results show that there are two main regions in the SOA and two main failure modes. The first region is characterized by high current density and voltage between 300V and 400V. In the second region, the current is lower than 0.35A/mm and the failure voltage extends to very high values (>600V).

5.2 Hard-switching sweep breakdown measurements

In this section the devices limits in terms of hard-switching robustness are assessed. In order to study the robustness of devices exposed to hard-switching conditions, the system proposed in section 3.4.2 was used. An automated Labview program able to carry out the sequence of operations reported in fig. 5.6 was developed. Fig. 5.6 also shows the circuit diagram of the system used to carry out the breakdown measurements. As can be noted, the measurement consists in applying the V_{DD} voltage, then, in order to induce hard-switching stress, the device is turned ON at a fixed frequency for 3 seconds and the switching waveforms are acquired and finally the device is turned OFF. This procedure is repeated increasing the V_{DD} with 20 V step until the device failure. Note that

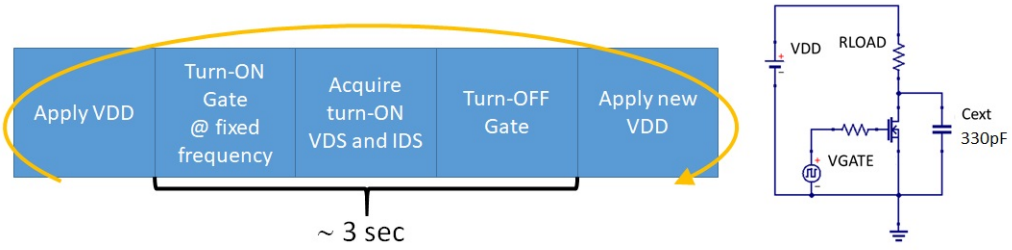

Figure 5.6: Hard-switching breakdown sweep measurement concept

an external capacitor big enough to provide destructive energy was used (C_{ext} = 330pF). In order to change the switching current level, the hard-switching breakdown measurement is carried out changing the ON gate voltage for the different devices. In particular, as already shown in section 3.4.3 the more is the overdrive the more is the current peak reached during the hard-switching transient. Table 5.1 summarizes the settings used in the measurement.

Table 5.1: Settings for Hard-switching sweep breakdown measurement

Symbol	Quantity	Value
D	Duty cycle	20%
F_{SW}	Switching frequency	10 kHz
R_{LOAD}	Load resistor	24 kΩ
V_{DD}	OFF voltage	from 100 V up to dev failure (max 600 V)
R_G	Gate resistor	10 Ω
V_G	Gate voltage	from 3.2 V to 5.5 V
C_{ext}	External capacitance added	330 pF (enough to get device failure)

Figs. 5.7, 5.8, 5.9, 5.10 report the results obtained with the hard-switching breakdown tests carried out at different gate voltages. Fig. 5.7 reports the turn-ON V_{DS} waveforms and the V_{DD} voltages for the tested devices just before the failure. As can be noted, the more is the overdrive the faster is the transient and the lower is the failure voltage.

Fig. 5.8 reports the turn-ON I_{DS} waveforms for the different devices just before the failure. Results show that the higher is the overdrive the higher is the current peak (I_{DSpeak}) during the turn-ON transient. Moreover, as explained in section 4.2, the current pulses are not rectangular as expected due both to the channel temperature increase (self-heating) and hot-electrons trapping.

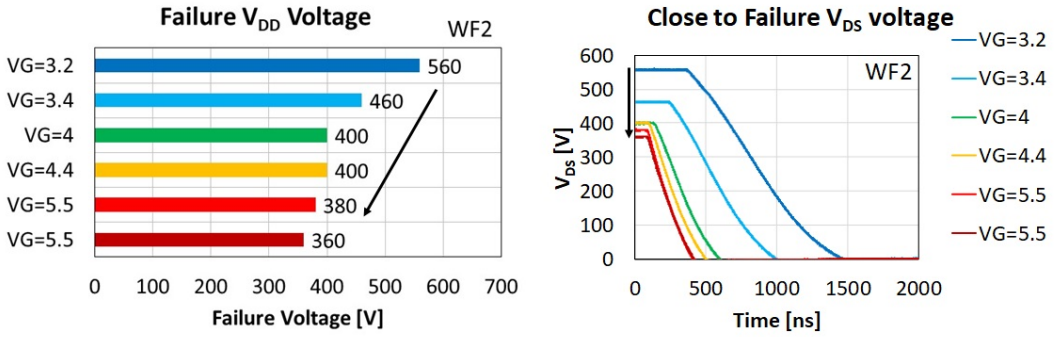

Figure 5.7: Transient turn-ON drain voltage (right) and V_{DD} failure voltage (left) before the failure for different devices increasing the gate voltage. The higher is the V_{GS} the faster is the V_{DS} transient and the lower is the failure V_{DD} voltage

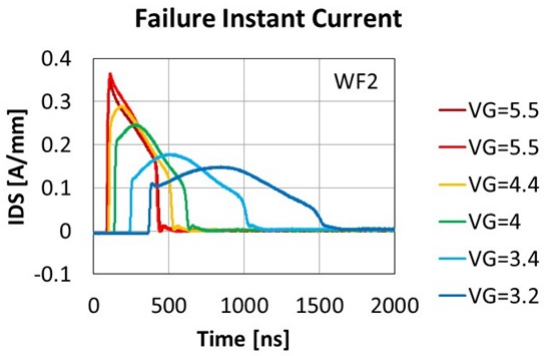

Figure 5.8: Transient turn-ON drain current before the failure for different devices increasing the gate voltage. The higher is the V_{GS} the higher is the I_{DSpeak} reached during turn-ON transient.

Fig. 5.9 shows the turn-ON instantaneous power and the related failure energy for the different devices just before the failure. Also in this case the higher is the overdrive the faster is the transient and the higher is the instantaneous power peak (see 5.9 (a)). On the contrary, the higher is the gate voltage the lower is the failure energy (see 5.9 (b)). By knowing the switching energy and the thermal resistance (R_{TH}) of the device we can calculate the maximum average temperature of the device during the hard-switching measurement. In fact, in the best case the maximum failure energy is about 50 μJ thus the average switching power loss at 10kHz is about 0.5W. From previous measurements a R_{TH} = 22.5 K/W can be assumed for the measured sample. This leads to an average temperature increase of 11.25°C. From this calculation we can conclude that the average

temperature increase is very low and cannot be the failure cause. Note that in chapter 4 the role of hot-electrons and temperature during hard-switching was already studied showing that (i) a large instantaneous temperature increase and (ii) hot electrons formation are present during dynamic operation. The results obtained in this section confirm that the instantaneous behavior of the devices is of crucial importance for robustness to hard-switching operation.

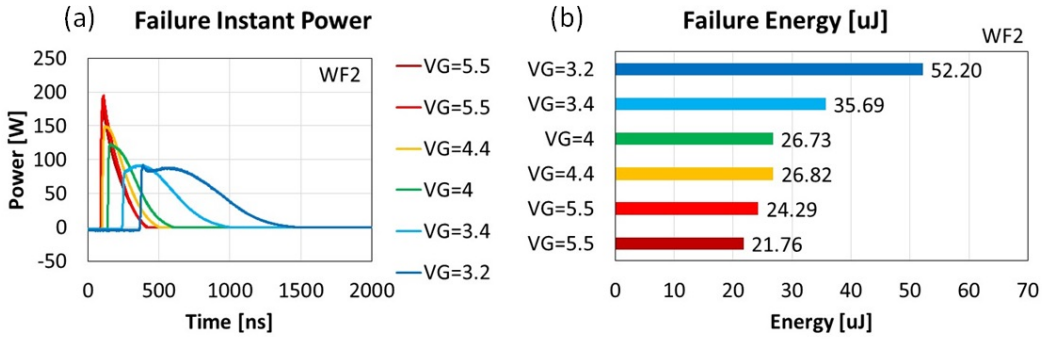

Figure 5.9: Transient turn-ON power (left) and respectively energy (right) before the failure for different devices increasing the gate voltage. The higher is the V_{GS} the higher is the transient failure power peak reached and the lower is the failure energy

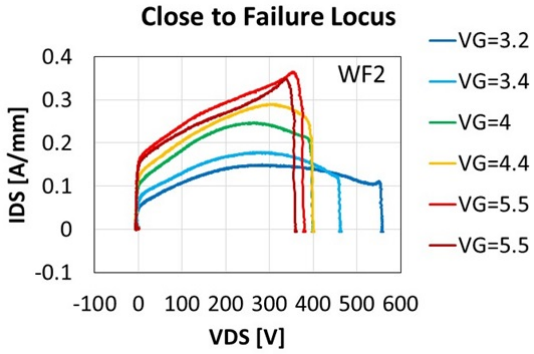

Figure 5.10: Locus before the failure for different devices increasing the gate voltage. The higher is the V_{GS} the higher is the locus

In order to better understand the results obtained, fig. 5.10 reports the turn-ON locus before the failure for the different devices. As can be noted the more is the overdrive the wider is the obtained locus. In particular, for $V_{GS} > 4$ V the locus broadens beyond 0.25 A/mm and the V_{DD} failure voltage goes down to

400V. This result is in agreement with the results obtained with the TLP SOA measurements in section 5.1. In fact, both results highlight that the devices break at lower voltage by increasing the overdrive and thus the instantaneous turn-ON current. Note that, in the breakdown hard-switching tests, the turn-ON time is larger then the SOA tests of section 5.1 thus the failure current levels can change.

5.3 Hard switching stress tests. Weibull statistics

After the analysis of the breakdown limits in term of hard-switching robustness, the system proposed in section 3.4.2 was used to implement stress tests in order to assess the hard-switching failure statistics of the devices. Fig. 5.11 reports the stress test concept. At first, the V_{DD} high voltage is applied to the device and then, in order to start the hard-switching stress test, the gate signal is turned ON at fixed frequency for a variable stress time or until the device failure. During the stress, in order to assess the device dynamic behavior, the R_{DSON} and the turn-ON switching waveforms are acquired each 20 s.

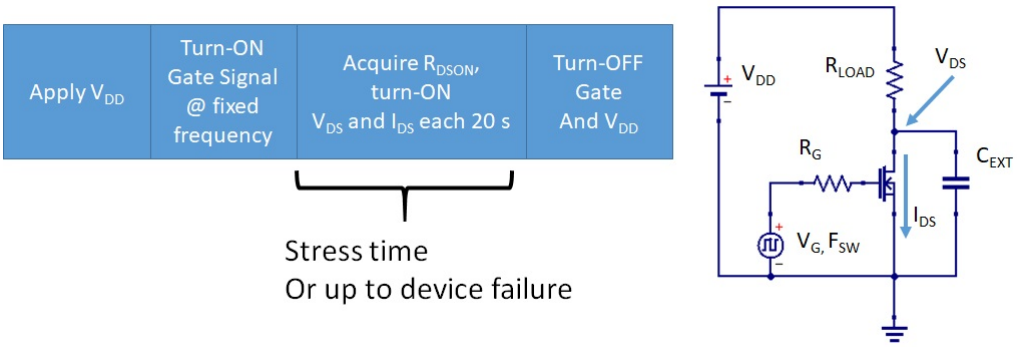

Figure 5.11: Hard-switching stress measurement concept

At first, in order to calibrate the stress conditions to obtain a time to failure in the order of tens of minutes, a preliminary stress with variable frequency and overdrive was carried out (see fig. 5.12). The V_{DD} was fixed to 600 V and an intermediate external capacitor value of 90 pF was used. In order to provide enough I_{DSON} current to measure the R_{DSON}, a load resistor R_{LOAD} equal to 24 kΩ was chosen. At first, the frequency and the gate voltage were fixed to 10 kHz and 4.5 V respectively. After 3 hours stress, the device was still alive and

the stress conditions were changed. In particular the frequency was increased to 50 kHz in the following steps. Then, in order to increase the I_{DSpeak} during the turn-ON switching transient the gate voltage was increased from 4.8 V to 5.1 V with 0.1 V step. As can be noticed, the device breaks when the step ($V_{GS} = 5.1$, $I_{DSpeak} \sim 0.3$A/mm) is reached.

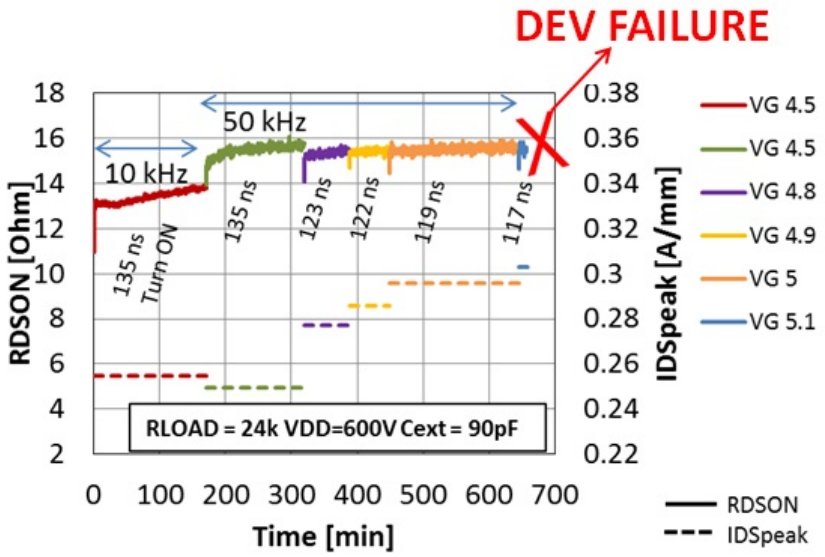

Figure 5.12: Preliminary stress test carried out to find proper failure stress conditions in order to reach device failure in tens of minutes range

After the preliminary stress test, the stress conditions to be used in the stress tests were obtained. Table 5.2 summarizes the stress conditions used for the stress tests of the current section. In order to keep the stress I_{DSpeak} close to 0.3 A/mm and thus to stress all the devices at the same current level, the V_G was adjusted in the range of 4.8 V - 4.9 V depending on the device behavior. In order to obtain a preliminary statistics of the time to failure in hard-switching operation, four devices were stressed until failure with the conditions reported in table 5.2. Fig. 5.13 shows the results obtained. As can be noticed, in order to obtain $I_{DSpeak} \sim$ 0.3 A/mm, the V_{GS} was adjusted between 4.8 V and 4.9 V. During the stress, the R_{DSON} and I_{DSpeak} slightly increase. Moreover, the four devices have a time to failure (TTF) between $\sim$ 3.5 hours and $\sim$ 10 hours.

A Weibull distribution was used to fit the obtained failure times. Before going on, it is worth recalling briefly some theoretically tips regarding the Weibull statistics. The random variable to be studied is the time to failure of the devices. Equation 5.1 reports the Weibull cumulative distribution function of the random

Table 5.2: Settings for Hard-switching stress

Symbol	Quantity	Value
D	Duty cycle	30%
F_{SW}	Switching frequency	50 kHz
R_{LOAD}	Load resistor	24 kΩ
V_{DD}	OFF voltage	600 V
I_{DSpeak}	turn-ON transient I_{DS} peak	0.3 A/mm
V_G	Gate voltage	adjusted to get $I_{DSpeak} \sim 0.3$ A/mm
C_{ext}	External capacitance added	90 pF

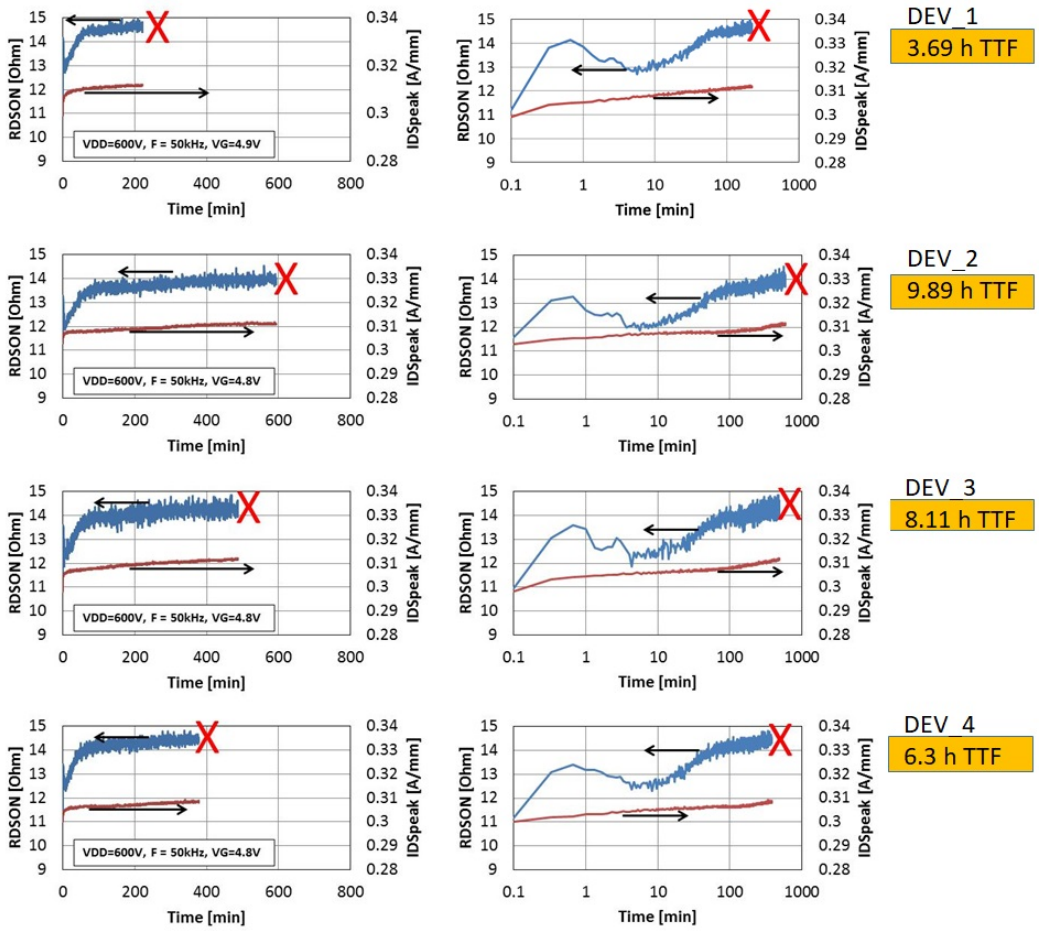

Figure 5.13: R_{DSON} and I_{DSpeak} evolution during stress tests on four different devices in hard-switching conditions: linear time scale (left) and log time scale (right). TTF can be extracted.

variable and represents the probability that a device breaks from 0 to time t or, in other words, having a population of devices, is the percentage of dead devices at time t.

$$F(t) = 1 - e^{[-(t/\alpha)^{\beta}]} \tag{5.1}$$

where $\alpha, \beta > 0$ are two parameters and t is the time. Note that α is the characteristics life, i.e. the time corresponding to 63.2 % device failed.

Starting from equation 5.1 and taking the natural logarithm we obtain:

$$-\ln\left[1 - F(t)\right] = (t/\alpha)^{\beta} \tag{5.2}$$

By using this equation and taking the natural logarithm another time the following equation can be written:

$$\ln\left\{\ln\left[\frac{1}{1 - F(t)}\right]\right\} = \beta \ln t - \beta \ln \alpha \tag{5.3}$$

Equation 5.3 shows that the term

$$\ln\left\{\ln\left[\frac{1}{1 - F(t)}\right]\right\} \tag{5.4}$$

has a linear dependency with ln(t). β is the slope and -βlnα is the intercept of the straight line. Fig. 5.14(a) shows this result.

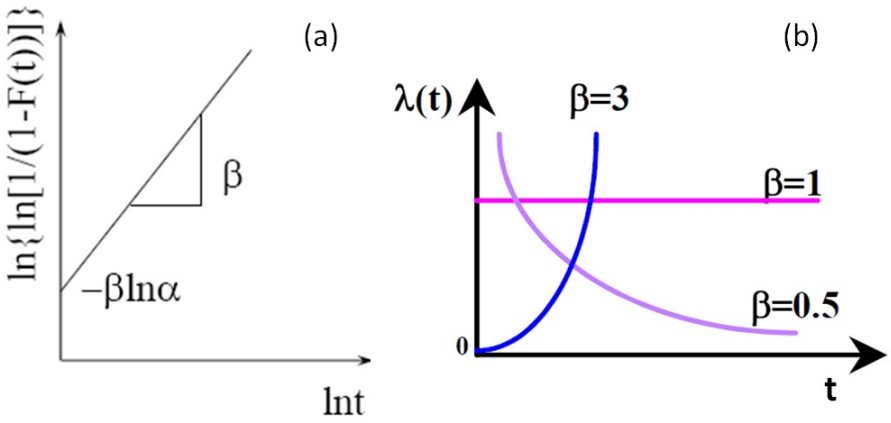

Figure 5.14: Weibull plot to calculate the α and β values (a) and failure rate of the Weibull distribution for different β values (b)

Finally to conclude the theoretical recall, it is worth reporting also the failure rate of the Weibull distribution:

$$\lambda(t) = \frac{\beta t^{\beta-1}}{\alpha^{\beta}} \tag{5.5}$$

Fig. 5.14(b) reports the plot of the failure rate for different β values. As can be noted, if $\beta < 1$ the failure rate decreases as a function of the time thus there is a high early mortality. If $\beta = 1$ the Weibull distribution does not have memory. If $\beta > 1$ the more is the time elapsed the more is the failure rate, thus the device aging has an impact on the failure.

In order to plot the equation 5.3 in the case of our study we need to have an estimator for F(t). In fact, we already have the four TTF (see fig. 5.13) but we need to know the related F(t) for each sample. One of the most commonly used method to estimate F(t) given a certain amount of samples if the median rank. This estimator estimates $F(t_i)$ by setting the probability that the i^{th} failure has occurred by the time t_i equal to 0.5. It can be demonstrated that in this case the $F(t_i)$ is equal to:

$$F(t_i) = \frac{i - 0.3}{N - 0.4} \tag{5.6}$$

where "i" is the index of each sample and "N" is the number of samples tested (N = 4 in our case). Using the four TTF measured and the equation 5.6 the plots reported in fig. 5.15 can be drawn. In order to calculate α and β of the Weibull distribution, the plot 5.15(a) reports the natural logarithm of the TTF as a function of the related F(TTF) and the linear interpolation of the data. From simple calculation we obtain:

$$\begin{aligned} \alpha &= 8.06 \\ \beta &= 2.34 \end{aligned} \tag{5.7}$$

In order to highlight the TTF values, fig. 5.15(b) shows the same result but with the logarithmic time scale in base 10. Results show that the linear interpolation fits well the experimental data so we can conclude that the Weibull distribution fits well the failure statistics of the devices. Usually, the Weibull distribution models failure mechanisms related to a weak point failure mode. In other words, there can exist a weak point in the device where the stress can cause a thickening of defects. From the analysis we obtained $\beta > 1$, thus we can conclude that the aging of the device cause an increase of the failure probability. Finally, it is worth mentioning that only four devices have been analyzed. The enlargement of the tested devices number will be a topic of the future activities.

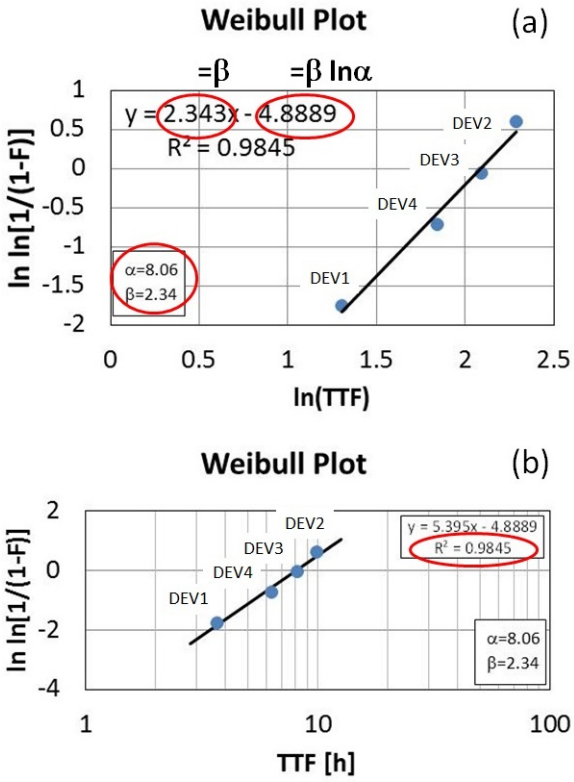

Figure 5.15: Weibull plot for the stressed devices: α and β are extracted from plot (a). base 10 logarithm highlights the TTF values (b)

5.4 Electroluminescence analysis during hard-switching operation

Until now, we demonstrated that hard-switching operation mode can be detrimental in terms of reliability. No direct measurements about the physical mechanisms involved during the stress have been carried out. In chapter 4, we demonstrated with indirect measurements that bot temperature increase and hot electrons can play a role during dynamic operation. In this section, in order to investigate with a direct measurement the physical behavior of the device working in switching mode, an electroluminescence analysis in hard switching conditions is presented. In particular, electroluminescence (EL) images have been acquired during the hard switching tests. The analysis reported in this section is aimed at investigating the emission behavior of the devices subjected to hard-switching conditions. In particular, it will be clear that the more stressful are the hard-switching conditions the more is the electroluminescence emission. This can be ascribed to the increase of the hot-electrons density within the structure of the

device.

5.4.1 Gate Bias EL analysis

At first, in order to investigate the impact of the gate current on electroluminescence, gate bias EL tests have been carried out. It is important to study the gate EL behavior because the gate electroluminescence (if present) can obscure the EL due to the drain current. In particular, fig. 5.16 shows the adopted measurement concept. In order to zeros the EL due to the ON drain current, the V_{DD} voltage was set to 0 V. The gate voltage was increased from 3.4 V to 6 V (step 0.2 V). The frequency and the duty cycle of the gate signal are 100 kHz and 30% respectively. For each step the EL image was acquired with an integration time of 25s.

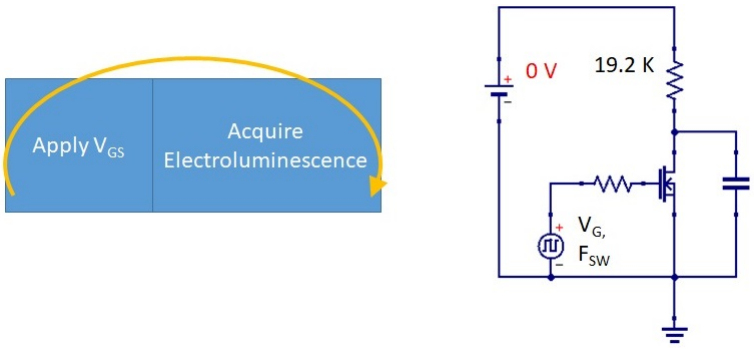

Figure 5.16: Gate bias EL measurement concept

Fig. 5.17 reports the results obtained with the gate bias EL measurement. The EL images show that the gate current causes emission within the structure of the device and the more is the V_{GS} the higher is the EL signal due to the increase of the gate current. In particular, it is easily noted that, in order to limit as much as possible the gate emission, a $V_{GS} < 4$ V is recommended. In order to conclude this section, it is clear that gate current related emission can occur and, in order to limit its contribute and not to cover the emission due to the hard-switching transients, a low gate voltage is suggested.

5.4.2 Drain Bias EL analysis

Fig. 5.18 shows the measurement concept adopted to investigate the drain EL during hard switching operation. The sequence of operations consists in applying the V_{DD}, turning ON the gate signal at fixed frequency and duty cycle, acquiring

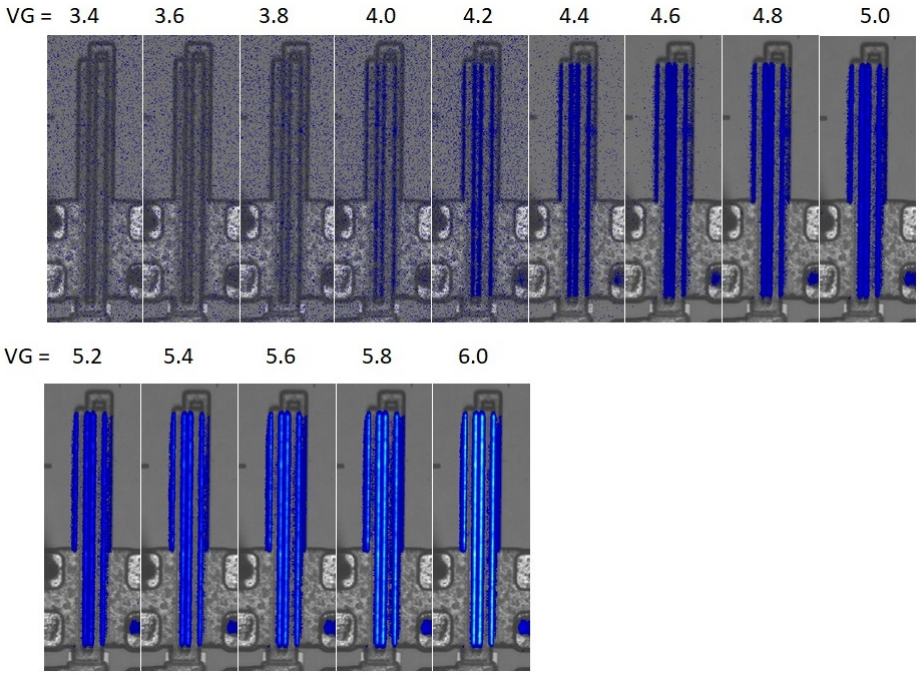

Figure 5.17: EL images acquired to study the gate stack emission

the EL signal for 35s and finally turning OFF the gate signal. This sequence is repeated for V_{DD} from 0 V to 500 V, with step 25 V. Before going on, it is worth mentioning that during this type of measurement the device switches continuously between four states as previously explained in section 3.4. The OFF state with high drain voltage, the hard switching state only during the turn-ON event, the ON state in linear region ($V_{DS} < 1$ V) and the soft-switching state during the turn-OFF commutation.

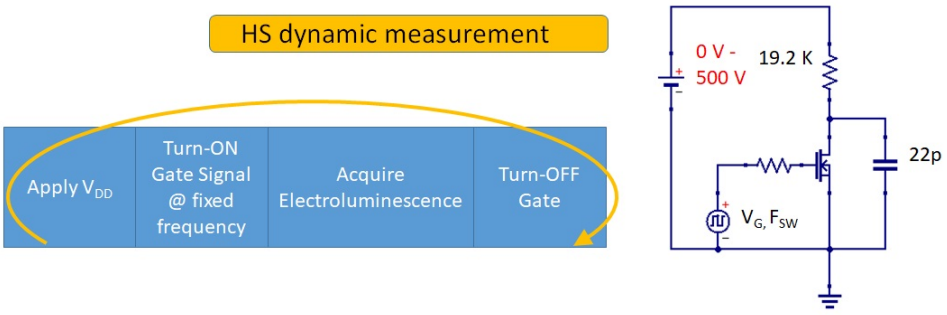

Figure 5.18: Drain bias hard-switching EL measurement concept

In order to better explain this concept, fig. 5.19 reports the simplified V_{DS} waveform of the DUT working in the system of fig. 5.18 with the four states

highlighted. In principle, the device can emit EL signal in each of the four states reported, thus a methodology to extract only the emission due to the HS contribution has to be studied. Moreover, the soft-switching turn-OFF state can be considered equal to the OFF state in terms of emission rate since the device first turns OFF (i.e. the I_{DS} zeroes) and then the V_{DS} increases. Therefore, first of all,

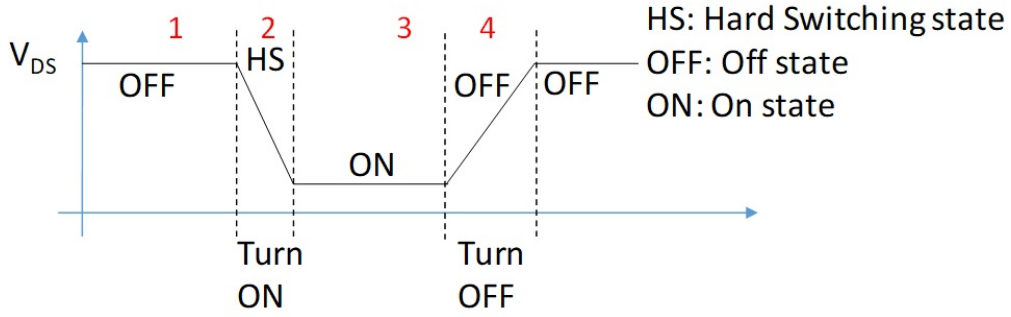

Figure 5.19: Simplified V_{DS} waveform during the hard-switching test. The device works in four states: (1) OFF-state (OFF), (2) hard-switching during turn-ON (HS), (3) ON-state (ON) and (4) soft-switching during turn-OFF (equal to OFF state since the device is already OFF during the transient)

it is worth studying the EL behavior in the states to be discarded, i.e. the ON state and the OFF state. Figs. 5.20 and 5.21 show the measurement concepts adopted to acquire the emission in ON and OFF states. In the ON state measurement the device is kept in ON state in linear region with $V_{GS} = 3.6$ V and the V_{DD} is increased up to 500 V with 50 V step. For each step, the EL signal is acquired with an integration time of 35 s. On the contrary, in the OFF state measurement the device is biased in OFF state and again the V_{DD} is increased up to 500 V with 50 V step. Also in this case, for each step the EL signal is acquired with an integration time of 35 s.

Fig. 5.22 shows the results obtained with the OFF state electroluminescence measurement. The images show that no emission is present within the device structure or the emission is under the sensitivity of the EL camera. Fig. 5.23 reports the integration of the EL count within the active region of the device. The value of the EL photon count is close to the camera noise. From figs. 5.22 and 5.23 it is possible to conclude that no emission is present in OFF state.

Fig. 5.24 shows the results obtained with the ON state electroluminescence measurement. The V_{GS} was set to 3.6 V. Note that (i) this value will be the same used to acquire EL in hard switching and (ii) this value is enough low

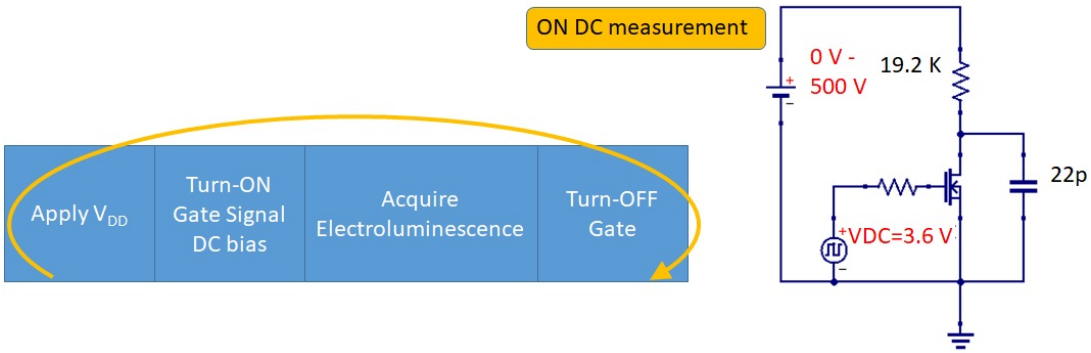

Figure 5.20: Drain bias ON state EL measurement concept

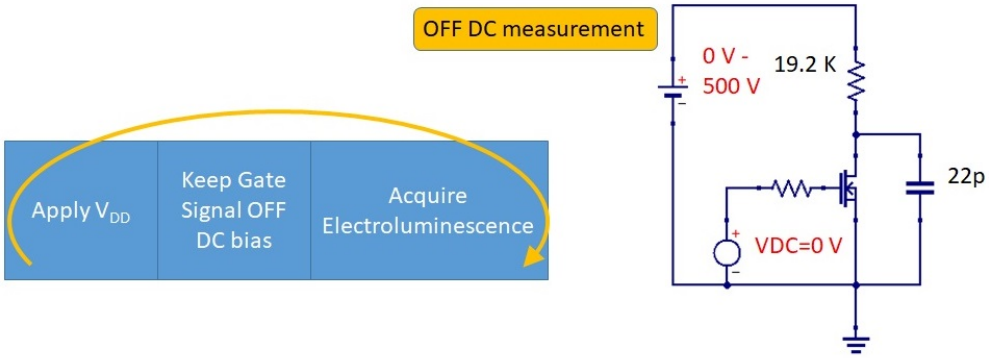

Figure 5.21: Drain bias OFF state EL measurement concept

to avoid the gate voltage emission (see fig. 5.17). EL images show that, in ON state, emission is present within the device structure due to the flowing drain current. In particular, the electroluminescence signal decreases with the increases of the V_{DD} and V_{DS}. Fig. 5.25 (a) reports the integration of the EL signal in the active region of the device as a function of the V_{DD}. The plots show that the EL intensity decreases as the V_{DD} and thus the V_{DS} increases. This behavior can be ascribed to both (i) the decrease of the V_{GD} and thus the lowering of electric field present in the access region between the gate and drain contacts and (ii) the expected slight increase of the device temperature at higher voltage, which causes an increase of the scattering mechanism and thus the lowering of the carriers energy due to the reduction of the mean-free path over which carriers are accelerated. Note that during the ON measurement the device is biased in

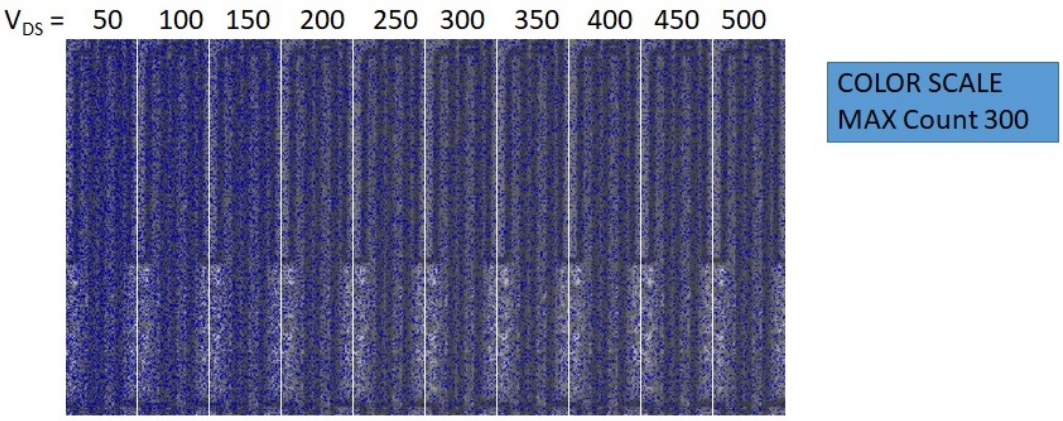

Figure 5.22: Electroluminescence in OFF state, $V_{DD} = V_{DS}$ from 50 V to 500 V.

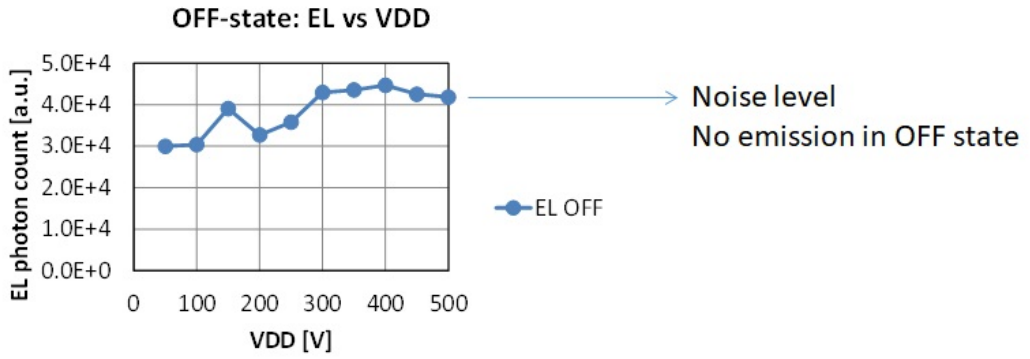

Figure 5.23: Total EL count in OFF state as a function of V_{DD}, the photon count is close to the camera noise

linear region (see 5.25 (b)) thus the V_{DS} is very low. This is due to the large R_{LOAD} value (19.2 kΩ in fig. 5.20) compared to the device R_{DSON} ($\sim$ 9 Ω)

In order to conclude the ON and OFF EL analysis, we showed that there is no emission in OFF state whereas emission in ON state is present. In order to limit as much as possible the ON emission and highlights the HS emission during the hard switching EL measurement explained in figs. 5.18 and 5.19, the ON phase has to be reduced as much as possible by reducing the duty cycle. Table 5.3 summarizes the settings used to carry out the electroluminescence measurement in hard-switching conditions. In order not to break the device, the external capacitance was reduced to 22pF. It will clear soon that this value is enough to see EL in hard switching.

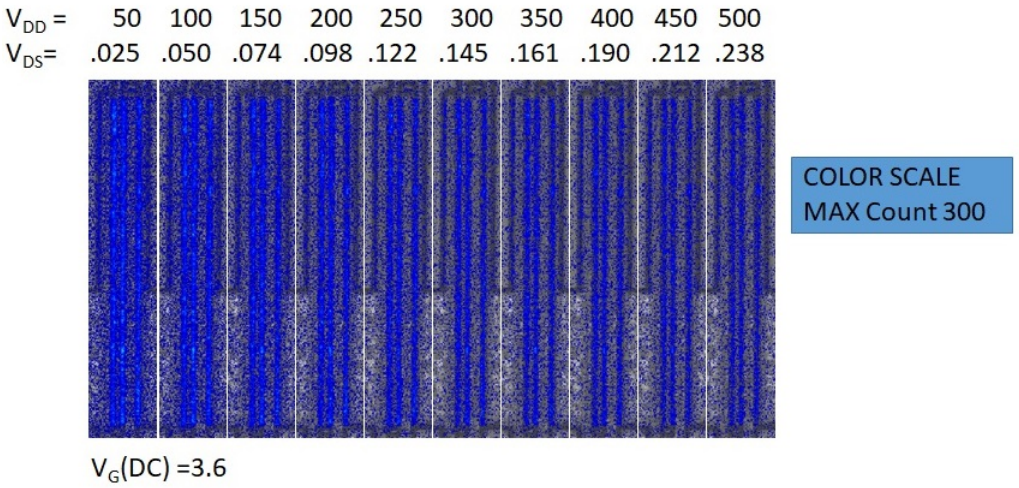

Figure 5.24: Electroluminescence in ON state, V_{DD} goes from 50 V to 500 V, V_{DS} goes from 0.025 V to 0.238 V in linear region

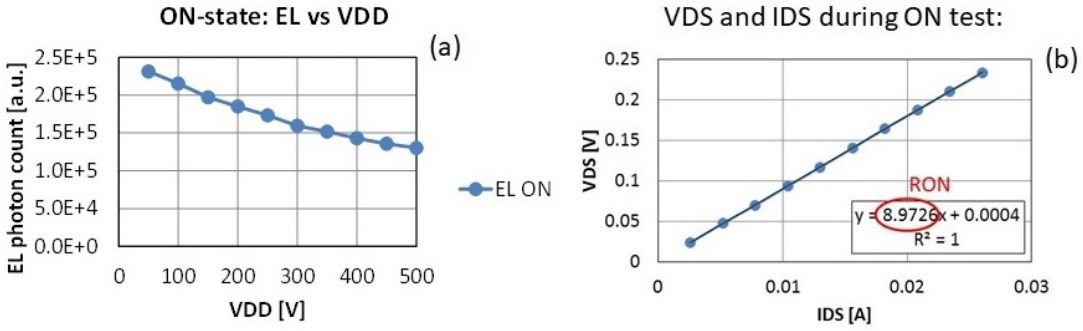

Figure 5.25: Total EL count in ON state as a function of V_{DD} (a) and V_{DS} vs I_{DS} for each step (b)

Fig. 5.26 reports the results obtained with the electroluminescence measurement carried out during hard switching operation. EL images show that beyond 300 V the EL signal increases with the increasing of the V_{DD}. Note that increasing the V_{DD} also the turn-ON energy and turn-ON power peak increase. Figs. 5.27 and 5.28 show this result. As can be noticed the electroluminescence signal increases with the increasing of the V_{DD}, the turn-ON power peak and the turn-ON energy. This behavior can be ascribed to the formation of hot electrons within the structure of the device which increases the EL signal [27].

Table 5.3: Settings for Hard-switching EL measurement

Symbol	Quantity	Value
D	Duty cycle	1.5%
F_{SW}	Switching frequency	100 kHz
R_{LOAD}	Load resistor	19.2 kΩ
V_{DD}	OFF voltage	from 50 V to 500 V
V_G	Gate voltage	3.6 V
C_{ext}	External capacitance added	22 pF

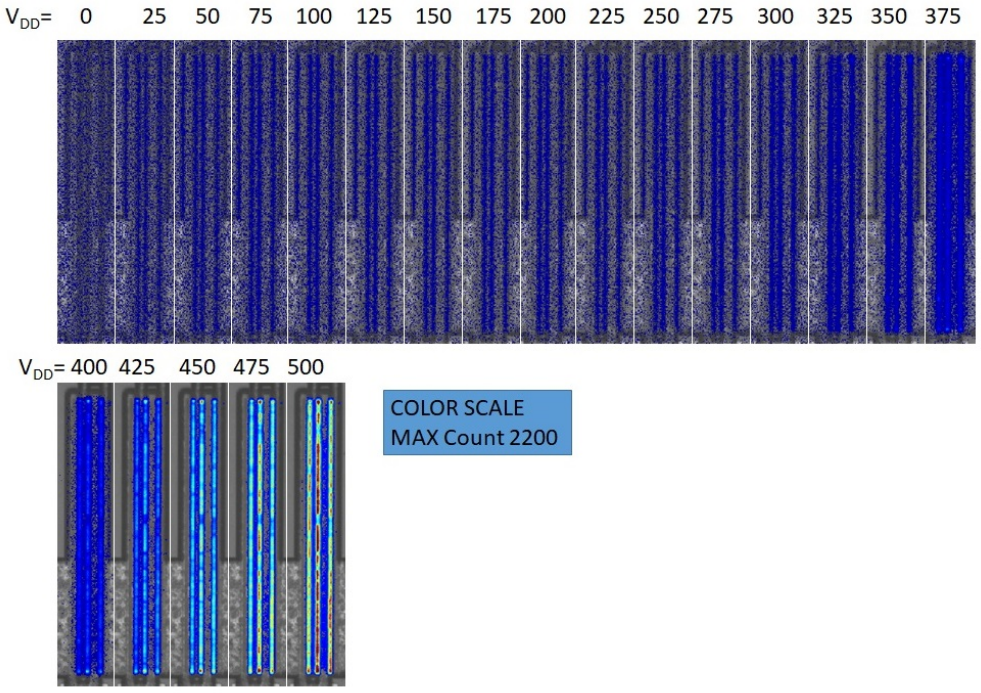

Figure 5.26: Electroluminescence images in HS state, V_{DD} goes from 50 V to 500 V

Fig. 5.29 shows the comparison of the EL signals as a function of the applied V_{DD} for the three different states. The comparison shows that the OFF state EL is very low and is close to the camera noise level. The ON emission is similar to the HS emission until 300 V and, as previously explained, decreases with the increase of the V_{DD}. Finally, the HS waveform slightly increases for $V_{DD} < 300$ V whereas it shows a large increase for $V_{DD} > 300$ V. Note that, during the

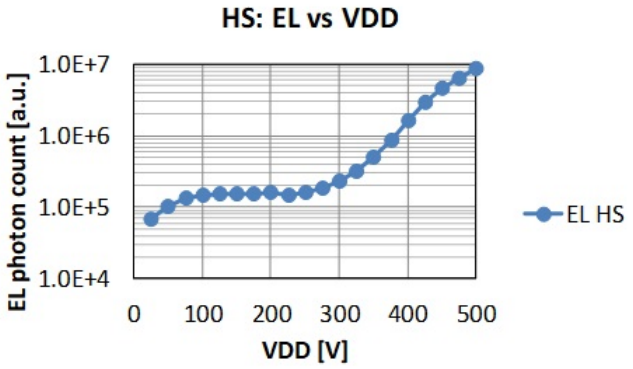

Figure 5.27: Total EL count in the HS measurement as a function of V_{DD}

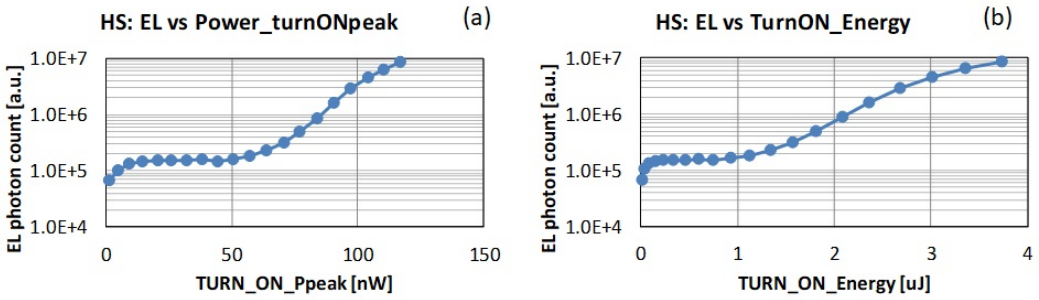

Figure 5.28: Total EL count in the HS measurement as a function of the turn ON power peak (a) and the turn ON energy (b)

HS measurement, a very reduced ON emission is expected due to the limited value of the duty cycle. For $V_{DD} < 300$ V, the EL ON waveform is similar to the EL HS curve (see fig. 5.29(b)). Despite this, due to the very reduced duty cycle and thus the short ON time during the HS measurement, the EL HS signal for $V_{DD} < 300$ V can be ascribed mainly to the contribution of the hard-switching transients and only partially to the ON phase emission. For $V_{DD} > 300$ V the hard switching emission increases a lot and becomes higher respect to the other contributions. This explains the large increase of the EL signal for $V_{DD} > 300$ V. This behavior can be ascribed to the formation of hot electrons within the device structure occurring during the hard-switching transients.

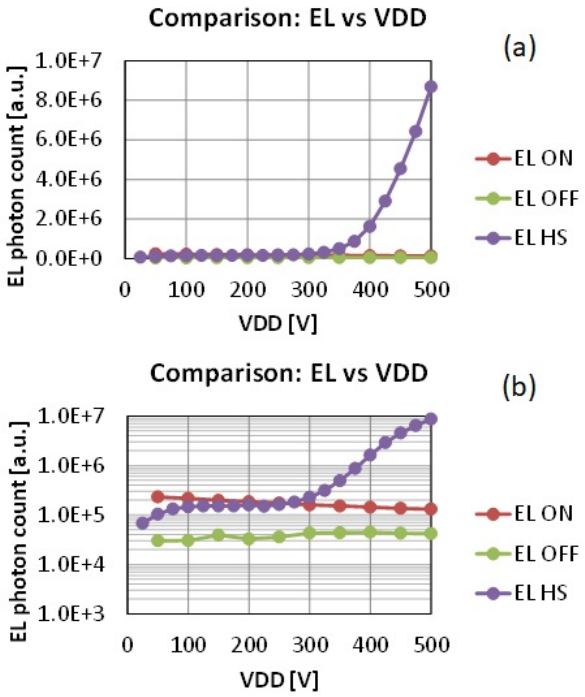

Figure 5.29: Comparison of the total EL count in the three states studied. linear scale (a) and log scale (b). Beyond 300 V the HS EL signal increases probably due to hot electrons formation

5.5 Chapter summary

In this chapter we presented the pulsed SOA of GaN power HEMTs transistors carried out with 100ns TLP system. Two main regions have been found. The former was mainly dominated by the high current and power level, the latter was characterized by high voltage and the high electric field plays a major role in the failure mode.

Then an extensive analysis of reliability in hard-switching conditions was presented. First of all, some breakdown measurements with different overdrive were reported. We found that the more is the overdrive the lower is the breakdown voltage during hard-switching operation. Moreover, by plotting the switching locus we found that the wider is the locus the lower is the breakdown voltage and energy. After the breakdown measurements, in order to find the failure statistics in hard-switching conditions, some dynamic stresses were carried out. Results demonstrated that the Weibull statistics fit well the times to failure of the devices tested. This is in agreement with a recent published work [26].

Finally, in order to better understand the device behavior working in hard-

switching conditions an EL analysis was carried out. It was found that the EL signal increases with the increasing of the stress voltage. This can be ascribed to the formation of hot-electrons within the device structure due to the high current and high electric field present during the hard-switching transients.

Conclusion and future perspective

In this thesis we demonstrated the feasibility of testing on-wafer GaH HEMTs devices in real-life conditions. Two main hard-switching systems have been developed. The former is based on a DC-DC boost converter board and was used to study the hard-switching transient behavior of GaN devices. An extensive analysis of the switching transients have been carried out demonstrating that external parasitics have a remarkable impact on the commutation waveforms. The last system is a simplified version of the former and is based on a resistive load and a capacitor connected in parallel to the DUT. This system was used to stress devices in real operation hard-switching conditions. With such systems we were able to mimic application conditions in laboratory measurement test procedures. In this way we were able to assess performance and reliability of GaN HEMT devices working in real life conditions already at wafer level. We demonstrated that this system enables novel measurement techniques able to study the real in-circuit reliability of GaN devices. We were able to study the impact of switching conditions both on trapping behavior and lifetime. We found that (i) the high power during the hard-switching events can lead to hot-electrons trapping and thus an increase of the R_{DSON} and (ii) the lifetime during switching operation is governed by the Weibull statistics. Some test methodologies to test GaN HEMT devices in hard switching conditions have been defined. In particular, with the developed systems the following measurements have been carried out:

- Voltage sweep R_{DSON} measurement (section 2.2.2): useful to investigate the R_{DSON} increase as a function of the high voltage and the hard-switching

stress conditions.

- Voltage sweep breakdown measurement (section 5.2): used to assess devices limits in term of hard-switching robustness.

- Short circuit hard-switching measurement (section 4.2): useful to investigate the device current collapse due to both temperature increase and hot-electrons trapping.

- Hard-switching stress tests (section 5.3): used to identify the failure statistics of the devices working in switching conditions.

- EL measurement during hard-switching operation (section 5.4): used to measure hot-electrons emission during hard-switching operation.

All these measurements concepts are available on-wafer thus the tested devices can be potentially easily analyzed after the possibly failure with spectroscopy or microscopy techniques. The main results obtained with the hard-switching analysis can be summarized as follows:

- GaN HEMT devices switch in saturation current limited mode and the external parasitics affect both the switching speed and the power loss.

- GaN HEMT devices can be tested in real hard-switching conditions using a resistive load circuit diagram.

- Hot-electrons can appear within the structure of the device during the switching transients due to high voltage and high current operation.

- Hard-switching operation mode can cause R_{DSON} increase due to both temperature increase and hot-electrons charge trapping.

- The Hard-switching locus extension affects reliability. In particular the wider is the locus trajectory the lower is the breakdown voltage of the DUT.

- Hard-switching operation is a detrimental condition and can led to early device failure. The TTF is governed by Weibull statistics.

As far as the future perspective is concerned, we think that these important results can be used in future to find a degradation law of GaN HEMT devices working in real dynamic conditions and try to extrapolate a lifetime model of such outstanding technology. This is the main important step to be achieved in future. The main idea is to enlarge the statistics by stressing more devices at different stress levels (i.e. different voltage, current, and power loss). By correlating the stress levels and the TTF set it is possible to find a degradation law of GaN devices working in hard-switching conditions. We think that this approach can lead to the identification of the main failure mechanisms of GaN HEMTs working in real life conditions. Finally we think that, by correlating the lifetimes set with the stress conditions, a lifetime model for GaN HEMT devices can be achieved.

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