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Characterization and Study of Reliability Aspects in GaN High Electron Mobility Transistors

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Caratterizzazione e studio degli aspetti di affidabilità nei HEMT in GaN

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To my beloved mother, Maryam, and beloved father, Hossein ...

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Padova, 20 September 2018 A. Tajalli

Abstract

GaN-based high electron mobility transistors (HEMTs) have excellent performance for power applications. Indeed, characteristics such as the high breakdown electric filed (3.3 $^{MV}/_{cm}$), the low ON-Resistance (R_{ON}) and the good thermal dissipation make the GaN-based diode and transistor a good potential for high frequency and power applications. The other outstanding feature of GaN-based HEMTs is the high electron mobility (> 1200 $^{cm^2}/_{V.s}$) of the 2-dimensional electron gas (2DEG), formed at the interface between AlGaN and GaN, which leads to a low channel resistance and a high current density.

This thesis presents an overview of the most relevant trapping and degradation mechanisms that limit the performance and lifetime of GaN-based transistors for power electronics applications. To that end, pulsed I-V and drain current transient measurements are employed in order to investigate the trapping effects.

The degradations of AlGaN/GaN MIS-HEMTs submitted to the gate step-stress experiments are investigated in the first part of this thesis. The results, that are obtained by a combined electrical and optical characterization over the different voltages, are discussed in chapter 2 which indicate the existence of a field- and hot-electron induced phenomena as the AlGaN/GaN MIS-HEMTs degradation mechanism.

A specific discussion is devoted to investigate the proton irradiation effect on the dynamic-Ron in HEMTs and is presented in chapter 3. It is shown that the proton irradiation is an effective and controllable method to reduce the dynamic-Ron in AlGaN/GaN HEMTs. Indeed, it is shown that samples that are submitted to a proton irradiation at high fluences (1.5×10^{14} cm^{-2}, 3 MeV) exhibit a complete suppression of dynamic-Ron (complete voltage range, 150°C). This chapter further continuous to describe the voltage and temperature-dependent pulsed I-V characteristics of 650 V-rated transistors. It also points out the physical origin of dynamic R_{ON} in these devices.

Furthermore, owing to the positive and stable threshold voltage, the low on-resistance and the high breakdown field, the p-GaN gate GaN-based transistors are commonly accepted as promising devices for application in power converters. To that end, chapter 4 deals with the mechanisms that limit the dynamic performance and the reliability of normally-off GaN-based transistors. This chapter proposed the suppression of threshold voltage instability by a suitable passivation on the p-GaN sidewall. The improved reliability of device highlights that hole trapping mostly takes place on the sidewalls.

Finally, in chapter 5, a low leakage current and a state-of-the-art vertical breakdown voltage of above 1400 V a carbon-free GaN-on-Si device are demonstrated. These characteristics are achieved thanks to a thick and excellent crystal quality of GaN buffer. Indeed, low trapping effects are observed all the way to 1200 V with a low dependency of the substrate bias on the current density. The first demonstration of trap-free at such high voltage with this material system, could paves the way for 1200 V applications with GaN-on-Si resulting in a lower Ron and thus higher efficiency as compared to SiC and Si devices.

Abstract

I transistor ad alta mobilità in nitruro di Gallio (GaN–HEMT) hanno eccellenti proprietà per applicazioni di potenza. Infatti, caratteristiche come l'alto campo elettrico di rottura (3.3 $^{MV}/_{cm}$), la bassa resistenza di canale (R_{ON}) e la buona dissipazione termica hanno reso i diodi e i transistor in GaN degli ottimi candidati per applicazioni ad alta frequenza e potenza. Un'altra eccezionale caratteristica dei transistor HEMT è l'alta mobilità (> 1200 $^{cm^2}/_{V.s}$) del gas bidimensionale (2DEG) che viene a formarsi all'interfaccia tra l'AlGaN e il GaN, che porta ad alte densità di correnti e a basse resistenza di canale.

Questa tesi presenta un panoramica dei principali meccanismi di intrappolamento di carica e di degrado che limitano le prestazioni e l'affidabilità di dispositivi GaN HEMT per applicazioni di elettronica di potenza. Per investigare i meccanismi di intrappolamento di carica sono state usate misure di transienti di corrente e misure I-V impulsate.

Inoltre nella prima parte della tesi è stato analizzato il degrado di GaN MIS HEMT sottoposti a step-stress al gate. I risultati (discussi nel capitolo 2), ottenuti da caratterizzazioni sia ottiche sia elettriche a diverse tensioni, indicano l'esistenza di meccanismi di degrado attivati dal campo elettrico e da elettroni caldi.

Nel capitolo 3 viene presentata una discussione specifica che analizza gli effetti dell'irraggiamento con protoni sulla resistenza di canale di GaN HEMT. Viene mostrato che l'irraggiamento da protoni è un metodo efficace e controllabile per ridurre il fenomeno dell'incremento della resistenza di canale nei GaN HEMT. Infatti viene mostrato che i campioni che sono sottoposti a irraggiamento con protoni ad alta fluenza (1.5×10^{14} cm^{-2}, 3 MeV) mostrano una soppressione completa del fenomeno della resistenza dinamica (nell'intero intervallo di tensione a 150°C). Questo capitolo continua a descrivere la dipendenza delle caratteristiche impulsate di transitor in GaN a 650 V dalla tensione e dalla temperatura. Inoltre viene sottolineata l'origine fisica

del fenomeno della resistenza dinamica presente sui dispositivi.
A causa della tensione di soglia positiva e stabile, della bassa resistenza di canale e dell'alto campo elettrico di rottura gli HEMT con gate in p-GaN sono dei dispositivi promettenti per applicazioni di potenza. Il capitolo 4 tratta i meccanismi che limitano le prestazioni dinamiche e l'affidabilità di transistor GaN HEMT con soglia positiva. Questo capitolo mostra come sia possibile sopprimere totalmente l'instabilità della tensione di soglia aggiungendo uno strato di passivazione sullo strato di p-GaN. Il miglioramento dell'affidabilità del dispositivo sottolinea come avvenga intrappolamento di lacune sullo strato di p-GaN e questo viene limitato grazie alla passivazione.
Infine nel capitolo 5 viene presentato un dispositivo verticale in GaN cresciuto su Silicio capace di sostenere 1400 V e a bassa perdita di corrente. Queste caratteristiche sono ottenute grazie alla possibilità di crescere un strato buffer in GaN molto sottile e di eccellente qualità cristallografica. Infatti sono stati osservati bassi effetti di intrappolamento di carica fino a 1200 V con una bassa dipendenza dalla polarizzazione del substrato sulla densità di corrente. La prima dimostrazione di un dispositivo cresciuto con questi materiali senza intrappolamento di carica può aprire la strada ad applicazioni a 1200 V realizzate con dispositivi in GaN sfruttando la minore resistenza di canale e quindi la miglior efficienza rispetto a dispositivi in carburo di silicio (SiC) e silicio (Si).

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1 Gallium Nitride Material and Device Properties

1.1 Gallium Nitride (GaN)

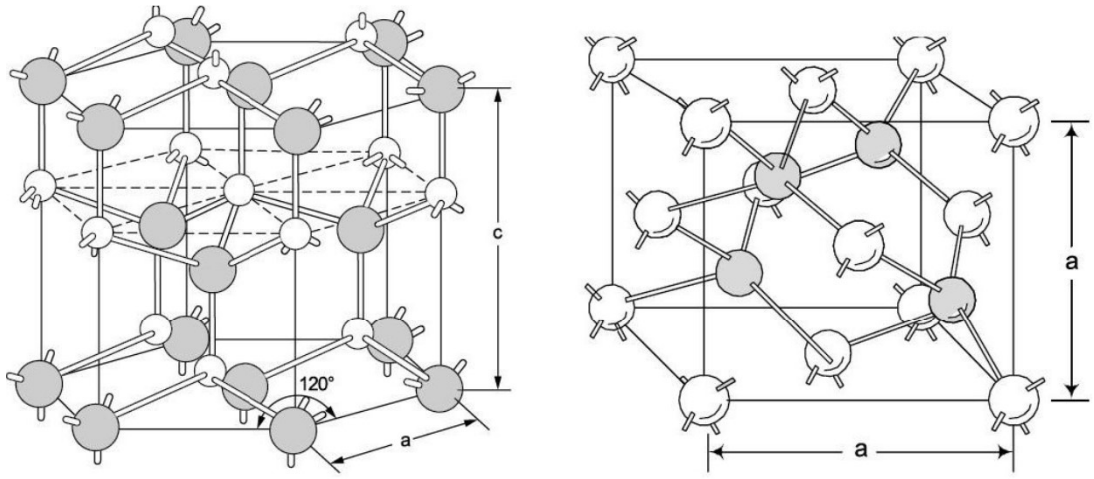
Gallium nitride (GaN) is a compound semiconductor with a high breakdown voltage of a basic material which is typically used for all device layers requiring fast carrier transport. There are two different crystal structures that are found so far: Wurtzite and zincblende. Figure 1.1 shows the structure of both of these crystals.

1. The wurtzite crystallographic structure consists of an elementary tetrahydric cell where each Gallium atom is bonded to four Nitride atoms. The subsequent lattice has hexagonal symmetry with planes formed by the same element alternating between them. In this case the lattice parameters are: a = b = c, $\alpha = \beta =$ 90°and γ = 120°.

2. Zincblende has identical lattice vectors a = b = c and orthogonal directions α = $\beta = \gamma$ = 90°. The unit cell follows the face-centered cubic bravais lattice, the vertices of the regular tetrahedron are occupied by the Nitrogen, whereas the Gallium links them together inside the cell.

The zincblend structure is metastable and naturally transmutes into the wurtzite structure. On the contrary, wurtzite structure is stable and thus used for electronic devices.

GaN is used as the channel material in various FETs as well as the base material in



(a) (b)

Figure 1.1 – (a) Visualization of wurtzite and (b) zincblende structures.

AlGaN/GaN HBTs, and ALGaN/GaN High Electron Mobility Transistors (HEMTs). Most of the ohmic contact layers in any device incorporate binary n-doped and p-doped GaN. Moreover, GaN can further be grown as a semi-insulating material with growth parameters close to those of the semiconducting layers. In order to elaborate more on the GaN some of its properties are explain in the following subsections.

1.1.1 Electrical properties

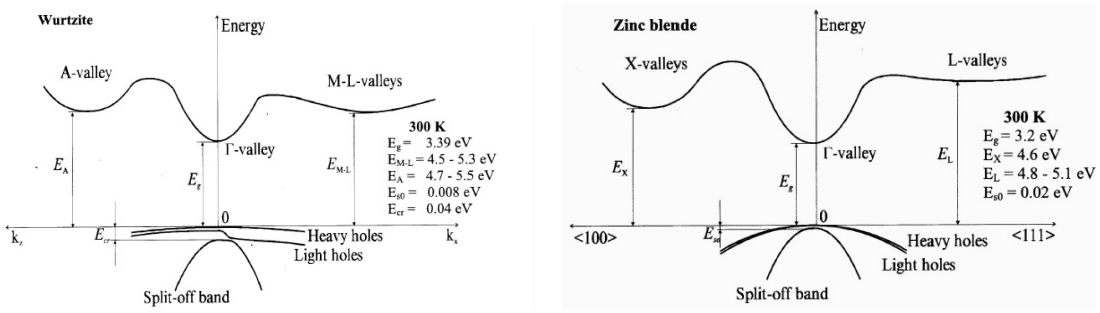
The crystal structure, mechanical and thermal properties of GaN are discussed in a number of publications. Table 1.1 reports some of the electronic properties of GaN and is comparing them to the other common semiconductors such as InN, AlN and Si. From this table clearly a high bandgap along with a high mobility, a high mobility along with a high breakdown field and a high saturation velocity of the GaN are standing out.

The band structure of Gallium Nitride in the first Brillouin zone is reported in Figure 1.2 which shows the GaN is a direct-bandgap semiconductor. In this way electron hole can be make a recombination without phonon interactions. GaN is a compound semiconductor, with a high carrier velocity saturation and high energy-gap. Its high energy-gap results in a very high breakdown voltage; due to the high electric field

Table 1.1 – Electronic properties of some semiconductors [1].

	GaN	InN	AlN	Si
Bandgap (eV)	3.4 eV	0.6 eV	6.4 eV	1.1 eV
Mobility ($cm^2V^{-1}s^{-1}$)	1500	3000	300	1000
Breakdown Field (MV/cm)	3	Low	11	0.3
Effective Mass	0.21 m_e	0.09 m_e	0.4 m_e	0.19 m_e
Velocity (cm/s)	2×10^7	2×10^8	-	1.0×10^7
polarization	High charge, carrier confinement			-

required for band-to-band impact ionization. These two properties (carrier velocity saturation and energy-gap) are typically combined to extract the Johnson's figure of merit (JM) which is an important index that gives the power and frequency limit of a material based only on the physical properties. GaN HEMTs are therefore extremely excellent and are promising for high-power and high-frequency applications. Owing to their high energy-gap, GaN HEMTs are also perfect for the space applications.



(a) (b)

Figure 1.2 – Wurtzite and zincblende band diagrams in the first Brillouin zone.

Furthermore, another attractive behavior of GaN compared to SiC is the ability to form the heterostructures. In fact, the great advantage that makes the GaN a more attractive material compared to SiC consist in its ability to form the heterostructures. This ability enables the HEMTs to have a better carrier concentration and channel mobility, whereas SiC can only be used to build Metal-Semiconductor Field-Effect Transistors (MESFETs) [2].

GaN layer are typically grown on different substrate with compatible lattice constant and thermal expansion coefficients. The most critical issue of the development of the GaN technology is the substrate choice in order to acquire proper epitaxial layers with low defects concentration. Silicon carbide shows a very good lattice matching with GaN; more details description of lattice mismatching is given in table 1.2 contrary to the other substrate approaches, such as Silicon or Sapphire. The latter offers a very good thermal conductivity which is useful for high-power applications. Furthermore, by introducing other thin layers before GaN deposition (better explained on the next section), the defects propagation from the substrate to the active area cab be reduced by means of a gradual variation of the lattice parameters.

Another substrate option comes from the hybrid substrates, which consist of a thin layer of Si or SiC supported by a thick layer of polycrystalline Silicon Carbide. The advantage of this substrate is the high thermal conductivity at low-cost, typical for poly-SiC layers, with a cheaper lattice-matched thin SiC layer or a single-crystal low-cost large diameter silicon wafer, grown on top of this substrate.

1.1.2 Piezoelectric properties

Spontaneous polarization is one of the most important behavior in each Gallium-nitride crystal, which is induced by the different electronegativity between Gallium and Nitrogen atoms, and generally in every III-Nitride compound. Each layer of GaN, or of its alloy, is characterized by a spontaneous polarization vector that strongly affects the electrical properties of any device processed on top of this layer. In the case of an alloy containing Aluminum, the higher the Aluminum content, the higher the polarization vector is.

Therefore, different physical virtues appears from the direction of the crystal growth: N-face and Ga-face. In the case of the N-face GaN layers, the layers start with Ga-atoms grow and end to the N-atoms. On the contrary in the Ga-face layer, the layers start from N-atoms grow to the Ga-surface (see Figure 1.3). It is worth noting that the device processing as well as the electrical properties of GaN based devices are completely dependent on the upper layer.

Besides, the mechanical strain can make a stress, or if two different lattice material are

grown it could present a charge due to the spontaneous and piezoelectric polarization vectors, and in consequence a high electric field. This is a fundamental properties operation for the electronics devices based on nitride heterostructures.

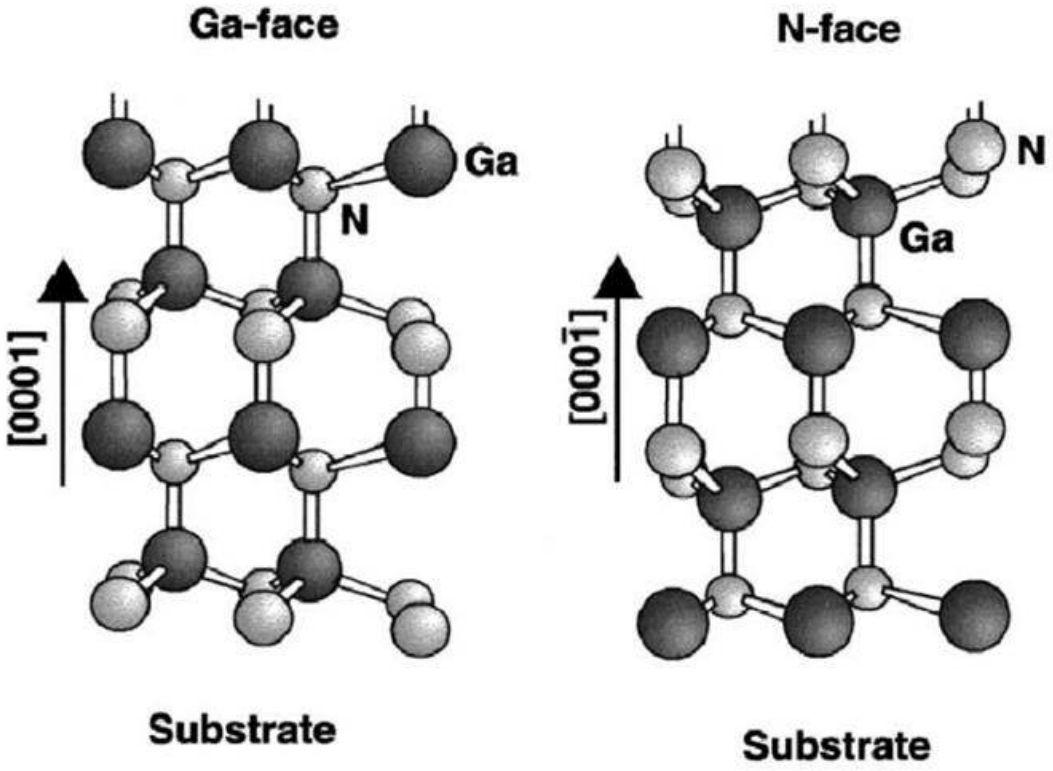


Figure 1.3 – Schematic drawing of the crystal structure of wurtzite Ga-face and N-face GaN layer.

The excellent properties of Gallium-Nitride make this semiconductor perfect candidate for both high-power and high-frequency applications. Furthermore, the high energy-gap make this material less prone to radiation effects, opening the possibility for future space applications. More on this will be discussed in chapter 3.

1.2 GaN High Electron Mobility Transistors

High Electron Mobility transistors (HEMTs), are featured with the high carrier mobility and are based on a high energy gap semiconductors heterostructures. As explained in the previous section the GaN as a based device enables the possibility to form a heterostructure which in turn enables the HEMTs to have a better carrier concentration

and channel mobility coming from its intrinsic semiconductors As a matter of fact, GaN with this properties is a perfect devices for high voltage and high power density operations.

When a semiconductor material is grown with epitaxial techniques on the top of another semiconductor material an heterostructure could be form. The behavior of the heterostructure is based on the different energy gaps (E_g) of the semiconductors. Indeed, there is a discontinuity on the band energy when growing a semiconductor on the top of another one which make a lattice constants difference. In the case of AlGaN/GaN heterostructure, the AlGaN is grown on the top of the GaN layer and adopts the lattice constant of the adjacent semiconductor.

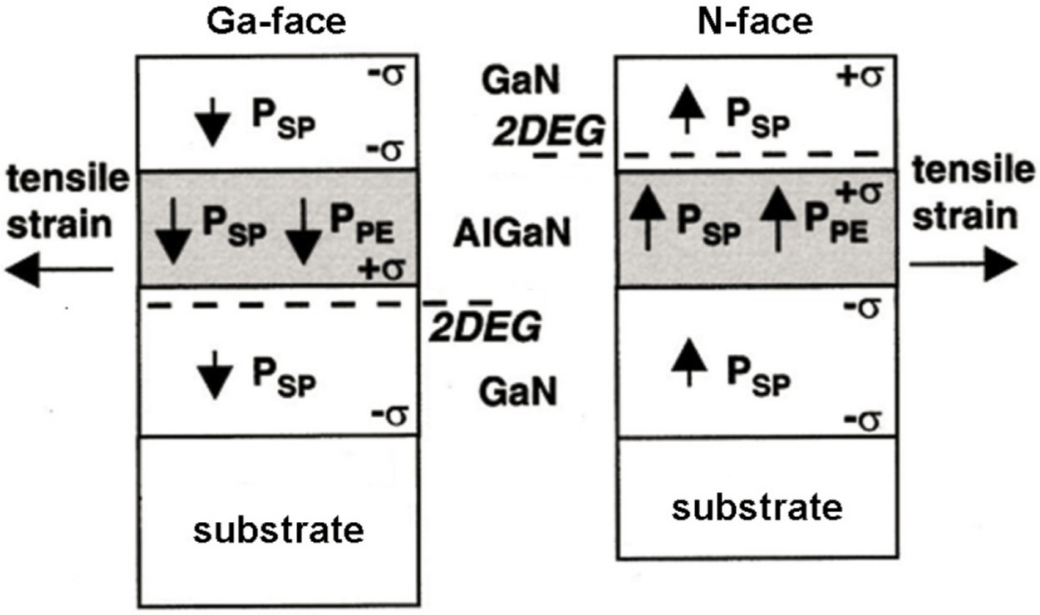


Figure 1.4 – Spontaneous piezoelectric polarization vectors in Ga-face and N-face topologies [3].

AlGaN has an intrinsic polarization field, this physical mechanism is called piezoelectric effect. The polarization field builds an electrical field and consequently, in AlGaN, this electrical field causes a charge distribution inside the heterostructure whiteout any doping. Figure 1.4 shows an HEMT structure in which the AlGaN layer with a strain polarization field is grown on the top of the GaN intrinsic or buffer layer. At the interfaces of Gan and AlGaN, a polarization charge density (σ_{pz}) forms a quantum well that is called Two-dimensional Electron Gas (2DEG). The important point is that

the electron concentration in the GaN layer at the heterointerface is increased significantly without any doping. As previously reported, the lattice mismatch between AlGaN and GaN is the origin of the the piezoelectric polarization.

Spontaneous polarization is another phenomenon to present a higher carrier concentration at the heterointerface. As discussed before, GaN presents a polarization which arises even in the absence of strain. The density of the 2DEG is related to the spontaneous polarization (P_{sp}) and the piezoelectric (P_{pe}) in this way the total polarization (P) is the sums of these two:

$$P = P_{pe} + P_{sp}. \tag{1.1}$$

The orientation of P_{sp} and P_{pe} depend on the type of strain: in compressive-strain they are opposed, and in tensile-strain they are aligned [4].

The advantage of a heterostructure is that the GaN buffer is an undoped semiconductor channel with the high intrinsic mobility thus there are no scattering phenomenon due to the reduction of impurities in the semiconductor.

Figure 1.5a shows a typical layer stack of AlGaN/GaN heterostructure, Figure 1.5b reports the electric charge distribution in a typical AlGaN/GaN heterostructure. The net charge Q_π is the sum of the spontaneous and piezoelectric polarization charge. The resulting band diagram is sketched in Figure 1.5c which also shows that the polarization field at the AlGan/GaN interface makes a 2DEG with the negative charge, it is still a question: *where does this charge come from?* J. P. Ibbetson *et al.* proposed in [6] that the polarization field in the AlGaN layer is high enough to change the band energy and distribute the charge, the electrons are injected from surface to the AlGaN/GaN heterointerface and form the 2DEG.

In Figure 1.6 a schematic representation of band energy is shown, if the thickness of AlGaN layer is less than the critical layer (t_{CR}), the 2DEG cannot be formed but when the thickness exceed the critical one the donor state is over the fermi level and

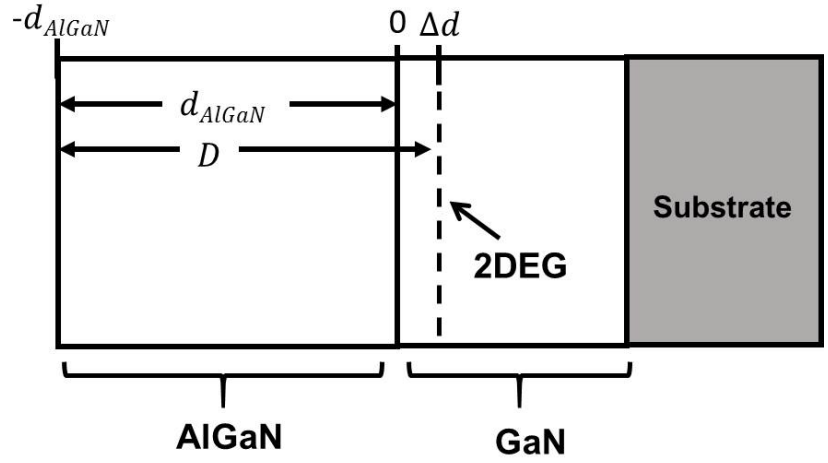
electron are de-traped and channel can be formed. The t_{CR} can be calculated as:

$$t_{CR} = \frac{(E_D - \Delta E_C)\epsilon}{q\sigma_{pz}}, \tag{1.2}$$

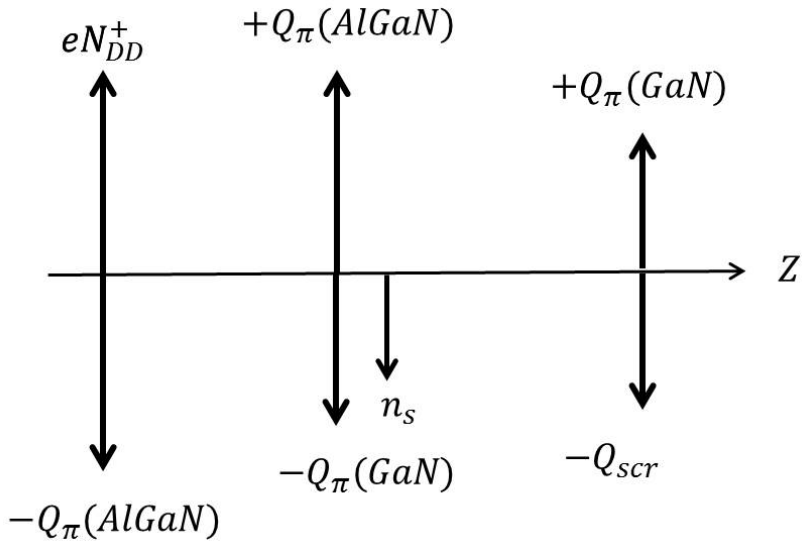
where E_D is the energy of the surface states, ΔE_C is the AlGaN/GaN conduction band offset and ϵ is the AlGaN relative dielectric constant. It is worth to notice that the offset between the AlGaN and GaN depends on the aluminium percentage in the AlGaN layer, which is the parameter for control the energy band gap ($E_{gap-AlGaN}$) between valance (E_v) and conduction (E_c) band. The energy gap can be calculated as:

$$E_{gap-AlGaN} = xE_{gap(AlN)} + (1-x)E_{gap(GaN)} - bx(1-x), \tag{1.3}$$

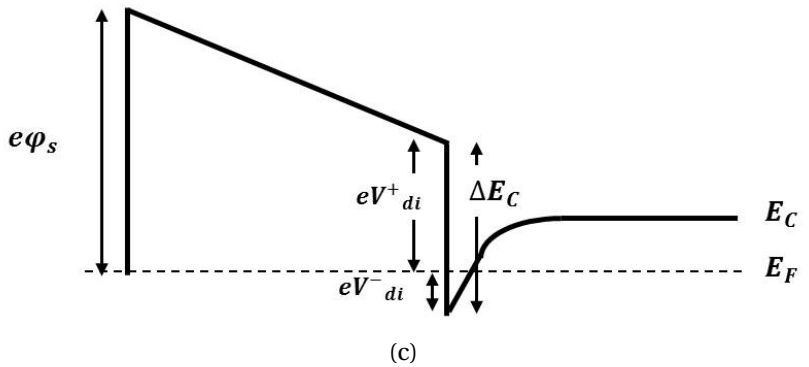
where $E_{gap(AlN)}$ = 6.1 eV, $E_{gap(GaN)}$ = 3.4 eV, x is the Al percentage and b is the bowing parameter, which is usually considered equals to 1.0 eV.



(a)



(b)



(c)

Figure 1.5 – (a) AlGaN/GaN heterostructure layer stack, (b) charge distribution and (c) conduction band diagram of the structure [5].

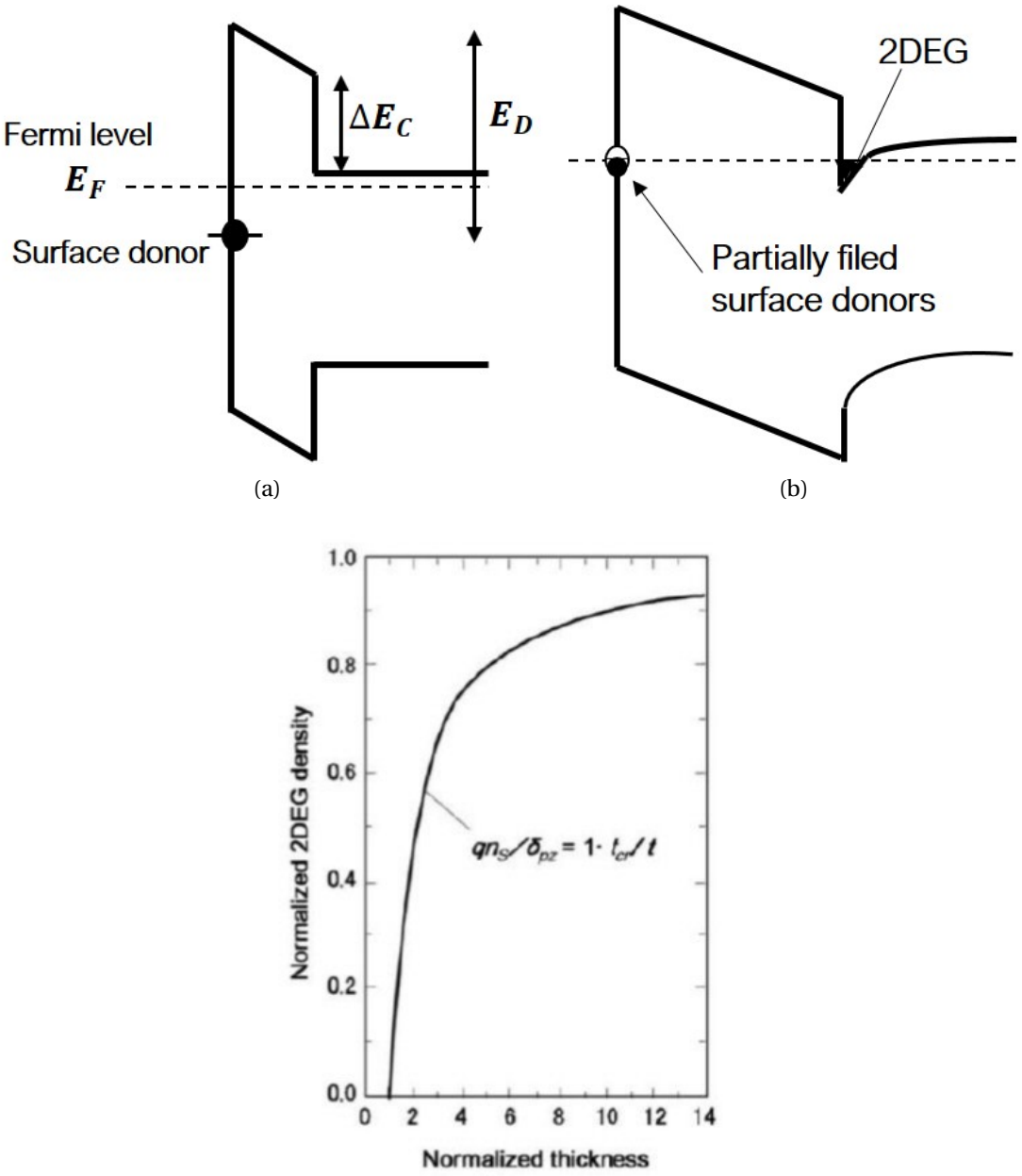


Figure 1.6 – Band diagram with (a) smaller and (b) bigger barrier thickness compared to the critical one necessary for the formation of the 2DEG, and (c) channel charge density as a function of the AlGaN thickness [6, 7].

1.3 The substrate

In fact, there is not a specific technique to grow the GaN crystals; sapphire (Al_2O_3), silicon carbide (SiC) and silicon (Si) are three typical substrates that are used for GaN. New processes (HVPE-hydride vapor phase epitaxy and high-pressure growth) allow the realization of a thick GaN layer that can be used without the carrier substrate. However, the process still needs the presence of an initial substrate to start the epitaxial deposition. In order to accommodate the mismatch between the two different crystal structures and to allow the growth of a high quality GaN-layer a nucleation layer, such as AlN or AlGaN, between the substrate and the GaN buffer is necessary

This section continues with a brief description of different substrates used for GaN technology. Table 1.2 summarises these substrates with their respective properties.

1. Sapphire: it has a ~15% lattice mismatch with GaN. Sapphire has a high resistivity, low cost and large area; in the other hand sapphire has a low thermal conductivity which results in a self-heating in the device. Therefore, sapphire is not suitable for power applications.

2. Silicon Carbide: it has a ~3% Lattice mismatch with GaN and a high thermal conductivity. Disadvantage of SiC is a high realization cost and a high dislocation density. For commercial devices SiC wafers are not available for diameter higher than 3 inches.

3. Silicon: it has a large lattice mismatch with GaN; very cheap and the processes for growth are well known with large diameter.

In addition, recent literatures report the hybrid substrates, witch can be used as alternative to the above mentioned substrates [9, 10]. These substrates are composed of a thick carrier from poly-crystalline silicon carbide as a carrier substrate and a thin layer of mono-crystalline by silicon or silicon carbide. They are two kind of composite substrates: SiCopSiC (SiC on polycrystalline SiC) and SiopSiC (Si on polycrystalline SiC). The advantage of these composite substrates are the high thermal conductivity ($3\ ^{W}/_{cmK}$), low cost and easy to produce [9, 10].

Table 1.2 – Properties of the different substrates used for GaN epitaxy [8].

Property	unit	Al_2O_3	6H-SiC	SI
symmetry	-	hexagonal	hexagonal	cubbic
Lattice constant a	Å	4.765	3.08	5.431
Lattice constant c	Å	12.982	15.117	-
Thermal conductivity	W/cmK	0.25	3.8	1.56
Lattice mismatch with GaN	%	15	3.1	17

1.4 Metal contacts

The metal semiconductor junction in AlGaN/GaN transistors are gate rectifying contact and source/drain ohmic contacts. In fact, the gate metal on top of the AlGaN barrier, with high work function (ϕ_m) are used to make a high junction barrier in order to reduce the gate leakage current [11]. Nichel ($Ni - \phi_m$ = 5.15 eV), platinum ($Pl - \phi_m$ = 5.65 eV) and palladium ($Pd - \phi_m$ = 5.12 eV) are the gate contacts which are usually used. Aluminium or gold are generally used to protect the contact from oxidation. Indeed, AlGaN/GaN transistors with these metal semiconductor junction contact have shown a lower gate leakage current and improved performances [12].

Ohmic contacts

Drain/source ohmic contacts are used to improve the contact conductivity. Titanium (Ti), gold (Au), aluminium (Al), molybdenum (Mo) are well known for drain and source ohmic contacts. Ti with low work function (ϕ_m = 4.3 eV), is a fundamental contact that combines with nitrogen atoms and creates a TiN layer which is in contact with the GaN-channel and allows the carriers passage [13, 14].

Gold is a proper metal for a low contact resistance [15]. However, the problem is the large diameter of GaN-on-Si processing and it is a contaminant element in Si-fabs. Therefore, the recent researches are focused on the new methods in order to get a new technology compatible with silicon processing [16].

1.5 Trapping effects

The trapping effect is one of the major concern in AlGaN/GaN HEMTs and plays a main role on the performance of these devices. Indeed, traps can cause a variation on the number of free carriers in the device, thus decrease their output power. This type of traps is generated from the lattice mismatch between the surfaces of the heterostructure during the deposition process. Moreover, traps can be related to a particular stress condition on the device such as a high electrical field and presence of hot-electrons in the channel, which will be discussed more in the following chapters. Possible traps level locations in the AlGaN/GaN HEMTs are shown in Figure 1.7. Below, the common practical methods to identify and locate the traps are summerized.

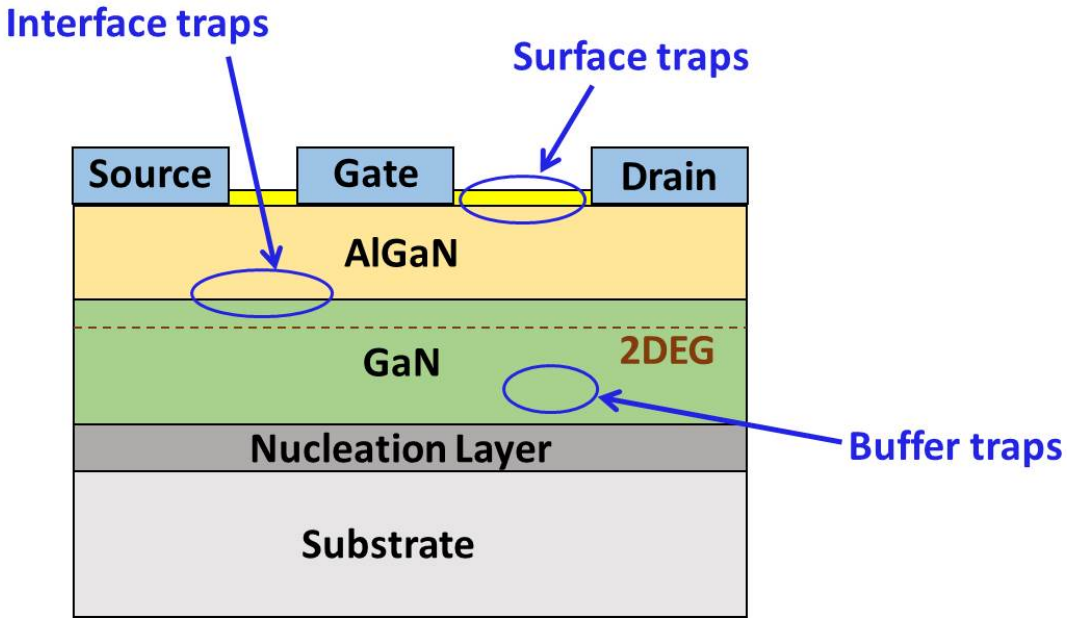


Figure 1.7 – Trapping-state in the AlGaN/GaN HEMT.

1.5.1 Current collapse

One of the practical ways to characterize the current collapse is pulsed drain-current versus drain- or gate-voltage measurements. This kind of measurement allows us to investigate the charge traps within the HEMT structure, by means of variation of current, on-resistance and threshold voltage. To this end, a schematic set up of the double pulse measurement is shown in Figure 1.8.

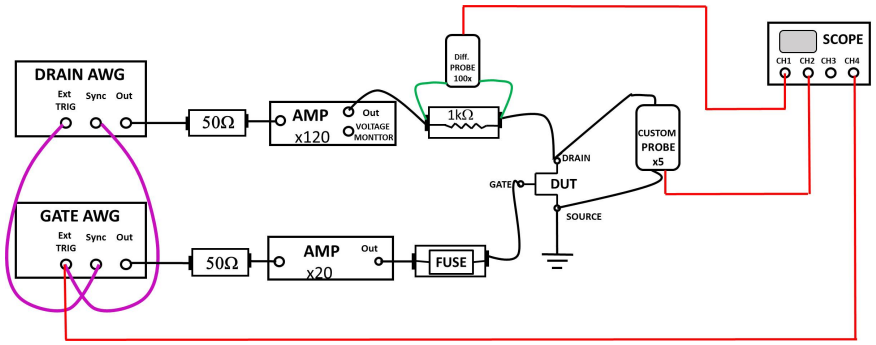


Figure 1.8 – Schematic of the set up for 600 V double pulse measurements.

On this measurement gate and drain are excited simultaneously with pulses at quiescent bias-point ($V_{G,Q}$;$V_{D,Q}$) for t = T_{OFF} = 100 μs–1 ms (depending on the device), and measurement bias-point ($V_{G,M}$;$V_{D,M}$) for t = T_{ON} = 1 μs. During the measurement, drain current, I_{DS}, is acquired as the potential drop across a sense resistor (see Figure 1.9). Typically, we measure the drain current at ($V_{G,Q}$; $V_{D,Q}$) = (0 V; 0 V) as a reference I_D-V_D, then sweep the voltage to the high off-state voltage and compare I_D-V_D with the reference curve to check the charge trapping effects and monitor the related degradation of electrical performance. On Figure 1.10, one can see an example of the charge trapping effect which induced the drain current collapse (I_{DS}) and change of $I_D V_G$.

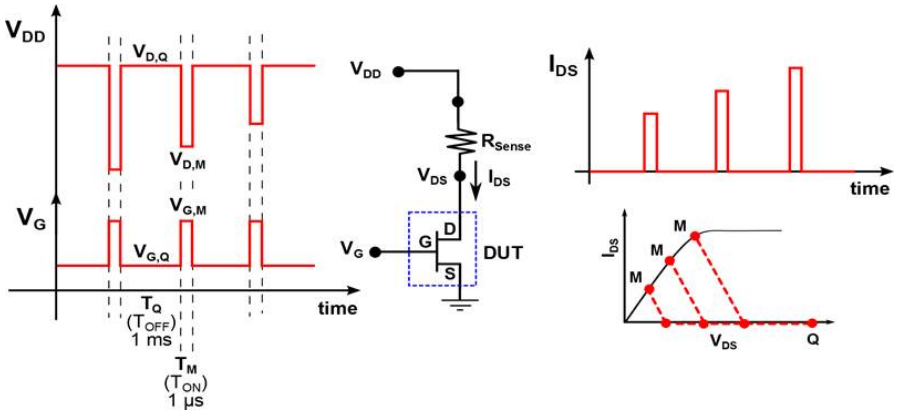
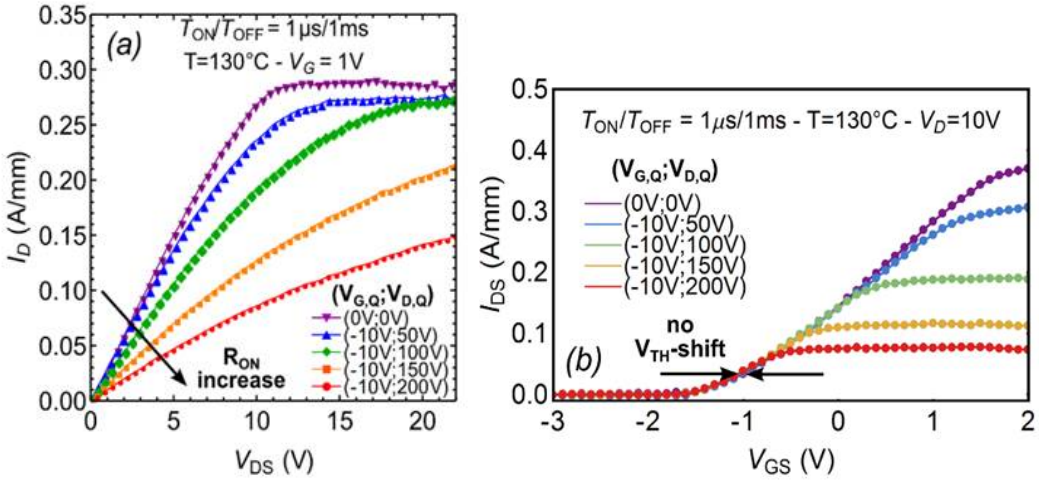


Figure 1.9 – Double pulse measurements, gate and drain are pulsed simultaneously from quiescent bias point to a measurement bias point and drain current collapse acquired as the potential drop across resistor [17].

The dynamic decrease of a drain current at a large gate-drain voltage could be related to the charge trapping in deep levels. In off-state the electric field between drain and



(a) (b)

Figure 1.10 – Double pulsed a) I_D-V_D b) I_D-V_G on a HEMT structure at multiple off-state quiescent biases, with increasing drain voltage [17].

gate captures the electron from the gate, forming a virtual-gate and depleting part of the channel. When the device is turned on, it is possible to observe a current drop. The depletion layer under the gate increases when the gate voltage is switched from positive to negative values. Davide Bisi *et al.* in [17] showed that the traps located in the region under the gate or in the gate drain access region can be separately identified by pulsed I_D-V_D and I_D-V_G characterization. Indeed, the net polarization charge and related 2DEG sheet charge density is affected by negative charge trapped under the gate of the devices with many defects in this region and thus result in a dynamical shift in the threshold voltage (V_{TH}). On the other hand, the presence of traps in the gate-drain access region determines a dynamic decrease in the transconductance peak, with no significant perturbation in V_{TH} (Figure 1.11). The emission efficiency of electrons from the wide gap interface states to the conduction band is very limited. The time constant of electron emission from interface states is given by Shockley-Read-Hall (SRH) statistics as (1.4).

$$\tau = \frac{1}{v_{th}\sigma_{th}N_C} exp(\frac{E_T}{kT}), \tag{1.4}$$

where E_T, v_{th} and N_C are the interface state energy, the electron thermal velocity, and

the density of states at the conduction band, respectively [18].

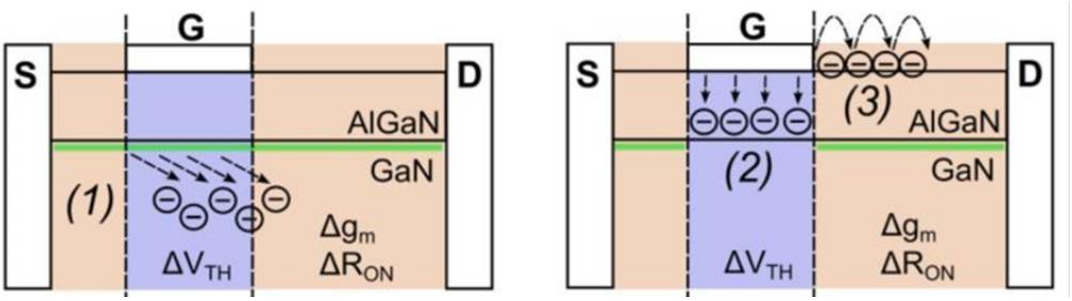


Figure 1.11 – Possible trapping mechanisms and their influence on electrical parameters in (a) semi-ON-state and (b) OFF-state bias operating points [17].

For the trapping phenomena, the trapping rate, c_n, depends on the electron concentration n. The activation energy, E_a, is the sum of ΔE_a and the distance of the Fermi level from the conduction band. But as shown by [17], the leakage current could influence on the electron concentration.

From the equation (1.4):

$$\frac{1}{\tau_n} = c_n = \upsilon_{th}\sigma_{th}N_C exp(-\frac{E_T}{kT}), \tag{1.5}$$

$$ln(\tau) = E_T\frac{q}{kT} + ln(\frac{1}{\sigma_{th}N_C}), \tag{1.6}$$

$$y = E_T x + b \tag{1.7}$$

The activation energy, $E_T(eV)$, is the slope of the line in the Arrhenius plot (look at Figure 1.12).

1.5.2 Drain Current Transient Spectroscopy

Drain Current Transient spectroscopy (DCT) has been widely employed to identify the deep level traps. The set up for this measurement is the same as the one of the

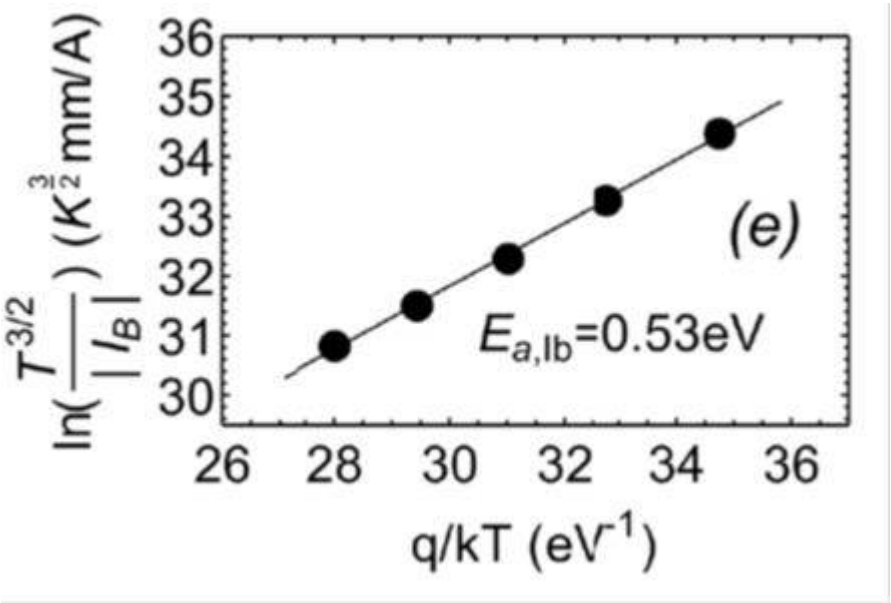


Figure 1.12 – Arrhenius plot with apparent activation energies (EA)

double pulsed shown in Figure 1.8. The device under test is subjected to a trapping phase which can be described as follow: the biasing voltage of the device ($V_{G,F}$; $V_{D,F}$), for a period of 100 s, is kept in the off-state or semi-on-state. Following this phase, the device is biased in a low-field, low-power on-state ($V_{G,M}$; $V_{D,M}$) which typically is in the linear or the saturation region close to the knee voltage in order to allow the acquisition of the drain-current response and the analysis of the related time-constant spectrum.

Although the procedure of this technique seems straight forward, in fact the choice of the parameters within this measurement as well as the analysis method of the transient results have direct and strong influence on the reliability of the outcome of this technique.

One example of the de-trapping transients at different trapping conditions is shown in Figure 1.13. It is worth to mention that in order to find the location of the trapping level, it is helpful to carry out the measurement at different temperature and look for the time dependency in the results. For your view, an example of a thermally activated trapping effect is shown in Figure 1.14.

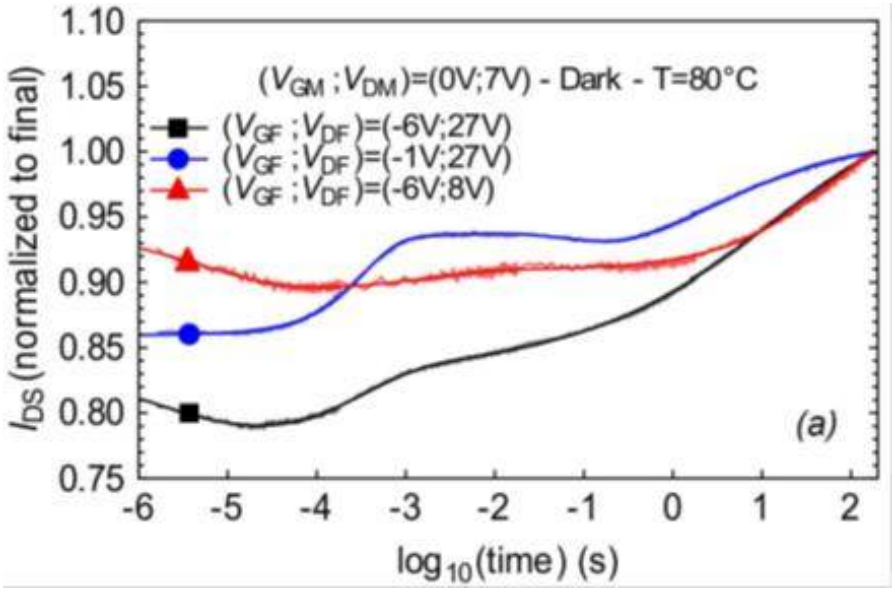


Figure 1.13 – Drain current transients recorded after different trapping conditions [17].

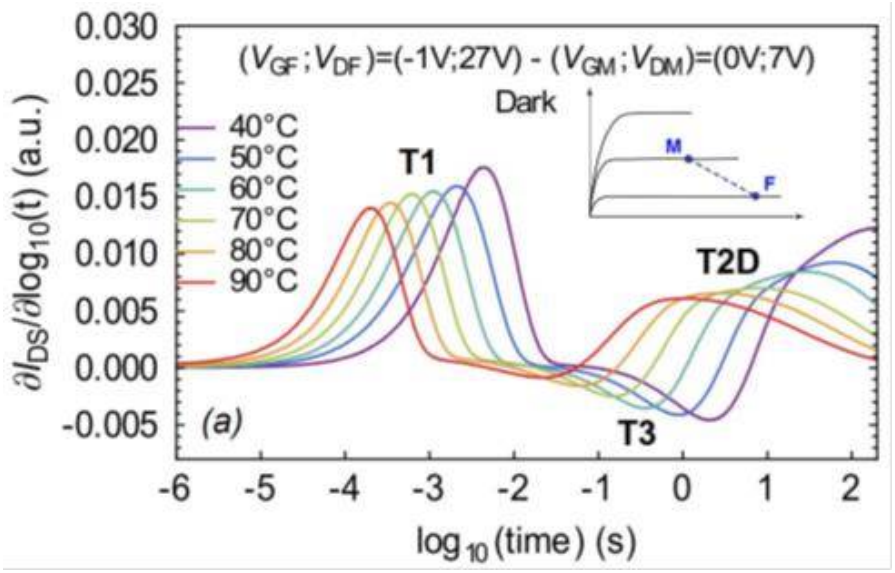


Figure 1.14 – Thermally activated trapping effects [17].

1.6 GaN HEMT Reliability

As discussed before, GaN-based devices are suitable for high-current and high-voltage bias applications. Therefore, studying the reliability of these devices become very important. Recent literatures on the reliability of the AlGaN/GaN transistors categorise different degradation mechanisms on AlGaN/GaN. Figure 1.15 shows the cross section

of a GaN HEMT along with the possible failure mechanisms and their corresponding location on the device.

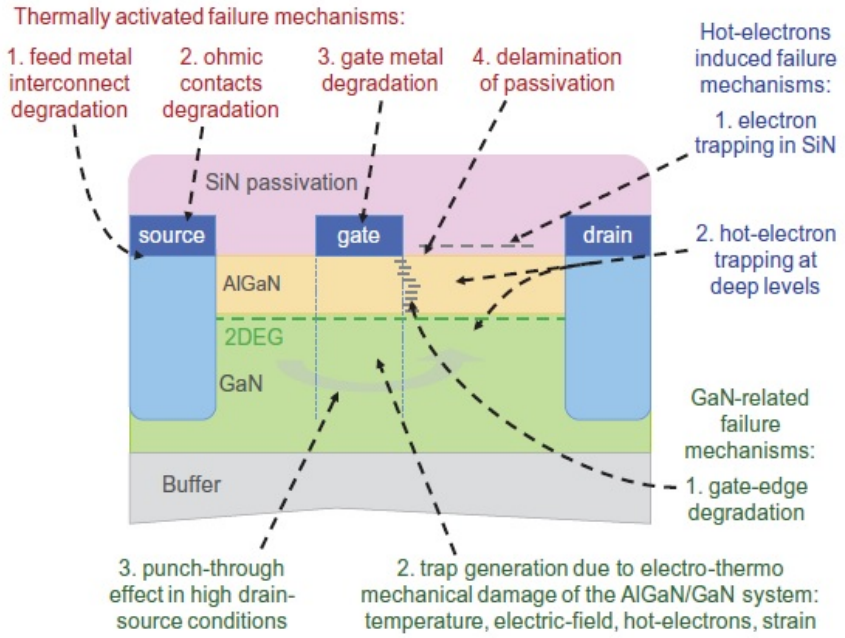


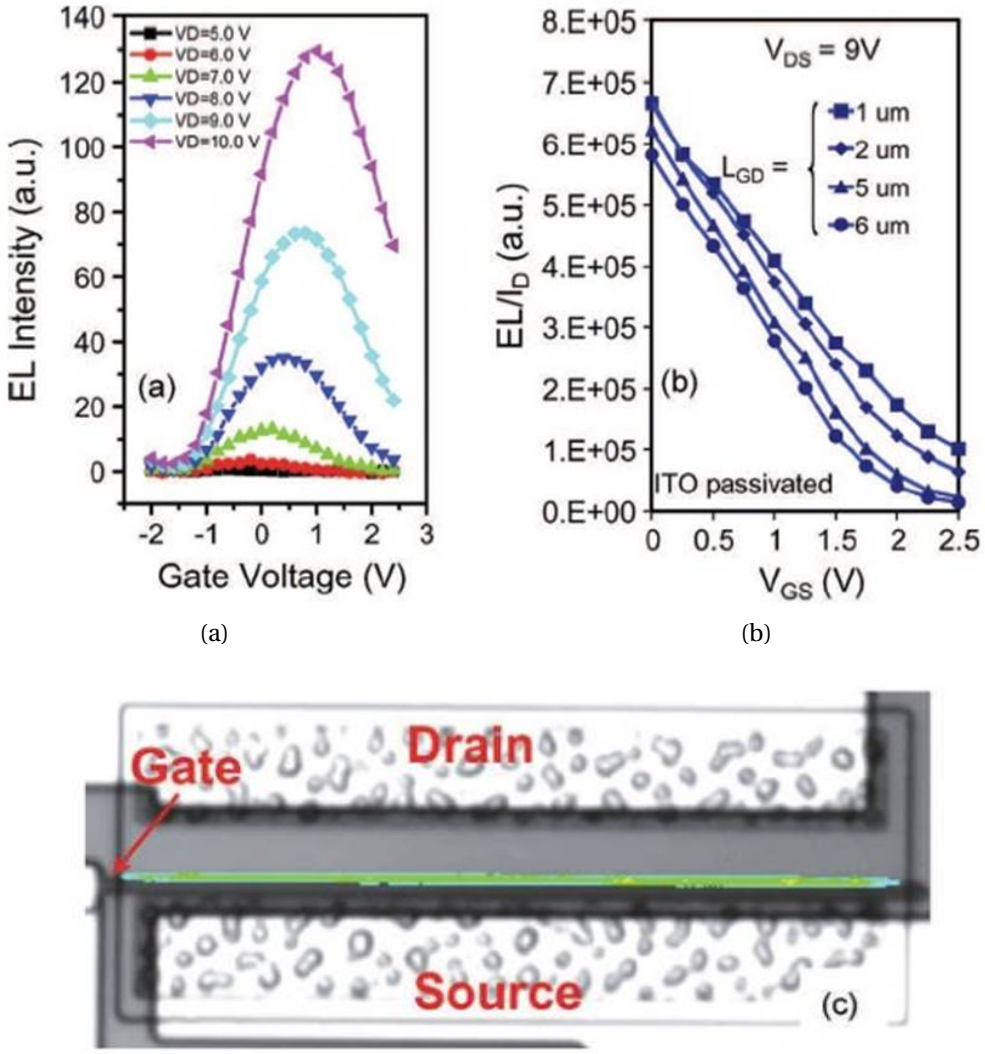
Figure 1.15 – Schematic figure representing the main mechanisms that can affect the reliability of GaN-based HEMTs [19].

From the summary of the degradation mechanism in GaN-based HEMTs shown in Figure 1.15 the following two degradations are more common than the others.

- Degradation of ohmic contacts: The main degradation mechanisms is the inter-diffusion of the metallic elements from the electrode to the semiconductor material. This type of degradation mechanisms cause an increase on the contact resistance as well as a crack in the passivation layer.

- Hot-electron Degradation: Another well known failure mechanisms of GaN-based devices. When the GaN HEMTs devices is biased at high drain-source voltages, there is electron injection to the gate from channel due to the high electric field which cause a degradation in the device [20]. Indeed, in this case, the hot-electron energy can make a relaxation on the strained AlGaN layer [21]. The hot-electrons effect can be identified by the electroluminescence

measurement as shown in Figure 1.16. In the next chapter the hot-electron failure will be discussed more in details.



(a) (b)

(c)

Figure 1.16 – a) Intensity of the EL signal as a function of gate drain voltage; b) intensity as a function of the gate voltage level for samples with different gate-drain spacing; c) false colour image reporting the distribution of EL along the gate [22].

Furthermore, recently few studies identify a particular degradation of GaN devices in off-state bias. This failure is observed with an increase of the gate leakage current and charge trapping and a decrease of I_D as well as an increase in the resistance of access

region. One hypothesis explained by Joh *et al.* and Del Alamo *et al.* [23,24] is that an increase of the strain in AlGaN/GaN, due to the high electric field in the gate-drain region, makes a crystallographic defect. Therefore, the high R_D could be related to the high electron concentration in the access region (see Figure 1.17).

Another observed degradation is an increase in the gate leakage current due to a gate bias constant stress [25,26]. Moreover, time to failure is also reported, in the literature as a kind of figure of merit of the device's life time, while applying an increasing voltage to the gate which increases the defect generation process along the gate's edges.

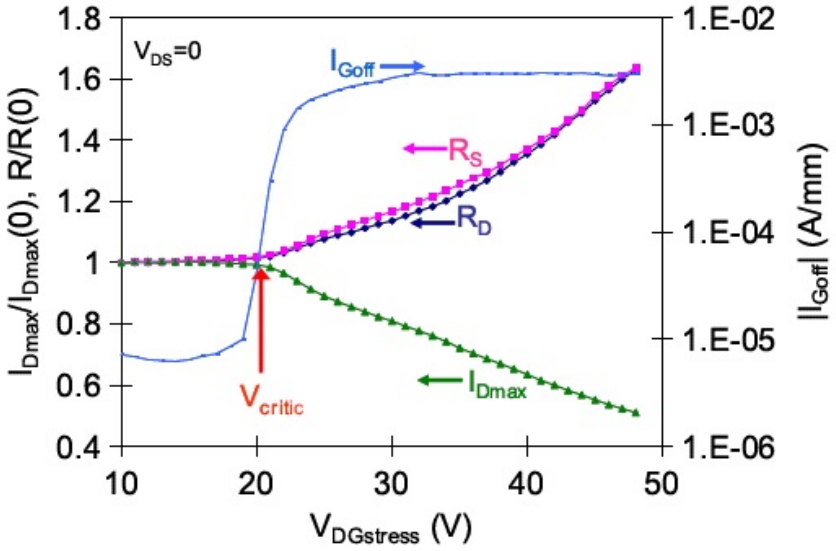


Figure 1.17 – Typical results of a reverse-bias step stress. We can see the change on I_{Dmax}, R_D and R_S, while the sudden increase of the gate leakage defines the critical voltage [23].

Finally, it is clear that the reliability of GaN-based HEMT is still a big issue and requires more efforts in order to improve its performance and prepare it to satisfy the market demand.

2 Field and Hot Electron-Induced Degradation in GaN-based power MIS-HEMTs

As discussed before the presence of traps is a big issue that increases the dynamic on resistance and has a consequence on the performance of GaN-based metal-insulator-semiconductor (MIS) HEMTs designed for power application.

On this chapter we investigate the degradation of AlGaN/GaN MIS-HEMTs submitted to the gate step-stress experiments and demonstrate the existence of field- and hot-electron induced in these devices. For a device that is submitted to the gate-step stress with a high V_{DS}>50 V, four different regimes can be identified:

1. For V_{GS}<-10 V, no significant degradation is observed, since the devices are in the off-state;

2. For -10 V<V_{GS}<0 V, hot electrons flow through the channel, as demonstrated by the (measurable) electroluminescence signal. These hot electrons can be trapped within the device structure, inducing an increase in the threshold voltage.

3. For V_{GS}>0 V, the density of hot electrons is significantly reduced, due to the increased interface scattering and device temperature. As a consequence, EL signal drops to zero, and the electrons trapped during phase (2) are de-trapped back to the channel, where they are attracted by the high 2DEG potential.

4. Finally, for V_{GS}>5 V, a significant increase in threshold voltage is detected. This effect is observed only for high positive voltages, i.e. when a significant leakage

current flows through the gate. Such gradual degradation is ascribed to the injection of electrons from the 2DEG to the gate insulator, which is a field-driven effect.

These results were obtained by means of the combined electrical and optical characterization carried out at different voltages during the step stress. The measurements are carried out for both the stress and the recovery.

2.1 Recent advancements in GaN technology

Recently, the research in the field of GaN-based power HEMTs has shown impressive advancements. As such, Moens *et al.* in [27], have demonstrated insulated-gate transistors with R_{on}<10 mΩ (shown in Figure 2.1) and 650 V breakdown voltage that are fully current collapse free over a complete range of voltage and temperature. In addition, with increasing the buffer layer (GaN) they have achieved a leakage current of ~100 nA for a GaN power device up to 1.2 kV. Thus, cleared the way for the fabrication of reliable and high performance GaN transistors.

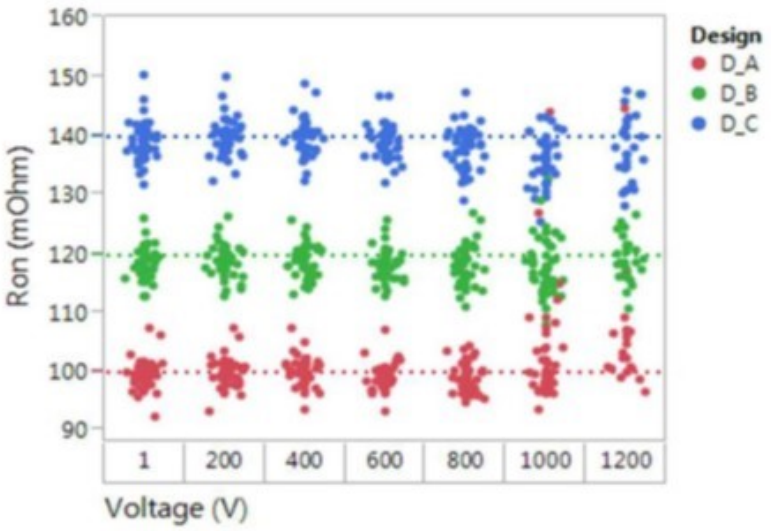


Figure 2.1 – R_{on} measured by forcing 10 A, up to 1.2 kV. Data for three different device layouts [27].

Figure 2.2 shows a maximum dynamic R_{on}~20% at a low V_{DS} (~100 V), but a negative dynamic R_{on} at V_{DS} above ~400-500 V. The results of the usual double pulse measure-

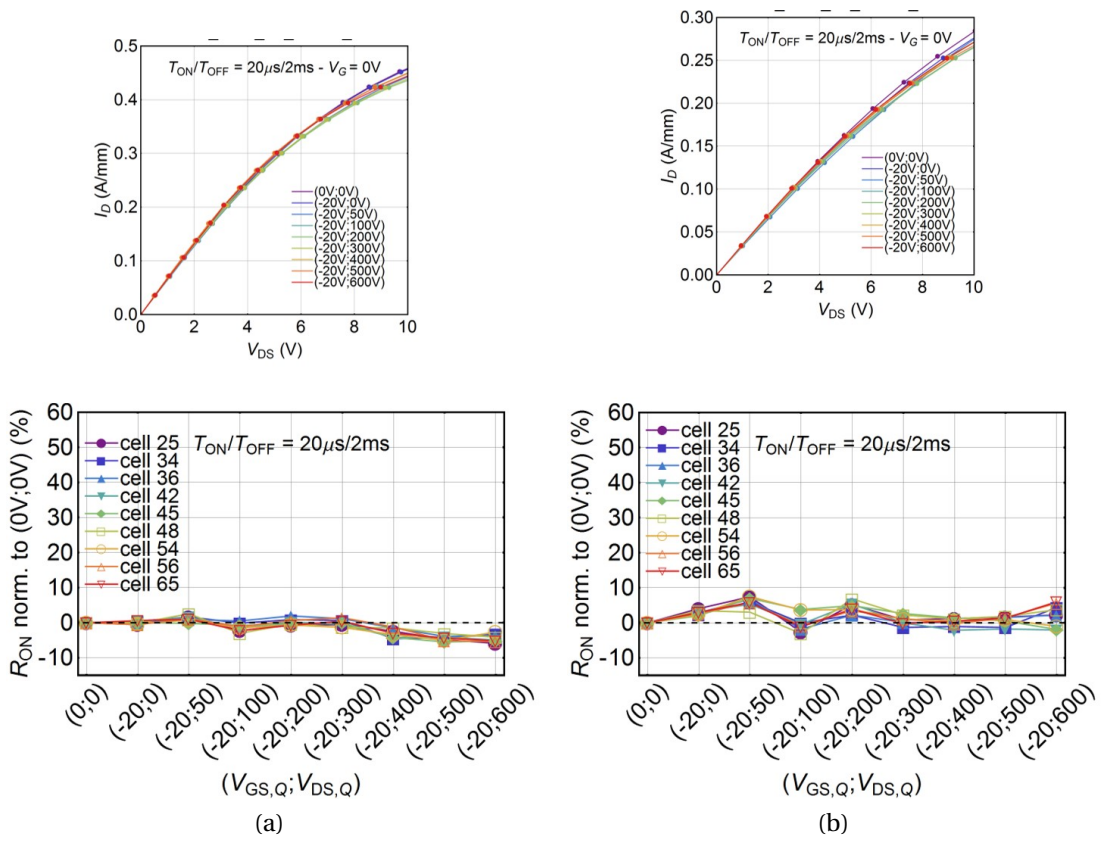


Figure 2.2 – Double pulsed I-V characteristics up to V_{ds}=600 V. (a) room temperature, (b) T=150°C. t_{off}=2 ms, t_{on}=20 μ s [27].

ment at room and high temperature (T=150°C) presented in Figure 2.2 are indicating almost no current collapse at drain current and the variation of dynamic R_{on} is almost flat.

For a massive adoption of GaN transistors, it is important to study the reliability and stability of these devices which, during operation, may cross different V_{GS}/V_{DS} ranges [19]. The device is under stress during the hard switching from the off-state to the on-state. In particular, during a hard-switching transition (see the example in Figure 2.3), the devices may be simultaneously subjected to a high drain voltage between drain and source and low current through the transistor. In the on-state condition the drain voltage drop rapidly to zero while the drain current increases, thus resulting in significant field- and hot-electron and trapping effects. The traps can be located under the gate (shift of the V_{TH}) and in the access region (decrease of the transconductance peak). Moreover, there is a need for elaborating the operation in

semi-on since it has not been described so far in the previous works.

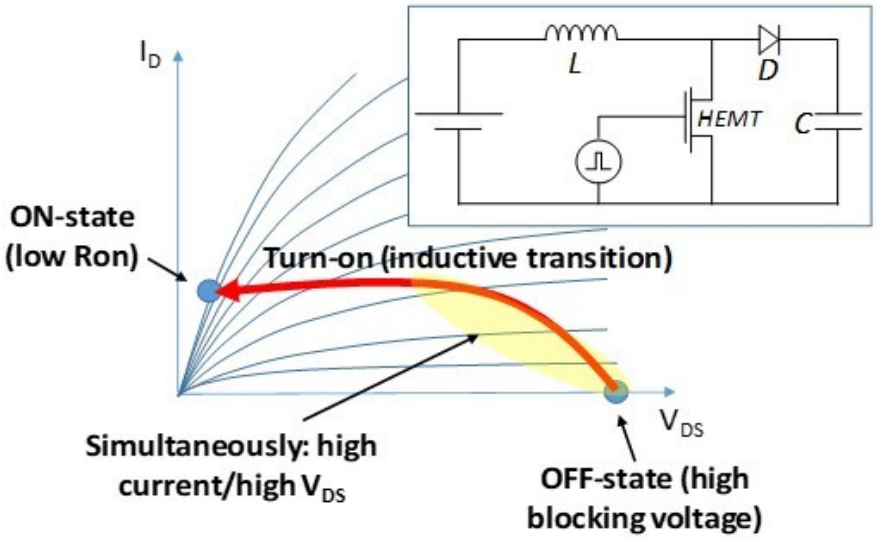


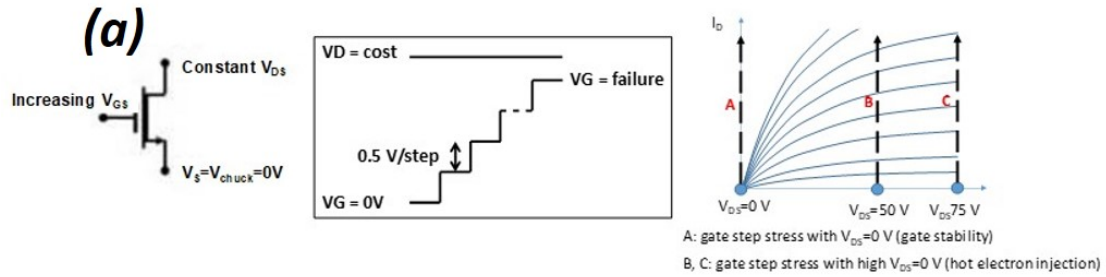
Figure 2.3 – Schematic representation of a hard-switching transition in a boost power converter. During the transition, high electric field and a non-negligible drain current are simultaneously present [19].

For these reason in this chapter the semi-on state degradation processes of GaN-based MIS-HEMTs that are submitted to the gate step-stress up to the failure of the device, as summarized in Figure 2.4, are presented. To clarify the impact of field- and hot-electron dependent degradation processes, the step-stresses were carried out at different drain voltage levels. The physical properties of the devices were investigated by combined electrical characterization and electroluminescence (EL) measurements. It is demonstrated that:

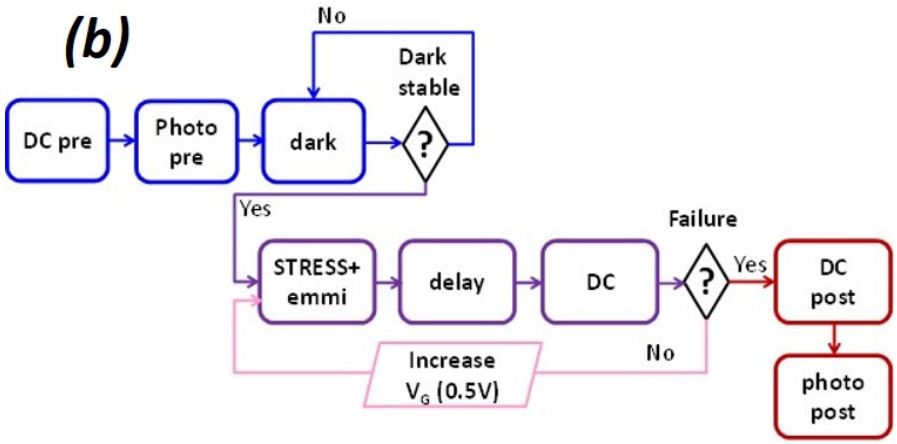
1. When the devices are submitted to the stress with V_{DS}= 0 V, degradation occurs due to the high electric field across the gate dielectric. This promotes the injection of electrons from the 2DEG to the insulator (resulting in an increase of V_{th}) and results in the breakdown of the SiN (for very high gate voltages, >35 V).

2. When a high drain bias (V_{DS}>50 V) is applied during the step-stress tests, hot electrons are present, as demonstrated by the high electroluminescence signal [19]. This results in a further charge trapping process, since hot electrons can be trapped in the AlGaN/SiN stack [28]. The resulting V_{th} shift is non-monotonic (with increasing V_{GS}) owing to the fact that the density of hot electrons drops

for positive V_{GS} values. This drop itself is due to the increase in the interface scattering and device temperature.



(a)



(b)

Figure 2.4 – a) Summary of the adopted stress conditions. A step-stress is applied to the gate (120 s/step, 0.5 V/step), with different drain voltages (V_{DS}= 0 V, no hot electrons, V_{DS}= 50 V, 75 V, hot electron injection). The stress conditions used within this experiment allow to explore regions of the I_D-V_{DS} plane that are not explored by means of conventional HTRB/HTGB stress tests, thus allowing to study the degradation processes related to hot-electrons. b) Measurement setup (routine) of the step stress up to failure.

2.2 Experimental details

The study was carried out on AlGaN/GaN MIS-HEMTs with the gate width of 200 μ m and L_{GD} = 16 μ m, designed for 650 V operations. The gate dielectric is in-situ SiN as show in the Figure 2.5. The device is provided by ON-semiconductor Belgium. Before the execution of the stress tests, a detailed characterization of the hot-electron

luminescence was carried out by means of EL test (Figure 2.2). Two different stress regimes degradation processes of GaN MIS-HEMTs, submitted to gate step stress, are discussed here:

1. High electric field: forward gate stress (V_{DS}=0 V)
2. Hot electrons: semi-on state stress (V_{DS}>50 V) which will discuss later.

The sequence of the measurement is based on the 1) DC characterization 2) photo by means of CCD camera (described bellow) 3) dark luminescence to count the photons of the dark room a kind of calibration till reach to the stable value 4) stress+emmi 5) delay of 10 sec 6) DC characterization 7) increase of the gate stress voltage in step of 0.5 V up to the failure. If the device failed there is a photo by CCD camera to observe the photo luminescence in the failure point (described in Figure 2.4b).

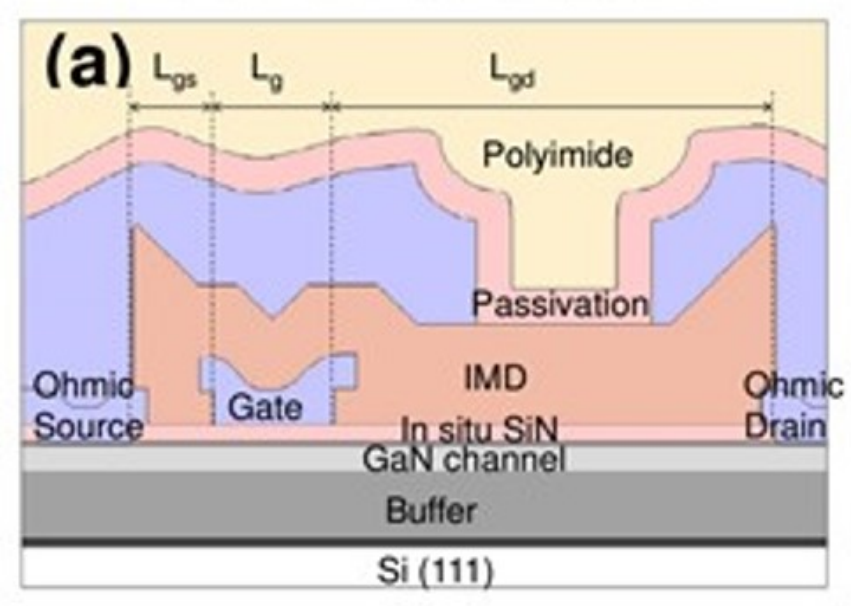


Figure 2.5 – GaN device structure.

2.2.1 Electroluminescence analysis

Electroluminescence analysis is one of the useful method to obtain information concerning the reliability of the device. In fact, the intensity of the EL signal could

be related to the amount of energy of hot electron which can be responsible for the degradation of GaN HEMTs. Hot electron effects are evaluated by means of EL measurements, the measurement system is based on an Electron Multiplying Charge Coupled Device (CCD) camera with the 20x lens, mounted on a microscope. Thanks to the Electron Multiplying technology, the device is characterized by a very high sensitivity. Moreover, during the measurement in order to reduce the background noise the temperature of the camera is kept around -20°C.

The electroluminescence analysis on the GaN-HEMTs and its results can be explained by means of hot-electrons: when there is a high electric field in the gate-drain, the carriers in the 2DEG that are accelerated by the electric field (Bremsstrahlung effect), hot-electrons, loose their energy in the channel. This energy is emitted by the transistor as a luminescence signal. If the signal emitted from the device is strong enough, the CCD camera could measure it by counting the number of emitted photons. As a result the presence of hot-electrons can be detected. Figure 2.6 shows the intensity of the EL signal on the gate overdrive for different drain voltage levels measured on one of the analysed samples submitted to the stress at V_{DS}= 50 V. When the gate is increased to higher values beyond the pinch-off, the concentration of electrons in the channel and the drain current increases, thus leading to a more scattering phenomena and intra-band transition; which enhance the emission of the photons. On the other hand, as the gate voltage is increased, the gate-to-drain electric field decreases: electrons therefore become less energetic, and the intensity of the luminescence signal decreases. In the other hand, the EL intensity starts to increase when the gate voltage is higher than the pinch off voltage (V_{GS}> -12 V). With the increase of the electrons in the channel by increasing the gate voltage, the electric field of the gate drain decreases, in the same time the average energy of the electrons in the channel decreases and consequently the EL signal increases [28, 29]. The EL signal is maximum at the edge of the gate toward the drain, where the electric field peaks. The EL analysis is a useful technique to characterise the presence of hot-electron in GaN-HEMTs to verify the role of hot-electron in the degradation mechanism [30].

The results (in Figure 2.7) indicate that a significant EL signal is emitted by the devices. As can be noticed that the intensity of the signal shows a monotonic increase with increasing V_{DS} (Figure 2.7a), and a non-monotonic increase with increasing V_{GS} (as

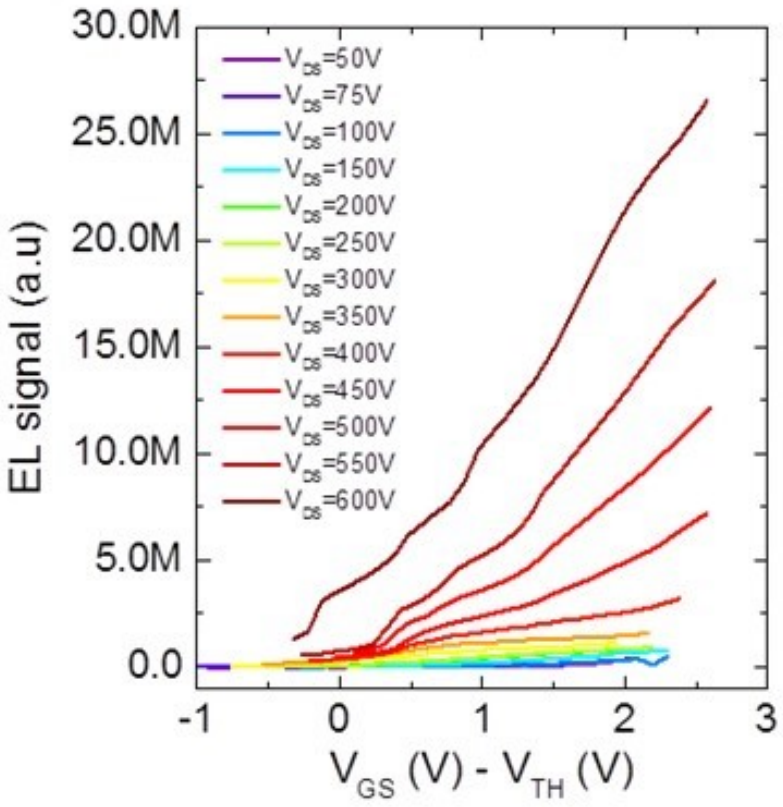
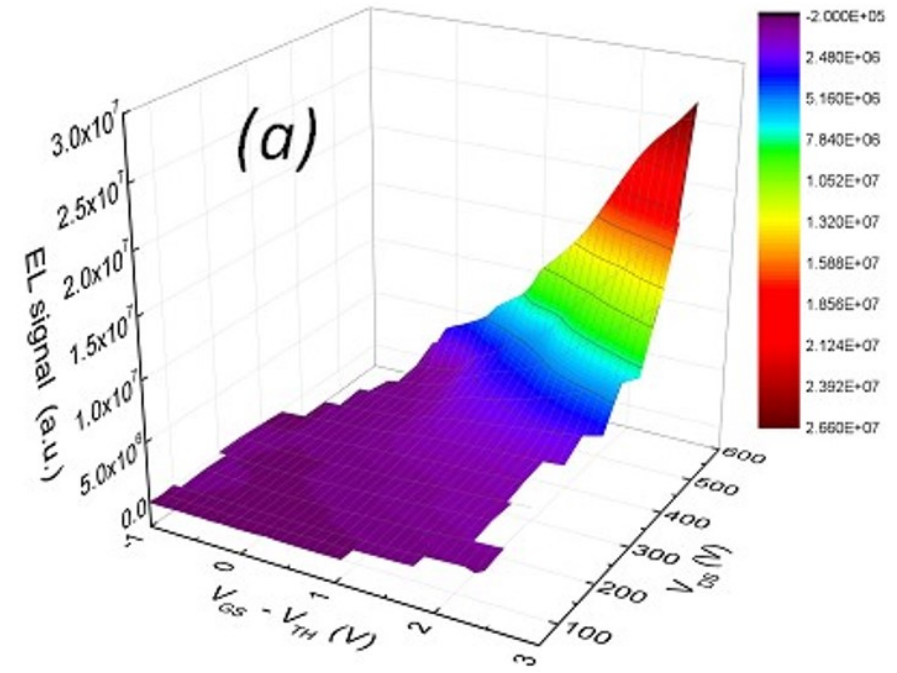
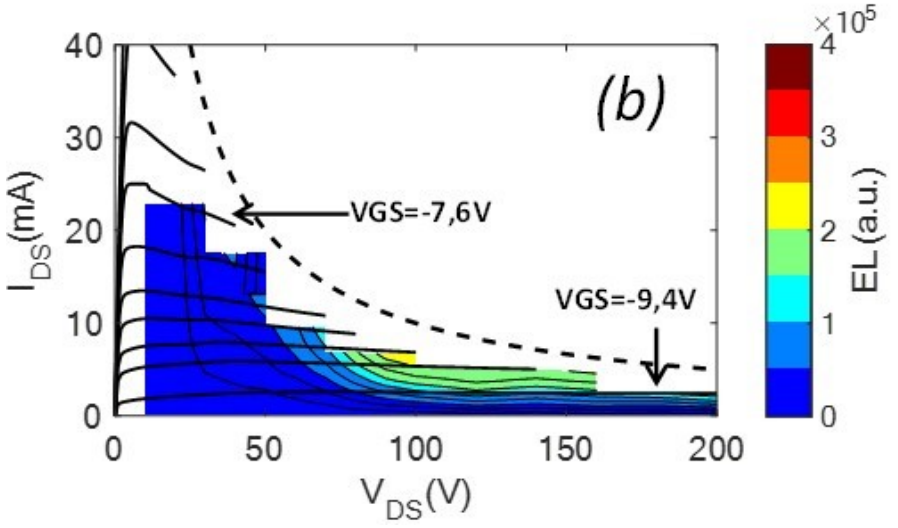


Figure 2.6 – EL intensity versus gate voltage curves measured at different drain voltages on a GaN-on-Si HEMT.

described in the following).



(a)

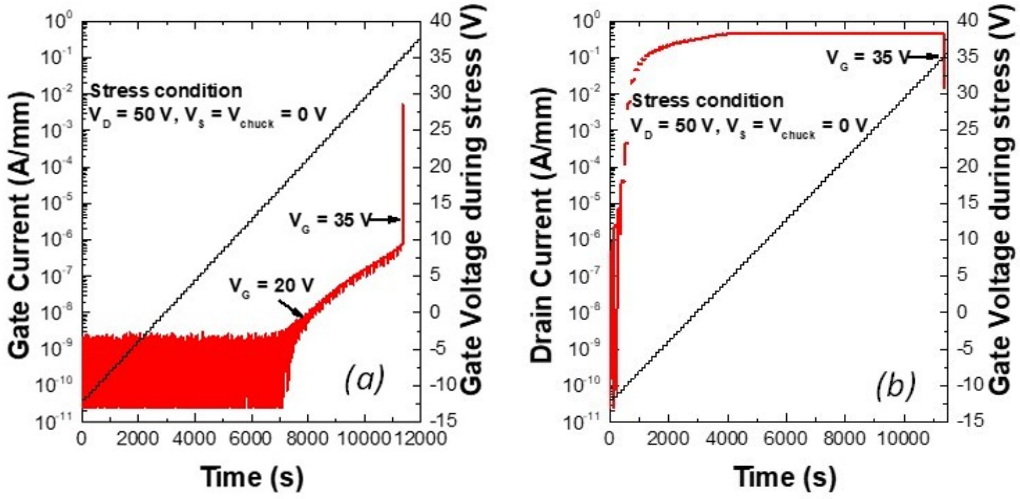


(b)

Figure 2.7 – a) EL intensity versus gate voltage overdrive at different drain voltage on a GaN HEMT, (b) Correlation between the EL intensity and the output curve measured at corresponding bias levels [31].

2.2.2 Degradation mechanism Step Stress

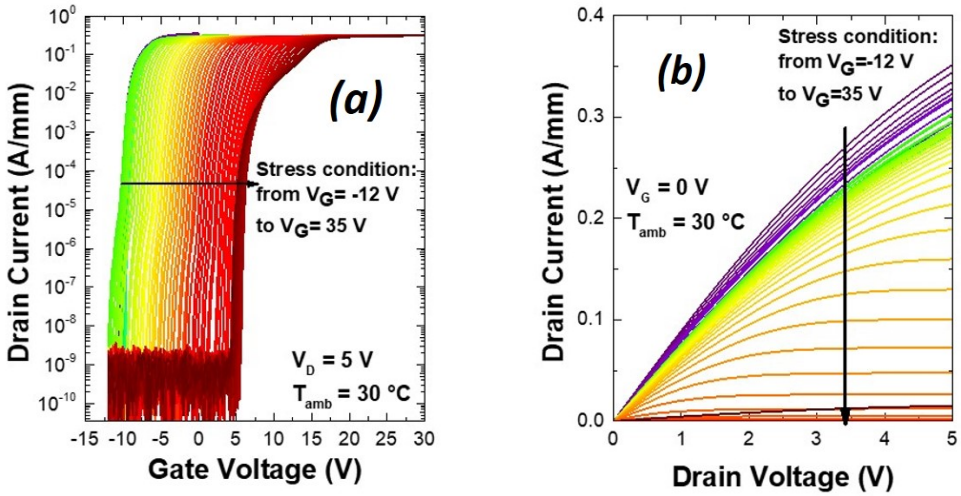
After this preliminary characterization, the devices were submitted to step-stress experiments (Figure 2.4). The gate voltage was increased from -12 V up to the failure of the device, at a step of 0.5 V (Bias time for each step = 120 s, texposure = 25 s, tacq = 30 s, T= 30°C). Several identical devices were stressed by using different drain voltages, between 0 V and 75 V, in order to promote the hot-electron degradation processes. At each stage of the stress tests, device properties were analyzed by means of DC and EL characterization. Figure 2.8 reports the gate and drain current measured on one of the devices submitted to the gate-step stress with V_{DS}= 50 V. The staircase indicates the gate voltage that was applied to the devices during stress. As can be noticed (Figure 2.8a), a significant gate current is measurable only for V_{GS}>20 V, due to the presence of the thick gate insulator. As shown in Figure 2.8b, a relatively high drain current is present during the stress, due to the high drain bias. For a gate voltage below 20 V, the gate leakage is very small and indeed below the instrument noise level. From V_{GS}=20 V, the gate leakage increases by three orders of magnitude till the breakdown of the gate at V_{GS}=35 V.



(a) (b)

Figure 2.8 – (a) Gate and (b) drain current versus gate voltage during a step-stress experiment carried out with V_{DS}=50 V, increasing V_{GS}.

Figure 2.9 reports the I_D-V_{GS} and I_D-V_{DS} curves measured after each stage of the step-



(a) (b)

Figure 2.9 – (a) Gate current versus gate voltage, the shift of the pinch-off voltage variation. (b). Drain current versus drain voltage, reduction of the on resistance.

stress experiment, each colour indicates one step measurement during the stress. As can be noticed, a shift in pinch-off voltage and increase in on-resistance are observed during stress. A more quantitative description is given by the plots in Figure 2.11, which reports the variation of V_{th} during step-stress at different V_{DS} levels. In Figure 2.10 the transconductance at V_{DS} = 5 V after each step of stress from V_G= -12 V to failure is shown.

2.2.3 Field-dependent degradation of devices stressed at low V_{DS}

In order to analyze both low- and high-field applied to the devices, the step stress measurements have been carried out at different drain voltages. The devices stressed with low V_{DS} (0 V, 2 V) only shows a small variation of V_{th} when the gate stress voltage is <5 V. For V_{GS}>5 V, a significant increase in threshold voltage is observed (pink and orange lines in Figure 2.11a). This process can be explained as follows: when the applied gate voltage is >5 V, the 2DEG is formed, and most of the field drops across the gate insulator [32]. As a consequence, electrons can be injected from the 2DEG to the SiN insulator, thus being trapped there. This results in a significant shift in V_{th}

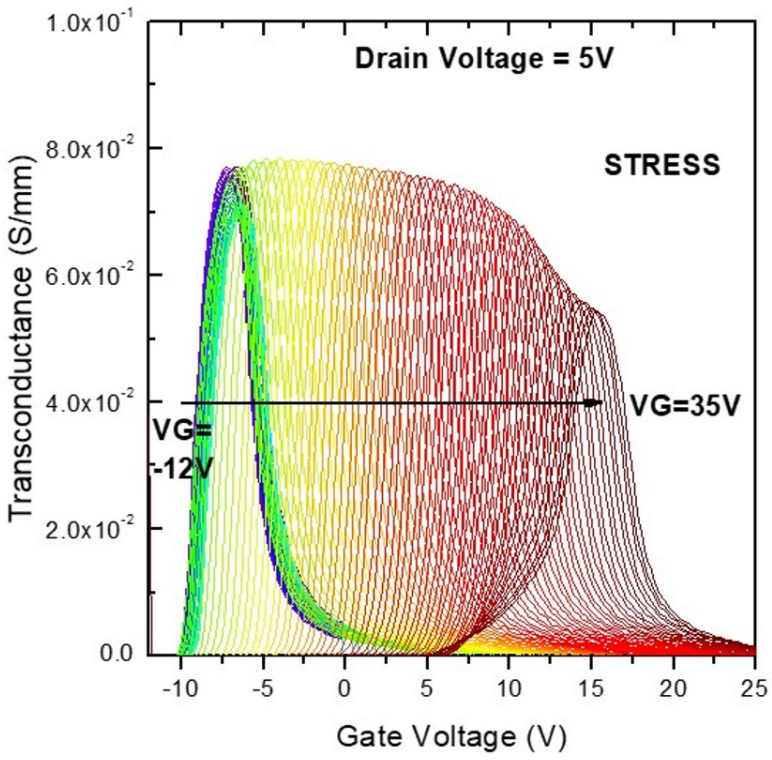
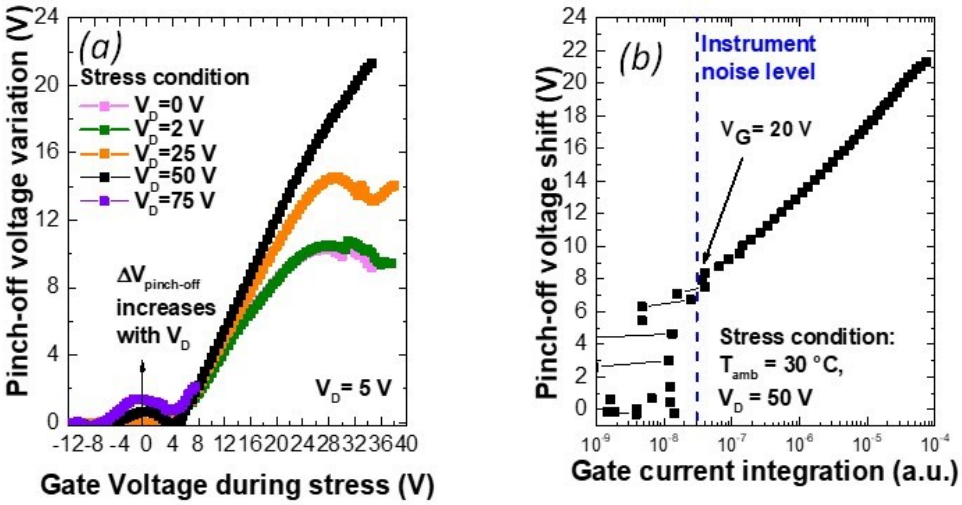


Figure 2.10 – Shift of the transconductance versus gate voltage after each step.

towards more positive values. The role of gate leakage in the observed degradation process is confirmed by the correlation between the increase in pinch-off voltage and the gate leakage current injected during the stress [33] (Figure 2.11b). Catastrophic failure is reached for V_{GS}=35 V, due to the breakdown of the SiN.

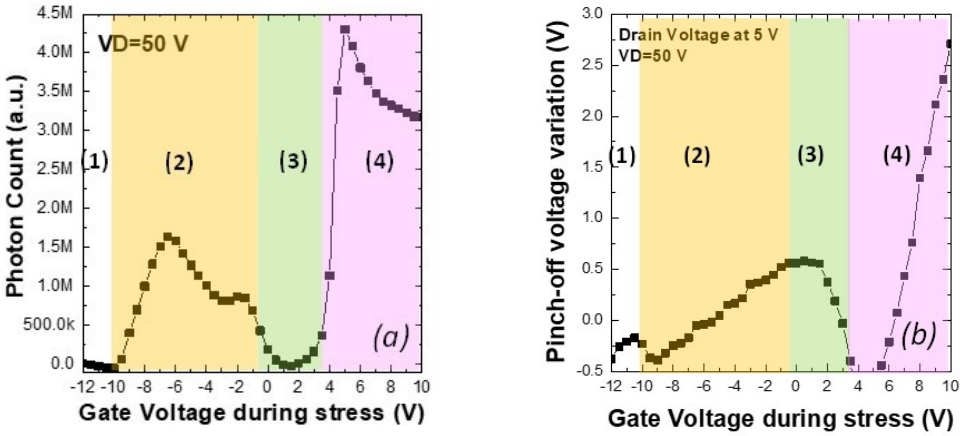
2.2.4 Hot-electron degradation of devices stressed at high V_{DS}

Figure 2.12a indicates that the samples stressed at high V_{DS} (>50 V) show an additional, non-monotonic, increase in threshold voltage when they are stressed with V_{GS} in the range between -10 V and 0 V. However, a monotonic shift is obsereved at high-fields, except for V_{DS} = 75 V due to the device failure, for low V_G values. The threshold voltage is calculated as the linear interpolation with the x-axis of the curve tangent to the I_D-V_G. What is the physical origin of this effect?



(a) (b)

Figure 2.11 – (a) Pinch-off voltage variation with increasing the gate voltage. (b) dependence of the pinch-off voltage shift and gate current. On the horizontal axis the integral of gate current during a 2 minutes stress step is reported.



(a) (b)

Figure 2.12 – (a) EL signal measured on a device submitted to step-stress with V_{DS}=50 V, increasing V_{GS}. (b) variation of V_{th} measured during the step-stress of the same device.

To clarify this aspect, we report in Figure 2.12a a more detailed summary of the results obtained by step-stressing one of the samples at V_{DS}=50 V, with increasing V_{GS}. Four different regimes are identified:

1. For V_{GS}< -10 V, neither light emission nor pinch-off voltage variations are detected. Gate and drain current are too low to have any impact on device characteristics.

2. For -10 V<V_{GS}<0 V a significant EL signal is measured. The EL vs V_{GS} curve has a bell-shape (Figure 2.12a), [19, 32]: above threshold, EL increases due to the increasing number of electrons in the channel. For higher V_{GS} levels (0 V<V_{GS}<6 V) the EL decreases due to the increased interface scattering (hot electrons are attracted closer to the interface) and device temperature (higher temperatures result in a stronger lattice scattering, reduction of the mean-free path, and decrease in the average energy of hot electrons). In this voltage range, an increase in V_{th} is observed (phase 2 in Figure 2.12a): when the density of hot electrons (and the EL signal) increases, these hot electrons can be injected towards the AlGaN/SiN stack [24], thus being trapped there (see the schematic in Figure 2.13a) [34].

3. For 0 V<V_{GS}<3 V, no hot electron luminescence is detected (Figure 2.12a), indicating that the average electron energy has significantly decreased due to the interface scattering and high device temperature. The 2DEG is still at high voltage (50 V), and the electrons trapped in the AlGaN/SiN stack are attracted back towards the channel (see the schematic in Figure 2.8b). This induces a shift of V_{th} towards more negative values (phase 3 in Figure 2.12b).

4. Finally, for V_{GS}>5 V, the electric field over the SiN dielectrics significantly increases, and – as a consequence – electrons are injected from the 2DEG towards the gate metal (see the schematic in Figure 2.12b) [32]. This induces a significant increase in the pinch-off voltage and the device luminescence [35] (phase 4 in Figure 2.12a and Figure 2.12b, the EL data above 5 V are saturated).

As mentioned before, EL microscopy can be very useful in detecting localized breakdown effect and evaluating degradation mechanisms in off-state. Figure 2.14 suggested different regions of the device submitted to the step stress at V_D= 50 V, and we can compare these regions with the image in Figure 2.15. At V_G= -10 V the device is in the off-state and there is no current flow the channel. At V_G= -6 V the channel is formed and the EL signal is in the maximum. With the injection of electrons from

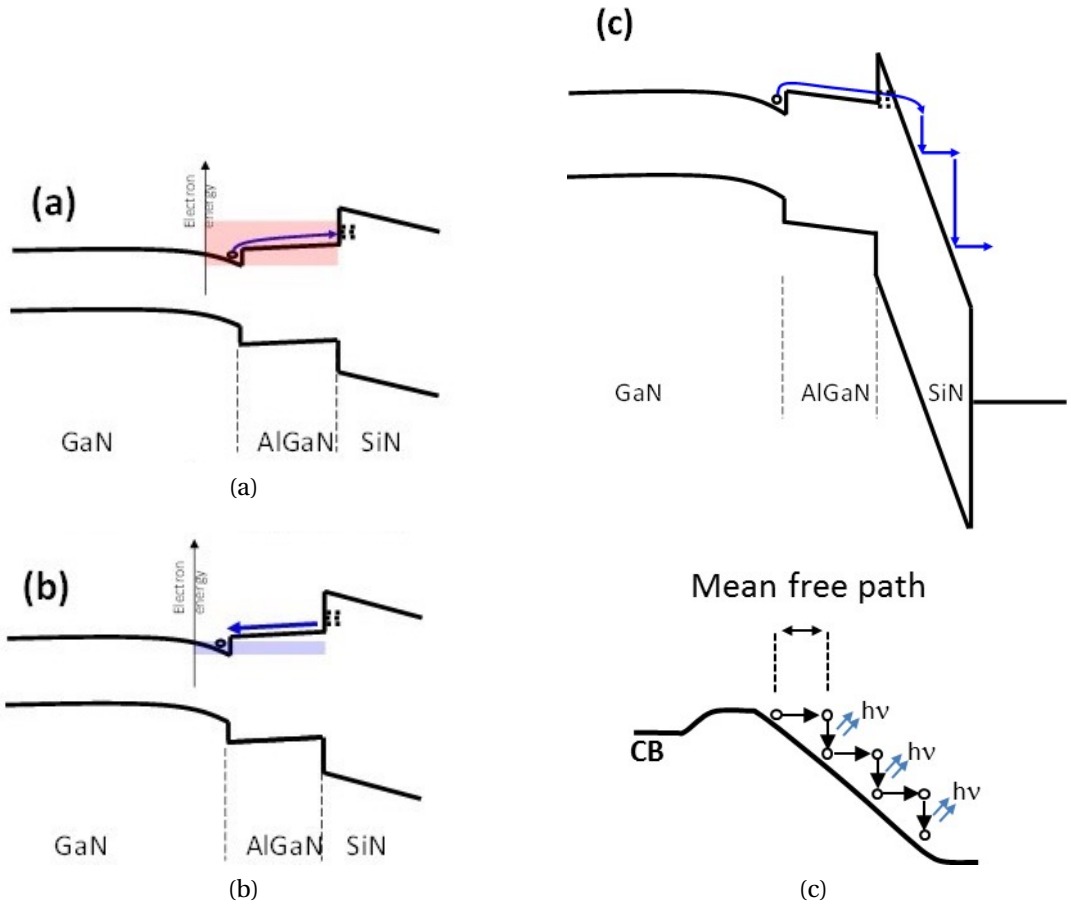


Figure 2.13 – Scheme of the band diagram of the device: a) injecting electrons in the AlGaN/SiN, b) De-trapping of electrons, c) electrons are injected to the gate insulator.

the source when the electrons are accelerating by gate drain bias they lose the energy due to the scattering by means of mean free path. The mean free path depends on temperature and amount of impurity in the semiconductors, for higher temperature there is a shorter mean free path so indicating enhance of hot electrons. At V_G= -2 V EL signal drops as we discussed before, and finally at V_G= 1 V there is no hot electron no EL signal. Therefore, we can say:

$$EL \sim I_D \times f(HE_{Energy}), \tag{2.1}$$

in which HE_{Energy} is a free path.

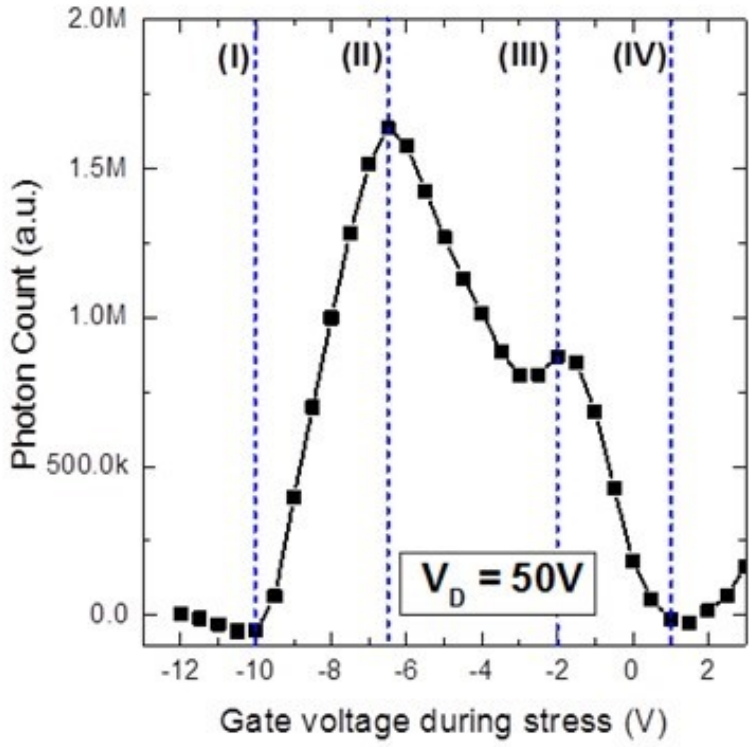


Figure 2.14 – Intensity of the EL signal as a function of gate voltage with V_{DS}=50 V.

There is a correlation between the on resistance and photon count as shows in Figure 2.16. In the lower gate voltage there is a higher number of electrons and injection of electron in to the AlGaN/Si stack. For higher gate voltage due to the higher electric field – electrons can be injected from the 2DEG towards the gate metal which increases the on resistance.

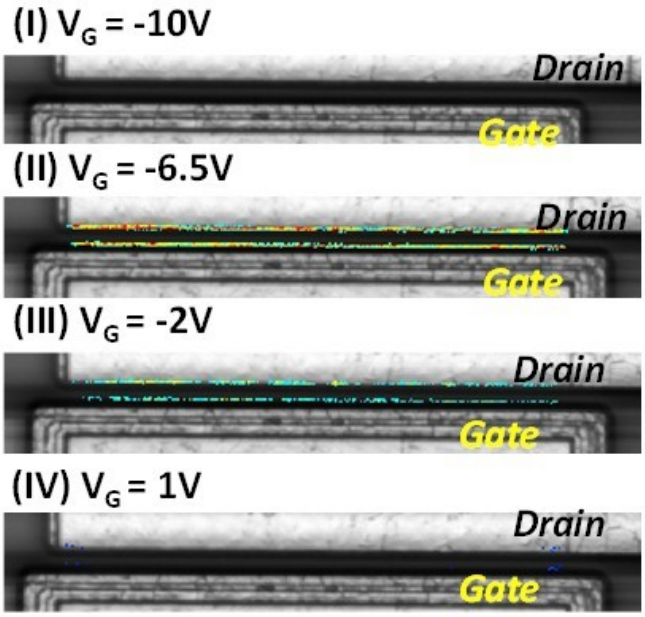
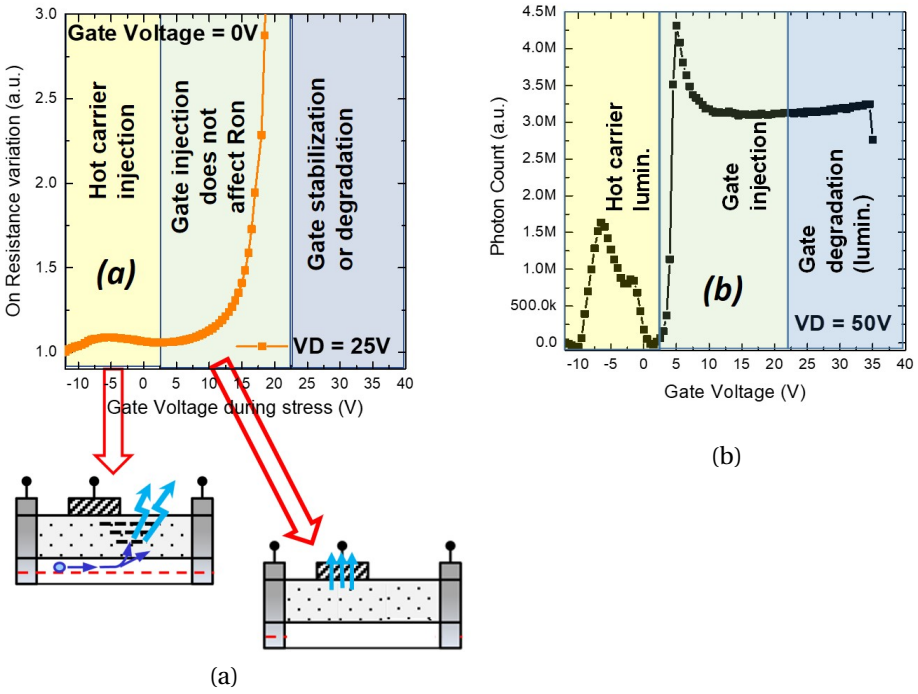


Figure 2.15 – False colour image reporting the distribution of EL along the gate a V_{DS} = 50 V at different V_{GS}.



(a)

(b)

Figure 2.16 – Scheme of the band diagram of the device: a) injecting electrons in the AlGaN/SiN, b) de-trapping of electrons, c) electrons are injected to the gate insulator.

2.3 Robustness analysis

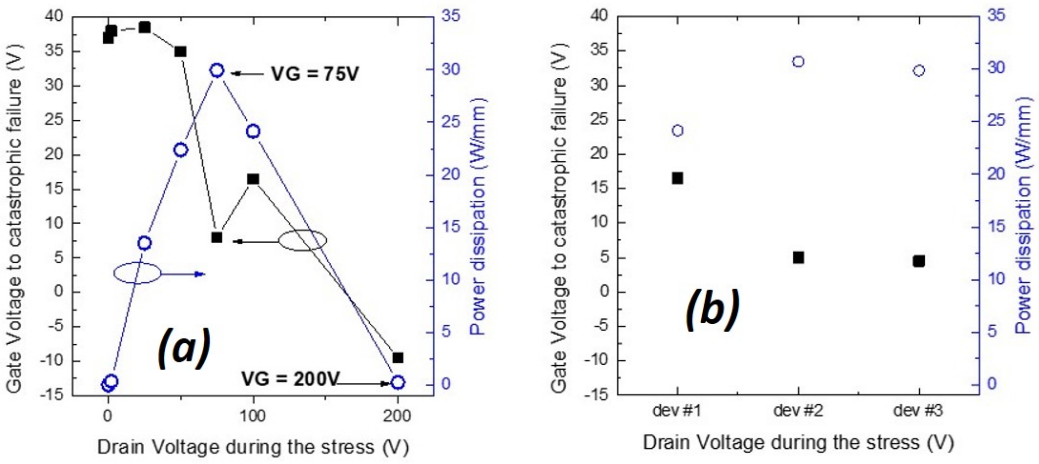
In this section we will discuss the robustness of the wafer under the test, two main aspects contribute to the catastrophic failure:

1. gate voltage applied;

2. power dissipated.

The devices have demonstrated a strong variability as well as a much higher robustness toward the gate voltage (Figure 2.17a).

Figure 2.17b shows the results from three tests which are performed at V_D = 100 V demonstrated a gate catastrophic failure ranging from V_G = 4.5 V to V_G = 18.5 V. Nevertheless, it is worth mentioning that this discrepancy is justified by the high corresponding power dissipation



(a) (b)

Figure 2.17 – a) power dissipation for one device versus drain voltage during the stress. b) power dissipation versus different devices.

2.4 Step Stress and Recovery

In this part, we don't let the device reach to the breakdown point and stop the stress before failure point.

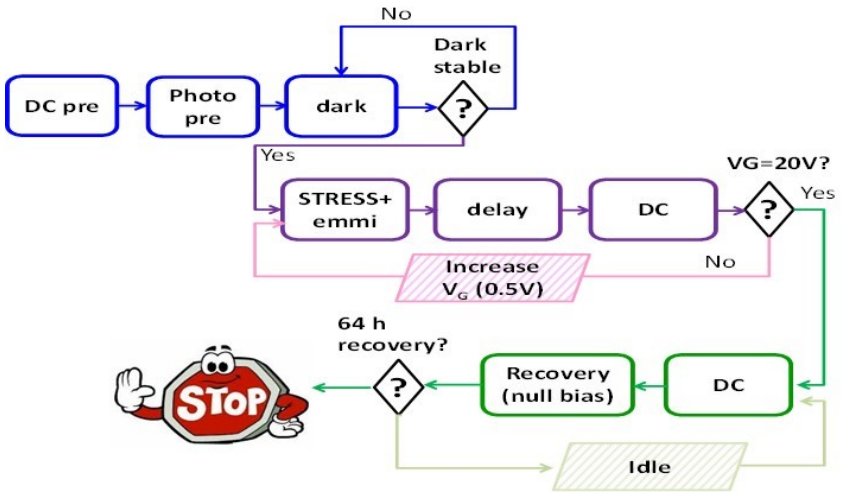
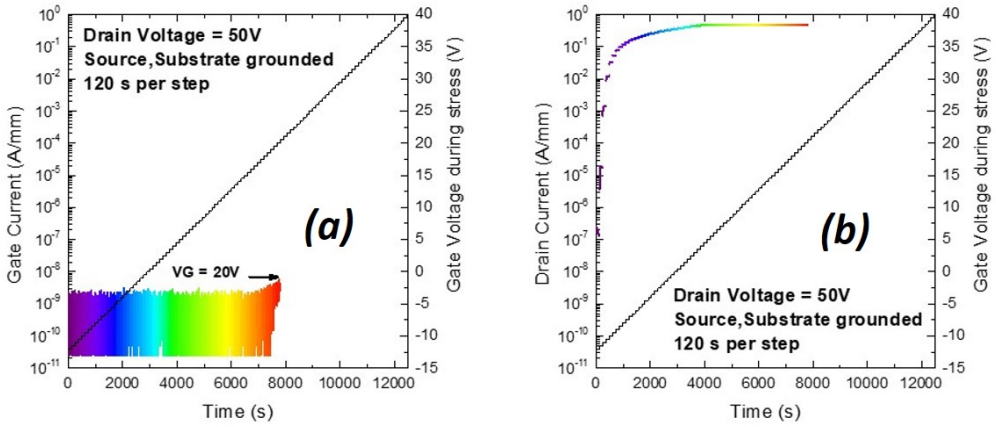


Figure 2.18 – Measurement setup(routine) step stress and recovery.

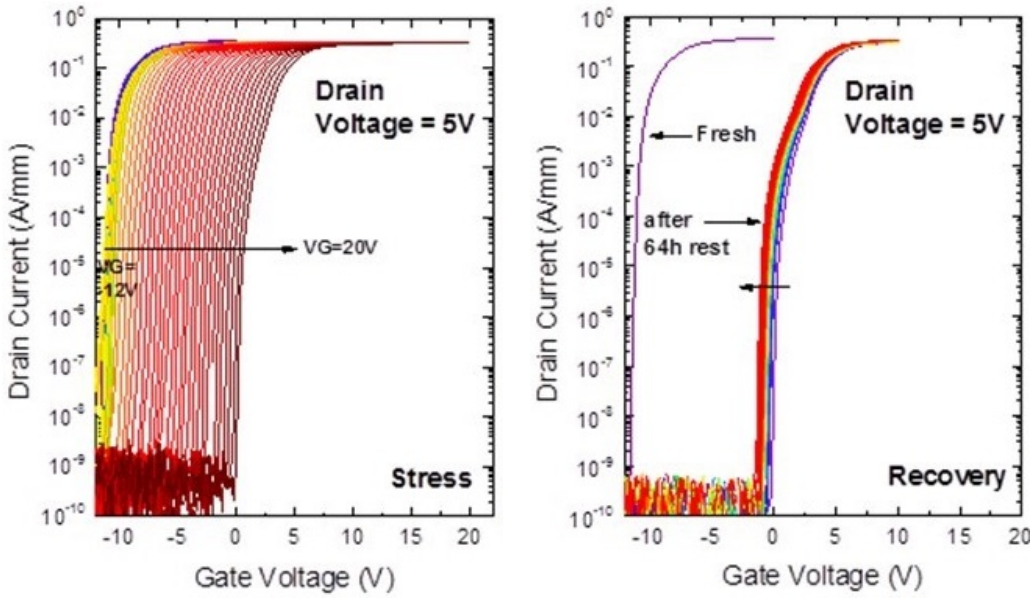
The sequence of the measurement is based on the 1) DC characterization 2) photo by means of CCD camera (describing bellow) 3) dark luminescence to count the photons of the dark room a kind of calibration till reach to the stable value 4) stress+emmi 5) delay of 10 sec 6) DC characterization 7) increase the 0.5 volt the gate stress up V_G=20 V 8) DC characterization to check the shift of the V_{TH} and R_{ON}, 9) photo by CCD camera to observe the photo luminescence in the last point. After the step stress, the devices were submitted to recovery (Figure 2.5). The recovery was checked at different conditions, at null bias, and high temperature (T=150°C).

Figure 2.18 reports the gate and drain current measured on one of the devices submitted to gate-step stress with V_{DS}= 50 V. For a gate voltage below 20 V, the gate leakage is very small and indeed below the instrument noise level the same results as previous section, the measurement has stopped at V_{GS}=20 V, before breakdown of device. Figure 2.20 reports the I_D-V_{GS} and I_D-V_{DS} curves measured after each stage of the step-stress experiment for stress and recovery; each colour indicates one step measurement during the stress. As can be noticed, a shift in pinch-off voltage and increase in on-resistance are observed during stress. We analysed the recovery at different situation such as high temperature and different voltage (doesn't show the



(a) (b)

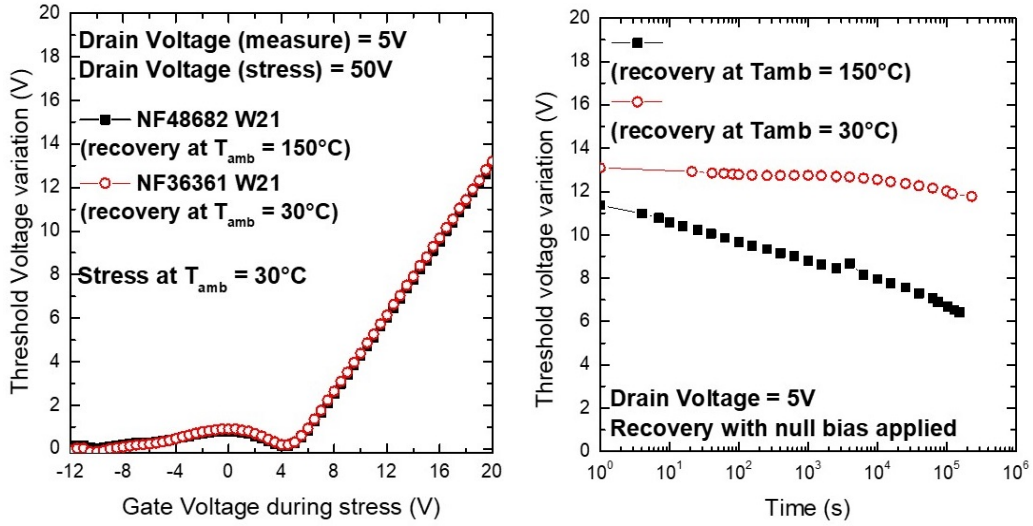
Figure 2.19 – (a) Gate and (b) drain current versus gate voltage during a step-stress experiment carried out with V_{DS}=50 V, increasing V_{GS}.



(a) (b)

Figure 2.20 – a) Gate current versus gate voltage, the shift of the pinch-off voltage variation. (b). Drain current versus drain voltage, reduction of the on resistance.

results). Figure 2.21 shows the results of recover. It can be seen that the recovery is more strong at high temperature than the room temperature.



(a) (b)

Figure 2.21 – a) threshold voltage variation during the step stress with increasing the gate voltage. b) threshold voltage variation during the recovery at room temperature and high temperature.

The analysis reveals that:

1. A null bias applied at room temperature induces a recovery of the threshold voltage shift. However, the device is still in normally-off condition after 64h of rest.

2. Conversely, a higher ambient temperature induces a more significant recovery. Although the V_{TH} does not completely recover, a normally-on condition is obtained.

3. The change in the I_D-V_G slope (log scale) is unchanged after the recovery phase.

2.5 Conclusions

In this work, we have demonstrated that gate and drain bias induce the degradation on MIS-HEMTs during the stress. We demonstrated the existence of field- and hot-electron induced degradation processes, which were never described before in the literature for GaN devices. Results from electro luminescence show that there is correlation with pinch-off voltage variation during the gate stress in the same voltage.

Based on the results, the increase of the pinch off voltage is directly correlated with the gate leakage current. Moreover, it has been demonstrated that for the stress and recovery analysis, the higher ambient temperature induces a more significant recovery for the threshold voltage variation.

3 Proton-Irradiation Effects on AlGaN/-GaN HEMTs

Radiation hardness is of crucial importance for devices aimed at space applications. Several works were discussed in the literature to determine the robustness of AlGaN/-GaN HEMTs (aimed at RF applications) toward radiation effects and to understand the corresponding degradation mechanisms. GaN-HEMT technology is an excellent choice for space application due to the high performance and high breakdown field (3.3 $^{MV}/_{cm}$) which is eleven times higher than silicon (0.3 $^{MV}/_{cm}$). As a matter of fact, it is very important to guarantee the performance and stability of these devices [36]. In this scenario, proton radiation represents one of the major limits to the device performance. According to the literature, the effects of proton radiation are due to displacement damage and they can be summarized as:

1. Positive shift in the DC threshold voltage, as a consequence of the creation of acceptor-like traps, which is related to the reduction in sheet carrier density [37–40];

2. Reduction of the DC drain current which is a consequence of a decrease in the mobility and the sheet carrier density [41–43];

3. Increase of the DC gate leakage current which is ascribed to the decrease of the barrier height. Furthermore, displacement damage influences the dynamic performance as demonstrated in [44, 45].

4. An increase of trapping effects in terms of the dynamic shift in the threshold voltage, dynamic decrease in the transconductance peak and the dynamic

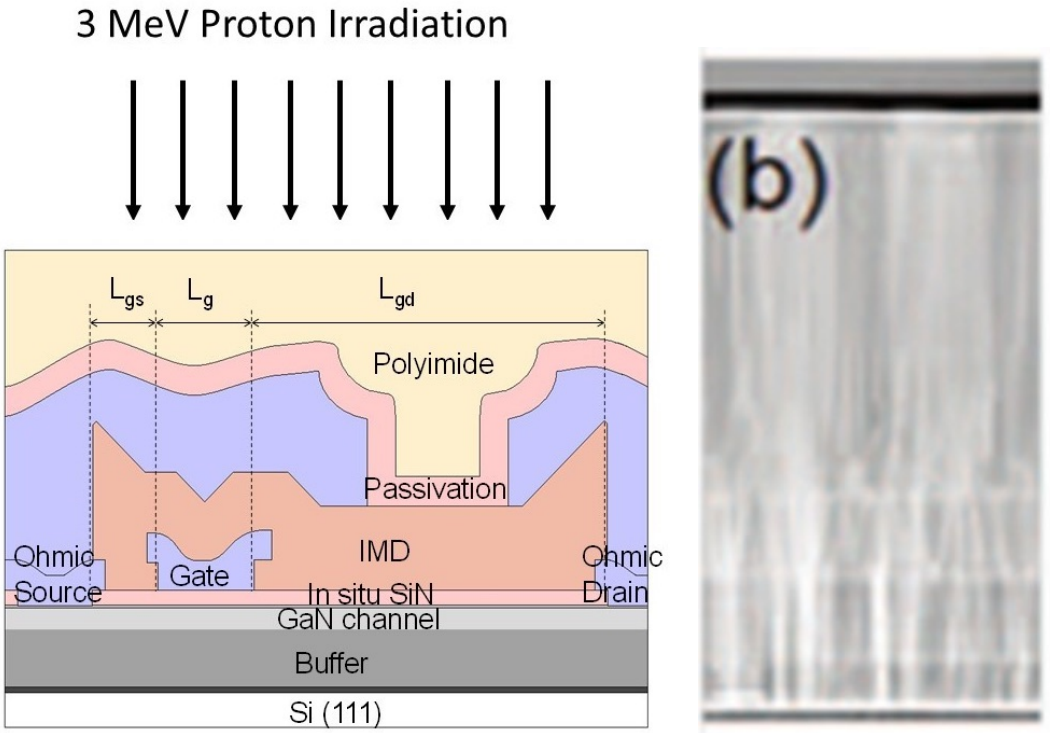
increase in the on resistance [46, 47].

5. By means of the drain current transient analysis, it has been demonstrated in the literatures that the increase of the trap amplitude is correlated to the applied proton fluence. GaN-based devices exhibit significant robustness to radiation, demonstrating negligible variation up to 1×10^{13} p/cm^2 (at 1.8 MeV) [38, 48–50].

3.1 Experimental details

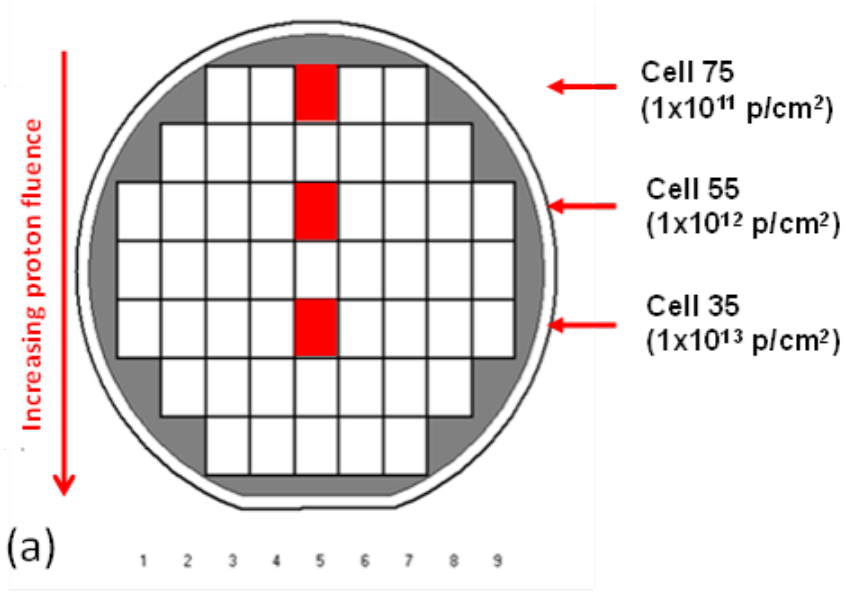
The analysis was carried out on GaN-on-Silicon power transistors (Figure 3.1). The epitaxial structure was grown by metal-organic chemical vapour deposition (MOCVD), and consists of an AlN/AlGaN/GaN strain relief layer (SRL), a thick C-doped GaN layer, an unintentionally-doped (uid) GaN channel layer, and an AlGaN barrier. An in-situ SiN layer was used as a gate insulator and as a passivation for the access regions [51–53]. Figure 3.1b indicates the cross section of the buffer of the analysed devices. After a full characterization of the DC, dynamic and transient performance of the devices the proton irradiation was carried out [54]. For each condition five devices with different gate-drain length ($L_{gd} = 15\ \mu m - 20\ \mu m$) were tested in order to monitor the variability and to study the influence of the device geometry on the performance variation. Figure 3.2a) depicts the wafer under test and highlights the irradiated cells. The position of the tested devices in the cell is furthermore provided (Figure 3.2b). Proton radiation was performed at National Laboratories in Legnaro Padova, Italy. Devices were submitted to proton irradiation at room temperature with no bias applied at 3 MeV.

Three cells were used to test different fluences with the same energy; increasing proton fluences from 1×10^{11} p/cm^2 to 1.5×10^{13} p/cm^2 were used. Figure 3.3 shows the test procedure: after a preliminary DC characterization, trapping effects are studied by means of pulsed measurement (at T=30°C and T=150°C) and drain current transient analysis (at V_{DSQ} = 200 V and 600 V). Just before radiation hardness a DC measurement is performed to verify that the variation on DC parameters is not influenced by pulsed measurements or drain current transients. On a different set of devices (GANE 19/ L_{gd}= 19μm) emission microscopy is detected. Identical analysis is performed after the radiation tests in order to evaluate the variations.

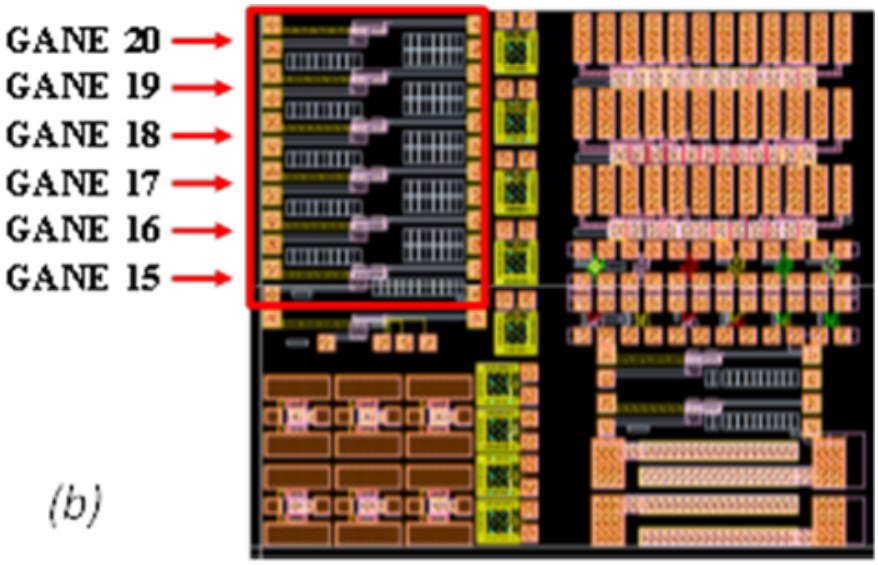


(a) (b)

Figure 3.1 – (a) schematic representation of the structure of the devices under analysis and of the proton implantation process used for eliminating dynamic R_{on}; (b) The cross section of the buffer of the analysed devices.



(a)



(b)

Figure 3.2 – a) Description of the test procedure and b) the devices used for each test.

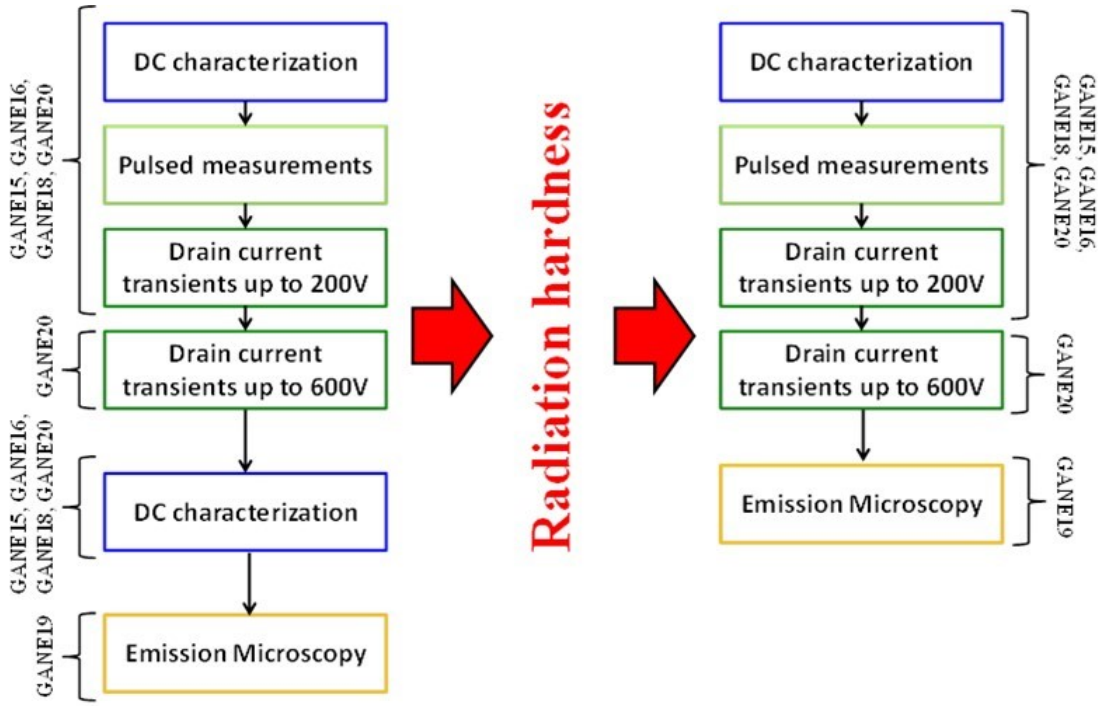


Figure 3.3 – Description of the test procedure and of the devices used for each test.

3.2 Experimental results Proton Irradiation up to 10^{13} p/cm²

GaN-based power transistors still suffer from the trapping and other degradation mechanisms that affect the dynamic performance and the reliability of the transistor [36, 55]. As a matter of fact, dynamic-Ron is a key issue in GaN power HEMTs [56]. The charge trapped during OFF-state operation has a negative impact on the ON-resistance in GaN-based power HEMTs [17, 57, 58].

Figure 3.4 reports a DC characterization which is performed before the radiation tests. Gate leakage current (not shown here), monitored in both the diodes and in the transistor, is below the instrument noise level. The threshold voltage (measured in saturation region) is found to be significantly changed by the cell position, presumably due to a variability in the deposition of the insulator under the gate (see Figure 3.1a). A slight dependency of the threshold voltage on the device geometry is furthermore observed. The on resistance (measured at V_{GS} = 0 V) significantly changes with the cell position in the wafer, consistently with the trend observed in the analysis of the threshold voltage. Furthermore, according to the basic principles of HEMTs, the on-resistance increases with gate-drain length with a linear trend. Drain current varies consistently with on-resistance and threshold voltage. The transconductance peak shows no variation with the cell position or with the device geometry.

3.2.1 Electrical characterization

All the measurements have been performed on the same devices after the proton irradiation as explained at Figure 3.3. After the radiation hardness, the threshold voltage faces a positive shift (Figure 3.5). Contrary to previous studies reported in [39, 59], no correlation between the variation of the threshold voltage and the proton fluence is established. Nevertheless, if we consider the threshold voltage value after the radiation test, we can observe that threshold voltage measured on the devices of the same cell has a low variability. Furthermore, a good correlation is noticed between the cell position and/or the proton fluence applied and the threshold voltage value monitored after the test. It is worth mentioning that, contrary to results previously reported in the literature, devices under test are MIS-HEMTs with an insulator layer deposited under the gate.

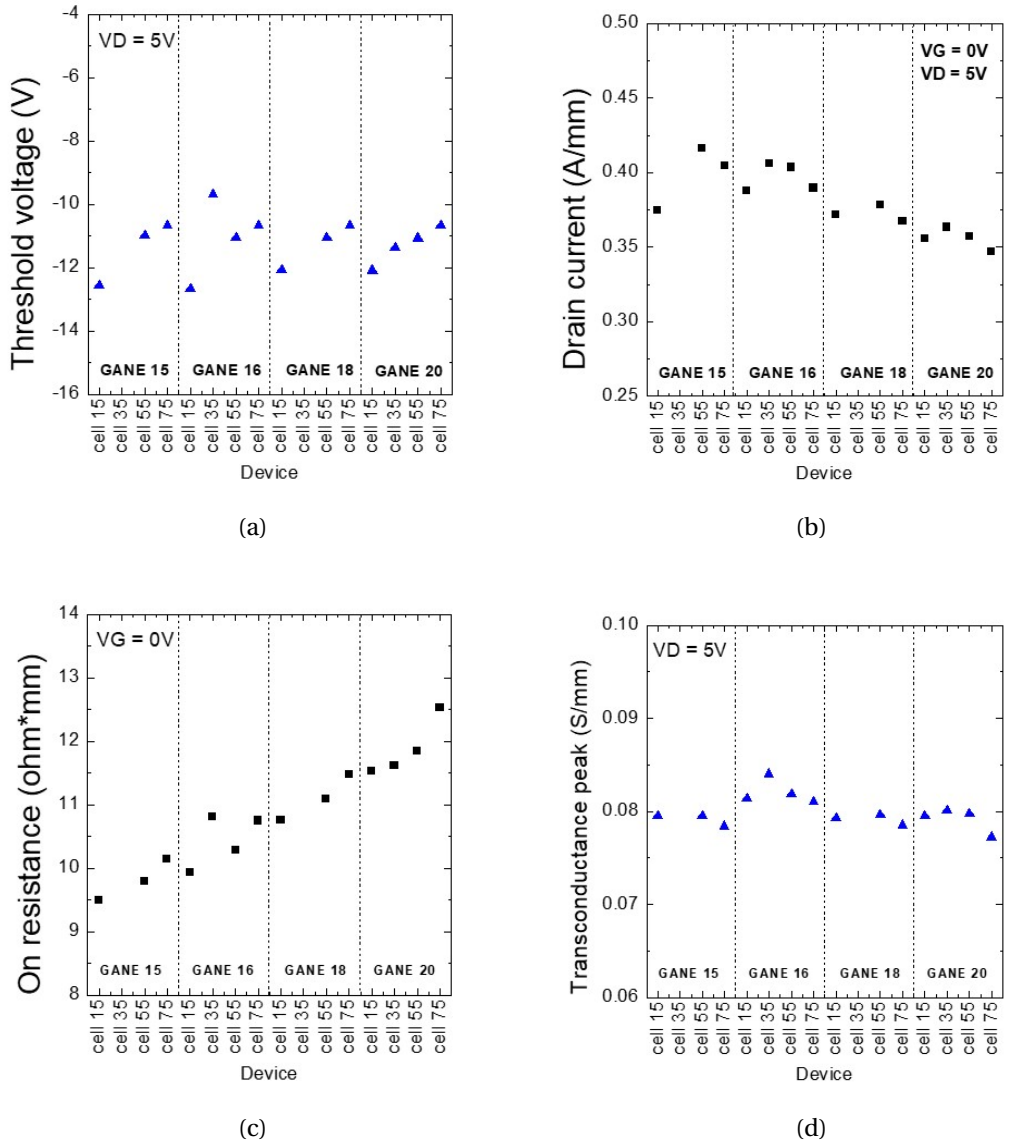
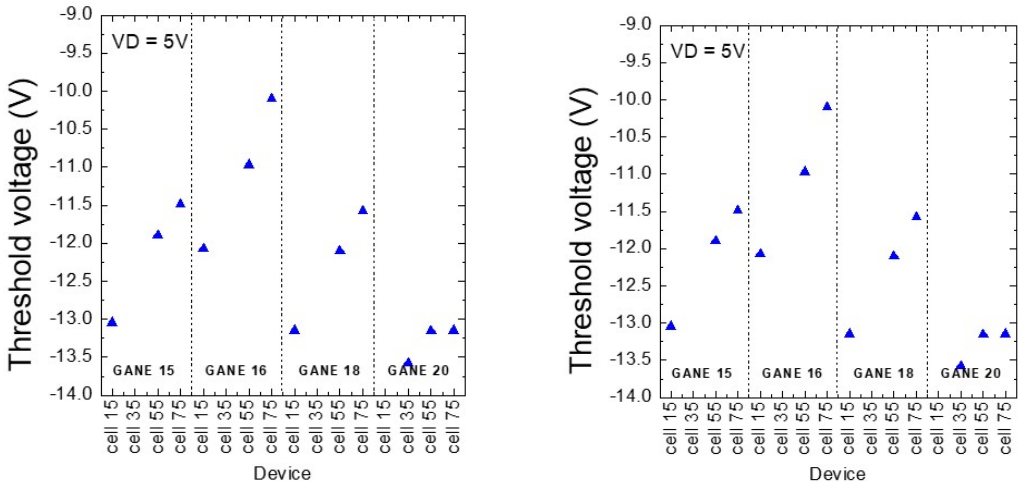


Figure 3.4 – DC preliminary characterization of devices before submit to proton radiation tests. Monitored parameters are: (a) threshold voltage, (b) drain current, (c) on resistance, (d) transconductance peak.

Transconductance peak, on resistance and drain current (monitored in saturation region at V_{GS} = 0 V) demonstrate a different behavior (Figure 3.6). Negligible variation is observed for proton fluence lower than 1×10^{13} p/cm^2. The variation is consistent with previous results reported in the literature and seems to change with the device geometry. The gate leakage current (not shown here), monitored on the diodes and on the transistor, is below the instrument noise level even after the radiation tests,



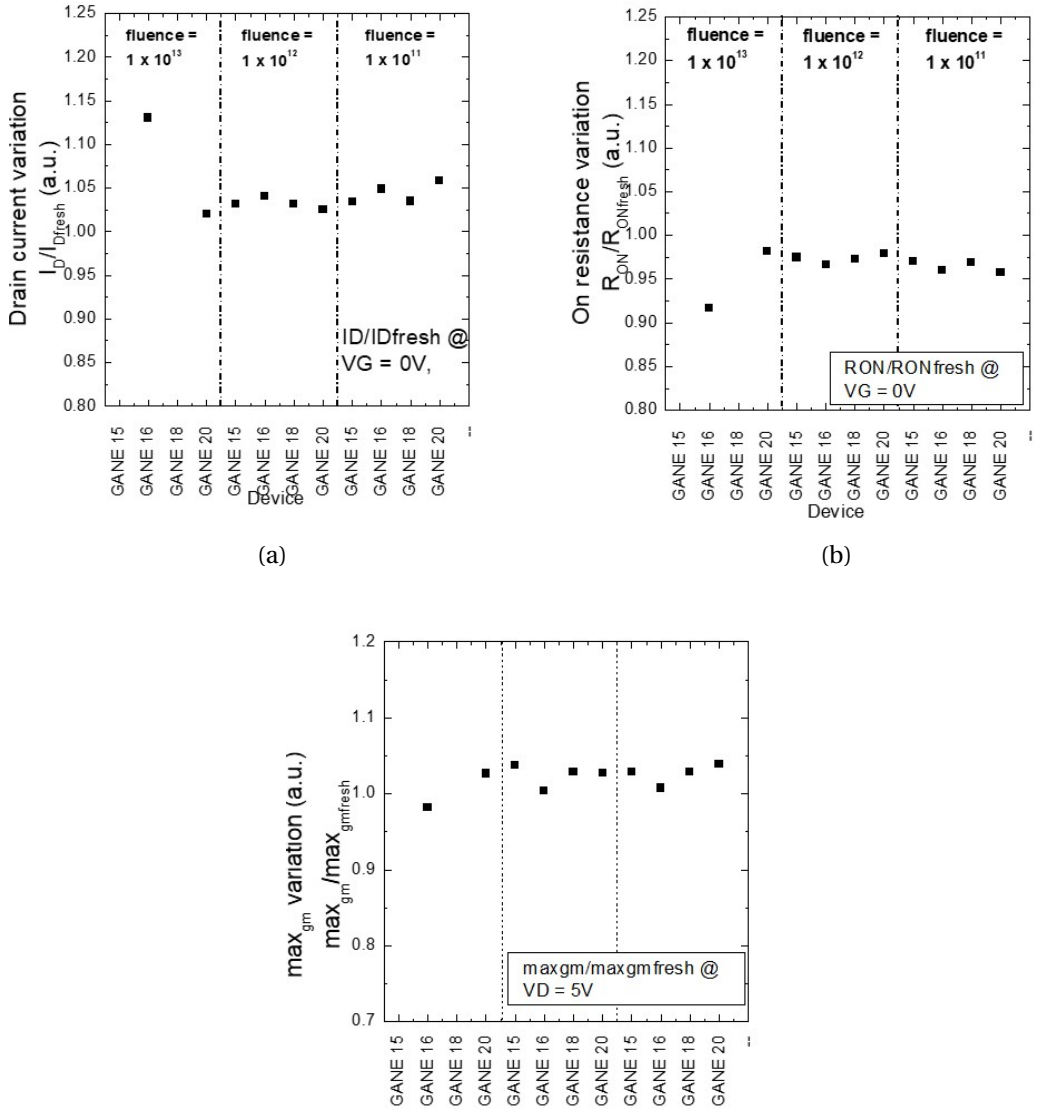
(a) (b)

Figure 3.5 – (a) threshold voltage measured after radiation tests and (b) threshold voltage variation monitored in devices tested at different proton fluence.

independently from the proton fluence [60].

The impact of proton radiation on the trapping effects was studied by means of pulsed measurements and drain current transients. Pulsed measurements were performed by means of a custom setup, by using a duty cycle of 1% (ton/toff = 20 μs/ms). During the quiescent bias point, the devices are kept in off state (V_{GSQ} = -20 V) with drain bias levels (V_{DSQ}) from 0 V to 600 V. During the pulse the condition is V_{GS} = 0 V, V_{DS} from 0 V to 4 V.

Pulsed measurements at room temperature reveal a bell-shape behavior with a maximum increase of the dynamic on resistance at V_{DSQ} = 200–300 V. The increase of the dynamic R_{ON} worsens at higher temperatures (ambient temperature = 150°C). A similar behavior is demonstrated in all the devices tested, showing a low variability among different cells and device topologies. Two representative examples on fresh devices are shown in Figure 3.7; analysis at T = 30°C and T = 150°C is respectively shown.



(a) (b)

(c)

Figure 3.6 – Variation of the (a) drain current, (b) on resistance, (c) transconductance peak in devices tested at different proton fluences.

Low proton radiation fluences induce no worsening in the trapping effects. At high temperature (Figure 3.7), a significant decrease of the dynamic R_{ON} is observed, showing negligible trapping effects even at V_{DSQ} = 200 V–300 V. Figure 3.8 highlights the dynamic variation of R_{on} and the non-normalized dynamic R_{on} are presented in

Figure 3.9. R_{on} variation = dynamic R_{on} variation and is calculated as:

$$Ron_{variation} = \frac{Ron(V_{GSQ}, V_{GDQ})}{Ron(0V, 0V)}. \tag{3.1}$$

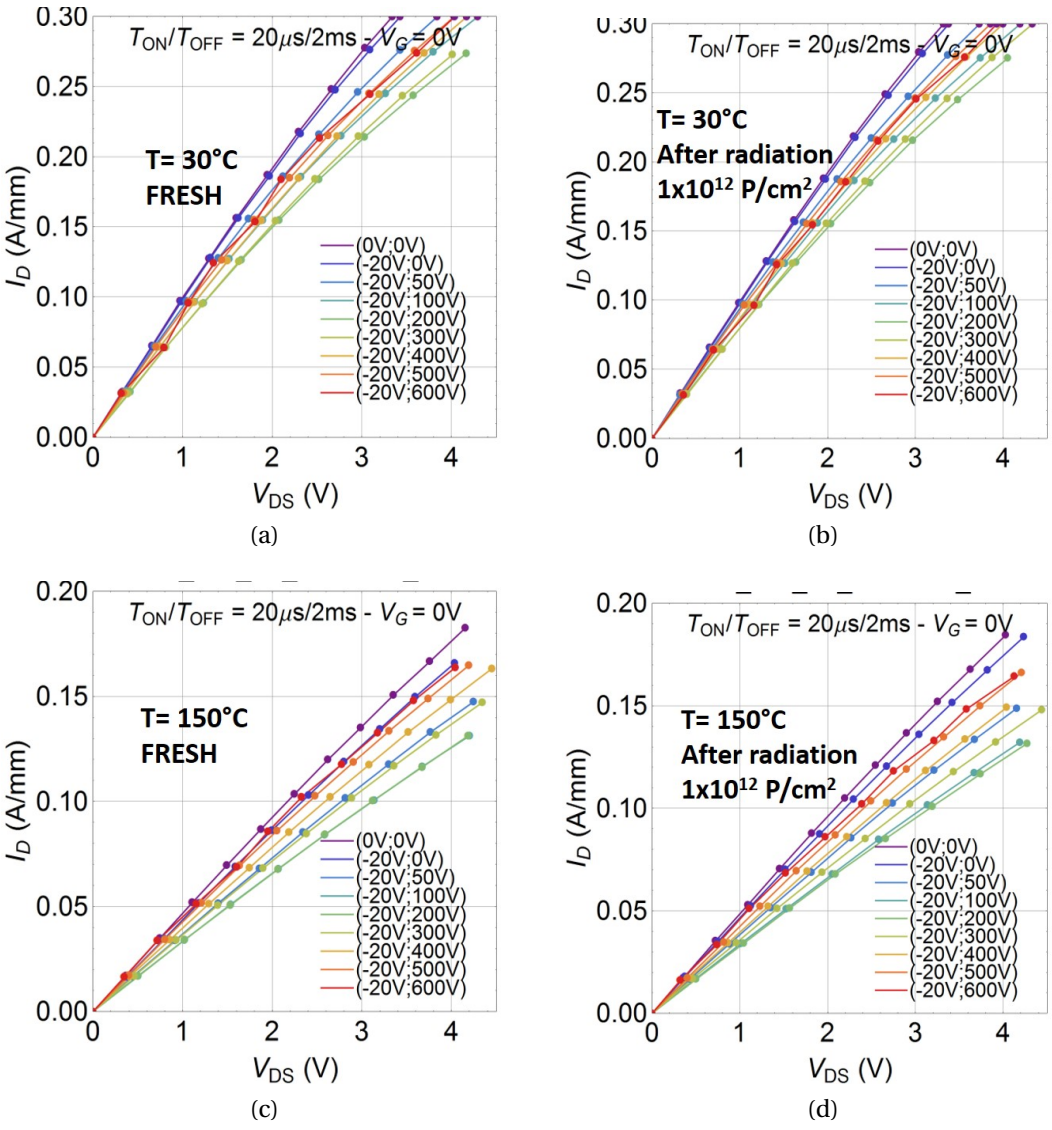


Figure 3.7 – Pulsed I_D-V_D curve measured at room temperature on representative device (a) before and (b) after radiation at 1×10^{12} p/cm². Analogous curves measured on the same device at Tamb = 150°C (c) before and (d) after radiation.

The results demonstrated by pulsed measurements are confirmed by the analysis performed with drain current transients. Drain current transients were performed on

fresh and post radiation devices with two different condition during the quiescent bias point, namely (V_{GSQ},V_{DSQ}) = (-20 V,200 V) and (V_{GSQ},V_{DSQ}) = (-20 V,600 V). De-trapping condition is V_{GS} = 0 V, V_{DS} = 3 V. Trapping and de-trapping time are, respectively, 10 s and 100 s. Several ambient temperatures (Tamb) were considered compatibly with the time constant: (i) with V_{DSQ} = 200 V four Tamb ranging from 110°C to 170°C were considered; (ii) with V_{DSQ} = 600 V three Tamb ranging from 140°C to 160°C were used.

Figure 3.10 reports the analysis on a representative example. Drain current transients were performed on a fresh device with (V_{GSQ},V_{DSQ}) = (-20 V,200 V) and Tamb ranging from 110°C to 170°C. One trap level, characterized by activation energy of 0.9-1 eV, was detected on the fresh device. Low proton fluences induce no variation in the trapping effects in terms of the variation of the activation energy and of the increase of the trap amplitude (Figure 3.11).

However, drain current transients confirm that the devices show no detectable trap level states, consistently to double pulse measurements (Figure 3.11). Analogous results are observed for drain current transients performed with (V_{GSQ},V_{DSQ}) = (-20 V, 600 V) and Tamb ranging from 140°C to 160°C. A representative example of a fresh device is shown in Figure 3.13. One trap level, characterized by activation energy of 0.4-0.6 eV (Figure 3.14), was detected. Low proton fluences induce slight variation in the trapping effects in terms of the variation of the activation energy and of the increase of the trap amplitude (Figure 3.13). The high poroton fluence (1.5×10^{15} p/cm^2) will be discussed on the next part.

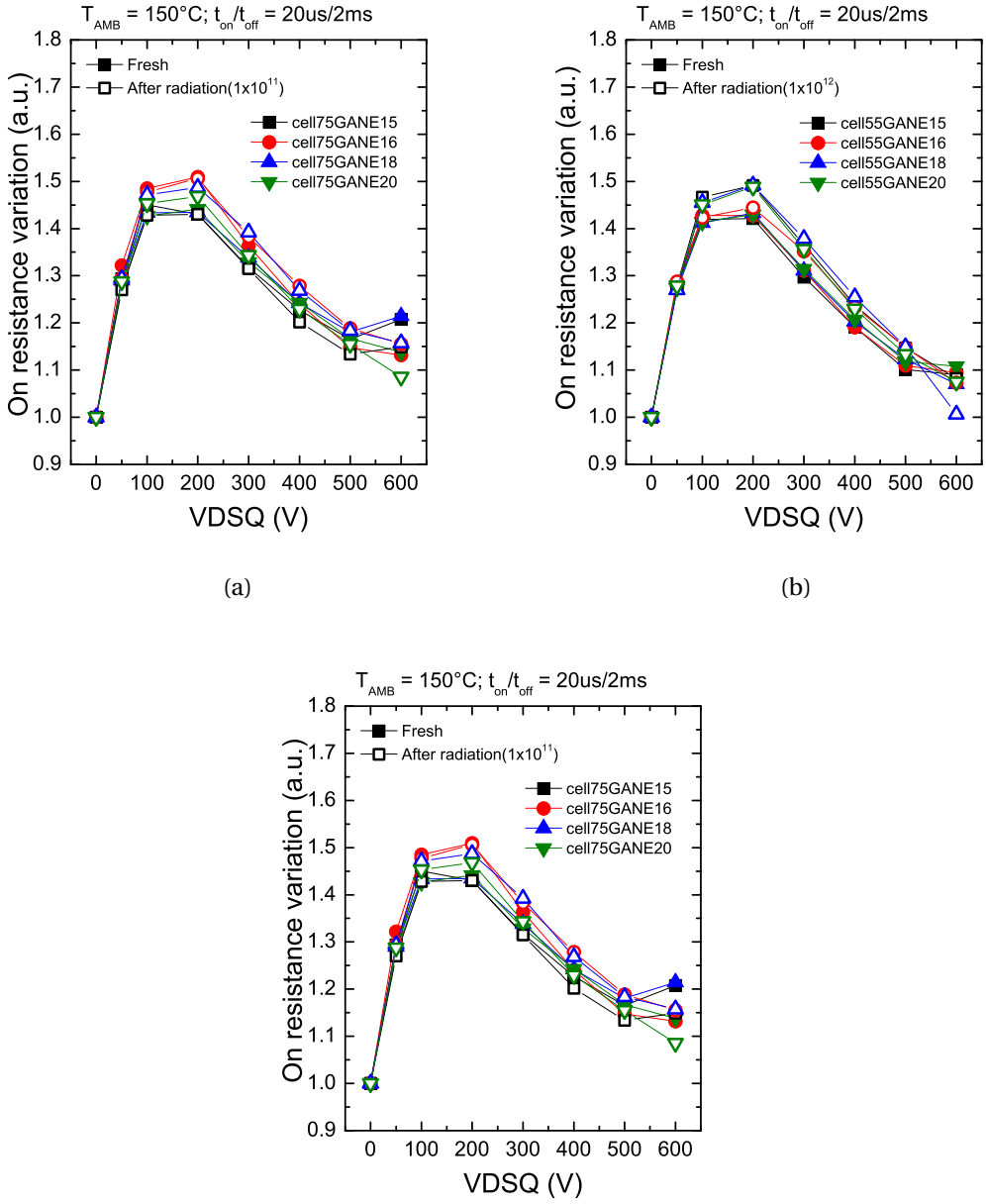


Figure 3.8 – Comparison of the R_{ON} dynamic increase on devices before (full square) and after (void square) radiationat T = 150°C. The behaviour after four proton fluences (a-d) is compared.

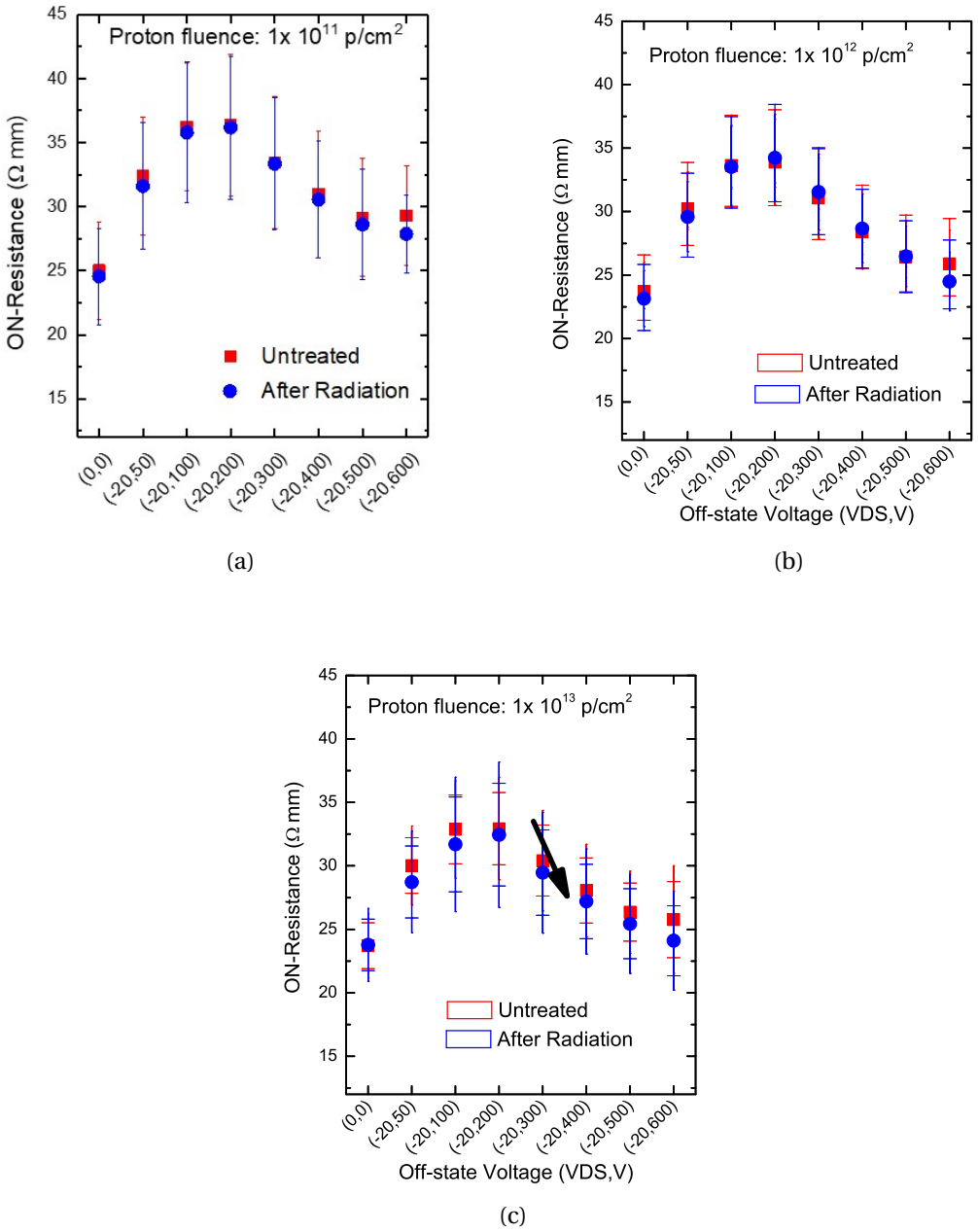
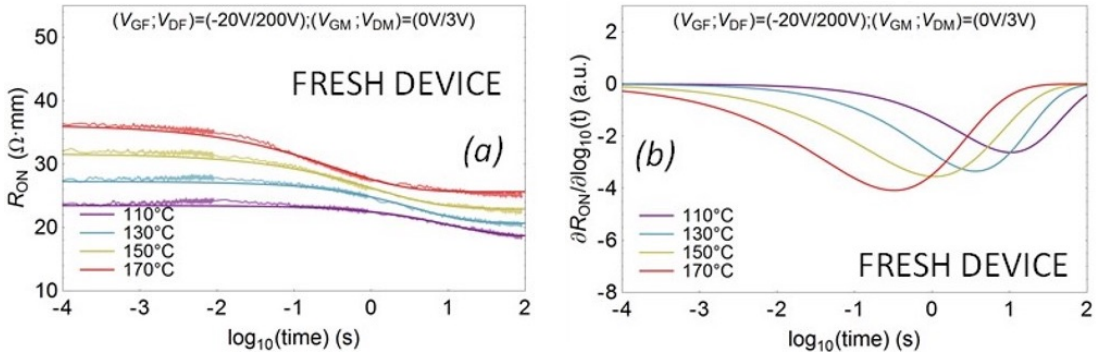
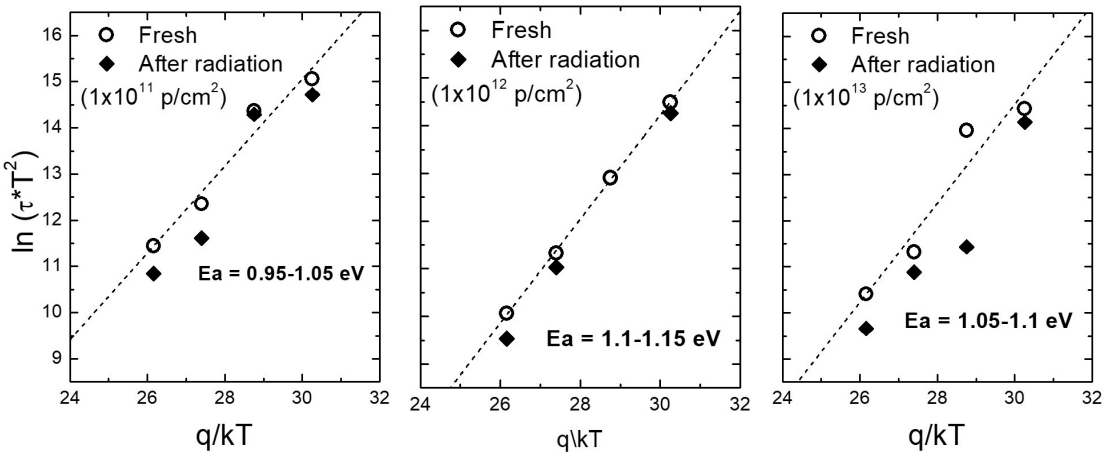


Figure 3.9 – Comparison of the R_{ON} dynamic increase on devices before and after radiationat T = 150°C. The behaviour after three proton fluences (a-d) is compared with non-normalized values.



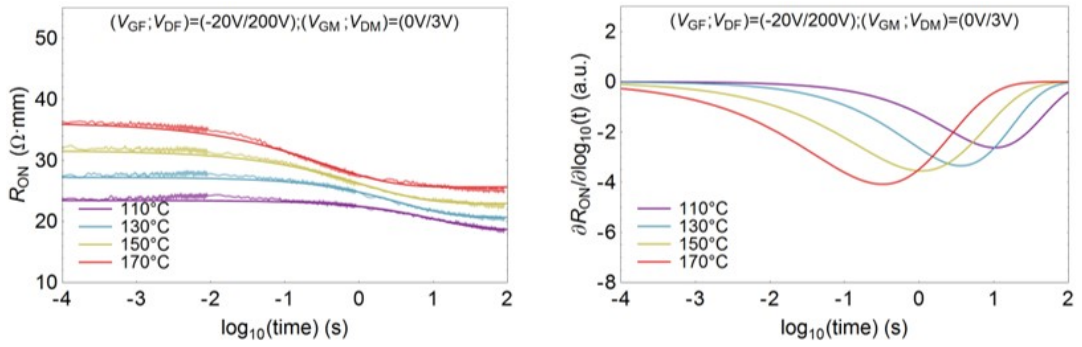
(a) (b)

Figure 3.10 – Drain current transients measured on a fresh device (representative example). (a) on resistance variation; (b) trap amplitude. A filling bias of (V_{GSQ},V_{DSQ}) = (-20 V, 200 V) is considered.



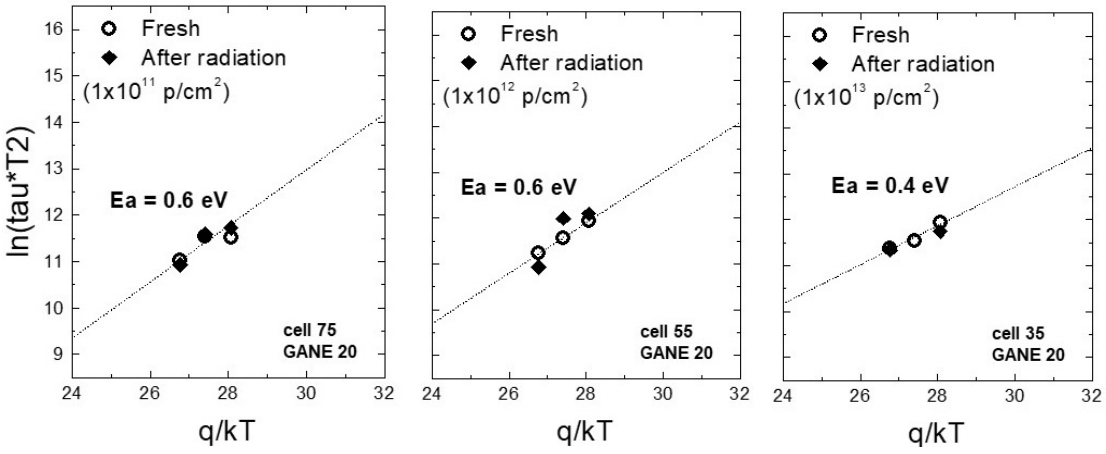
(a) (b) (c)

Figure 3.11 – Arrhenius plot calculated for a representative device (GANE 16) per cell. The impact of three different proton fluences is compared, namely (a)1×10^{12} p/cm², (b) 1×10^{13} p/cm² and (c) 1×10^{14} p/cm². A filling bias of (V_{GSQ},V_{DSQ}) = (-20 V, 200 V) is considered.



(a) (b)

Figure 3.12 – Drain current transients measured on a fresh device (representative example). (a) on resistance variation; (b) trap amplitude. A filling bias of (V_{GSQ},V_{DSQ}) = (-20 V, 600 V) is considered.



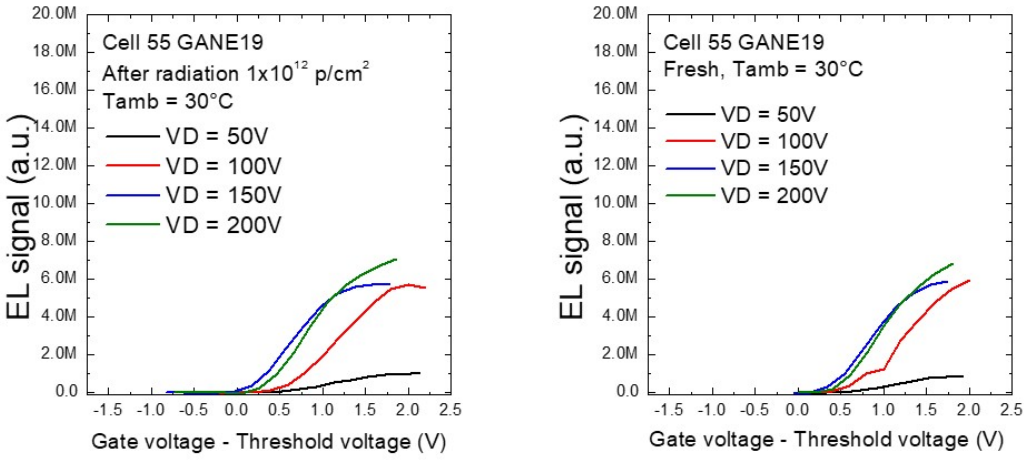
(a) (b) (c)

Figure 3.13 – Arrhenius plot calculated for a representative device (GANE 20) per cell. The impact of three different proton fluences is compared, namely (a)1×10^{11} p/cm^2, (b) 1×10^{12} p/cm^2 and (c) 1×10^{13} p/cm^2. A filling bias of (V_{GSQ},V_{DSQ}) = (-20 V, 600 V) is considered.

3.2.2 Optical characterization

Finally, the impact of proton radiation on the device performance was studied by means of emission microscopy. The electroluminescence (EL) signal was detected for several gate and drain voltage levels. In this analysis, the drain voltage levels range from 50 V to 200 V; the gate voltage levels were chosen according to the threshold voltage of the device and to the dissipated power (not to induce device degradation). An acquisition time of 25 s and an EM gain of 200 were used.

After radiation a significant threshold voltage shift (not correlated to proton fluence) was observed; therefore, we preferred to plot the EL signal as a function of the difference between the gate and the threshold voltage (V_{GS}-V_{TH} level). Devices that are stressed at low proton fluence exhibit no variation neither in terms of EL signal nor in terms of the EL/ID ratio. The EL signal (at V_{DS} = 200 V and consistent V_{GS}-V_{TH} level) doubles after radiation at the highest proton fluence. Emission microscopy (Figure 3.14) detected before and after radiation demonstrates that the EL signal uniformly increases along the gate finger. Devices stressed at low proton fluence exhibit no varaition neither in terms of EL signal nor in terms of EL/ID ratio.



(a) (b)

Figure 3.14 – EL intensity versus gate voltage overdrive at different drain voltage on a GaN HEMT. (a) before radiation at V_D from 50 V up to 200 V (b) the samples after radiation show a higher EL signal.

3.3 Total Suppression of Dynamic-Ron in AlGaN/GaNHEMTs Through Proton Irradiation

In this part we have investigated the effect of the high-power proton irradiation on the dynamic-Ron in HEMTs, as we already know, the dynamic-Ron is still a key issue in GaN power HEMTs. We have demonstrated that proton irradiation is an effective and controllable way to reduce dynamic-Ron in AlGaN/GaN HEMTs [61,62]; this beneficial effect is ascribed to the minute increase in the leakage of the uid-GaN layer, promoting charge de-trapping from the buffer [63]. The effect is dependent on L_{GD}, shorter L_{GD} is better. The shorter L_{GD} corresponds to a shorter region for trapping, and therefore the dynamic-Ron is not strong when L_{GD} is short. We have demonstrated that samples submitted to proton irradiation at high fluences (1.5×10^{14} p/cm^2, 3 MeV) show a complete suppression of dynamic-Ron (complete voltage range, 150°C), without significant modifications in the other device parameters.

In this part, the proton irradiation method is employed to control the dynamic-Ron of GaN-based power HEMTs. The effects of proton irradiation are studied by variety of measurements such as double pulse, drain current transient (DCT) characterization, electroluminescence (EL) analysis and hard switching analysis on untreated and irradiated devices we demonstrated the following relevant results:

1. Samples submitted to proton irradiation at high fluences (1.5×10^{14} p/cm^2, 3 MeV) show a complete suppression of dynamic-Ron (complete voltage range, 150°C), without significant modifications in the other device parameters.

2. As we have seen in section 3.2 for fluences higher than 1.5×10^{13} p/cm^2, the devices show a substantial reduction of dynamic-Ron. Analysis on the highest fluence (1.5×10^{14} p/cm^2), dynamic-Ron is completely suppressed at 600 V/T=150°C, without measurable changes in the gate and sub-threshold leakage and in the threshold voltage.

3. The results of the transient and hard switching analysis shows the total suppression of the trap-related transients identified before radiation testing. The results could be explained by increasing the leakage through the channel. This

increases the de-trapping rate, and leads to the suppression of dynamic-Ron at high V_{DS} [61, 64].

Recently [20,65], the research in the dynamic-Ron of GaN-based power HEMTs demonstrated a non-monotonic dependency on the trapping voltage applied to the drain: on optimized buffers (Figure 3.15), the maximum increase in on-resistance is observed at V_{DS}=100-300 V, while at higher voltages (up to 600 V) the on-resistance decreases to its initial point. This effect has been explained by considering the "leaky-dielectric" model [38], as depicted in Figure 3.16:

1. At low and moderate V_{DS} levels, the ionization of the carbon acceptors promotes trapping (C_N) in the buffer, the negative charge under the gate causes an increase in the on-resistance.

2. At higher voltages (V_{DS} >100-300 V, depending on the sample and on temperature), the leakage through the uid-GaN channel layer promotes the transfer of electrons from the C-doped GaN to the 2DEG. This results in an increase of the electron density in the 2DEG, as a consequence, positive charges (holes or ionized donors) are formed at the interface with the strain relief layer which induces a decrease in the dynamic-Ron. Possible leakage processes through the uid-GaN are band-to-band tunneling or trap-assisted conduction. By optimizing the leakage through the uid-GaN, a complete suppression of dynamic-Ron can be obtained a 600 V, 150°C (see Figure 3.16: and [39]) [56].

However, controlling the conductivity of the uid-GaN during the growth is not straightforward, and reproducible methods have not been proposed so far in the literature. For the first time we propose to use the proton irradiation to accurately control the leakage of the uid-GaN layer, thus achieving a complete suppression of dynamic-Ron in the whole voltage range between 0 V and 600 V (at 150°C). The change in the conductivity of the uid-GaN permits to significantly modify the dominant trapping process in the C-GaN buffer, by moving from a dominant-negative charge trapping, to a situation where the accumulation of positive charge is prominent, as demonstrated by substrate ramp measurements. The proposed method is effective also for minimizing the charge trapping during hard switching transitions [56].

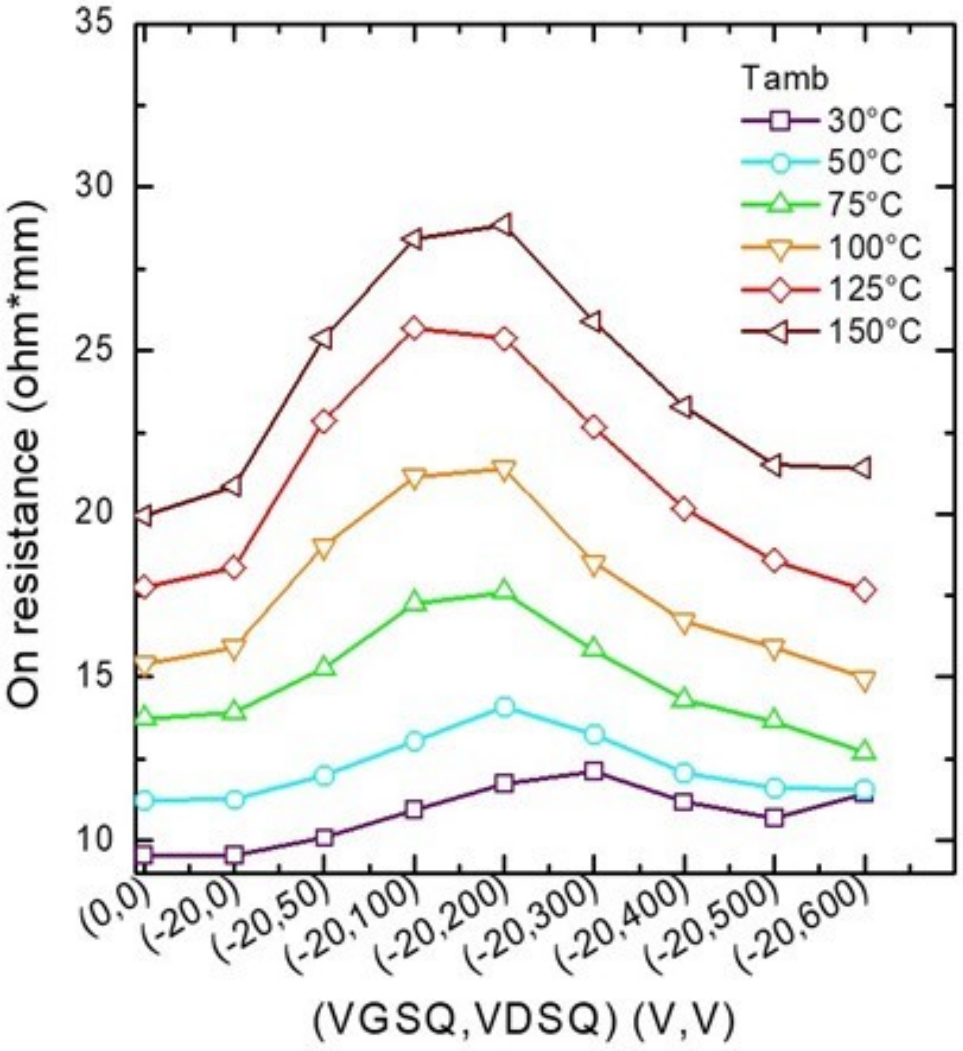


Figure 3.15 – Non-monotonic dependence of dynamic-Ron on trapping voltage, measured at different tempratures between 30°C and 150°C. The drop for V_{DS}>200 V is ascribed to the build up of positive charge in the buffer.

3.3.1 Electrical characterization

In Figure 3.15, before irradiation we observed a non-monotonic dependency of the dynamic-Ron to the trapping voltage. In fact, when temperature increases the conductivity of an undoped layer increases (in agreement with the model in Figure 3.15).

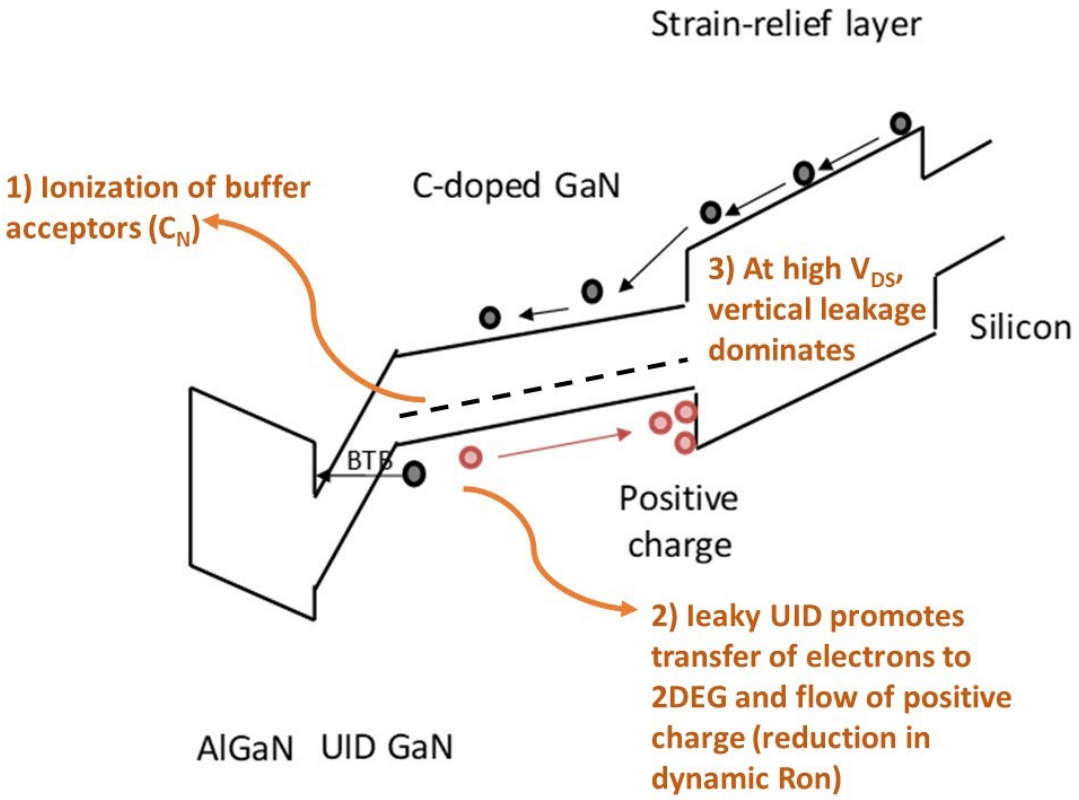
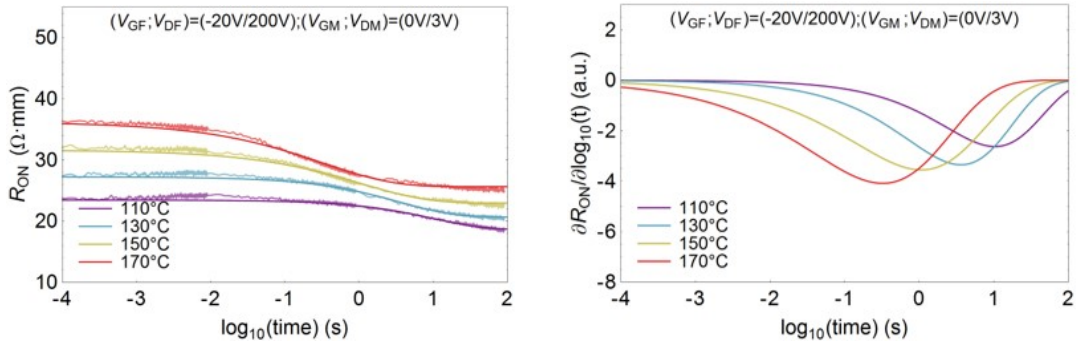


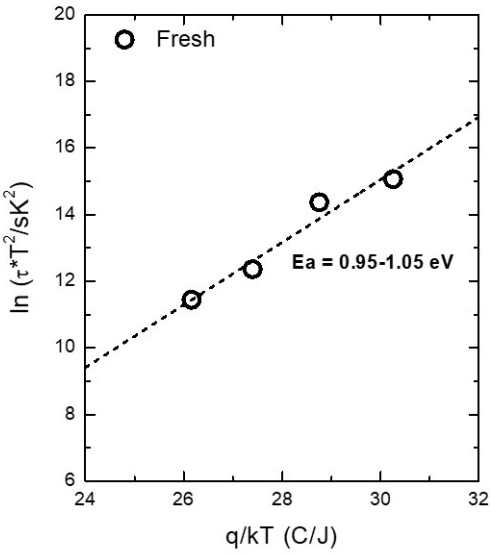
Figure 3.16 – Schematic model explaining the non-monotonic dependence of dynamic-Ron on the trapping voltage (V_{DS}): 1) In the off-state, at V_{DS}< 200 V, the C_N acceptors in the buffer are ionized, and this includes a significant increase in dynamic-Ron. 2) For higher V_{DS}, electrons in the C-doped buffer can transfer to the 2DEG either through BTB or trap-assisted leakage. As a consequence, positive charge(holes or ionized donors) are formed at the interface with the strain relief layer, and this induces a decrease in dynamic-Ron. 3) For higher V_{DS}, vertical (drain to substrate) leakage becomes relevant [61].

The physical origin of the decrease in dynamic-Ron is characterized by means of drain current transient measurements. DCT measurements were performed with (V_{GSQ},V_{DSQ}) = (-20 V, 200 V) (corresponding to the maximum dynamic-Ron before radiation) and Tamb ranging from 110°C to 170°C step of 20°C with time constants in the range 0.1-10 s (see Figure 3.17a, Figure 3.17b). One trap level, having activation energy of 1.05-1.1 eV, was detected and is correlated to the carbon acceptors in the buffer (C_N traps, [53]) (Figure 3.17c). No trap level state was detected after the proton irradiation (1.5×10^{14} p/cm^2), which is in accordance to the total suppression of dynamic Ron.

Proton irradiation did not change the DC performance of the devices. Both threshold voltage and lateral/vertical leakage components showed a good stability, as demonstrated by Figure 3.18, which refer to the maximum fluences used in this analysis. No significant variation was detected, indicating a good stability of the devices and a high robustness to proton irradiation. Figure 3.18b indicates that no significant change is observed after stress in gate, drain, source and vertical leakage.

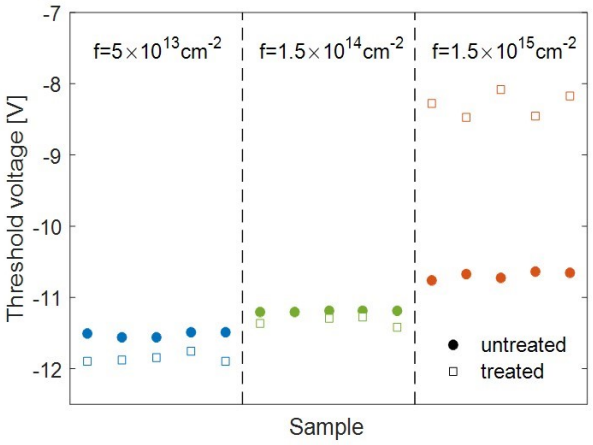


(a) (b)

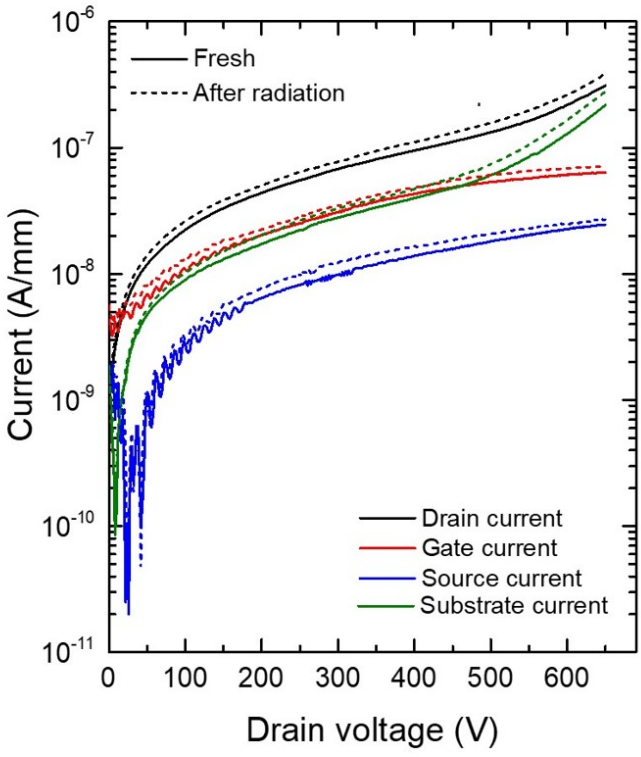


(c)

Figure 3.17 – (a) drain current transient measurements and (b) corresponding spectra measured at V_{DS}= 200 V, showing the existence of a dominant buffer-related trapping process (ionization of the C_N acceptors), which is responsible for high dynamic Ron. (c) Arrhenius plot of the defect responsible for peak dynamic Ron, with activation energy around 0.95 eV.



(a)



(b)

Figure 3.18 – a) Threshold voltage measured before and after the irradiation test at the highest fluences b) leakage current components measured in the off-state (V_{GS}= -20 V) before and after radiation.

In order to analyze the dynamic ON-resistance, pulsed I-V measurements have been performed at 150°C (the worst case for dynamic-Ron) [66] before and after proton irradiation up to V_{DSQ} = 600 V (pulse times: ON=20 μs, OFF=2 ms), the I_D-V_D before and after irradiation at room temperature and high temperature are reported in Figure 3.19. Figure 3.20a shows a current collapse before irradiation on the device at T= 150°C while Figure 3.20b shows no current collapse after irradiation, indicating total suppression of the dynamic-Ron post irradiation. This effect is for the first time reported in [37, 61] (this work). Figure 3.20c and Figure 3.20d report the results of pulsed-I-V measurements carried out on four devices with different gate drain distance (L_{GD} =15-20 μm) before and after radiation at T=150°C. As can be noticed, the dynamic-Ron is completely superimposed after radiation at 1.5×10^{14} p/cm^2. Figure 3.21 shows the pulsed-IV measurements carried out on 5 devices/wafer before/after radiation at different fluences. As can be noticed, proton implantation at the highest fluence induces a complete suppression of dynamic-Ron, even at 600 V /150°C.

The physical origin of the decrease in dynamic-Ron is characterized by means of drain current transient measurements. DCT measurements were performed with (V_{GSQ},V_{DSQ}) = (-20 V, 200 V) (corresponding to maximum dynamic-Ron before radiation) and Tamb ranging from 110°C to 170°C step of 20°C with time constants in the range 0.1-10 s (see Figure 3.22a, Figure 3.22b). One trap level, having activation energy of 1.05-1.1 eV, was detected which is correlated to carbon acceptors in the buffer which was clearly visible on the untreated devices (C_N traps, [28, 36]) (Figure 3.22c). No trap level state was detected after the proton irradiation (1.5×10^{14} p/cm^2) which results in a flat current transient and is in accordance to the total suppression of dynamic Ron [67]. In order to understand what changes in the devices after radiation, we carried out substrate ramp measurements. During substrate ramp tests, the devices are biased in the linear region, with V_{DS}=1 V, and V_{GS}=0 V. The drain current is measured while the substrate bias is ramped from 0 V to -800 V (go-sweep) and back to 0 V (return-sweep).

3.3.2 Substrate ramp

The substrate voltage influences the density of electrons in the 2DEG and, in turn, the drain current. If the coupling between substrate and 2DEG is purely capacitive (i.e. not influenced by trapping effects), the go-sweep and the return-sweep yield

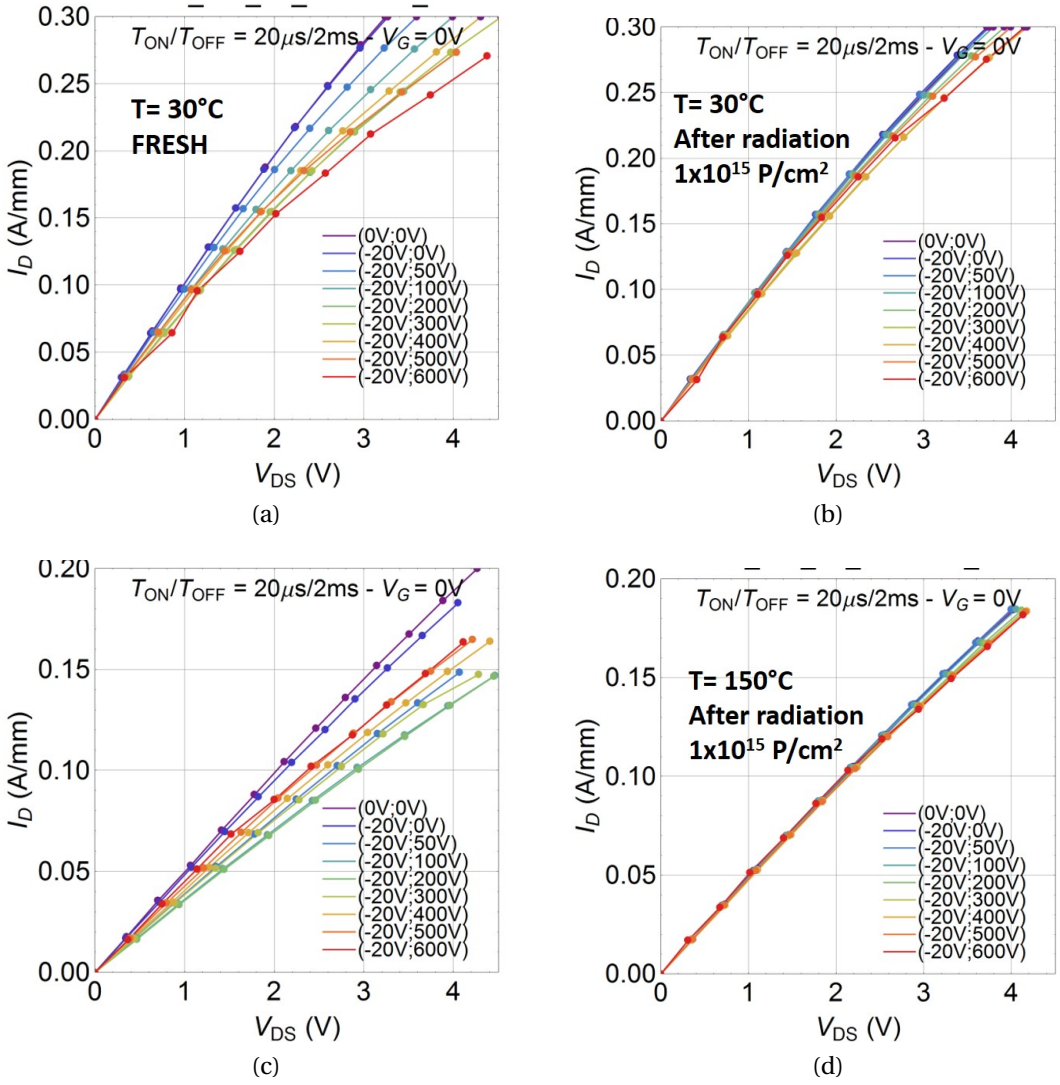


Figure 3.19 – Pulsed I_D-V_D curve measured at room temperature on representative device (a) before and (b) after radiation at 1.5×10^{15} p/cm^2. Analogous curves measured on the same device at Tamb = 150°C (c) before and (d) after radiation.

overlapping curves. If negative charge is stored in the C-doped buffer during the go-sweep, the drain current during the return-sweep is significantly lower, due to the partial depletion of the 2DEG induced by the electrons trapped in the buffer. If positive charge is stored in the buffer during the go-sweep, the opposite behavior is observed, i.e. the drain current is higher during the return-sweep, due to the effect of positive carriers. Substrate ramp testing represents a reliable method to understand if buffer-trapping is dominated by the storage of positive or negative charges [53]. Substrate ramps were measured on untreated and irradiated devices.

The results (Figure 3.23a) show that negative charge trapping in the buffer (ionization of carbon acceptors) dominates in the untreated devices. Remarkably, on the irradiated devices (Figure 3.23b) the opposite behavior is observed, and the trapping of positive charges is dominant. The results obtained within this measurement can be explained as follows (see Figure 3.24). When the transistor is in the off-state, negative charges are stored in the buffer, due to the ionization of the C-acceptors. The overall increase in dynamic-Ron depends on the balance between the trapping and de-trapping rates under off-state conditions. If there is a bottleneck that prevents de-trapping, a significant increase in dynamic-Ron takes place [56]. On the contrary, if trapped charge can easily be extracted when the device is in off-state (e.g. via high leakage current), this results in a smaller dynamic-Ron.

1. Before proton treatment (Figure 3.24a), the uid-GaN layer is highly insulating, and prevents the transfer of the trapped electrons from the buffer to the 2DEG (which is at high potential, 100-200 V). As a consequence, the trapped electrons can leave the buffer only after the high drain bias is removed (trapping rate is higher than the de-trapping rate in off-state), and this leads to an increase in dynamic Ron.

2. Proton irradiation increases the leakage through the uid-GaN channel layer (Figure 3.24b). In a 2DEG, holes or ionized donors can pile-up at the interface between the C-doped GaN and the strain-relief layer [68]. These two processes lead to a reduction of the overall amount of negative charge that is trapped when the device is in the off-state, and thus to a suppression of dynamic Ron. Since the C-doped GaN is highly resistive, the increase in the conductivity of the uid-GaN layer does not lead to an increase in the drain and vertical leakage current (see Figure 3.19b, which is consistent with the results in [40]).

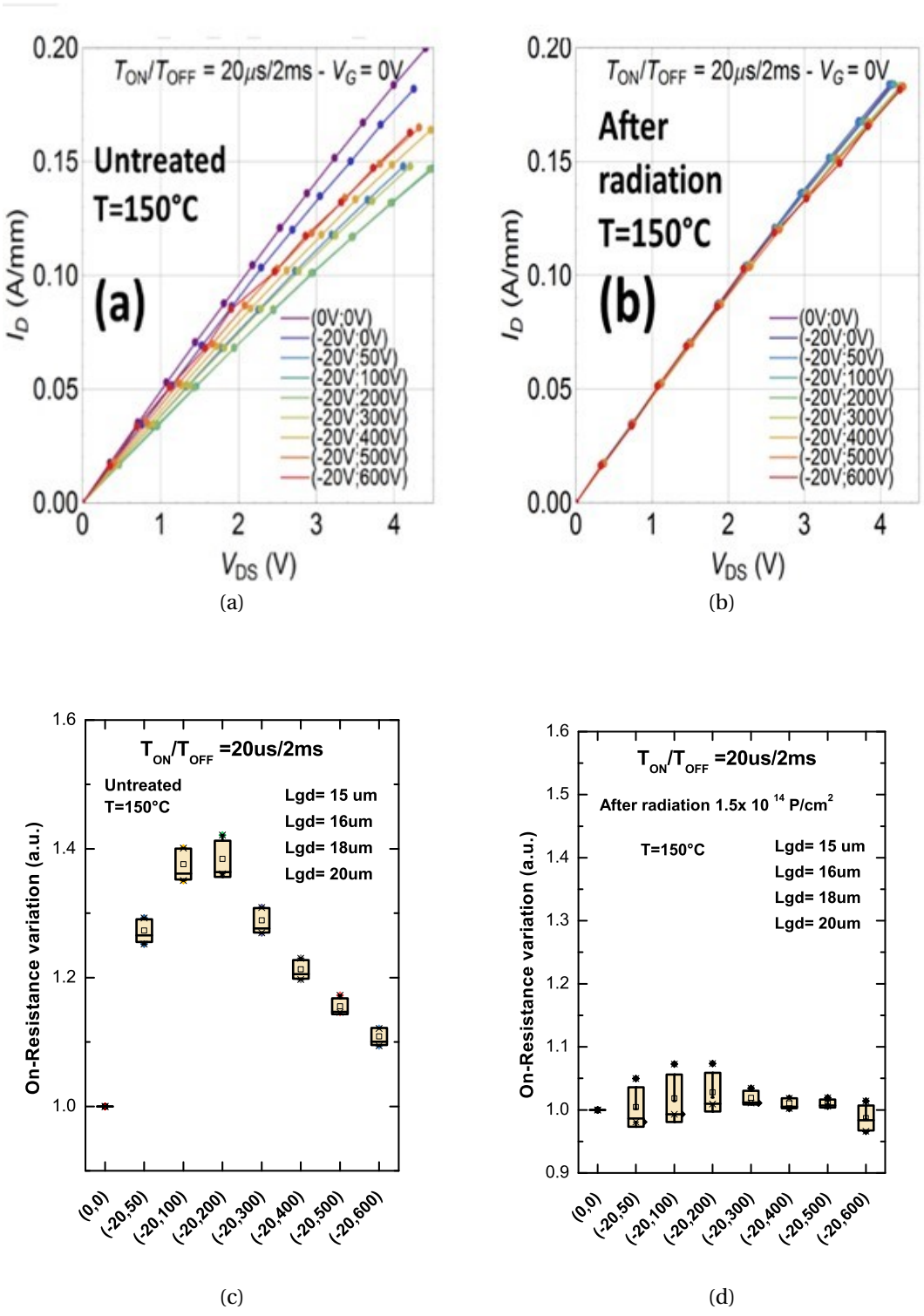


Figure 3.20 – (a) current collapse before radiation at 150°C; (b) current collapse after radiation at 150°C. Variation of dynamic Ron, with the quiescent bias up to 600 V for different L_{GD}. (c) untreated devices, (d) after radiation at T= 150°C.

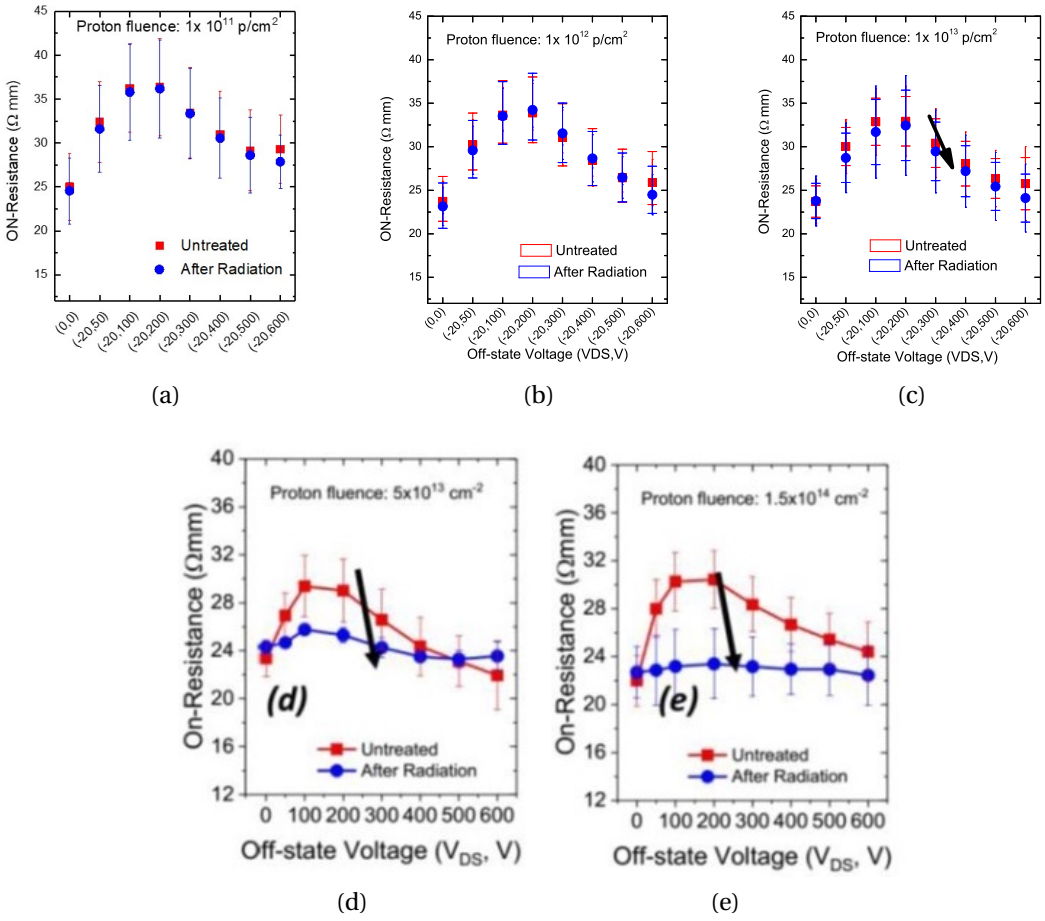


Figure 3.21 – dynamic-Ron measurement as a function of the trapping bias on untreated samples and after radiation at different fluences. (a) Fluence = 10^{11} cm^{-2}; (b) Fluence = 10^{12} cm^{-2} (c) Fluence = 10^{13} cm^{-2} (d) Fluence = 5×10^{13} cm^{-2} (e) Fluence = 1.5×10^{14} cm^{-2}; All measurements were carried out at 150°C. As can be noticed, proton implantation at the highest fluence induces a complete suppression of dynamic-Ron, even at 600 V/150°C.

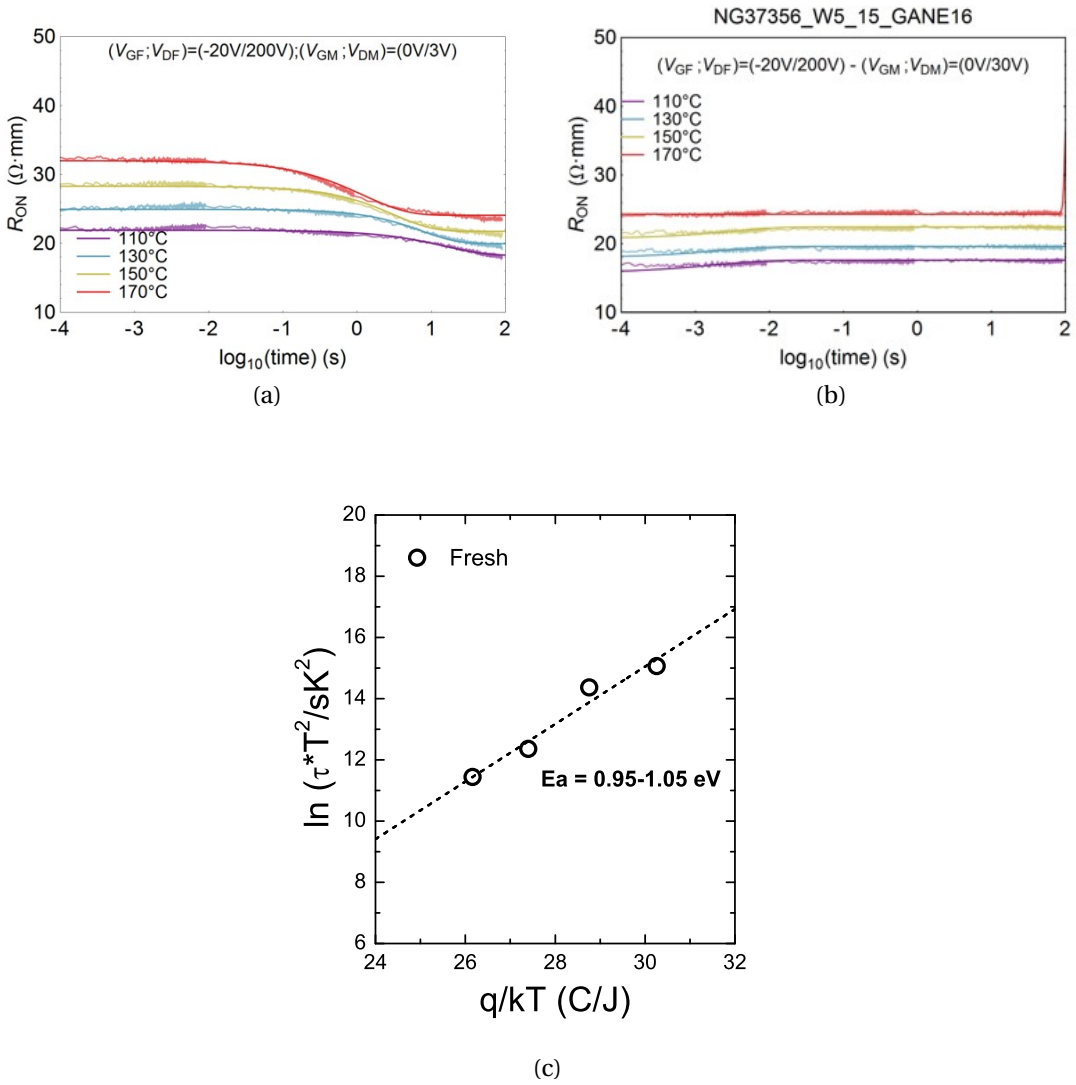
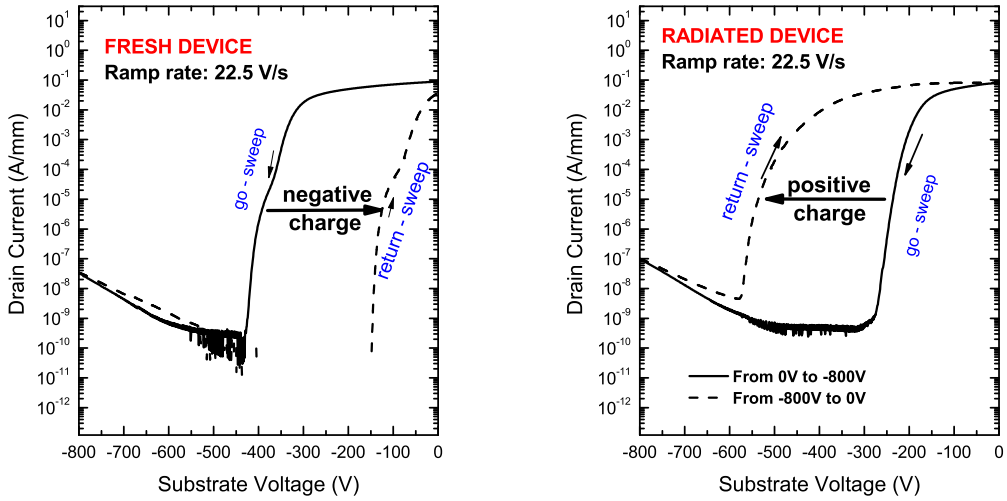
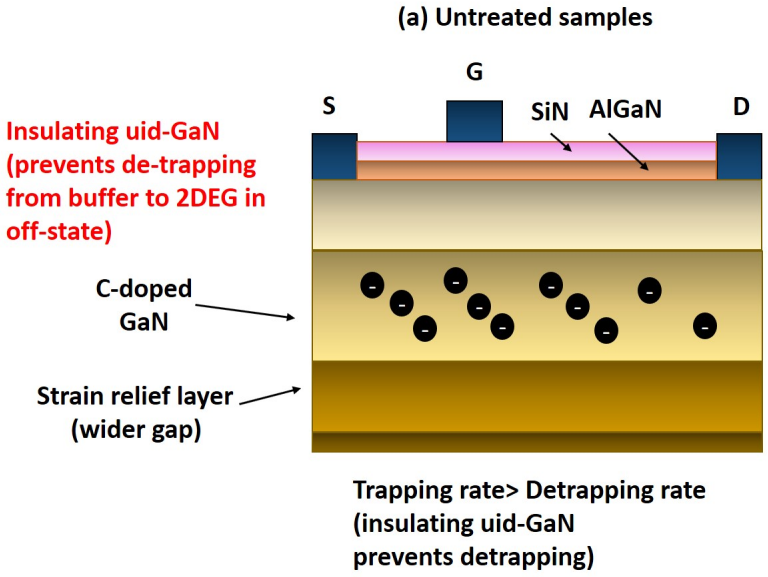


Figure 3.22 – Drain current transient measurement before and after radiation at V_{DSQ} = 200 V.(b) no detectable trap level states shows after irradiation. (c) Arrhenius plot of the defect responsible for peak dynamic Ron, with activation energy around 1.05 eV.

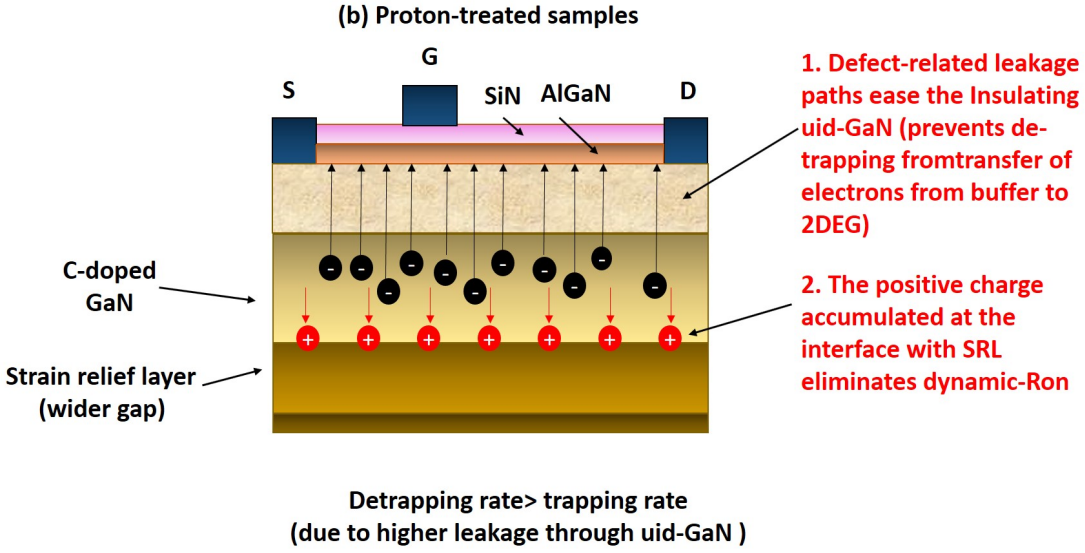


(a) (b)

Figure 3.23 – Substrate ramp caried out a) on an untreated sample and b) after proton irradiation at the highest fluence. Before irradiation, a negative substrate sweep induced a rightwards shift of the curve, indicating a significant trapping of negative charge (from the ionization of the buffer acceptors). b) after radiation, a negative substrate sweep induced a leftwards shift of the curve, due to the increase in positive charge. Such positive charge originates from the increase in the leakage of the uid-GaN channel layer.



(a)



(b)

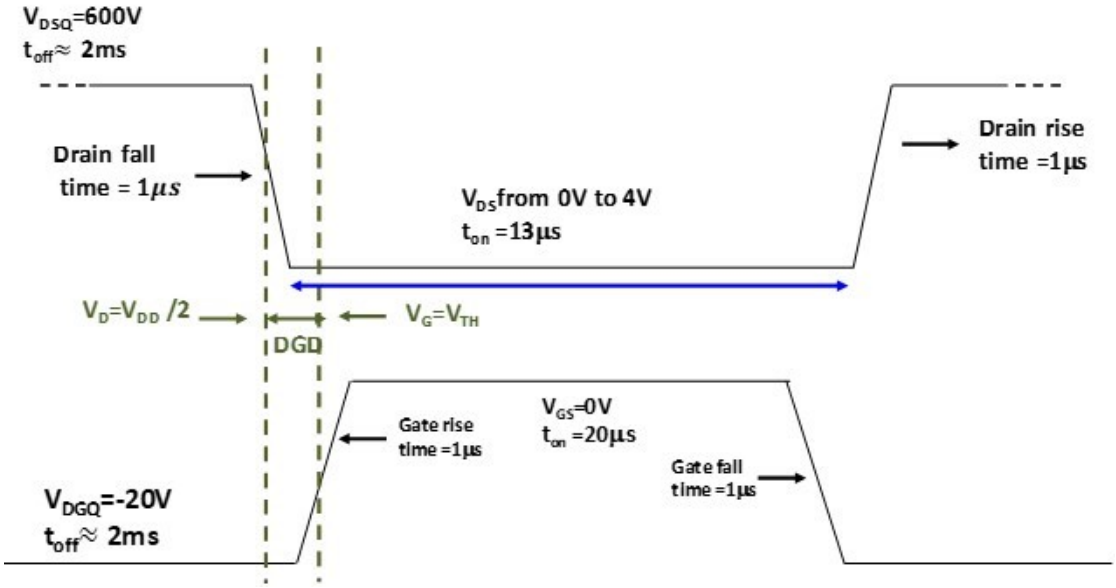
Figure 3.24 – Schematic representation of the process responsible for reduced dynamic-Ron after proton irradiation. Before irradiation, the uid-GaN is insulating, and prevents the transfer of electrons from the buffer to the 2DEG when the device is in the off-state. After radiation, the increased leakage through the uid-GaN leads to an increase in the de-trapping rate. Positive charge is also accumulated at the interface between c-GaN and SRL.

3.3.3 Hard switching

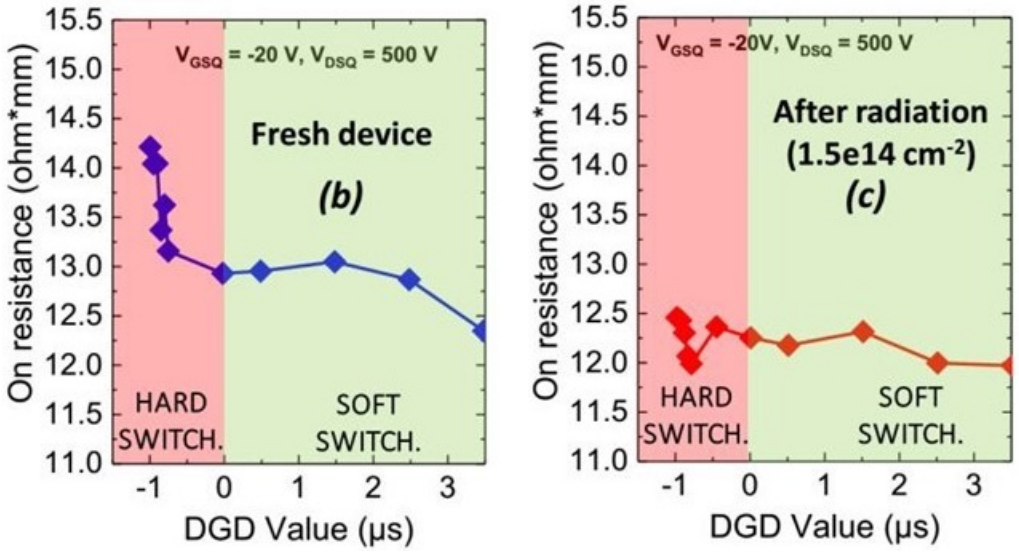
Proton treatment was found to have a beneficial impact also on the hard switching performance, which (Figure 3.25a) was evaluated by biasing the devices under square-wave operation. We gradually decreased the interval between the drop in drain voltage and the turn-on of gate bias (referred to as drain-gate delay, DGD, Figure 3.25a), in order to move from soft-switching (DGD>0) to hard-switching (DGD<0). DGD levels in the μs range were used to maximize the impact of hard switching. As shown in Figure 3.25b, the untreated devices showed a significant increase in their dynamic-Ron when submitted to hard switching at 500 V (see the values for DGD<0), compared to the case of soft switching (DGD>0). The additional dynamic-Ron detected during hard switching is ascribed to the trapping of hot electrons in the buffer [66]. After proton treatment (Figure 3.25c), the de-trapping of electrons from the buffer becomes easier, and this results in a negligible dynamic-Ron increase during hard switching.

3.3.4 Optical characterization

The impact of proton radiation on the device performance was studied by means of emission microscopy. The electroluminescence (EL) signal was detected for several gate and drain voltage levels. In the discussed analysis the drain voltage levels range from 50 V to 200 V are used to investigate the presence of hot electrons before/after proton irradiation [31], see Figure 3.25b; the gate voltage levels were chosen according to the threshold voltage of the devices and to the dissipated power (not to induce device degradation). An acquisition time of 25 s and an EM gain of 200 were used. We plot the EL signal as a function of the difference between the gate and threshold voltage (V_{GS}-V_{TH} level). After the radiation the samples irradiated at 1.5×10^{14} p/cm^2 show a higher EL signal, which is indicative of a higher electron current/energy, also a consequence of the reduction of the trapping phenomena [40, 66]. Irradiated samples have less trapping, i.e. less virtual gate leakage, i.e. higher electric field for the same drain voltage. For this reason, the EL signal is higher in the irradiated samples. On the other hand, having less defects, the irradiated device has less hot electron trapping (or an easier de-trapping). Figure 3.26c shows the false color EL maps (a) current collapse before radiation at 150°C; (b) current collapse after radiation at 150°C [69]. The results showing the distribution of the EL signal before and after radiation. an acquisition



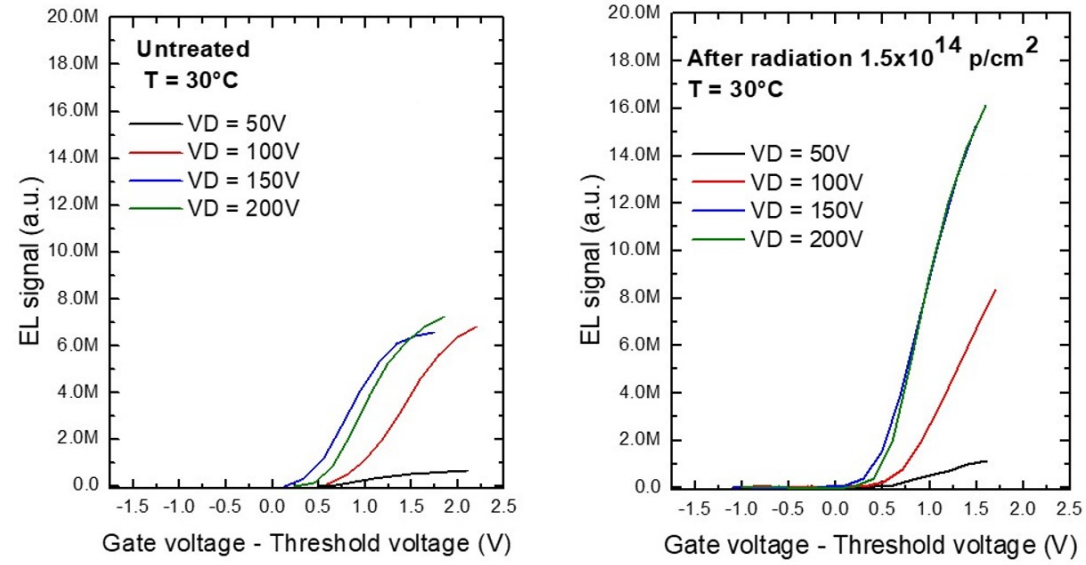
(a)



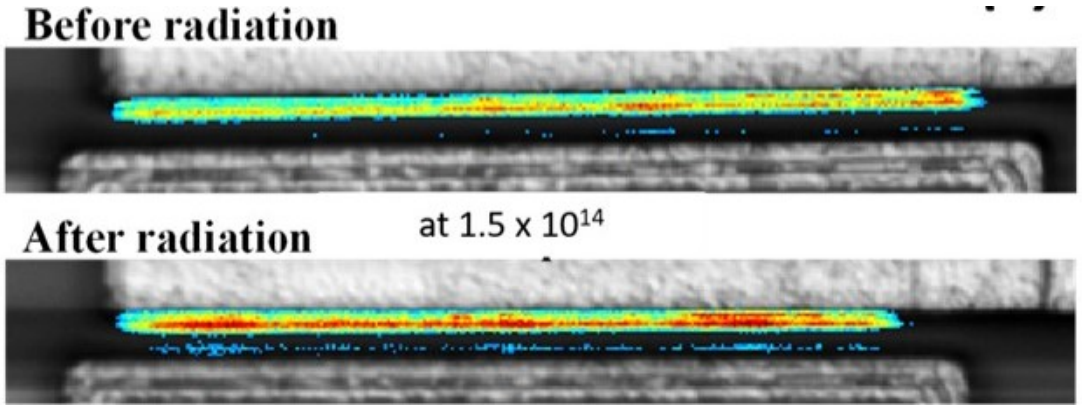
(b) (c)

Figure 3.25 – Schematic represe of the waveform timing used to test the hard switching behaviour of the devices b)and c) dynamic Ron induced by soft switching (drain-gate-delay, DGD> 0 s) and hard switching (DGD< 0 s) on b) an untreated sample and c) a sample submitted to the highest radiation fluence. After radiation, the device dose not show any significant increase in dynamic-Ron in hard switching, contrary to the untreated sample.

time of 25 s and an EM gain of 200. The electroluminescence signal increased on the device after radiation from 8 M to 18 M for instance at VD = 200 V.



(a) (b)



(c)

Figure 3.26 – EL intensity versus gate voltage overdrive at different drain voltage on a GaN HEMT. (a) before radiation at VD from 50 V up to 200 V (b) the samples after radiation show a higher EL signal. (c) false color EL maps showing the distribution of the EL signal before and after radiation. an acquisition time of 25 s and an EM gain of 200.

3.3.5 Capacitance characterization

As we have seen dynamic performance of the device significantly changes after radiation at the highest proton fluence. Now the question is, does the behavior of the capacitance versus voltage curve change after radiation and/or with proton fluence?

Capacitance analysis was performed at room temperature on fresh devices and on samples submitted to radiation at the highest proton fluence. In order to evaluate the C-V behavior two different configuration were used, namely: (i) two terminal we applied gate voltage at 0 V; the source is floating the and drain voltage sweeped up to 200 V; (ii) three terminal with 0 V; at source at room temperature. We demonstrated the following relevant results: (i) No significant change is observed in behavior of the C-V curve measured in devices before (fresh) and after proton radiation. (ii) A slight change is observed in devices tested at the highest proton fluence. Figure 3.27 shows the integral of the C-V curve demonstrates that although with different intensity, consistent results are observed in the 2-terminal and 3-terminal analysis. We can notice the devices before radiation demonstrate a dependency to the cell position and a more relevant variation is calculated after radiation at the highest fluence [45].

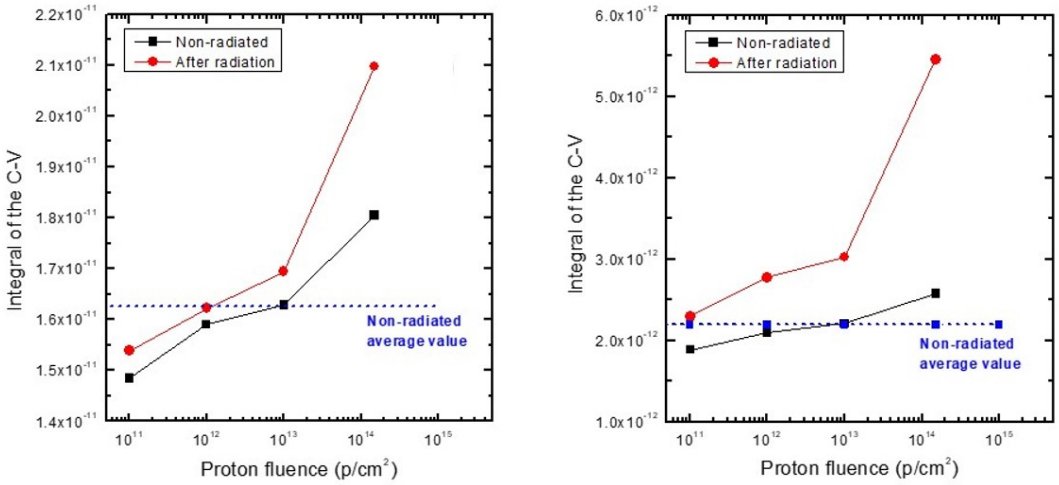


Figure 3.27 – Integral of the C-V curve (a) 2-terminal (b) 3-terminal, demonstrates that although with different intensity, consistent results are observed in the 2-terminal and 3-terminal analysis.

3.3.6 On-resistance on power bars devices

The on-resistance variation of large power transistors in the vicinity of the irradiated area is shown in Figure 3.28. A circular pattern of increasing dynamic Ron at V_{DS} = 200 V is visible spreading outward from the two irradiation zones. The highest

proton fluence corresponds to the lowest dynamic Ron. For die in the irradiated zone, devices with smaller gate/drain spacing (L_{GD}) exhibit a larger Ron decrease. This can be seen when comparing devices below (L_{GD} = 20 μm) to those above (L_{GD} =14 μm) the irradiated cells indicated with arrows. The inset of Figure 3.28 shows the source leakage at V_{DS} = 200 V after normalization of the leakage with respect to the median of the leakage distribution at every L_{GD}, to filter out the L_{GD} dependency to the drain leakage. So, the color of each cell represents the relative drain leakage with respect to all the other devices measured with the same L_{GD}. A similar pattern arises, corresponding to a higher drain-to-source leakage close to the impact zone, which gradually decreases with distance from the latter.

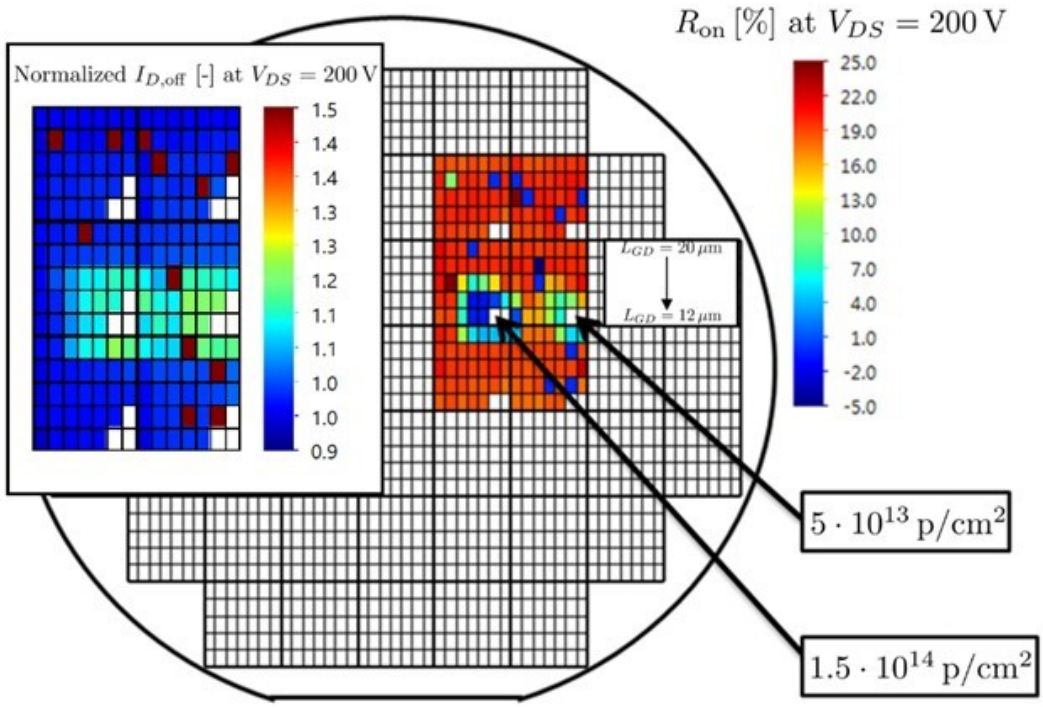


Figure 3.28 – Wafer map of the on-resistance variation at V_{DS} = 200 V and T = 150°C on large power transistors (W=140 mm). Inset: source leakage at V_{DS} = 200 V normalized with respect to the median of all devices with the same L_{GD}.

The graph shows the off-state drain leakage of large transistors as a function of their measured Ron variation at V_{DS} = 200 V and T = 150°C. The distinction is made between devices out of and within the vicinity of the impact zone of both proton beams. Overall, devices that are irradiated with the highest proton fluence correspond to the cloud with lowest Ron combined with a high $I_{D,off}$ at V_{DS} = 200 V. Shorter L_{GD} devices show

the lowest dyn-Ron after irradiation. It means that the shorter L_{GD} corresponds to a shorter region for trapping, and therefore the dynamic-Ron is not strong when L_{GD} is short. The effects are reproduced on several batches of proton irradiation, and they are very consistent. We believe that dynamic Ron in the non-treated devices results from the absence of de-trapping process due to the uid acting as an insulator thus preventing the vertical transfer of electrons – at high trapping bias – from buffer to the 2DEG [68]. The irradiated devices exhibit a reduced dynamic Ron thanks to a process of de-trapping induced by well-controlled but minute increase of leakage in the uid layer. In this case, the transfer of electrons is not vertical (from buffer to 2DEG) but lateral (from source to drain). The blue dots represent devices located far away from the proton impact zone. Green and red dots represent devices within the close vicinity of the irradiation beam center with fluences of 5×10^{13} cm^{-2} and 1.5×10^{14} cm^{-2}, respectively. Several observations can be made:

1. Dynamic Ron is reduced within vicinity of the proton beam and improves with increasing proton fluence.

2. Off-state drain leakage current increases with vicinity towards the proton impact zones.

3. Dynamic Ron decreases with decreasing gate drain spacing after proton irradiation. The first two observations have been thoroughly explained throughout this section, the last deserves some special attention. Devices with shorter gate-to-drain distance exhibit larger lateral fields, favouring a larger region where positive charge build-up at the bottom of the C:GaN layer occurs. Hence, the effect of the positive charge build-up is larger on devices with short L_{GD}, or alternatively, they have lower dynamic Ron.

We have observed that irradiating small transistors with high proton fluences leads to a complete suppression of the dynamic Ron. The impact of proton irradiation on the dynamic Ron is schematically explained in Figure 3.29. The “leaky dielectric model” [68] is based on the GaN:C being highly resistive and strongly compensated. It suggests that the dynamic Ron under high voltage off-state bias originates from the voltage drop between the 2DEG and the GaN:C layer, resulting in a negative depletion

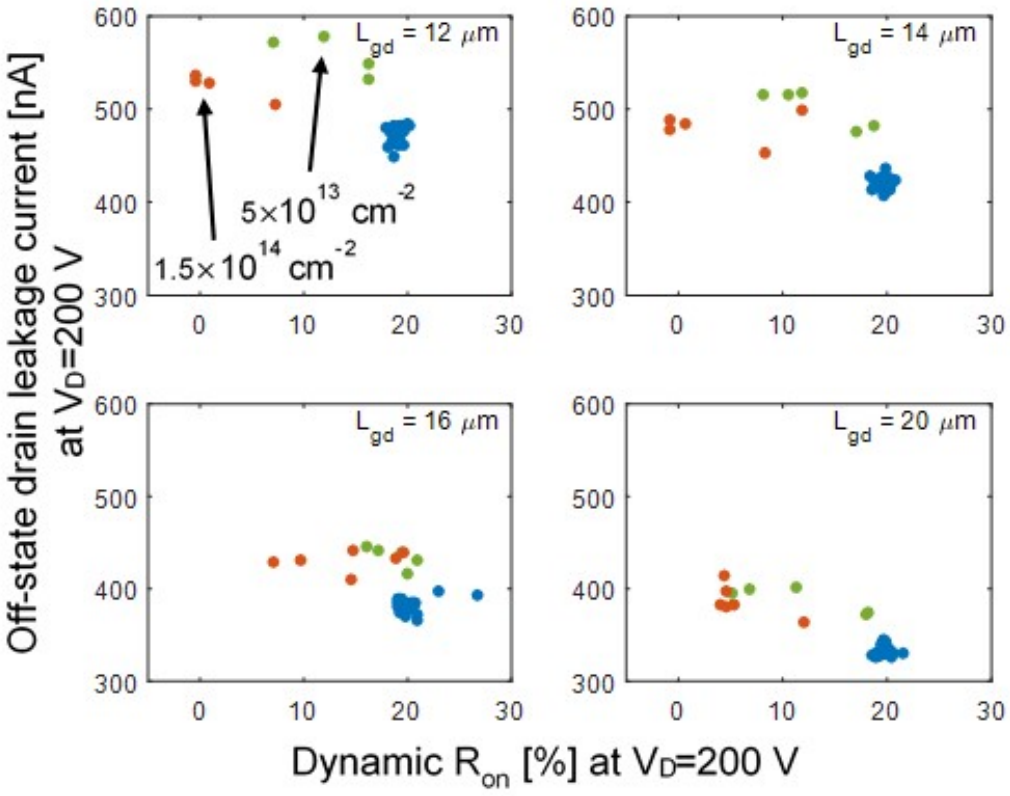
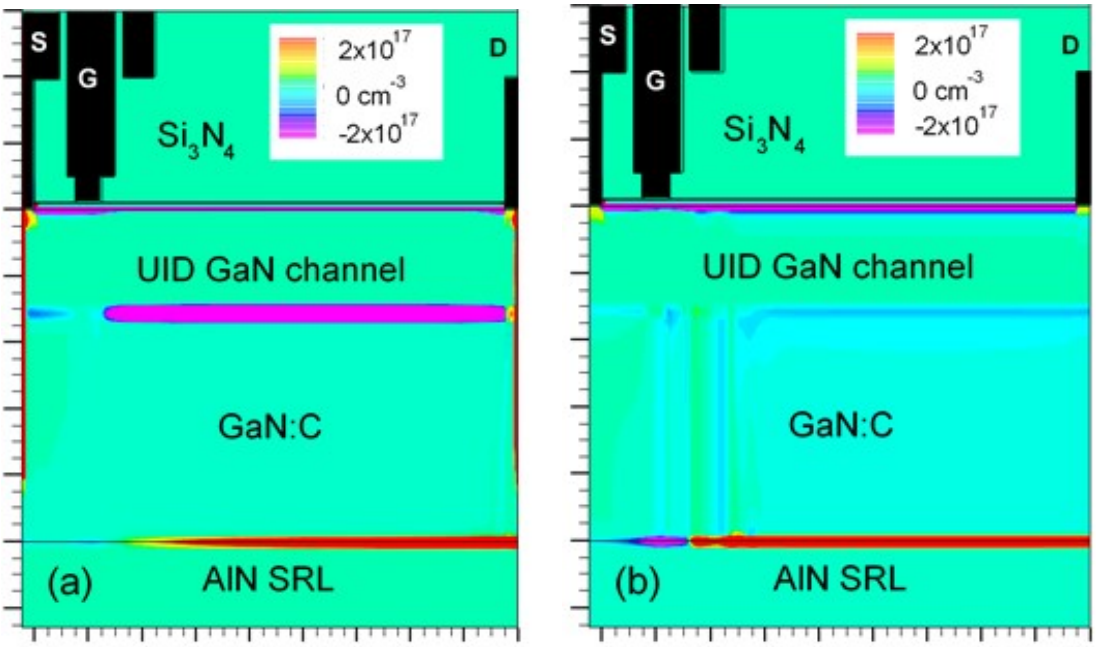


Figure 3.29 – Off-state drain leakage at V_{DS} = 200 V and T = 150°C on large power transistors (W=140 mm). Blue dots represent large transistors out of the vicinity of any impact zone, while red and green dots represent those in the direct vicinity of the impact zone with proton fluence of 5×10^{13} p/cm^2 and 1.5×10^{14} p/cm^2, respectively.

charge of ionized C_N acceptors at the top of the GaN:C layer. This negative charge can be present along the complete gate-to-drain access region but will be concentrated in the vicinity of the gate. At the same time, the field dropped across the SRL between the GaN:C and the Si results in the neutralization of ionized C_N acceptors at the bottom of the GaN:C layer, exposing positive compensating donor charge. The resulting build-up of positive charge increases from gate to drain. It is this interplay between negative and positive charge that explains the bell-shaped curve in dynamic Ron. Furthermore, it is suggested in [68] that the best solution to minimize dynamic Ron is to have a combination of a slightly conductive (or "leaky") GaN UID layer in combination with an insulating strain relief layer. This would allow the 2DEG to remain in electrical contact with the top of the GaN:C layer, under which condition the negative charge

build-up i.e. ionization of the C_N acceptors, would not occur. Tuning of the resistivity of the GaN UID layer is hence key to minimize dynamic Ron. In fact, the requirement for full suppression is that the resistivity of the UID GaN layer is less than or equal to the GaN:C layer over the entire desired operating bias and temperature range. We achieved this condition by subjecting the wafers after complete processing to well-controlled proton irradiation. Higher proton fluences cause more damage to the lattice, further enhancing the conductivity.



(a) (b)

Figure 3.30 – TCAD simulated cross-section depicting the total charge density distribution 1 μs after resistive switching from (V_{DS},V_{GS}) = (200 V,-5 V) to (1 V,0 V). (a) Situation with insulating UID GaN channel, where the 2DEG is pinched off by the negatively ionized C_N acceptors at the top of the GaN:C layer. (b) Situation with a leaky UID GaN channel, in which the negative charge build-up at the top of the GaN:C layer does not occur [70].

3.4 Conclusion

As described above, proton treatment at 3 MeV was found to have a beneficial impact on the dynamic performance of GaN HEMTs, up to a fluence of 1.5×10^{14} cm^{-2}. Fluences higher than 10^{15} cm^{-2} induced a complete suppression of dynamic-Ron,

but also a permanent shift (+2 V) of threshold voltage, possibly due to a permanent degradation of the insulator/semiconductor interface. For this reason, fluences in the range $10^{13} - 10^{14}$ cm^{-2} are recommended to suppress dynamic-Ron without altering the DC characteristics of the devices. For the first time we demonstrated that proton irradiation can be effective for suppressing the dynamic Ron in GaN-based power transistors. The decrease in dynamic-Ron after irradiation is ascribed to the increase in the leakage through the uid-GaN layer, which results in an increase in the de-trapping rate under off-state conditions. We demonstrate that proton irradiation is an effective and controllable way to reduce dynamic-Ron in AlGaN/GaN HEMTs. The effect is studied by means of combined pulsed characterization, transient measurements and EL on untreated and irradiated devices. We demonstrate the following relevant results : the electroluminescence signal is increased on the device after radiation, while dynamic-Ron in AlGaN/GaN HEMTs is decreased after irradiation; this beneficial effect is ascribed to the minute increase in the leakage of the uid-GaN layer, promoting charge de-trapping from the buffer. No trap level state was detected after the proton irradiation (1.5×10^{14} p/cm^2) by means of drain current transient. These observations are confirmed on large power devices, where additionally the effect of both the off-state drain leakage current and the dynamic Ron can be seen in the vicinity of the proton impact zone.

4 Reliability of Normally-Off GaN HEMTs with p-Type Gate

Owing to the positive and stable threshold voltage, the low on-resistance and the high breakdown field of p-GaN gate, GaN-based transistors are commonly accepted as promising devices for application in power converters [55, 71]. In this section, technological issues related to the development of a p-GaN gate, and solutions for minimizing the gate leakage current will be discussed. The chapter will be continued with a discussion on the most relevant mechanisms that limit the dynamic performance and the reliability of GaN-based normally-off transistors.

For a massive adoption of GaN transistors it is important to study the reliability and stability of these devices which, during operation, may cross different V_{GS} and V_{DS} ranges [72, 73]. In particular, during a hard switching transition, the device might be simultaneously subject to a high drain voltage and a high drain current, thus resulting in significant field-and hot-electron effects [31, 74, 75]. To better understand the issue, let's consider a simple example of a boost power converter based on a normally-off HEMT as show in Figure 4.1 along with its V_{DS} and I_D waveforms during a switching event [74].

The following observations should be noted:
1. When the transistor is in the off-state (condition (1) in Figure 4.1), the input voltage V_{in} (for instance 600 V) appears between drain and source, and no current flows through the transistor while a high drain-source voltage is applied to the HEMT. The high resulting field (Figure 4.2) may lead to charge trapping mechanisms, by filling or depletion of defects located in the C-doped buffer [51] due to the injection of electrons

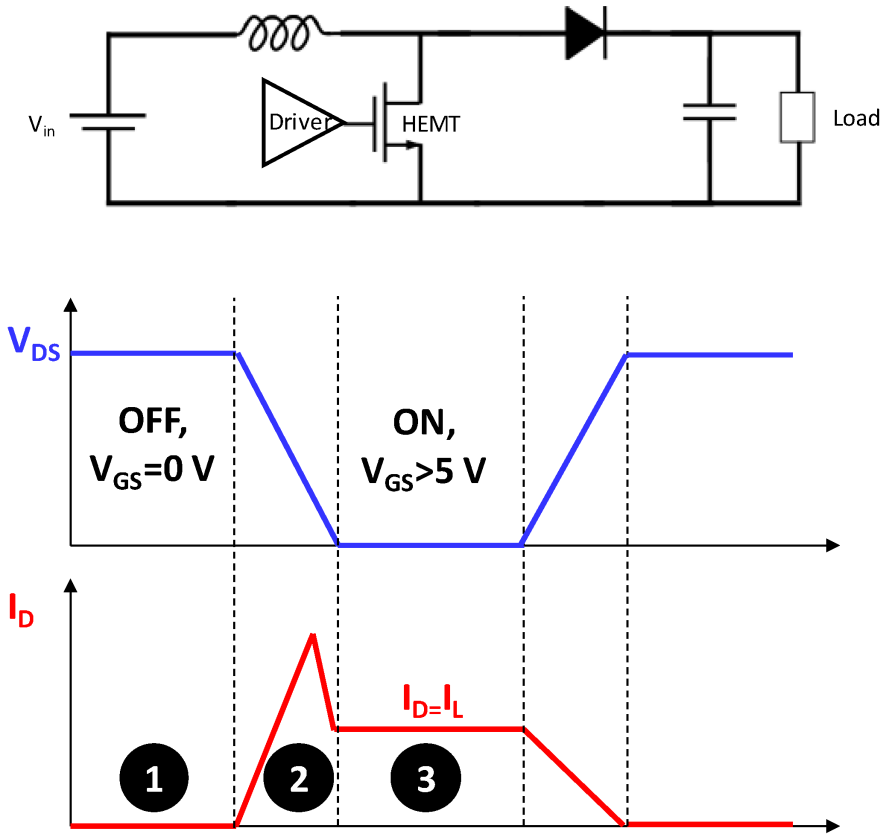


Figure 4.1 – Schematic representation of a boost power converter and of the switching transitions during operation [74].

from the substrate [76], and surface trapping processes [75]. These mechanisms are typically fully recoverable. In addition, the exposure of the transistors to a high off-state bias may trigger the time-dependent degradation processes that lead to a permanent failure of the transistors [77].

2. During the turn-on condition, the voltage on the drain (V_{DS}) of the HEMT drops from input voltage to a very low or almost zero voltage while the drain current I_D increases and reach to the inductor current (see in Figure 4.1). The peak of the current is related to the discharge of the drain-source capacitance through the channel [78]. This transition is not immediate and the device experiences the presence of high current and high voltage simultaneously, which might leads to the hot electron degradation and charge trapping affected by the hot-electrons. This also results in a power dissipation in the device. Indeed, in the hard switching event (2 in figure 5.1), current and voltage should never be high, simultaneously.

3. During part 3 in figure 5.1 the device is in the on-state condition, there is a positive bias on the gate-source junction between 5-7 V. This may lead to a time dependent degradation resulting in an increase of the gate leakage current (discussed more in [79]).

Usually the GaN HEMT which used in power converters should be normally-off for the safety reason. For instance if the gate driver fails and there is no output, so the HEMT switches to the off-state. In this case if there is a AlGaN/GaN heterojunction for the HEMT structure, the device shows a normally-on behavior. In fact, when the gate bias is zero, the 2DEG is formed at the AlGaN/GaN heterojunction, this is due to the spontaneous and piezoelectric polarization of nitrides. To attain the normally-off devices, there are several ways which have been suggested during last years:

1. One of these solutions is the implantation of fluorine ions under the gate. In this way the negative charge of the F-ions under the gate, shift the threshold voltage to a positive value. However, while improving the threshold voltage significantly, it has been reported that the high electrical stress results in a change in the threshold voltage. Chen *et al.* in [80] have demonstrated an excellent stability by the F-plasma ion implantation.

2. Another way to achieve a normally-off HEMT devices is to use the MIS-type gate stack, by D-mode and E-mode recess of the gate AlGaN/GaN transistors. While this method decreases the gate leakage and the threshold voltage around one volt the device still suffers from the the positive bias temperature instability (PBTI) [81], the negative bias temperature instability (NBTI) [82] which are related to the trapping effect in the insulator, and time-dependent dielectric breakdown (TDDB) [79] for thin insulator.

One solution is the cascode system, combination of a Si MOSFET series to a normally-on GaN HEMT. This combines all the advantages of positive threshold voltage and high voltage capability and low on-resistance and the possibility of using standard Si drivers. The latter is well estimated for the fabrication process and the reliability issues. On the other hand, cascode complexity is the main drawback of the cascoded solution.

P-type doped GaN cap layer is introduced under the gate metal on the top of the AlGaN/GaN heterojunction. These devices show a significant improvement of threshold voltage. It means the p-GaN/AlGaN interface lifts up the energy band diagram thus results in a complete depletion of the 2DEG with a V_{GS} = 0 V and a positive threshold voltage. In fact, this stack is a back-to-back diode model, a metal/p-GaN Schottky diode combined with a p-GaN/AlGaN/GaN p-i-n diode [22]. At high reverse gate bias, the p-i-n diode blocks the gate current, while at high forward gate bias the Schottky diode is blocking.

From the scientific and industrial community point of view the P-GaN HEMT has been considered as a suitable normally-off solution, that is the reason that the investigation on the stability issues of these devices are very important.

4.1 Origin of Leakage Current of p-Gate AlGaN/GaN HEMTs

In order to obtain an enhancement mode device, which is more desirable in applications, a p-type doped GaN cap layer is introduced under the gate metal. However, while improving the threshold voltage significantly, high gate leakage values are reported despite the implementation of a Schottky gate. In this part, the origin of the reverse gate conduction mechanism is studied and linked to the perimeter-dependent part of the forward gate leakage. The latter is used in order to explain the dynamic pinch-off voltage behavior at high forward gate stress.

4.1.1 Device and stress procedure description

The study was carried out on p-GaN gated AlGaN/GaN grown on a silicon substrate with the gate width of 200 μm. The p-GaN top structure is similar to [83] and more information on the 6" 650 V rated GaN-on-Si buffer can be found in [56]. A schematic cross-section of the gate region in a p-GaN gated HEMT is depicted in Figure 4.2. In fact, the negative polarization charge at the p-GaN/AlGaN interface lifts up the energy bands, resulting in a positive threshold voltage. The p-type doped GaN layer acts as a depletion buffer for the Schottky junction. In essence, this stack is electrically equivalent to a back-to-back diode model: a metal/p-GaN Schottky diode combined

with a p-GaN/AlGaN/GaN p-i-n diode [22]. At high reverse gate bias, the p-i-n diode blocks the gate current, while at high forward gate bias the Schottky diode is blocking. The devices under analysis can be grouped into two types to investigate the gate leakage, the various device combinations for the analyzed samples are summarized in table 4.1: process A, on the Schottky metal/p-GaN interface and process B, improved the p-GaN sidewall. In these section we will compare these process variations with a reference process (the reference process is without these improvements) by means of an extensive electrical characterization. Devices with process A show an increased quality of the Schottky metal/p-GaN interface, primarily reducing the electron supply towards the edge of the p-GaN. Furthermore, devices with process B are fabricated, showing improved p-GaN sidewall roughness by passivation on top of the improved Schottky/p-GaN interface quality as seen in process A. In order to investigate a reverse gate condition mechanism, temperature dependent DC measurements are carried out on the devices. The dynamic pinch-off voltage behavior is studied by applying a forward gate stress double pulse and capturing the transfer characteristic in a very small time frame.

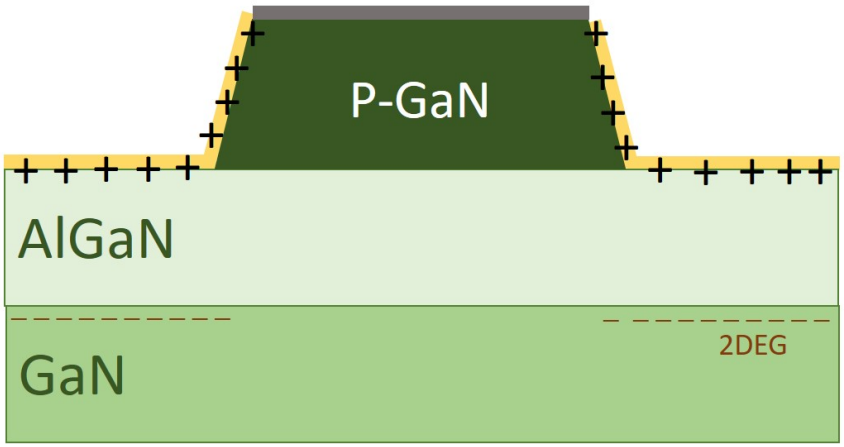


Figure 4.2 – Schematic representation of the p-GaN gate in AlGaN/GaN HEMT.

Table 4.1 – Overview of the process variations studied in this part [52].

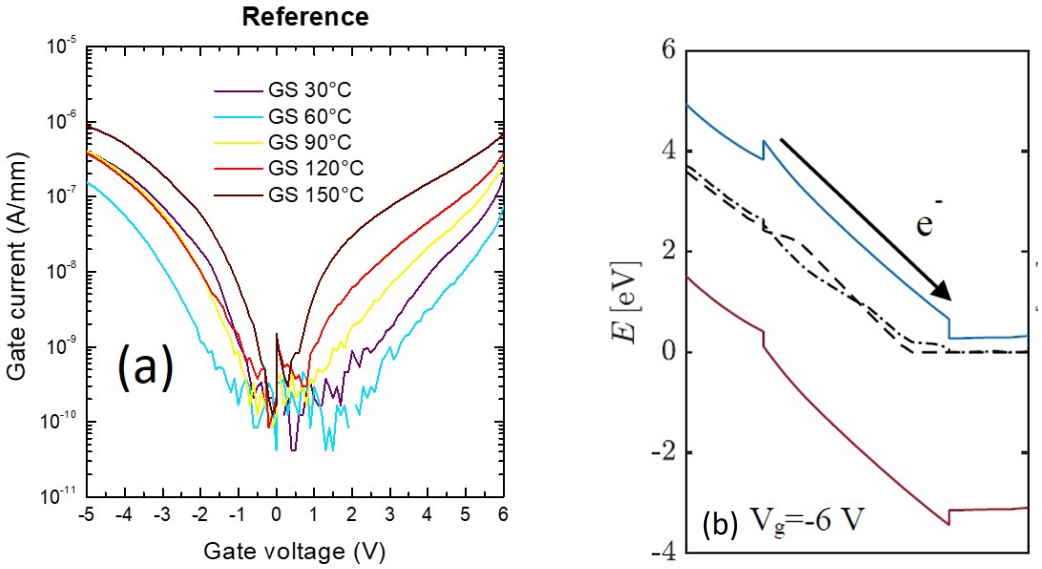
Process	Schottky barrier	p-GaN sidewall
Reference	ref.	ref.
A	improved	ref.
B	improved	improved

4.1.2 Reverse and forward gate bias

The reverse gate leakage current investigated by DC characterization at different temperatures. Figure 4.3 shows the diode characterization at different temperature for two samples on small devices. The reference structure transistor shows a high reverse leakage current (100 $^{nA}/_{mm}$ at V_G = -5 V at room temperature) which is dependent to the gate width. Concerning to the high electric field due to the polarization of AlGaN barrier [84]. Worth noting that the reverse gate leakage current shows a good fit to the Poole-Frenkel. Poole-Frenkel equation:

$$ln\left(\frac{J}{E}\right) = -\frac{q(\phi - \beta\sqrt{E})}{kT} + ln(c), \tag{4.1}$$

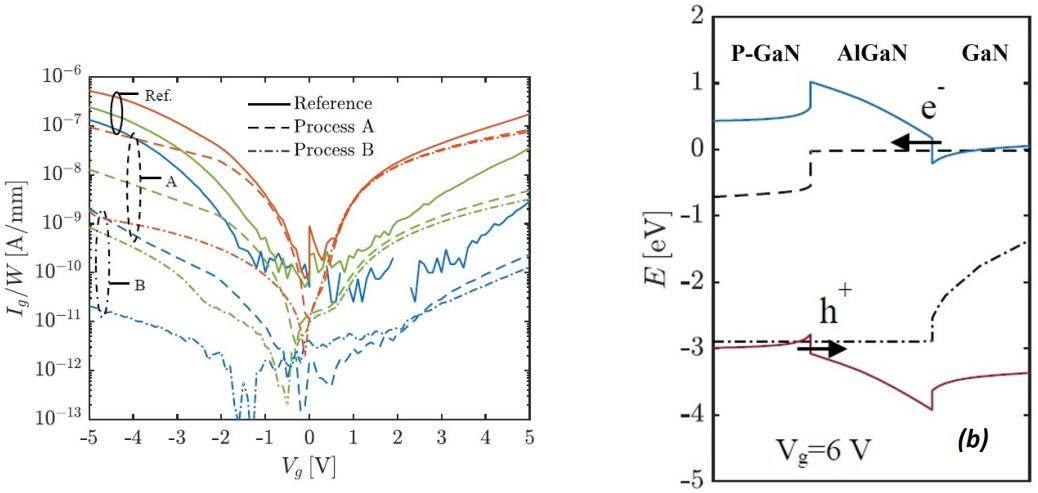
where, q is the elementary charge, k is the Boltzmann's constant, ϕ is the the trap depth, β is the Schottky factor and c is a prefactor. This is plotted in Figure 4.3 at different gate biases. A trap depth of 0.97 eV is extracted.



(a) (b)

Figure 4.3 – Gate current versus voltage on different processes for single finger transistors normalized by gate width at T=30, 90, 150 °C in blue, green and red, respectively. Measured at V_{DS}=0 V.

Such gradual leakage current is ascribed to the injection of electrons from Schottky metal near the gate edges along the p-GaN sidewall to the 2DEG, which is a field-driven effect. By improving the Schottky/p-GaN interface quality in sample A the electric field decreases which results in a reduction of the gate leakage current by two orders of magnitude. In order to eliminate the interface states, process B has been fabricated with additional p-GaN sidewall passivation step. The results in figure show the reverse gate leakage current is decreased by suppression of electron injection at the Schottky interface.



(a) (b)

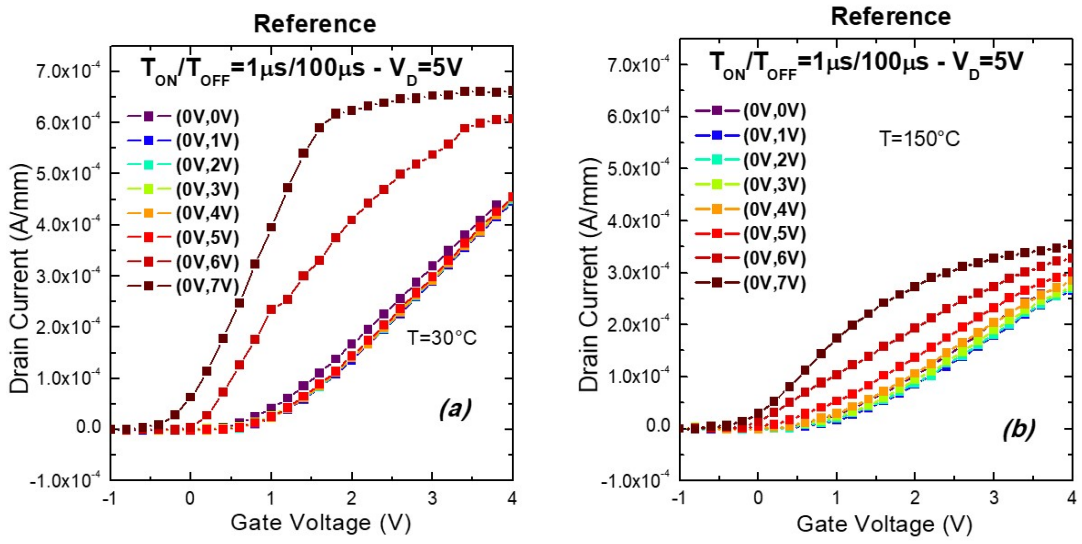
Figure 4.4 – (a) Gate current versus voltage on different processes normalized by gate width at T=30, 90, 150 °C in blue, green and red, respectively. Measured at V_{DS}=0 V. (b) Energy band diagram of the p-GaN/AlGaN/GaN gate stack at V_G=-6 V: cross-section taken at the gate foot where the electric field in the barrier is maximal. The direction of the electron conduction through Poole-Frenkel emission is indicated [52].

4.1.3 Forward gate bias

Regarding the forward gate bias leakage current, when the polarization of the electric field has reversed. Process A and B shows the suppression of the forward gate leakage current.

In order to study more on the dynamic behavior of the p-GaN gate stack, forward gate voltage double pulse measurements are performed on three devices, double-

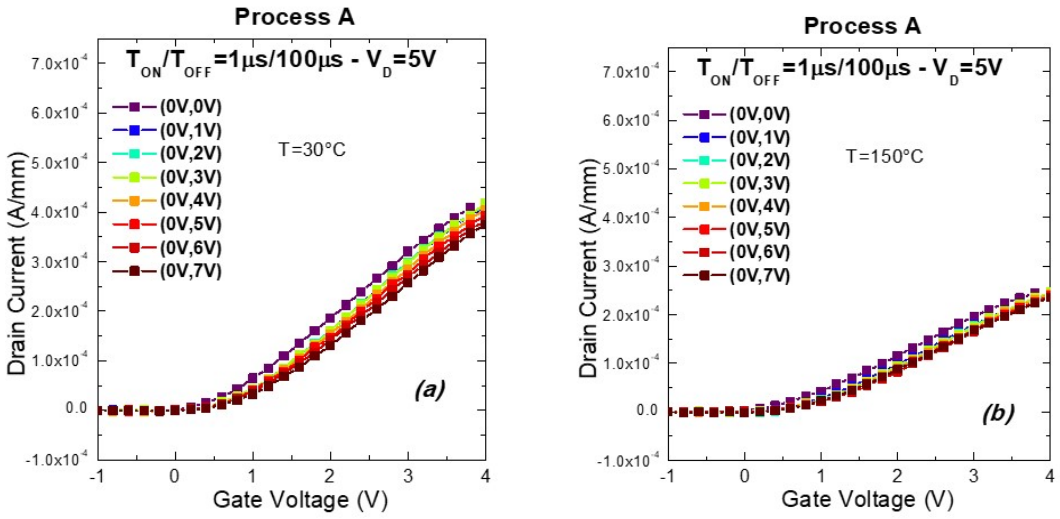
pulse measurements were carried out (using a custom system), starting from several quiescent (V_{GS}, V_{DS}) bias point with a positive V_{GS} value (up to 7 V) and zero volt on the drain. This allows to induce a significant trapping under the gate and in the access regions, thus studying the instability of the threshold voltage. I_D-V_D and I_D-V_G curves were tested at room temperature, by adopting a duty cycle of reverse and forward gate leakage current of 1% (pulse width = 1 ms, pulse period = 100 ms). The transfer characteristics are measured (fast) at a drain potential of 5 V and are plotted in Figure 4.5 , Figure 4.6a . The reference forward gate bias pulsed I_D-V_G shows a significant negative shift after a gate voltage stress of higher than 6 V, which can be explain by hole injection from 2DHG to the AlGaN barrier and enhance the negative shift of threshold voltage [73]. In the high temperature (150 °C) the threshold voltage shifted to the left as well, due to the high temperature the current is lower compare to the pulsed I_D-V_G at room temperature, which we have seen before.



(a) (b)

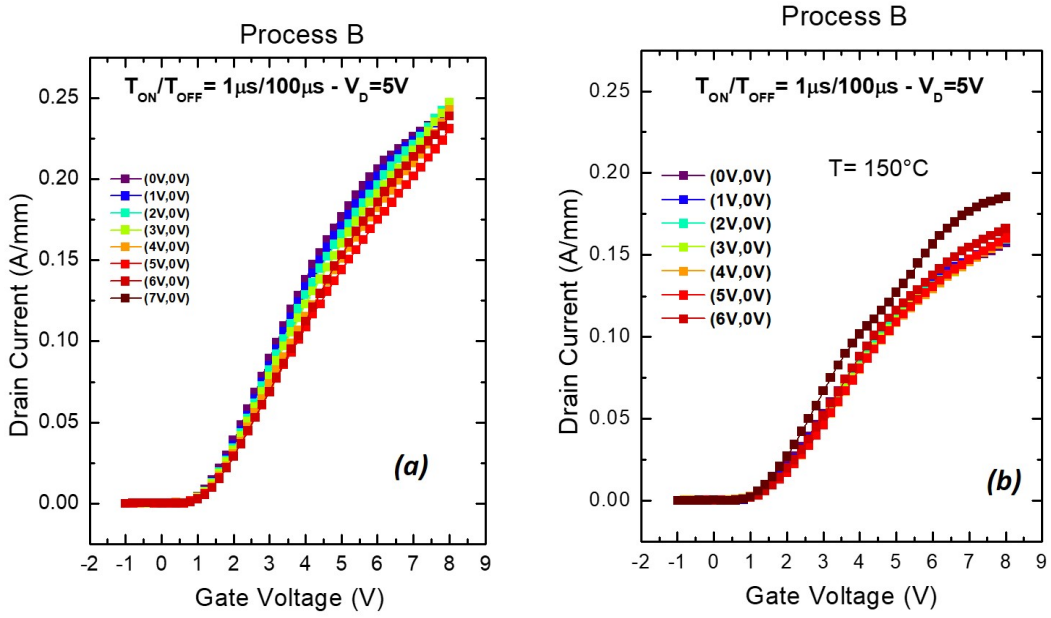
Figure 4.5 – Drain current versus gate voltage after different forward gate voltage stress on the reference process (a) at room temperature and (b) at high temperature.

On the contrary, the device fabricated with process A shows a gradual positive shift, even at high forward gate stress (the pinch-off voltage calculated at I_D= 100 μA/mm), which is indicative of electron trapping in the AlGaN barrier and shift the threshold voltage to the right. Figure 4.9b. shows the energy band diagram in the gate region.



(a) (b)

Figure 4.6 – Drain current versus gate voltage after different forward gate voltage stress on the process A (a) at room temperature and (b) at high temperature.



(a) (b)

Figure 4.7 – Drain current versus gate voltage after different forward gate voltage stress on the process B (a) at room temperature and (b) at high temperature.

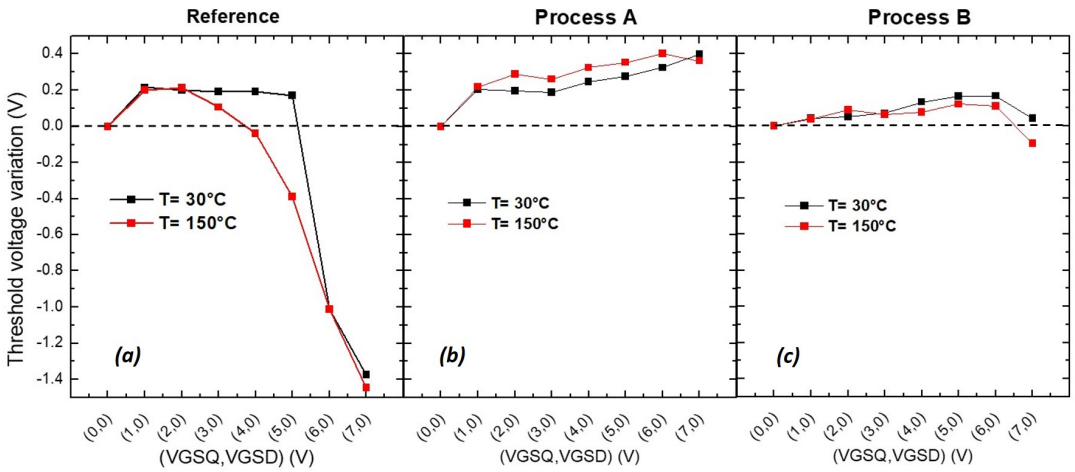
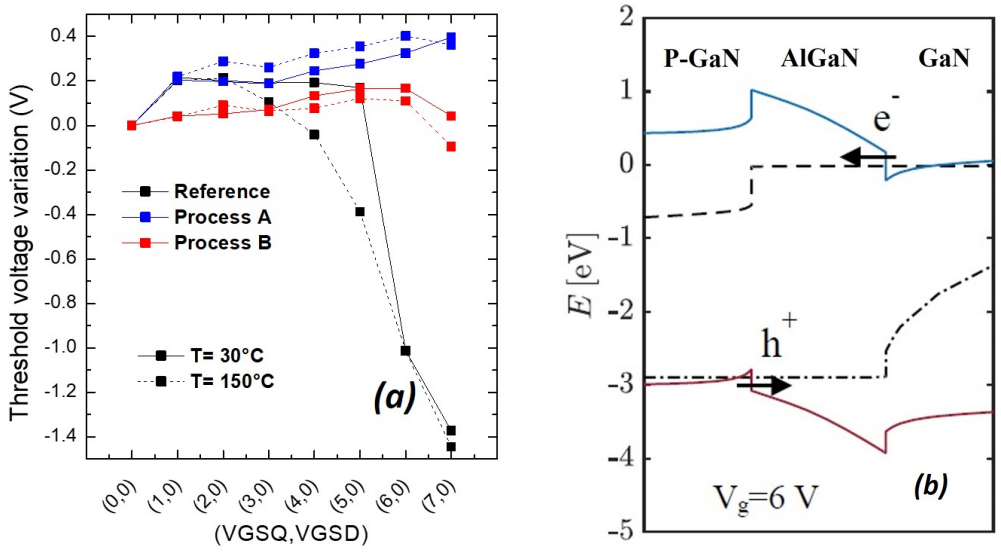


Figure 4.8 – Pinch-off voltage variation versus forward gate voltage stress for the (a) reference, (b) process A and (c) process B at room temperature (black) and high temperature (red).

When the gate bias increases to values higher than 0 V (the pinch-off voltage) the electrons can be trapped in the gate region. As can be notice in Figure 4.9a. which shows smaller positive threshold voltage shift than the other process. The p-GaN sidewall passivation decreases the trapping effect in the AlGaN barrier and also reduces the 2DEG density, therefore we can see the lower positive shift of the threshold voltage in process B but the best stability. In this case, both electron and hole trapping has been reduced.

4.2 Impact of sidewall etching on the dynamic performance of GaN-on-Si E-mode transistors

To complete the previous section, now we present a detailed study of the trapping process induced by positive gate bias in GaN HEMTs with p-type gate. By analyzing two different gate processes, we study the kinetics of the threshold voltage variation, and –for the first time– we demonstrate that etching of the sidewalls of p-GaN can significantly influence device stability. The original results described within this section demonstrate that: (i) the exposure to a positive gate bias induces a dynamic increase of the drain current, ascribed to a negative shift of the threshold and to a



(a) (b)

Figure 4.9 – (a) Pinch-off voltage variation versus forward gate voltage stress for the reference, process A and B (b) Energy band diagram of the p-GaN/AlGaN/GaN gate stack at (b) V_G= 6 V: cross-section taken at the gate foot where the electric field in the barrier is maximal: the arrows depict the trapping of electrons and holes in the barrier. Electron trapping occurs throughout the whole barrier under the gate, while the hole trapping occurs predominantly near the gate foot. Simulated with a high density of Mg in the p-GaN, such that the depletion region does not reach the p-GaN/AlGaN interface [52].

decrease in on resistance, in the devices with non-optimized etching ("Etch A"). (ii) Two dominant trapping mechanisms occur. The first one is associated with charge-state transition of Carbon impurities in Nitrogen substitutional position (C_N). The second mechanisms are indicative of the hole de-trapping process from traps at the AlGaN barrier and/or at the passivation/AlGaN interface. (iii) The threshold voltage variation is investigated using temperature dependent pulsed measurement: higher temperatures, higher threshold voltage shift, indicating a thermally-activated hole injection mechanism. (iv) The negative threshold voltage variation can be suppressed by the p-GaN sidewall etching for the same epitaxy.

Enhancement-mode AlGaN/GaN power HEMTs with p-type gate fabricated on Si substrate are considered in this work [56]. A schematic cross-section of the gate region in a p-GaN gated HEMT is depicted in Figure 4.1. As discussed before, the

negative polarization charge at the p-GaN/AlGaN interface lifts up the energy bands, and the threshold voltage shows a positive value. At high reverse gate bias, the p-i-n diode prevent the gate. In order to study the gate leakage two different process have been implemented. The devices have identical epitaxy but the untreated ones have undergone a reference process without improvements, referred to as "Etch A", while the devices "Etch B" are fabricated with a process variation, resulting in higher p-GaN sidewall and access regions quality (different etch chemistries were used for case "A" and "B") (table 4.2). It is shown that the same process reduces the reverse and forward gate leakage current significantly [52].

Table 4.2 – Overview of the process variations studied in this part. Size of the devices under test (W = 200 µm).

Sample	Lgd (µm)	p-GaN sidewall
A	15	ref.
B	15	improved

4.2.1 Preliminary DC characterization

Figure 4.10 shows DC gate leakage measurements at different drain voltage on small transistors the gate I_G-V_G characteristics with "Etch A" and "Etch B" reported in the plots below shows a difference in leakage current. This effect could be explained by taking into account the sample with improved side wall "Etch B" is reducing the trap density, so the injection of holes becomes lower because of the better surface quality.

In Figure 4.11 it is reported the catastrophic breakdown on nine devices for each wafer, concerning to the comparison of the leakage current at V_G= 7 V and the failure voltage for tow wafer on Figure 4.12, indicating a high leakage current and lower breakdown voltage for etch tool A, which is due to the side walls effect and the variability of the pinch-off voltage on etch tool A. To make an overview of the wafer and check the dependency of the position of deices we performed the leakage current and breakdown measurement on all the devices (Figure 4.13) The leakage current and breakdown voltage strongly depends on the cell position and on the device topology.

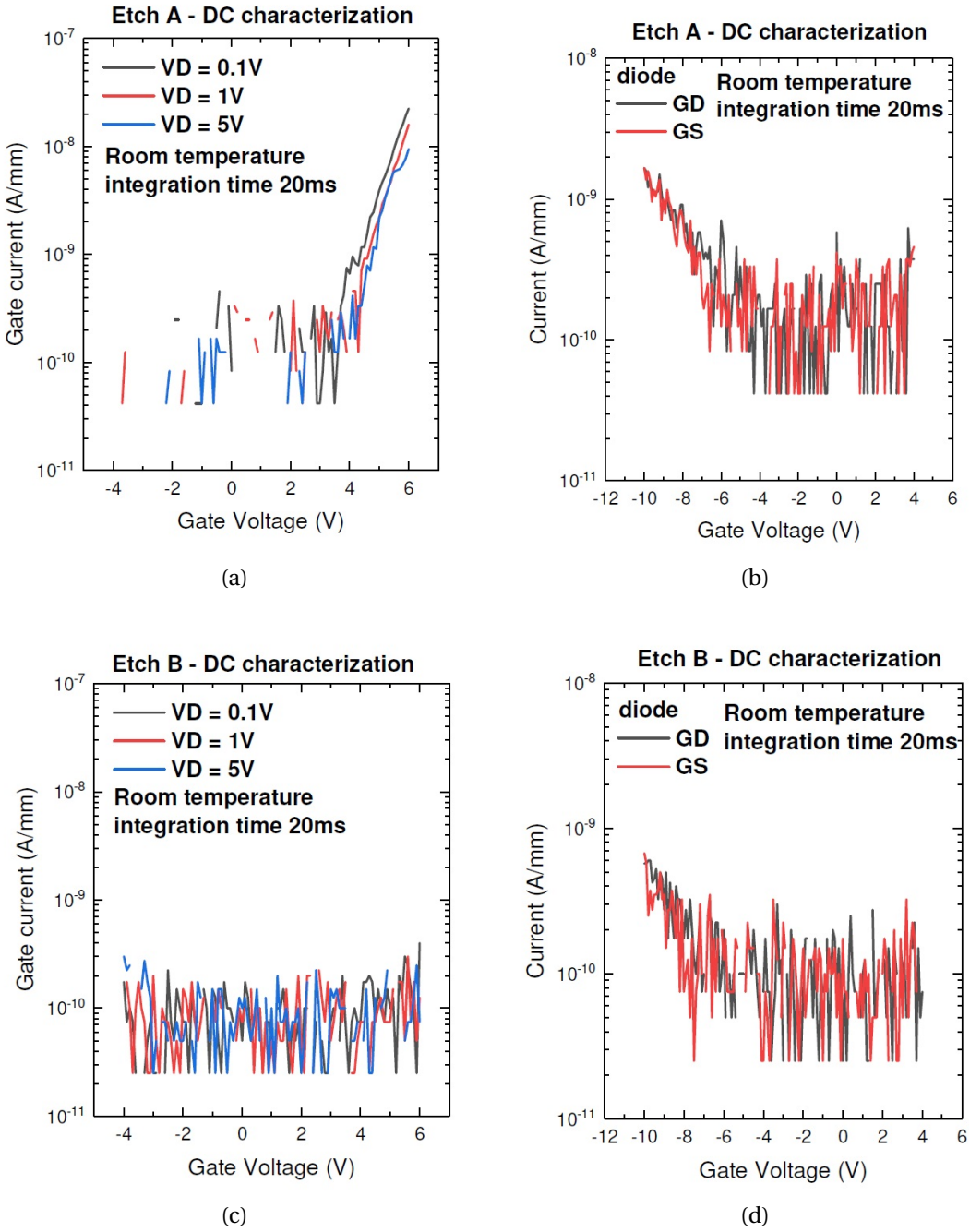
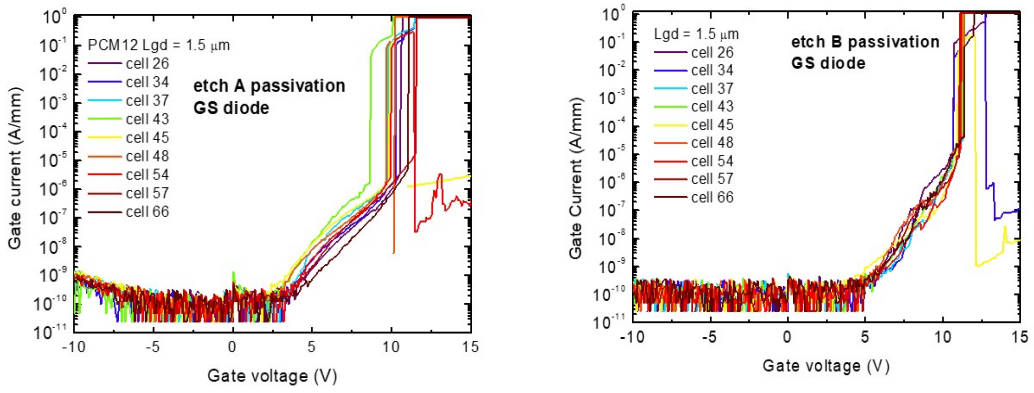
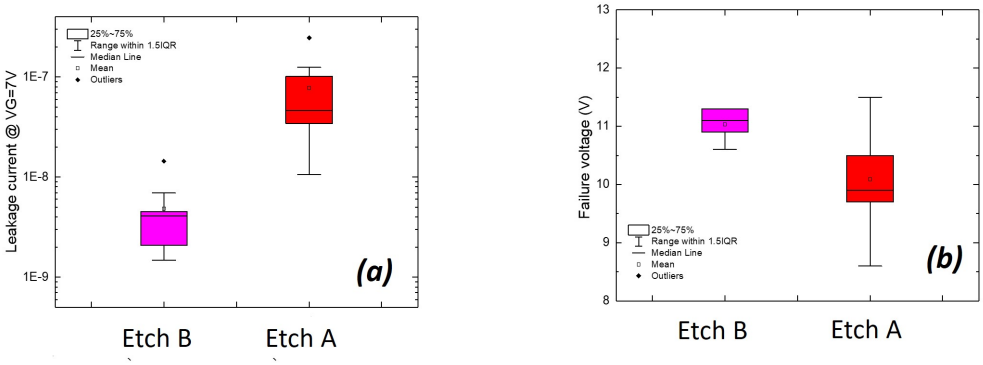


Figure 4.10 – DC gate leakage measurements on small transistors.



(a) (b)

Figure 4.11 – Catastrophic breakdown, 9 device per wafer.



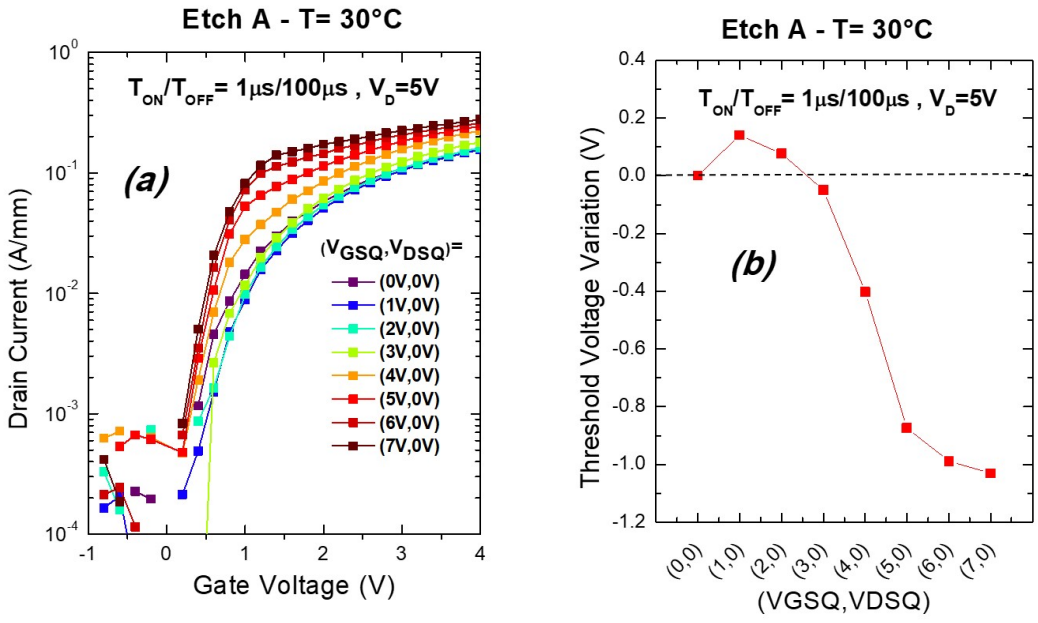
(a) (b)

Figure 4.12 – (a)Leakage current at V_G= 7 V for tow devices. (b) Failure voltage for etch A and B.

Figure 4.13 – The spatial map of leakage (at 7 V) breakdown voltage. The leakage current and breakdown voltage strongly depends on the cell position and on the device topology.

4.2.2 Pulsed characterization of reference devices

In order to study the dynamic behavior of the p-GaN gate stack, forward gate voltage stress measurements are performed on two samples. Measurements were performed using short (1 µs) pulses, while quiescent (trapping) bias was applied for 100 µs at each measurement point. Output characteristics were measured for V_G levels in the range 0–4 V, and with V_D levels around 5 V to prevent hole injection from the gate. During all these analyses the source was grounded. From the comparison between the various quiescent bias points, it is possible to evaluate the response of the drain current to the applied trapping voltage. Figure 4.14 reports representative output characteristics, measured starting from different quiescent bias points: The results for the device fabricated with process A demonstrate that a positive gate bias induces a dynamic increase of the drain current, ascribed to a variation of the pinch-off voltage (see the region around 10-3 A/mm in Figure 4.14a) and a decrease in on-resistance (see the high current region in Figure 4.14a). The pinch-off voltage variation is calculated and plotted as function of quiescent bias applied to the gate in Figure 4.14b. The device shows a slight positive pinch-off voltage shift after stressing at 1 V, followed by significant negative shift for positive gate trapping level. The small positive shift is ascribed to the injection of electrons from the 2DEG towards the AlGaN barrier (Figure 4.15). On the other hand, the physical mechanisms underneath the negative shift and the decrease in dynamic-R_{on} is the accumulation of positive charges (holes), injected from the gate metal. These holes can be trapped at the AlGaN barrier (thus inducing a negative V_{TH} shift, Figure 4.15) and/or at the passivation/AlGaN interface (inducing a decrease in R_{on}).



(a) (b)

Figure 4.14 – (a) Sidewall process A: drain current versus gate voltage after different forward gate voltage stress. (b) Pinch-off voltage variation versus forward gate voltage stress for sidewall process A.

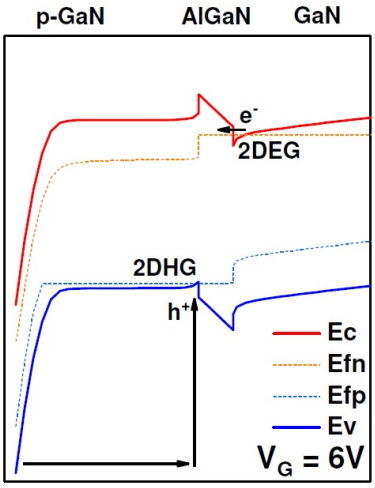


Figure 4.15 – Band diagram under the region at V_G = 6 V (simulated with Sentaurus provided by Synopsys). Two mechanism are reported: 1) injection of electrons from the 2DEG towards the AlGaN barrier; 2) accumulation of positive charges (holes), injected from the gate metal.

4.2.3 Transient characterization of reference devices

The characterization of trapping phenomena was carried out by drain-current deep-level transient spectroscopy (I-DLTS), which is based on the analysis of drain current transients (i.e. drain current variation with time) as a function of the channel temperature. This technique can provide very accurate information on the activation energy and cross section of the trap levels that limit the performance of GaN-based transistors [36].

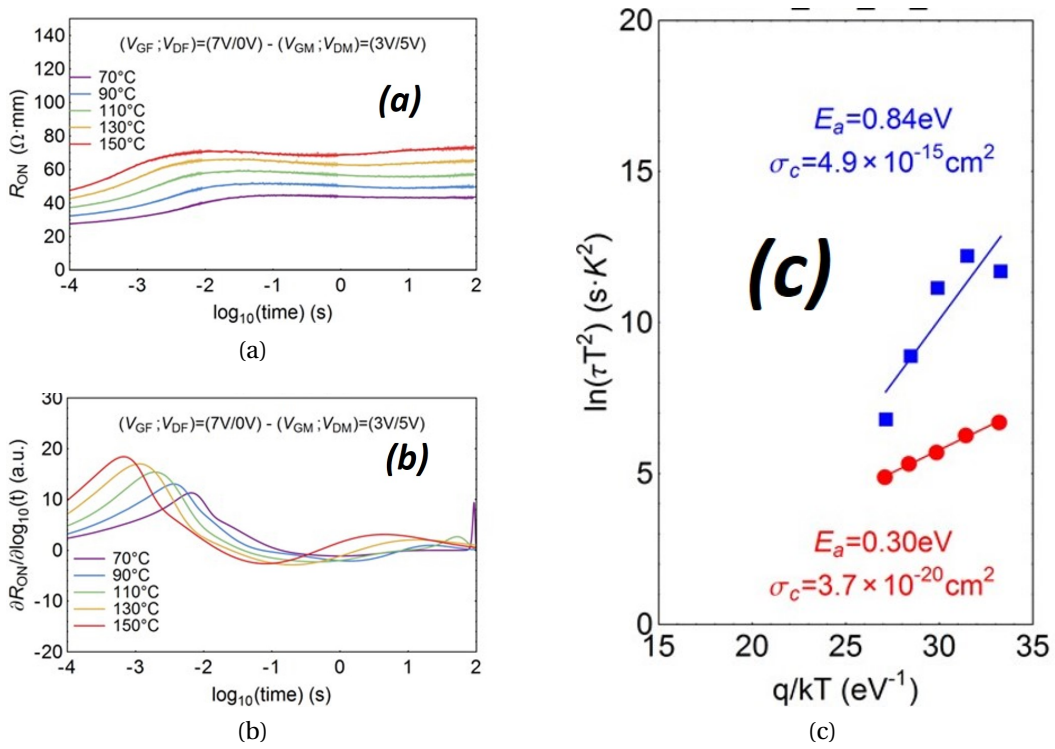


Figure 4.16 – Sidewall process A: analysis of de-trapping kinetics reveals two traps (one is carbon, the second represents the hole-de-trapping).

The measurements were carried out by analyzing the charge de-trapping transients in the linear region at several temperature levels. The results of this investigation are summarized in Figure 4.16 and were obtained by carrying out the set of transient measurements with filling bias condition (V_{GF}; V_{DF}) = (7 V; 0 V) and de-trapping condition (V_{GM}; V_{DM}) = (3 V; 5 V). Several ambient temperatures were considered compatibly with the time constant (from 70 °C to 150 °C, 20 °C/steps). For a better understanding of the properties of the trap levels responsible for negative threshold

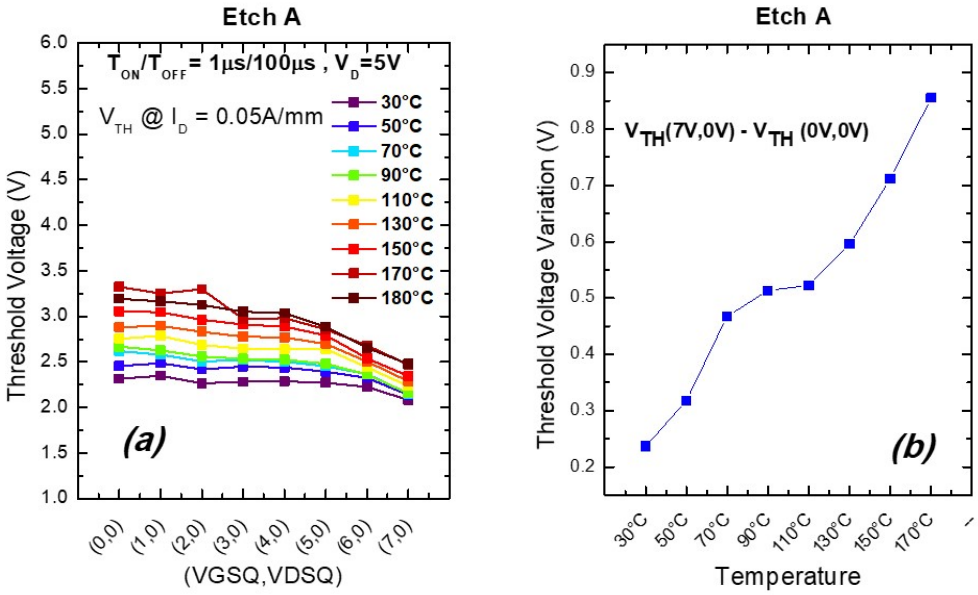
voltage shift, it is necessary to extrapolate the Arrhenius plots of the traps and their signature in terms of activation energies and capture cross-sections. The results reveals two traps summarized in Figure 4.16c: the signatures of T1, T2 correspond to apparent activation energies and apparent capture-cross sections of 0.84 ±0.24 eV/ 4.9 $\times 10^{-15}$ cm^2 for T1 and 0.30 eV/3.7 $\times 10^{-20}$cm^2 for T2. Level T1 is similar to the other literature as possible charge-state transition of Carbon impurities in Nitrogen substitutional position (C_N). The signatures of T2 is related with hole de-trapping responsible for the threshold voltage and R_{on} instabilities, and the activation energy E_a= 0.30 eV is indicative of relatively fast traps (~ms range), located at the AlGaN barrier and/or at the passivation/AlGaN layer.

4.2.4 Temperature dependent characterization of reference devices

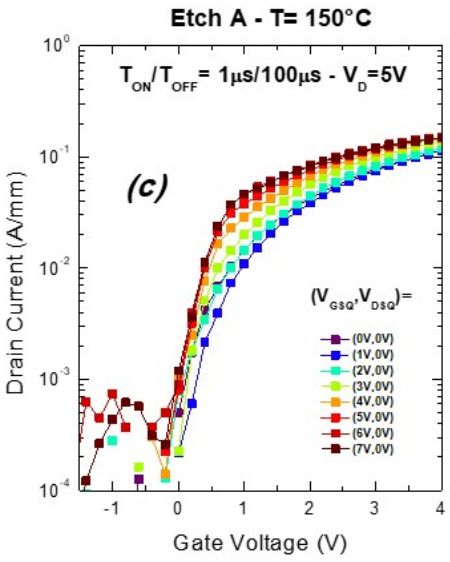
Figure 4.17a indicates the threshold voltage (for I_D =50 $^{mA}/_{mm}$) extracted from pulsed forward gate measurements at different temperatures (from 30° C to 170° C, 10 $^{°C}/_{steps}$), aimed at further investigating the trapping mechanisms underlying the negative threshold voltage shift. High temperature does not strongly increase the threshold voltage shift of the reference structure transistor, even if the overall shift is greater at higher temperatures as is shown in Figure 4.17b. Hence, an influence of the temperature on the negative threshold voltage variation occurring during double pulse measurement is shown. This is consistent with the enhanced trapping process due to the stronger hole injection at higher temperature. For example on one device we can observe the shift of the threshold voltage at T=150° C in Figure 4.17c.

4.2.5 Characterization of devices with improved p-GaN sidewall

In this section we present the same experimental analysis performed on the devices with the same epitaxy of reference ones but fabricated with the process variation for sidewall etching, referred to as “Etch B”. By optimizing sidewall surface and changing etch tool, we found that the exposure to positive gate has no effect on the threshold voltage. This demonstrates that the pinch-off voltage instability has been solved, as can be seen in Figure 4.18, only through optimization of the sidewall treatment. We therefore conclude that the V_{TH}/R_{on} shift reported for Etch A samples mostly takes



(a) (b)

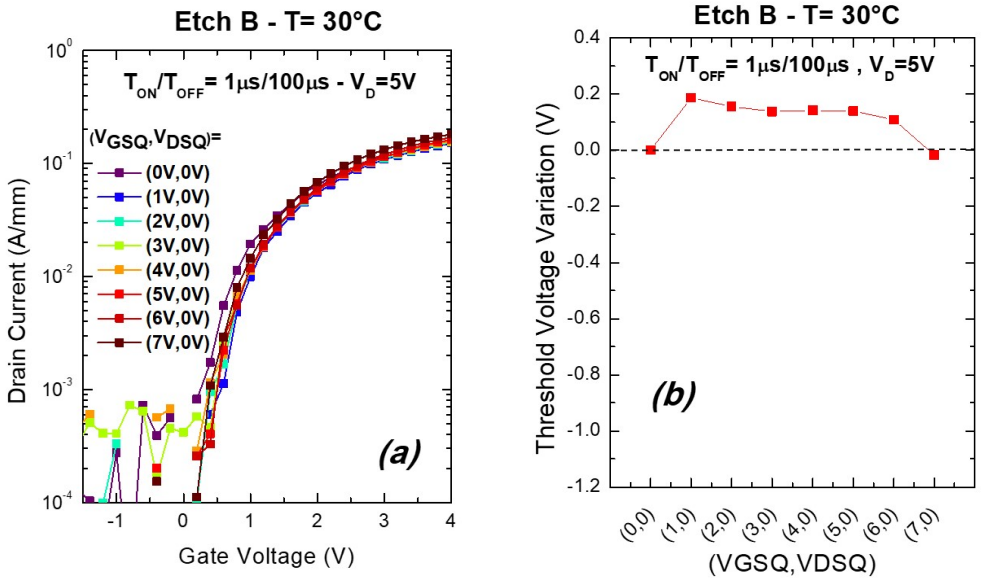


(c)

Figure 4.17 – Sidewall process A: (a) V_{th} at different temperatures. (b) V_{th} shift is stronger at higher temperatures (stronger hole injection, enhanced trapping process). (c) drain current versus gate voltage after different forward gate voltage stress.

place due to injection of holes through traps located at the sidewalls of p-GaN, rather than in the "bulk" p-GaN layer. Such holes, once injected to the sidewall/passivation

interface, can reach the access region thus favoring also a decrease in R_{on}. A careful optimization of sidewall etching is therefore a necessary step towards the fabrication of devices with stable V_{th}/R_{on} under high positive gate bias. Figure 4.19 shows that the improvement of the p-GaN sidewall quality implies excellent pinch-off voltage stability also at high temperature.



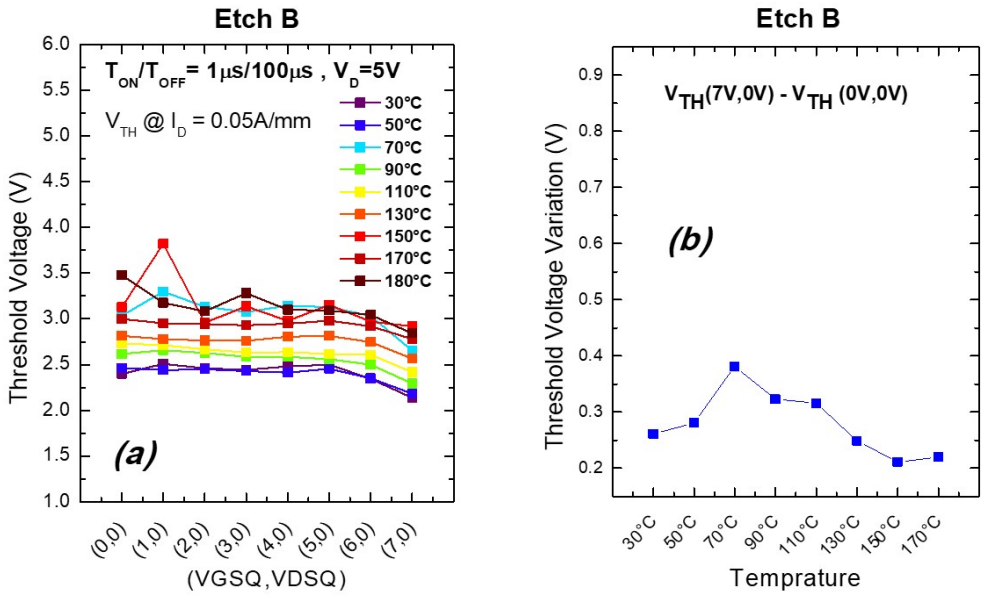
(a) (b)

Figure 4.18 – (a) Sidewall process B: drain current versus gate voltage after different forward gate voltage stress. (b) Pinch-off voltage variation versus forward gate voltage stress for sidewall process B.

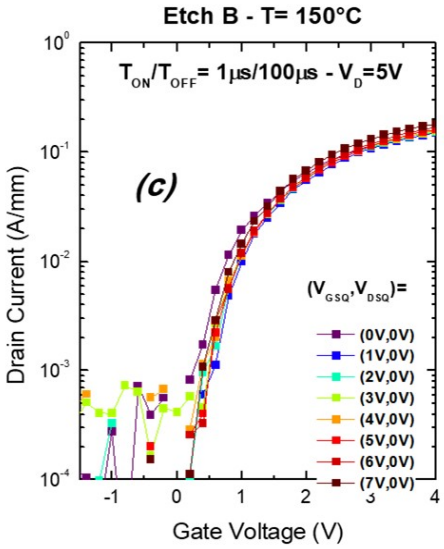
In etch B we have found no shift of pinch-off voltage at room temperature and high temperature, reported in Figure 4.18 and Figure 4.19.

4.2.6 Step stress experiments

We investigate the semi-on state degradation processe of p-GaN HEMT submitted to a gate step-stress up to failure of the devices (Figure 4.20) in order to clarify the impact of field electron dependent degradation process, the physical properties of the devices were analyzed by electrical characterization. The devices were submitted to step-stress experiments (Figure 4.20). The gate voltage was increased from -1 V up to failure, at step of -0.5 V (Bias time for each step = 120 s, texposure = 25 s, tacq = 30 s,



(a) (b)

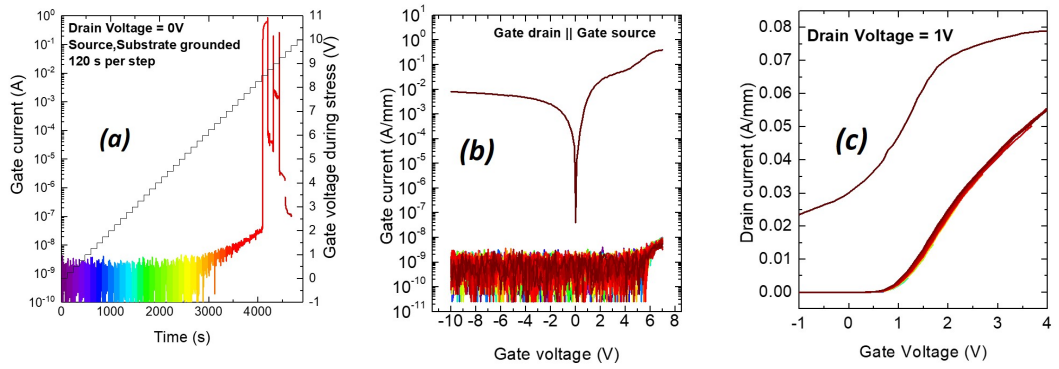


(c)

Figure 4.19 – Sidewall process A: (a) V_{th} at different temperatures. (b) V_{th} shift is stronger at higher temperatures (stronger hole injection, enhanced trapping process). (c) I_D-V_G at high temperature for Etch B.

T= 30° C). Several identical devices were stressed by using different drain voltages, between 0 V and 75 V, in order to promote the hot-electron degradation processes at each stage of the stress tests [31]. Figure 4.20a and Figure 4.21a reports the gate

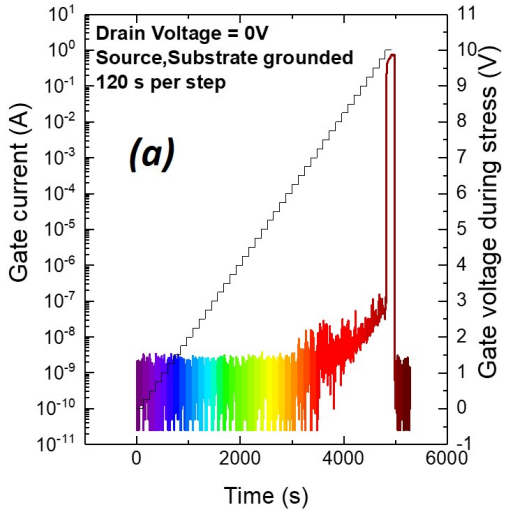
current measured on one of the devices submitted to a gate-step stress with V_{DS}= 0 V.



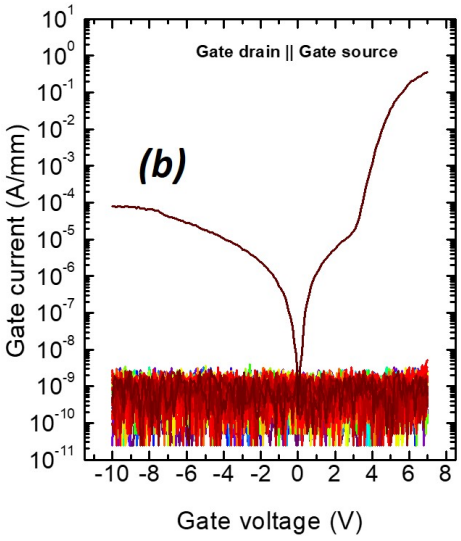
(a) (b) (c)

Figure 4.20 – (a) Gate current during the stress. (b)Gate current versus gate voltage during a step-stress experiment carried out with V_{DS}=0 V, increasing V_{GS}. (c) Drain current versus gate voltage, the shift of the pinch-off voltage variation (Etch A)

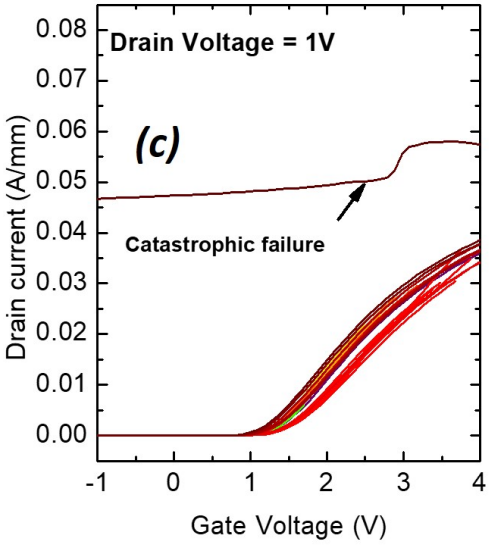
Figure 4.20 reports the gate current during the gate step-stress and Figure 4.20b is gate current versus gate voltage during the stress till breakdown. The results indicate the weak behavior of etch A, consistent with the data from step-stress and breakdown I-V tests. As we can see in Figure 4.22 the life time for etch A is much less than the life time for etch B. The results allow to understand the basic impact of epi/process modifications on performance and reliability. Figure 4.22 reports the average of life time (TTF) for etch A and etch B, the etch B shows two order of magnitude higher life time than etch A.



(a)



(b)



(c)

Figure 4.21 – (a) Gate current during the stress. (b) Gate current versus gate voltage during a step-stress experiment carried out with V_{DS}=0 V, increasing V_{GS}. (c) Drain current versus gate voltage, the shift of the pinch-off voltage variation (Etch B)

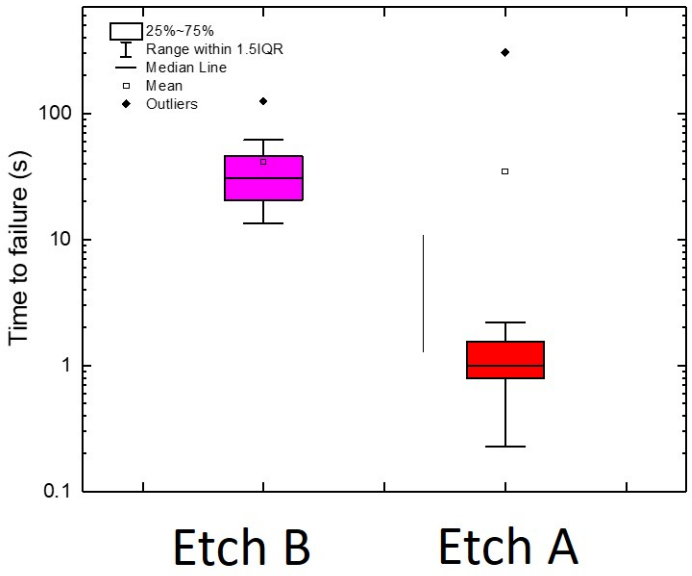


Figure 4.22 – Average of life time (TTF) for etch A and B.

4.3 Conclusions

The suppression of gate leakage along the p-GaN sidewall is essential to obtain enhancement mode devices with a stable pinch-off voltage when stressing the gate at the forward voltage. Untreated, this gate leakage is most prominent under reverse gate bias, where Poole-Frenkel conduction through the barrier at the gate edges yields the best fit. Two processes are introduced to suppress this perimeter-dependent leakage: (A) improving the Schottky/p-GaN interface quality in order to decrease the supply of carriers from the gate metal and (B) proper passivation of the p-GaN sidewall to suppress any interface states and surface roughness leading to a conductive path. The pinch-off voltage shifts positive due to electron trapping from the 2DEG into the barrier. Left untreated, the hole current along the p-GaN sidewall will induce hole trapping in the barrier, leading to a sharp decrease in the pinch-off voltage. An estimated value for the trapped charge hints that outdiffused Mg acceptor states may lie at the origin of the trapped positive charge. Both trapping phenomena can be suppressed by combination of high Schottky/p-GaN interface quality and proper p-GaN sidewall passivation.

The threshold voltage instability induced by pulsed gate forward stress has been investigated in p-GaN gated AlGaN/GaN-on-Si HEMTs. For the first time the role of the etching of the sidewalls of p-GaN on the dynamic threshold voltage behavior has been analyzed. In particular, under double pulse testing an untreated device shows a negative threshold voltage shift at positive gate voltage, which is explained by hole injection under the gate and/or the gate-source region. Transient measurements indicate that two trapping mechanisms take place, with activation energies of 0.84 eV (C_N defects) and 0.30 eV (hole de-trapping process). In addition, the hole trapping mechanism is thermally-activated because the threshold voltage shift increases at higher temperatures. Overall, we have demonstrated in this chapter that the suppression of threshold voltage instability by opportunely passivate the p-GaN sidewall. The improved reliability of “Etch B” highlights that hole trapping mostly takes place on the sidewalls.

5 GaN-on-silicon material system for 1200 V applications

Recently, GaN-on-Si epiwafers became a very important material to be used in high power applications [85–87]. However, this kind of transistors still suffer from a low breakdown voltage due to the poor critical electrical field of the Si substrate and the parasitic conduction at the buffer/substrate interface. As discussed before in chapter 1, silicon is a good candidate as a substrate for GaN-based transistors due to the low cost and large size of the wafer. However, silicon has a significant intrinsic lattice mismatch and thermal expansion coefficients of substrate/epitaxial films thus GaN heteroepitaxy on the silicon was not convenient. Recently, the growth process improvement provided a path for large volume, low cost epitaxial films [88–91]. In fact, SiC substrates are also well-known due to the small thermal expansion and lattice constant mismatches with GaN, but the cost is higher than silicon. Sapphire has a very good lattice match but suffers from a poor thermal conductivity. In order to achieve the high performance of GaN based HEMTs for power applications, high-Al-content barrier layer heterostructures have been proposed [92–97].

It is found [98] that the critical electric field for GaN is 1.23-times larger than that for 4H–SiC and 7.97-times larger than that for silicon. Figure 5.1 compares the values for the specific on-resistance for GaN with those for silicon and 4H-SiC devices [98]. It can be concluded that the ideal specific on-resistance for GaN vertical power devices is 1.78-times smaller than that for 4H-SiC and 2130- times smaller than that for silicon at all breakdown voltages.

Several buffer layer techniques such as graded AlGaN buffers [88,99,100], AlN interlay-

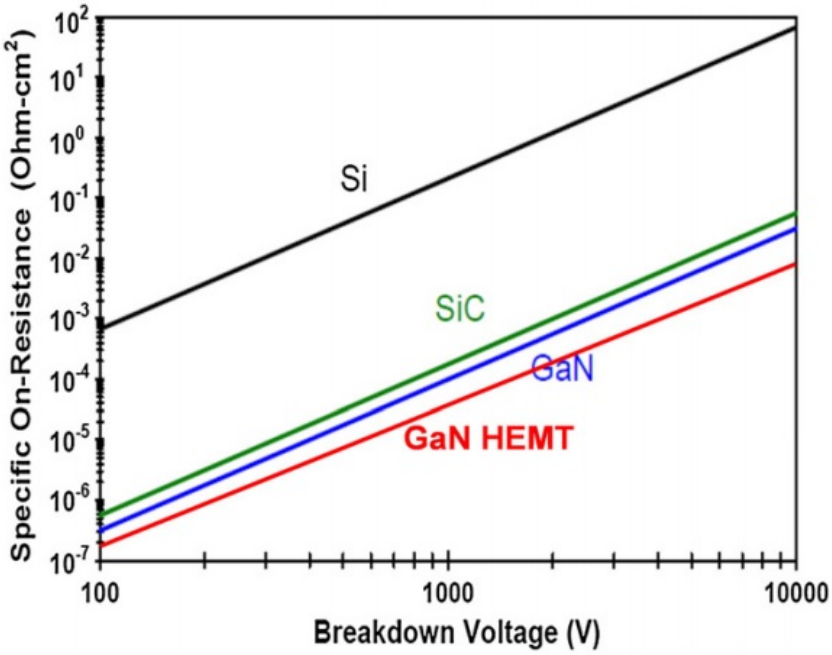
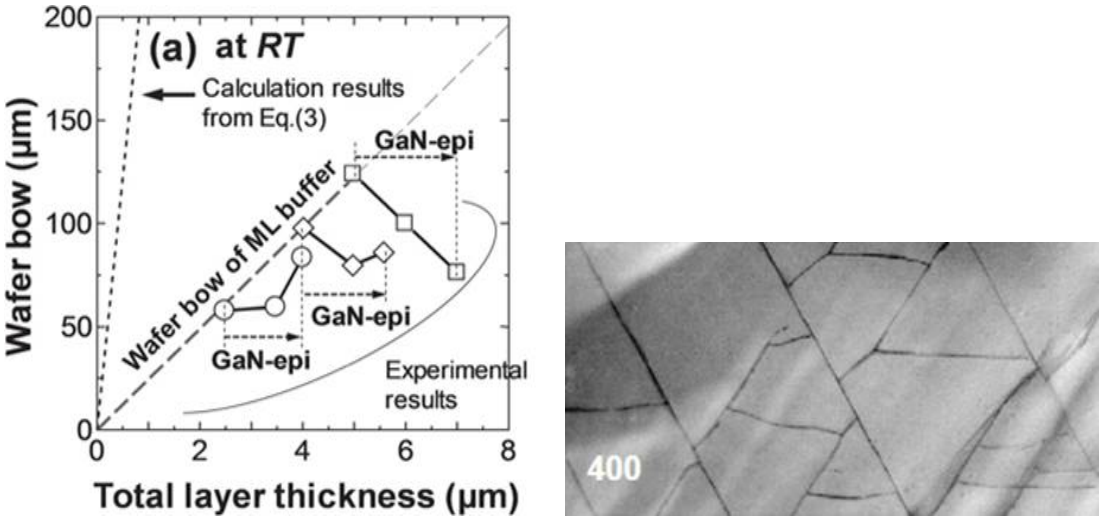


Figure 5.1 – Comparison of specific On-resistance for GaN, Si and SiC [98].

ers [101–103] have been suggested for realizing large diameter epiwafers. Multilayer (ML) buffer structures is the most important solution to grow thick GaN epilayers on Si substrates [104–106]. Indeed, growing a thick buffer layer results in a higher breakdown voltage. However, the main issues with the growing the thick films are usually with bow or cracks on the films. Therefore, carbon doped buffer are usually used to increase the buffer resistivity and allows proper electron confinement. For the wafer bow of GaN-on-Si epiwafers, it is generally understood that the ML buffer structure acts as a strain compensated buffer layer [107–109]. The relationship between wafer bow and total layer thickness that has been suggested by Miyoshi *et al.* [85] is shown in Figure 5.2.

The effects of buffer traps are studied by means of substrate bias ramp measurements. This approach is surface insensitive and applies a 1-D vertical field. Various sweep rates have been used because with slower sweep rates, the thermal generation rate of traps is expected to be enhanced [110].

This chapter presents an assessment of a GaN-on-silicon buffer structure from the epi-wafer provider, ALLOS Semiconductors GmbH, targeting the 1200 V power ap-



(a) (b)

Figure 5.2 – a) relationship between the wafer bow and the total layer thickness for MOCVD-grown GaN-on-Si epiwafers, b) cracks on the films [85].

plications. It will discuss about the low leakage current and state-of-the-art vertical breakdown voltage above 1400 V. Furthermore, the buffer traps are analyzed by means of the substrate ramp measurement.

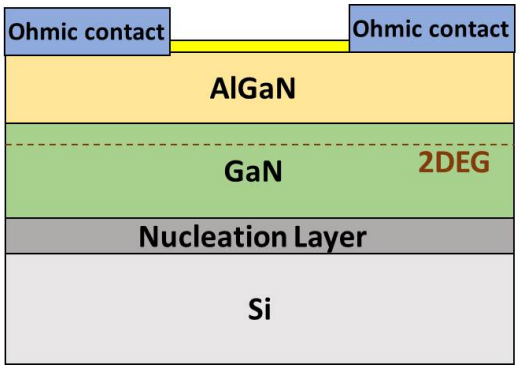
The work of this chapter was carried out in IEMN-Lille-France and supervised by Dr Farid Medjdoub.

5.1 Device structure

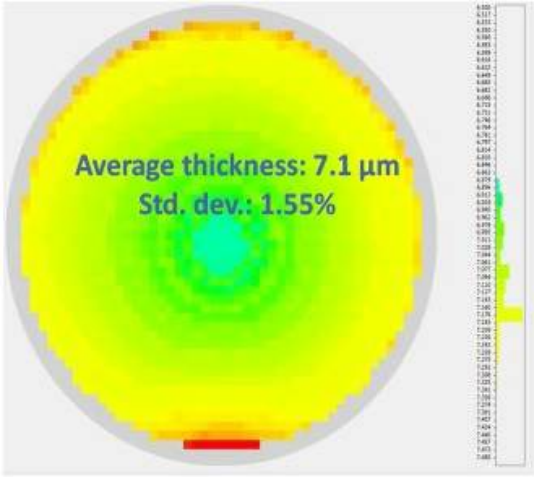
The devices under test are GaN-on-silicon buffer structures, from ALLOS Semiconductors GmbH epi-wafer provider. Epiwafers with 150 mm diameter were grown by MOCVD on Si (111) substrates. Total GaN thickness is 7.1μm with several interlayers for strain management. Thanks to ALLOS' GaN-on-Si growth technologies, high crystal quality of GaN is obtained, with XRD FWHM of (002) and (102) being 395 and 423 arcsec, respectively (Figure 5.3).

In these devices, the effects of buffer traps are studied by means of substrate bias ramp measurements. This approach is surface insensitive and applies a 1-D vertical field. Various sweep rates have been used because with slower sweep rates, the thermal generation rate of traps is expected to be enhanced. Because of the thick

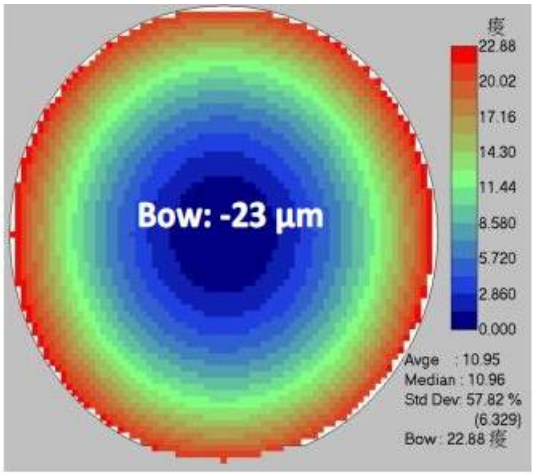
and excellent crystal quality of GaN buffer, low leakage current and state-of-the-art vertical breakdown voltage of above 1400 V was achieved at room temperature [111].



(a)



(b)

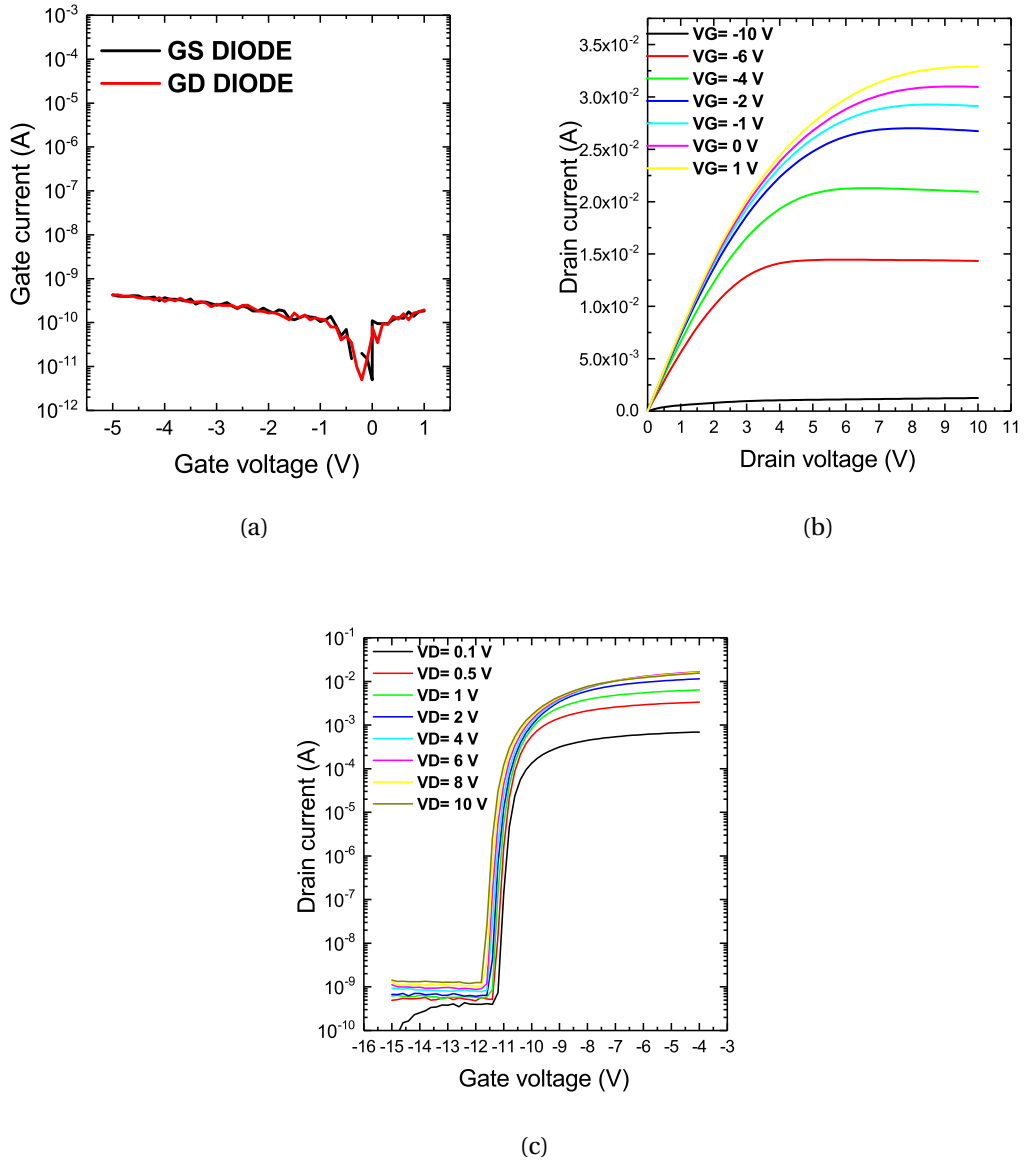


(c)

Figure 5.3 – a) Schematic representation of the GaN-on-silicon buffer structure. b) PL mapping and c) bow data of ALLOS wafer.

5.2 DC characterization

Figure 5.4 shows the DC characteristics indicating low leakage and excellent pinch-off. That reflects the absence of punch-through effects despite the fact that a carbon-free buffer has been used. Moreover, Figure 5.2 and Figure 5.3 show the vertical and floating lateral breakdown voltage characteristics which are due to the benefit of the $7\mu m$ buffer over the thinner commercial buffers.



(a)

(b)

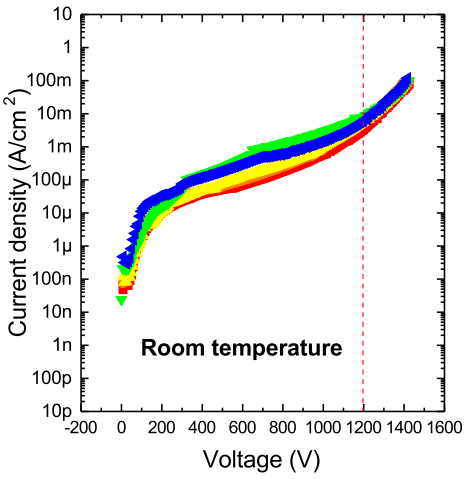
(c)

Figure 5.4 – DC characterization on Allos device (a) diode I_G-V_G, shows a low gate leakage current (b) I_D-V_D at different gate voltages (c) I_D-V_G at different drain voltages, indicates absence of punch-through effects despite the fact that a carbon-free buffer has been used.

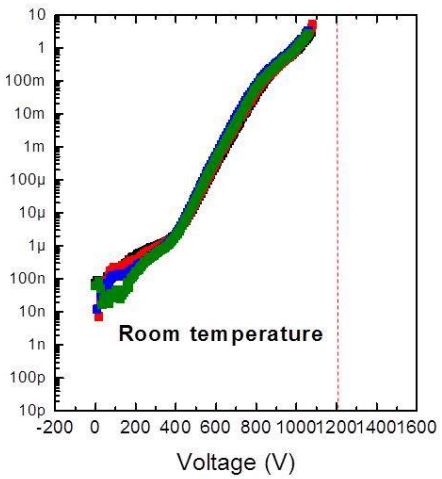
5.3 Vertical, Lateral breakdown

Vertical V_{BD} measurements were conducted on various devices, with grounding the substrate and increasing the voltage on the ohmic contact. The V_{BD} was defined as the

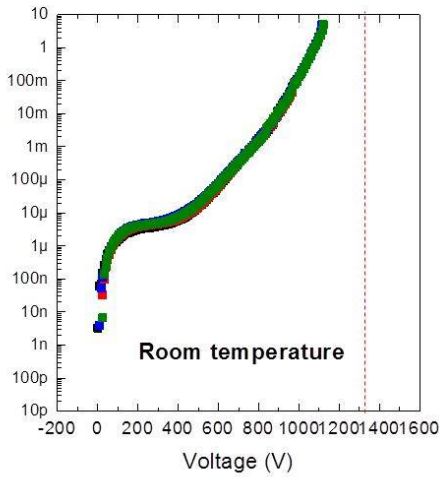
current is increasing with high voltages until the device failure. Figure 5.5 a indicates the vertical breakdown voltage of different devices in the various position on the wafer. The degradation of the devices is about 1400 V, compare to the other commercial devices which breakdown voltage is at lower than 1200 V due to the thinner buffer.



(a)



(b)

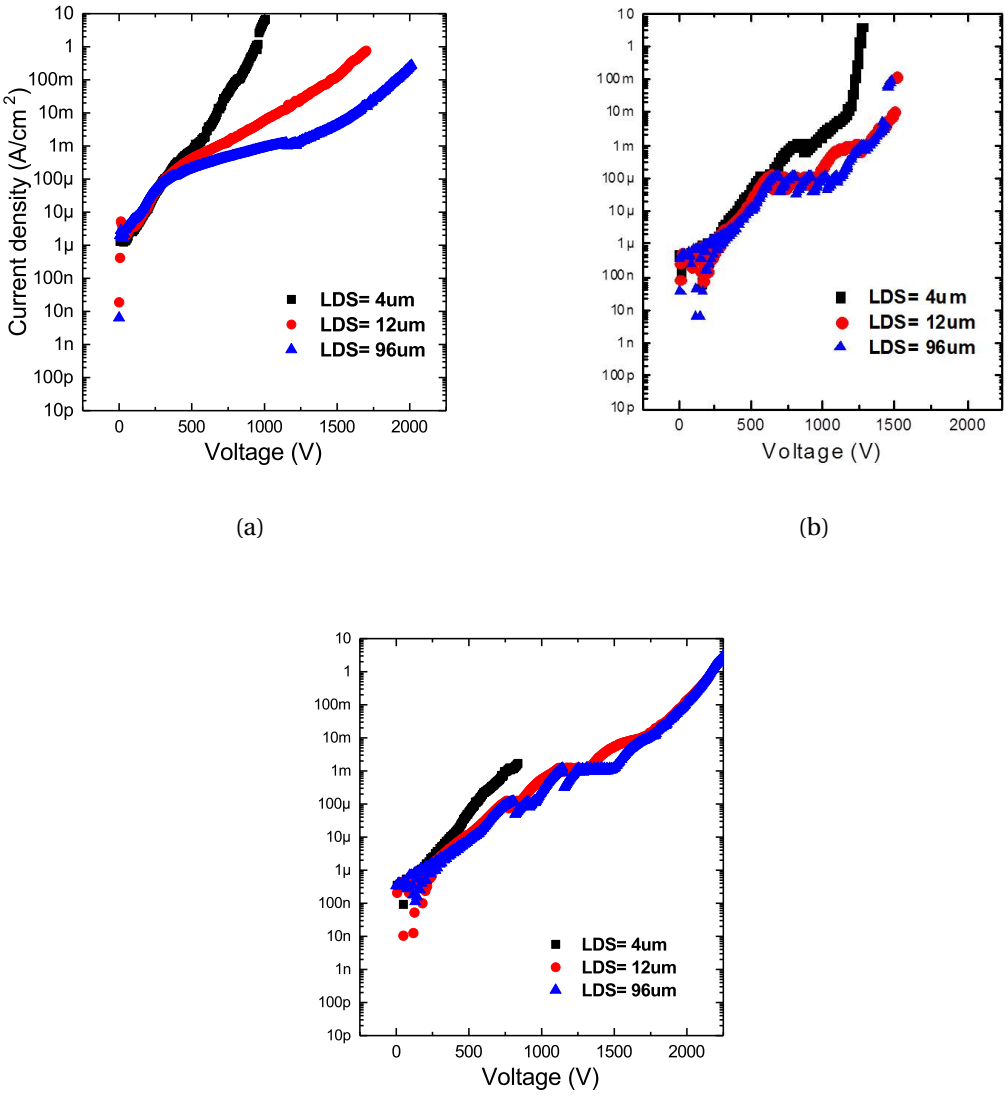


(c)

Figure 5.5 – Vertical breakdown voltage for three samples (a) device under the test (b),(c) commercial devices.

The two-terminal off-state leakage characteristics of the GaN devices are plotted

as a function of voltage for three different length of ohmic contacts L= 4,12, 96μm in Figure 5.6a. The results shows lateral breakdown is as good as state-of the-art commercial wafers (Figure 5.6b, 5.6c).



(a)

(b)

(c)

Figure 5.6 – Lateral breakdown voltage (floating) for three samples (a) device under the test (b),(c) commercial devices.

5.4 Substrate ramp

Substrate ramp is a technique which is able to give information about the magnitude, the sign and the position relative to the 2DEG of charge storage. The operation is in the off-state under the drain contact by ramping the substrate to a high (negative) potential, and monitoring the channel conductivity and to observe the electric field changes close to the 2DEG. A schematic of the substrate ramp setup is shown in Figure 5.7. Any charge redistribution in the buffer upon reverse bias will changes the electric field and if the charge is in close proximity to the 2DEG it will be sensed as a change in the 2DEG conductivity. As such, the buffer charge trapping or storage will be visible in the substrate ramp characteristic.

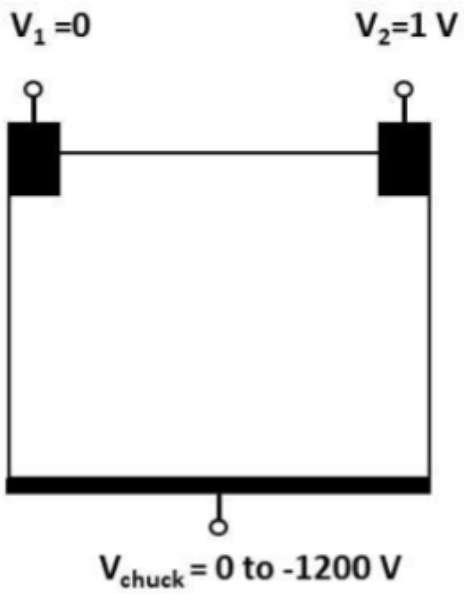
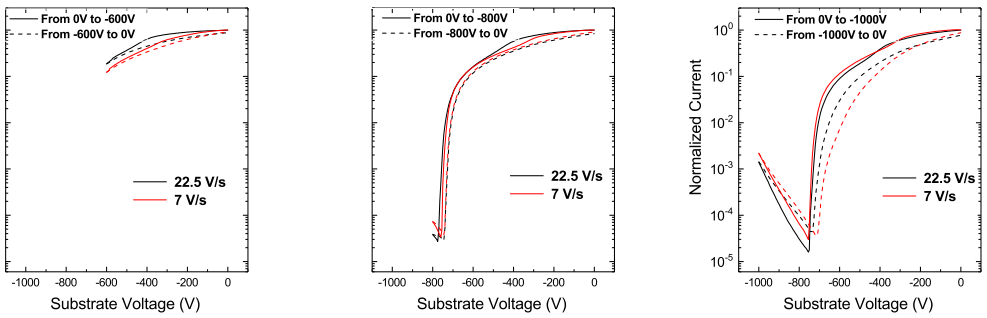


Figure 5.7 – substrate ramp measurements on the TLM.

Under off-state conditions, the buffer stack is subject to large electric fields (lateral and vertical), causing dynamic charge storage in multiple regions within the buffer. Any negative charge build-up close to the 2DEG partially depletes the transistor channel and will increase the on-resistance. The different layers in the buffer stack cannot be probed separately and not much is known about the exact current transport mechanisms [112].

Figure 5.8 and Figure 5.9 show the example of the state-of-the-art 650 V commercial



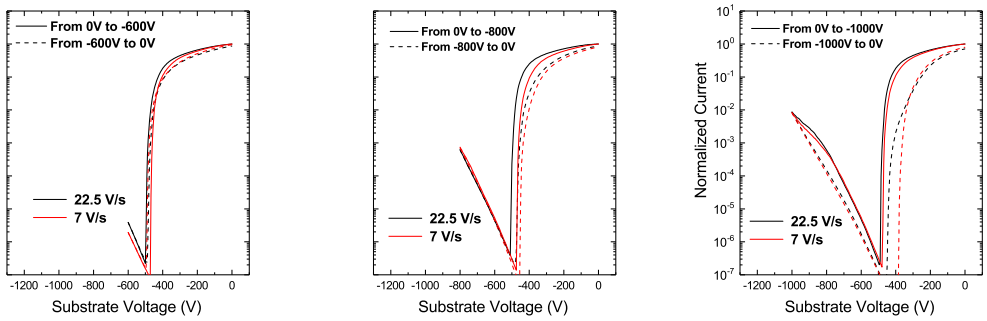
(a) (b) (c)

Figure 5.8 – Substrate ramp experiment, for different ramp-rates of the back-gate voltage sweep a) from 0 V to -600 V go and back b) from 0 V to -800 V go and back c) from 0 V to -1000 V go and back on commercial device 1.

structures that have been used as the benchmark. The normalized conductivity measured at room temperature and for the buffer stack are studied in this work. The results show a low trapping effect down to -800 V in both cases while traps are observed at 1 kV. A negative substrate sweep induced a rightwards shift of the curve, indicating a trapping of negative charge.

In the presence of trapping at 1 kV, the trapping is enhanced with slower sweep rates as expected. In the other words, for the slower ramping (7 V/s), the hysteresis is bigger so charges has more time to be trapped (Figure 5.8, Figure 5.9). To elaborate more on these results, one can say that when the transistor is in the off-state, negative charges are stored in the buffer, due to the ionization of the C-acceptors. The overall increase in dynamic-Ron depends on the balance between the trapping and de-trapping rates under off-state conditions. If there is a bottleneck that prevents de-trapping, a significant increase in dynamic-Ron takes place.

In the case of carbon-free thick buffer, low trapping effects are observed all the way to 1200 V with a low dependency of the substrate bias to the current density in Figure 5.10. This demonstrates the potential advantage of using carbon-free buffers; not only in terms of trapping effects but also paves the way to GaN-on-silicon for 1200 V applications with low on-resistance due to much higher electron mobility as compared to other existing technologies operating above 1 kV.



(a) (b) (c)

Figure 5.9 – Substrate ramp experiment, for different ramp-rates of the back-gate voltage sweep a) from 0 V to -600 V go and back b) from 0 V to -800 V go and back c) from 0 V to -1000 V go and back on commercial device 2.

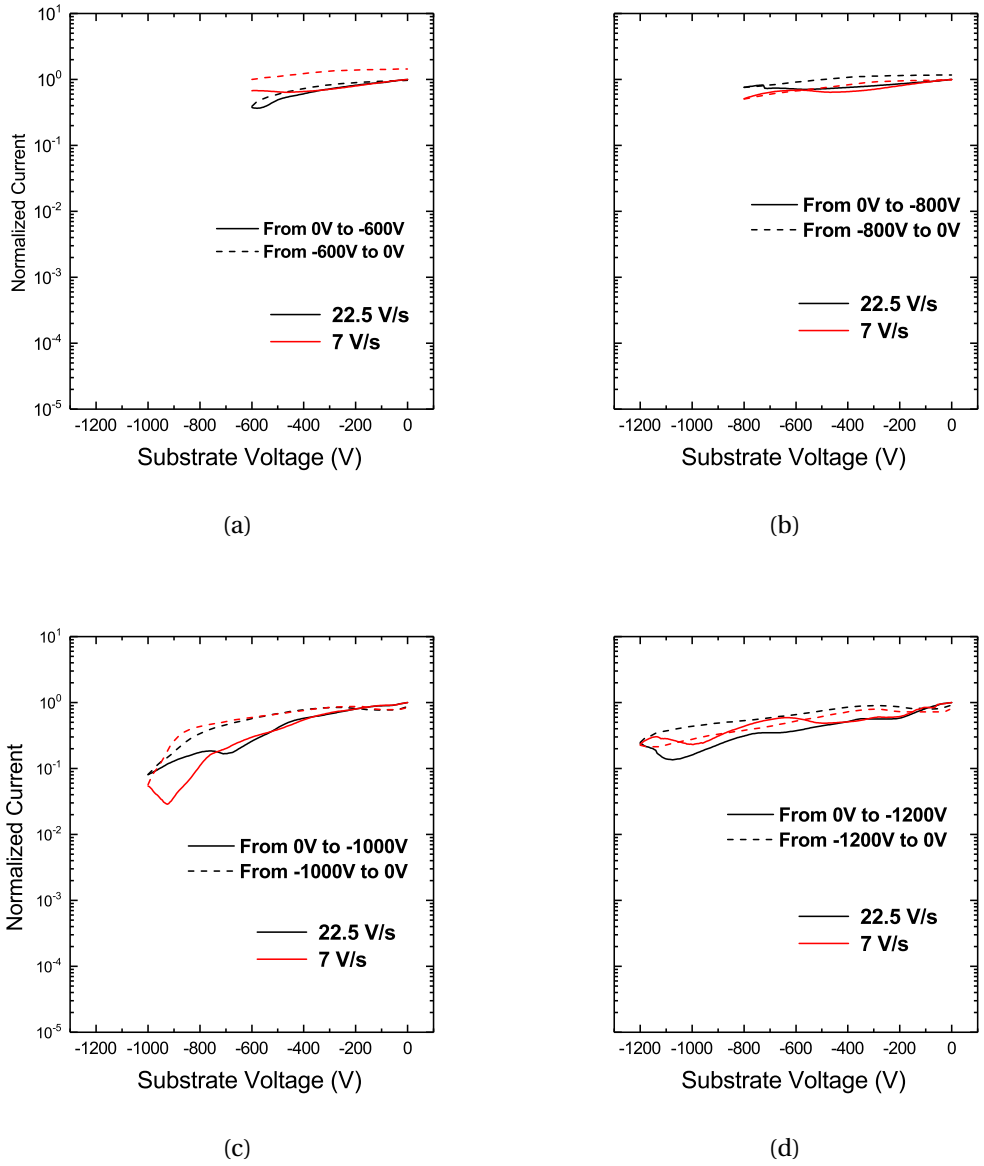


Figure 5.10 – Substrate ramp experiment, for different ramp-rates of the back-gate voltage sweep a) from 0 V to -600 V go and back b) from 0 V to -800 V go and back c) from 0 V to -1000 V go and back d) from 0 V to -1200 V go and back on device under the test. Low trapping effects are observed all the way to 1200 V with a low dependence of the substrate bias on the current density.

5.5 Conclusion

We demonstrated an assessment of a GaN-on-silicon buffer structure from the epi-wafer provider ALLOS Semiconductors GmbH targeting 1200 V power applications. A low leakage current and state-of-the-art vertical breakdown voltage above 1400 V was achieved thanks to the thick and excellent crystal quality of GaN buffer. Low trapping effects are observed all the way to 1200 V with a low dependency of the substrate bias on the current density.

6 Conclusions

This thesis presents a study of reliability aspect in GaN-based devices. The activities involves from electrical and optical measurements, high voltage measurements to the study of tapping effect in the device. It also includes long term and short term stress to evaluate the reliability aspect of the devices.

The main outcomes of this thesis are summarized as follow:

- A combined electro-optical methodology has been developed for the study of traps in GaN-based power MIS-HEMTs. The degradation effects are investigated on AlGaN/GaN MIS-HEMTs submitted to the gate step-stress experiments. A correlation between pinch-off voltage variation of the gate stress and the results of electro luminescence measurements is clearly observed. Moreover, the high temperature dependency on the recovery process is also discussed.

- The effect of proton irradiation hardness on the dynamic performance of GaN HEMTs are studied. Following relevant results are demonstrated: the electroluminescence signal increased on the device after radiation, while dynamic-Ron in AlGaN/GaN HEMTs decreased after irradiation; this beneficial effect is ascribed to the minute increase in the leakage of the uid-GaN layer, promoting charge de-trapping from the buffer. No trap level state was detected after the proton irradiation (1.5×10^{14} p/cm^2) by means of drain current transient. These observations are confirmed on large power devices, where additionally the effect of both the off-state drain leakage current and the dynamic Ron can be seen in

the vicinity of the proton impact zone.

- P-GaN gate GaN-based transistors are well-known for positive and stable threshold voltage, the low on-resistance and the high breakdown field for power applications. A discussion on the solutions for minimizing the gate leakage current on this devices is presented. Furthermore, the limitation of dynamic performance and reliability issue in GaN-based normally-off transistors are described. Two processes are introduced to suppress this perimeter-dependent leakage: (A) improving the Schottky/p-GaN interface quality in order to decrease the supply of carriers from the gate metal and (B) proper passivation of the p-GaN sidewall to suppress any interface states and surface roughness leading to a conductive path. Moreover, the pinch-off voltage shifts positive due to electron trapping from the 2DEG into the barrier. If left untreated, the hole current along the p-GaN sidewall will induce hole trapping in the barrier, leading to a sharp decrease in the pinch-off voltage. An estimated value for the trapped charge hints that out-diffused Mg acceptor states may lie at the origin of the trapped positive charge. Both trapping phenomena can be suppressed by combination of high Schottky/p-GaN interface quality and proper p-GaN sidewall passivation.

- The last chapter presents an assessment of GaN-on-silicon buffer structure in order to achieve a high breakdown voltage with low bow and cracks. The assessment was carried out on the structure from the epi-wafer provider ALLOS Semiconductors GmbH targeting 1200 V power applications. Owing to the thick and excellent crystal quality of GaN buffer despite using a carbon-free buffer, a low leakage current and state-of-the-art vertical breakdown voltage above 1400 V was achieved. Moreover, low trapping effects are observed all the way to 1200 V with a low dependency of the substrate bias on the current density. Indeed, this was the first demonstration of trap-free at such high voltage with this material system that could paves the way for 1200 V applications with GaN-on-Si resulting in lower Ron and thus higher efficiency as compared to SiC and Si devices.

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