

Low-cost power gating solution to increase energy efficiency optimising duty cycling in wireless sensor nodes with power-hungry sensors

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Abstract: In this study, a solution focusing on energy efficiency of wireless sensor nodes is presented. Energy dissipation is a key factor affecting the usability of wireless sensor networks (WSNs) in that, in worst cases, in systems without electric mains, the life of a sensor node battery may last even only a few hours. The proposed solution is characterised by very low costs thanks to the use of a small number of electronic components: it allows the optimisation of duty cycling (i.e. the ratio between activity and inactivity periods of sensor nodes) by power gating the node (i.e. turning the whole circuitry off). In particular, this solution is useful for applications that use active power-hungry sensors that are sampled regularly 10 to 1000 times a day. The described power control logic system is able to optimise the duty cycling, notably reducing the power consumption during idle periods, thus increasing the battery life at best up to 100–200 times: this means that the autonomous operation time of a WSN can increase from a few days to several months or even to some years according to the required sampling rate.

1 Introduction

Wireless sensor networks (WSNs) represent nowadays one of the most significant technological frameworks to develop real-time remote monitoring systems. Indeed, WSNs have been realised for the most disparate application scenarios [1], from environmental [2, 3], industrial [4, 5] and cultural heritage [6] monitoring to the smart city context [7]. Due to their small dimensions, sensor nodes can be deployed in large quantities to set up pervasive infrastructures able to collect large quantities of data. Anyway, the final cost of each sensor node represents one of the key parameters affecting the actual realisation of efficient monitoring infrastructures: indeed, sensor nodes whose final cost is of few euros can be easily replicated in large quantities and then pervasively deployed in the environments to be monitored. In many of these scenarios, WSNs are deployed in places where no power grid connection is available: this means that energy efficient solutions for the powering of the sensor nodes have to be found.

Together with costs, energy consumption is the second key factor affecting the usability of monitoring infrastructures, particularly when they have to be deployed in remote areas [8]. In this case, sensor nodes require to be positioned in sites difficult to be reached and thus can be powered only by batteries or through energy harvesting solutions: in both cases, this means that energy efficiency is fundamental to ensure the operativeness of the monitoring infrastructure for long spans of time.

Even if every single component in a sensor node is responsible for power consumption, it is possible to identify three subsystems that are the most significant cause for energy dissipation [9]:

- The data transmission subsystem [10]: Even if employing low power technologies like, for example, LPWAN (LoRa, SigFox) radio modules [11], energy consumption during data transmission cannot be neglected.
- The sensing subsystem: Energy consumption becomes crucial when energy-hungry sensors are employed [12]. In this case, this subsystem may become the most significant cause for energy consumption.
- The data processing subsystem: If no ‘sleep’ procedures are applied, an always-on microcontroller may drastically reduce the lifetime of a sensor node [13].

In addition to these key factors, other less significant components may have a negative impact on the overall power consumption of the node, for example voltage regulators. If we sum up all these factors, the energy dissipation of the circuit may be so high as to reduce the node lifetime to only a few hours.

The aim of this paper is to address these two key parameters, i.e. cost and energy consumption, in order to propose a minimal sensor node prototype composed of a small number of low cost, off-the-shelf components, and characterised by very low power consumption.

The best way to reduce the overall cost of a sensor node is probably to use a small number of off-the-shelf electronic components, identifying the task that the node has to perform and then shaping its operation on it. This means that the features of the node should not be overestimated, the components should be the lowest cost ones and in the smallest number possible. For this purpose, the proposed sensor node architecture is basically composed only of the sensor, the radio module and the power control circuitry. The radio module has been chosen to avoid the use of an *ad-hoc* microcontroller for data processing, while no other components, like memories or analog to digital converters (ADCs) are required since all these features are included in the radio module. In this case, the overall cost of the node is mainly due to this module, while the cost of the sensor is strictly dependent on the parameter to be monitored. The power control logic has been conceived using a few number of components that have negligible prices, almost not affecting the final cost of the node.

Regarding the optimisation of power consumption, several techniques have been studied, focusing on different features of WSNs. Some techniques have focused, rather than on modifying the node architecture, on the realisation of optimised communication protocols, both at MAC layer [14–17] and at Network layer [18–23]. Other solutions have dealt with the ideal node positioning and the network topology [24–30] as well as on clustering algorithms [31]. Anyway, these solutions optimise the power consumption of transmission modules, but have no effect on the dissipation of other components. Software solutions based on the development of *ad-hoc* firmware can be used to power off energy-hungry sensors, with a notable reduction of dissipation [32]. Anyway, they have no effect on other circuit dissipators.

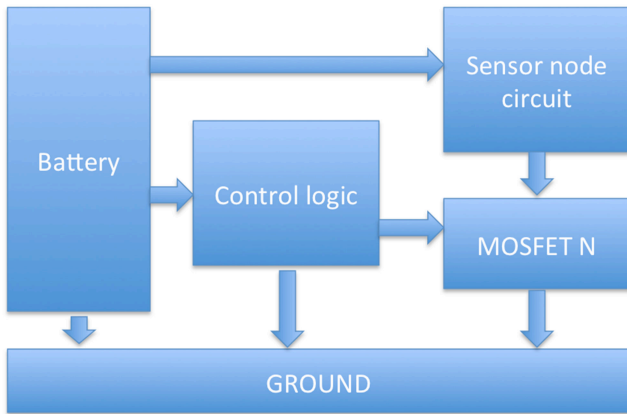


Fig. 1 Architecture of the proposed power gating solution

The best solutions are based on the development of *ad-hoc* power gating systems that can turn off the whole node optimising duty cycling, thus allowing long idle periods and then no power consumption: some solutions based on this approach can be found and will be discussed in detail in Section 3. The solution proposed in this paper follows this philosophy: an *ad-hoc* power gating solution has been designed, realised and tested, proving that the sensor node lifetime can notably increase applying a strict duty cycling policy able to totally switch off the sensor node during the idle periods. Moreover, as anticipated, the proposed architecture is based on a very few number of low price components, and is then fully compliant with the sensor node low-cost requirement. To our knowledge, a power gating system for wireless sensor nodes based on the architecture presented in this paper has never been applied before.

The paper is structured as follows. In Section 2, some related work discussing possible power gating solutions to be applied to wireless sensor nodes is discussed. Section 3 is devoted to the description of the power control logic structure, i.e. the circuit in charge of the power consumption optimisation, while in Section 4 the overall architecture of the sensor node is described. Section 5 focuses on the analysis of the sensor node power consumption while in Section 6 the analytical results are validated through a set of tests. Finally, in Section 7 some conclusive remarks are presented.

2 Related works

Power gating techniques foresee the use of different circuitual solutions that allow to switch off whole electronic systems, or parts of them, in order to reduce power consumption due to the presence of leakage currents [33]. While this technique is commonly applied in integrated circuits [34] and very large scale integration (VLSI) design [35], its application in the WSN context has been treated in very few cases, and a limited number of actual implementations can be found.

A first power gating implementation for wireless sensor nodes was proposed in [36]: anyway, the presented solution is still related to the world of integrated circuit design and is thus very far from the application scenario proposed in this paper. The use of a power gating system for a wireless sensor node is also discussed in [37]: the described solution foresees the realisation of a sensor node provided with two different microprocessors, a high-end one and a low-end one, the second of which is in charge of waking up the first one. While this solution is only proposed and not realised, it is still by far more complex and power hungry than the solution described in this paper since the low-end microprocessor still has to be powered. A similar architecture based on the use of an *ad-hoc* controller is also discussed by Panic *et al.* [38, 39].

The use of power gating in wireless sensor nodes is also introduced by De Nil *et al.* [40]: while no technical solution is proposed, the authors analyse the impact of this technique according to the applied duty cycling rate, concluding that it is efficient only for low duty cycle systems, encouraging its adoption for the scenario discussed in this paper. A similar approach is also

proposed in [41], where the authors analyse the actual power consumption reduction achievable by applying a power gating system to a wireless sensor node.

A few number of papers propose different solutions to control the wake up of the circuit, i.e. the trigger of the switches that in all cases are simple metal-oxide-semiconductor field-effect transistor (MOSFETs), applied in the same way as in the solution proposed in this paper. Chen *et al.* [42] present the use of differential monostable multivibrational delay elements to realise full-swing slow timers, while Popovici *et al.* [43] propose two different solutions: the use of the internal microcontroller of the sensor node and the use of a wake-up radio. The first solution, also discussed by Nikolic *et al.* [44] that propose the use of the internal real-time clock (RTC) is still not efficient enough because the microcontroller (MCU) has in some way to be kept on. The second one, also discussed in [45], is not cost-effective because it requires an *ad-hoc* radio module. To the best of our knowledge, the solution presented in this paper is the first one based on the use of an *ad-hoc*, low cost, control logic, able to trigger the wake up of the whole sensor node, minimising at the same time sensor node power consumption and overall cost.

3 Power gating system structure and functioning

The solution proposed in this paper is described in Fig. 1 and is based on the optimisation of the duty cycle through the total disconnection of the power supply when the node is not sampling or transmitting. In this way, power dissipation depends only on the power gating control logic components, and is then very low in comparison with the one of the entire circuit (in particular, 5–6 order of magnitude less).

The proposed power gating control logic is built using only the following components: a binary counter/divider and an oscillator (with two resistors and two capacitors to set the clock), a switch (e.g. a MOSFET) and an AND gate. Through the right connections between the control logic components, it is possible to determine how long and when the sensor node will work.

As stated above, an *ad-hoc* switch has to be inserted, to connect/disconnect the power supply to the whole circuit: for this purpose, a MOSFET can be placed between the sensor node ground (connected to the drain) and the negative pin of the battery (connected to the source). When the MOSFET is 'ON', the circuit is closed and the sensor node works. It is important for the MOSFET choice to take care of the device resistance when it works as a switch (i.e. in triode region). Indeed, it has to be as small as possible to avoid a too high voltage drop over the MOSFET, when the current of the circuit flows through it. The gate of the MOSFET is controlled by the output of the AND gate. The MOSFET is activated if the voltage difference V_{GS} (between gate and source) becomes greater than the threshold voltage V_{TH} . If the source voltage V_S is equal to the ground voltage V_G , V_{GS} will be equal both to V_G and to the voltage of the AND gate output. Therefore, the latter can assume two states: '0' and '1'. The value '0' corresponds to a low voltage that tends to 0 V, whereas the value '1' corresponds to the supply voltage of the logic gate. For this reason, it is mandatory that the supply voltage of the control logic is higher than the threshold voltage of the MOSFET to ensure that a high output of the AND gate activates the MOSFET. When the control logic circuit is turned on, the counter starts setting the output pins high or low until it finishes the count and resets itself [the voltage value is V_{cc} (high) and 0 (low) like the AND gate].

The binary counter has an internal oscillator whose oscillation frequency is settable through a resistor and a capacitor: the relationship between these two components and the oscillation frequency of the selected counter will be discussed later. In order to build a synchronised network where all sensor nodes are working simultaneously, a trimmer must be used instead of a simple resistor to set the counter's clock because the tolerance of the resistor and the capacitor can generate different cycle times for components with the same par value. Through the trimmer it is possible to regulate the time constant RC to set the clock times of the nodes.

To drive the AND gate output, it is possible to choose a combination of 'high levels', connecting the output pins of the

counter to the AND gate inputs: the AND gate output will be high only when all inputs are high. There are several possible combinations. Using the most significant bits (MSBs), the binary counter allows to set the switch OFF for a 'long time' and ON only for the 'sampling time', reducing duty cycle. Instead, using the least significant bits, the sensor node can be turned on more times in a single cycle counter, thus increasing duty cycling.

Table 1 shows a simple example based on a 5-bit counter where pins Q_2 , Q_3 and Q_4 (the most significant ones) are connected to the AND input. This combination of bits allows 28 clock times with the sensor node set OFF, and a little window, 4 clock times long, when the sensor node is ON. If supposing cycle counter $CC = 32 \cdot T_{ck} = 3600$ s where $T_{ck} = 112.5$ s is the clock time, and energy dissipation tending to 0 when the sensor node is OFF, the sensor node is switched ON 24 times per day for 7 min and 30 s ($T_{ck} \cdot 4 = 450$ s), thereby allowing a small time interval when battery consumption is greater than during the rest of day.

This configuration can be changed, for example, by connecting also pins Q_1 and Q_0 to the AND input. In this case, only one combination is obtained when the sensor is active, 24 times per day for about 2 min ($T_{ck} = 112.5$ s).

While this simple example is based on a 5-bit counter, usually 14/16-bit counters are employed. These counters do not allow large time clocks: the maximum achievable for a full cycle count is around 1–2 h. For this reason, the proposed solution is ideal for applications that sample regularly and where the sample frequency is not too low.

As shown in Table 1, more samples in a single cycle counter can be acquired. The advantage of this solution is to have shorter time windows with the same number of AND gates and thus a greater saving of the battery. For example, with one AND gate with

Table 1 5-bit counter

Q_4	Q_3	Q_2	Q_1	Q_0	Decimal	State
0	0	0	0	0	0	off
0	0	0	0	1	1	off
0	0	0	1	0	2	off
0	0	0	1	1	3	off
0	0	1	0	0	4	off
0	0	1	0	1	5	off
0	0	1	1	0	6	off
0	0	1	1	1	7	off
0	1	0	0	0	8	off
0	1	0	0	1	9	off
0	1	0	1	0	10	off
0	1	0	1	1	11	off
0	1	1	0	0	12	off
0	1	1	0	1	13	off
0	1	1	1	0	14	off
0	1	1	1	1	15	off
1	0	0	0	0	16	off
1	0	0	0	1	17	off
1	0	0	1	0	18	off
1	0	0	1	1	19	off
1	0	1	0	0	20	off
1	0	1	0	1	21	off
1	0	1	1	0	22	off
1	0	1	1	1	23	off
1	1	0	0	0	24	off
1	1	0	0	1	25	off
1	1	0	1	0	26	off
1	1	0	1	1	27	off
1	1	1	0	0	28	on
1	1	1	0	1	29	on
1	1	1	1	0	30	on
1	1	1	1	1	31	on

8 inputs and a 14 bits counter it is possible to use bit 6 as the output instead of the most significant one (bit 8) to drive the AND gate. For this reason, it is often preferable to choose the longest possible time constant, and subsequently to decide the number of sampling windows in one cycle counter.

An additional feature that can be added to save energy is to give two different power supplies to the control logic and to the rest of the circuit, according to the different powering voltages. It is then possible to supply the control logic with a certain number of batteries in series (e.g. one, two or three) and to supply the rest of the circuit by simply adding additional batteries. This can be done because, despite the control logic constantly being on, the whole power dissipation is very low in comparison with the interval when the whole node sensor is on. Thus, the energy dissipation difference between the batteries that are connected to the whole circuit and the batteries that are connected only to the sensor node control logic becomes negligible. This additional solution will be discussed in the next section.

4 Power-gated sensor node prototype

In this section, the realisation of a sensor node prototype based on the proposed power gating solution will be presented: this node is expected to be integrated into a mesh WSN which samples regularly 20–25 times a day. According to the low cost requirement, the sensor node is composed only of a transmission module (XBee Series 2, with a current absorption declared in the datasheet being of around 40 mA in transmission [46]) that allows the setup of a ZigBee mesh network, an energy-hungry active sensor (in this case a GP2Y0A21YK Sharp Infrared Proximity Sensor whose current absorption declared in its datasheet is 30 mA [47]), two voltage regulators and a small number of other components (resistors and capacitors).

The XBee radio module has been chosen because it is provided with an internal ADC and with a set of analogue ports that allow the direct connection of a sensor, without the need for an additional microcontroller. When turned on, the module automatically samples the values available on the activated analogue ports and transmits them: its shutdown does not pose any kind of problem on the saved states of its internal RAM.

The power control logic is integrated into this structure, between the power source (batteries) and these components. Its structure is very simple and is made of the following components, characterised by very low costs:

- 1 HEF4060BP 14-stage ripple carry binary counter/divider and oscillator;
- 1 HEF4073BP triple inputs AND gate;
- 1 STP55NF06 power MOSFET;
- 1 CB10LV trimmer;
- 2 resistors (R_1 and R_2) and 2 capacitors (C_1 and C_2).

The sensor node prototype is shown in Fig. 2 while Fig. 3 shows the power control logic wiring diagram.

As mentioned above, the choice of the MOSFET is very important. The device must sustain the entire current flowing through the sensor node circuit and furthermore it must offer an ON resistance as small as possible.

The resistor R_1 and the capacitor C_1 have to be chosen to satisfy the condition that the counter cycle is a multiple of the sampling time. The oscillation frequency of the counter is

$$f_{osc} = \frac{1}{R_1 \cdot C_1 \cdot 2.3} \quad (1)$$

According to the component features, a resistor (R_2) and a capacitor (C_2) have also to be connected to pin 11, such that

$$R_1 \ll R_2 \quad (2)$$

and

$$R_2 \cdot C_2 \ll R_t \cdot C_t. \quad (3)$$

In order to choose the right value for these components, the oscillation frequency has to be calculated through the formula

$$f_{osc} = \frac{2^n}{T} \quad (4)$$

where n is the bit number of the binary counter and T is the total time of the cycle counter. Using $T = 1h = 3600$ s and $n = 14$ the following values can be obtained:

$$f_{osc} = \frac{16384}{4.5511} \text{ Hz} \quad (5)$$

and

$$t_{ck} = \frac{1}{f_{osc}} = 0.219726562 \text{ s}. \quad (6)$$

Since a synchronised network is expected to be realised, first it is suggested to choose the capacitor C_t , and then to place a trimmer

(or a resistor in series with a trimmer) whose value is R_t , in order to set the exact time constant RC for the circuit.

While a $C_t = 220$ nF capacitor was chosen, an $R_t = 434243.3 \Omega$ value was calculated.

It is now necessary to check whether the trimmer covers or not the range of the error generated by the product of the time constant. As is known, when a product is made, the tolerances associated with the nominal values are multiplied, further increasing the error. For this purpose, a simple resistor (220 k Ω) and a trimmer $0 - 470$ k Ω (CB10LV) were placed in the circuit.

The connection between the counter and the AND gate had then to be selected. First, the number of the available AND gate inputs had to be determined. The HEF4073BP circuit has three logic gates with three inputs. Considering that the combination of bits that turns the sensor node ON is unique, two of the outputs of the logic gate are connected to two of its inputs; therefore, seven available inputs remain. Having chosen the cycle counter equal to the sampling time, the MSBs have to be connected from the counter to the logic gate. In this way, the sampling time is

$$T_{on} = T_{ck} \cdot 2^m = 14.062499968 \text{ s} \quad (7)$$

where m is the number of disconnected bits.

HEF4060BP counter does not have all the bits represented by a pin: the fourth MSB pin is missing. This means that there will be two different sampling sessions near the end of the count. When there are 1088 clock pulses at the end of the count (about 4 min), there will be a first sampling session about 14 s long, while a further session will start 14 s before the end of the count, ending simultaneously with it.

The sensor node will be on for a total of 28 s each hour, while it will be totally off during the remaining time. Since the XBee module only has to sample the sensor value and transmit it through ZigBee connection, the total disconnection of the node from the power supply has no effect on the internal states of the RAM that will be reset at the end of each cycle. When turned on, the XBee module will have to connect to the base station in charge of receiving the sampled data: the procedures of activation, association to the network and polling to determine if the network coordinator (i.e. the base station) has indirect messages for the XBee itself, require a time interval that has been experimentally measured in <5 s. This means that this delay does not constitute a problem if compared with the 28 s activation period. Indeed, this

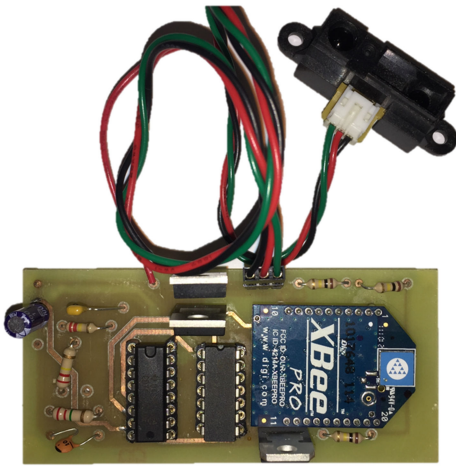


Fig. 2 Sensor node prototype

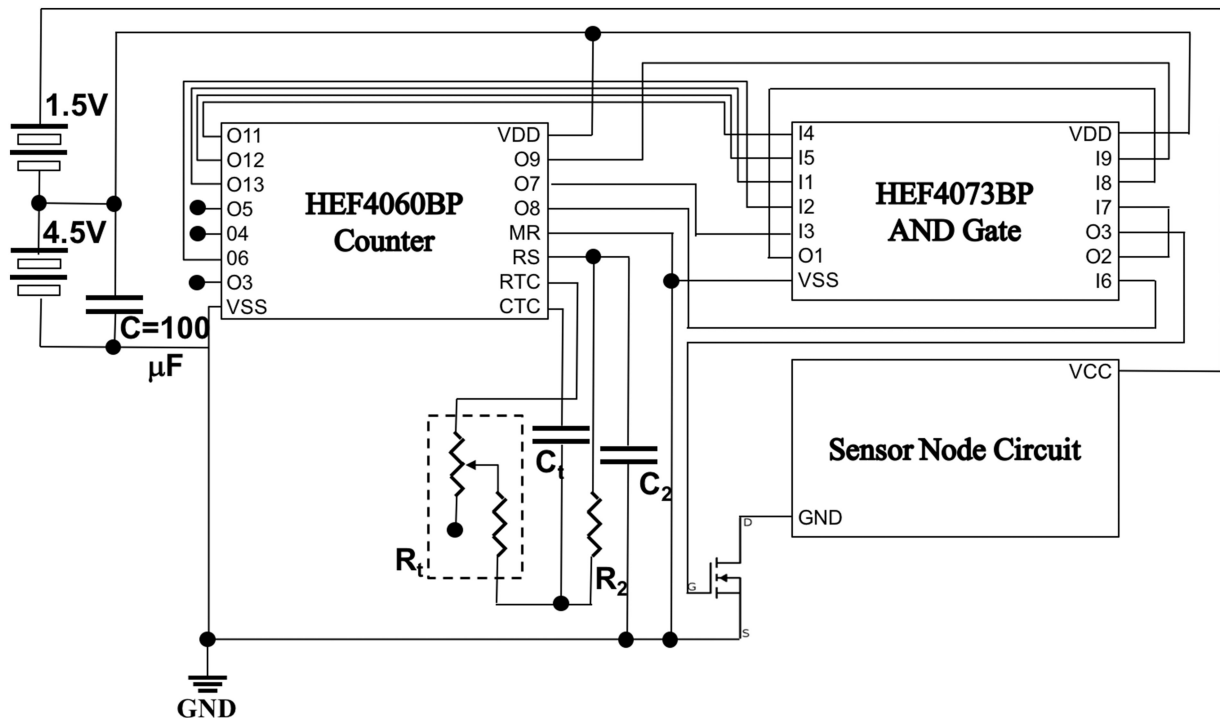


Fig. 3 Power control logic wiring diagram

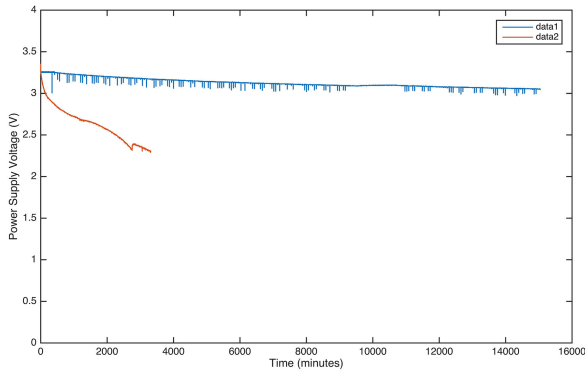


Fig. 4 Two consumption curves deriving from the experiment performed with and without the power gating system, in blue and in red, respectively

fact has been confirmed during the tests described in Section 6 when, along the whole testing period, no packet loss occurred.

5 Sensor node power supply

In this section, the most suitable method to power the control logic is analysed for the example described in the previous section, and the ideal sensor node lifetime is calculated. Both the chosen components support a voltage from 3 to 15 V, but, obviously, power dissipation is directly proportional to the applied voltage: in order to maintain the energy consumption as low as possible, the lowest allowed supply voltage is required.

On the other hand, the correct working of the sensor node must also be ensured when the voltage of the batteries starts to decrease due to their usage. The minimum voltage required by the control logic components is 3 V: while 1.5 V batteries are employed, the best choice for the control logic power supply is 4.5 V.

An important factor that must be taken into account is that energy dissipation of the control logic network has to be negligible with respect to the power dissipation of the sensor node circuit, even if this one is turned on only for a short amount of time. According to the previous calculations, the sensor node is turned on 28 s per hour and during this period the average value of the absorbed current (I) is about 60 mA. Instead, regarding the control logic, the current absorption is 19 μ A. These values have been experimentally acquired by powering the circuits with a laboratory DC power supplier and then measuring the absorbed current with a digital multimeter.

In order to compare the energy dissipation of the two circuits, it is convenient to think in terms of battery capacity, that is usually expressed in mAh: since the power control logic is always on, it consumes around $C_{cl} = 19 \mu$ Ah.

Instead, the consumption of the sensor node C_{sn} can be measured by applying the following formula:

$$C_{sn} = 60 \text{ mA} \cdot \frac{28}{3600} \approx 0.467 \text{ mAh} = 467 \mu\text{Ah}. \quad (8)$$

The current dissipation, and thus the energy consumption of the sensor node is then $467 \mu\text{Ah}/19 \text{ Ah} \approx 25$ times greater than the current dissipation of the power control logic. Since the control logic dissipation can be considered negligible, it is possible to use a single set of batteries to feed both the circuits, taking the voltage to feed the power control logic from a lower number of cells and, instead, using the complete set of batteries to feed the sensor node circuit (see Fig. 3).

The overall consumption C_{tot} is

$$C_{tot} = 19 \mu\text{Ah} + 467 \mu\text{Ah} = 486 \mu\text{Ah}. \quad (9)$$

To calculate the lifetime of the node, a powering solution based on the use of four high-capacity AA lithium batteries (1.5 V 3000 mAh) connected in series to feed both the circuits is considered.

The lifetime of the system L_{wo} without the power control logic is given by the capacity of the batteries divided for the consumption of the sensor node considered always on (60 mAh)

$$L_{wo} = \frac{3000 \text{ mAh}}{60 \text{ mAh}} = 50 \text{ h} \approx 2 \text{ days} \quad (10)$$

The lifetime of the power gated structure (i.e. the sensor node plus the power control logic) L can then be calculated dividing the capacity of the battery for the overall consumption C_{tot}

$$L = \frac{3000 \text{ mAh}}{0.486 \text{ mAh}} \approx 6173 \text{ h} \approx 257 \text{ days}. \quad (11)$$

This result shows that by applying the proposed power gating solution the lifetime of the node increases by a factor equal to $257/2 = 128.5$. While the calculated lifetime value is ideal, this factor is expected to be preserved in a real application since it only depends on the applied duty cycling procedure.

6 Experimental results

In order to validate the analytical results calculated in Section 5, a comparative experiment to measure the actual lifetime of the power gated sensor node has been performed. The experiment has been set up as follows:

- The sensor node has been activated with a set of four brand new, off-the-shelf 1.5 V AA batteries without the power gating system, measuring every minute the voltage across two of the four batteries used to power supply the circuit. The sensor sampling and transmission rate has been set at 1 sample each 5 s in order to measure the power consumption with the sensor node fully active. The lifetime of this node has been ~ 50 h;
- In order to verify the correct operation of the system, another sensor node, configured as a base station, has been activated, receiving data from the first one;
- Then, the same experiment has been set up replacing the batteries with another brand new set, and activating the control logic system to power gate the sensor node. The node has been kept operative for around 250 h (precisely 15,045 min).

The results of the experiment show that, as it is expected, the lifetime of the sensor node without the control logic is ~ 50 h (exactly 2750 min). On the other hand, the whole lifetime of the power gated sensor node can be estimated using the values achieved through the voltage measurement. Indeed, all batteries present a characteristic discharge rate that can be used to estimate their lifetime. Fig. 4 shows the results of the experiments: it is possible to notice the rapid falling of the red line (first experiment) with respect to the blue line. The saddle point that can be easily seen at the end of the red line indicates the end of the working of the non-power gated sensor node (after 50 h as anticipated).

In order to estimate the lifetime of the power gated sensor node, a comparison between the data obtained with the two configurations has been performed. After the 15,045 min (~ 250 h) activation period of the power gated sensor node, the measured voltage of the batteries reached the value of 3.0498 V: this value has been reached by the non-power gated configuration after 125 min. The voltage drop is only due to the discharge rate of the batteries, which is characteristic and almost equivalent for batteries of the same type and brand. Therefore, since the lifetime of the non-power gated sensor node has been measured in 2750 min, the overall lifetime \tilde{L} of the power gated node can be calculated through the following proportion:

$$\tilde{L} = \frac{2750 \times 15045}{125} = 330990 \text{ min} \approx 230 \text{ days}. \quad (12)$$

This value is perfectly in line with the lifetime value calculated in Section 5: the slight difference is mainly due to the not ideal operating conditions of the real scenario.

7 Conclusion

In this paper, the architecture of a power gating solution for sensor nodes based on the use of low-cost components has been presented. The control logic system described is able to notably reduce the power consumption of sensor nodes: this is especially important in the case of nodes equipped with energy-hungry sensors. At the same time, the control logic system is realised with very low-cost components: this means that the overall cost of each single sensor node is kept as low as possible, allowing the deployment of a monitoring infrastructure composed of a large quantity of nodes.

This kind of solution can cover a wide range of applications, especially for monitoring systems to be deployed in remote areas or out-of-reach sites: environment, cultural heritage or home automation are just a few examples of scenarios where the proposed solution can play an important role in developing an efficient monitoring infrastructure.

While efficient and cost effective, the proposed solution still has some limitations that need to be treated and overcome. In particular, its main drawback derives from the fact that any error in the design phase can only be corrected by changing the hardware of the control logic: this means that the circuit design phase has to be carried out with a high level of precision. A more flexible architecture is then expected to be designed in the future.

8 References

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