Understanding the impact of split-gate LDMOS transistors: analysis of performance and hot-carrier-induced degradation

P. Magnone[1], A. N. Tallarico[2], S. Pistollato[1], R. Depetro[3], G. Croce[3]
[1]*DTG, University of Padova, Vicenza, Italy*
[2]*ARCES and DEI, University of Bologna, Cesena, Italy*
[3]*Technology R/D, STMicroelectronics, Agrate Brianza, Italy*
E-mail address of corresponding author: paolo.magnone@unipd.it

Abstract

In this paper a split-gate LDMOS transistor is investigated. A dedicated terminal, namely split-gate, is introduced in order to control the field plate region separately with respect to the channel region. The performances of the device, in terms of on-resistance, breakdown voltage and capacitances, are compared with those of a conventional device. The hot-carrier-induced degradation of the device is also investigated, highlighting the influence of the split-gate voltage. This work allows identifying a tradeoff between the performance and reliability of the component, which is controlled by the voltage applied to the split-gate terminal.

1. Introduction

LDMOS transistor represents a suitable solution for integrated smart power applications. Its structure features an extended gate field-plate aimed at ensuring a good trade-off between performance and reliability. However, the relatively large gate area, hence the gate capacitance, may limit the dynamic performance of such devices. To mitigate this issue, a separate secondary gate can be considered for the field-plate region, namely split-gate LDMOS [1-4]. In high-frequency applications, the split-gate contact can be biased with a constant voltage, allowing to reduce the capacitance seen from the gate terminal.

Hot-carrier degradation (HCD) is a typical effect, limiting the lifetime of LDMOS transistors [5-7]. The large lateral electric field leads to the creation of interface traps in the drift region, hence degrading the on-resistance of the device.

This work aims at experimentally investigating the performance and the reliability of split-gate structures, which is described in section 2. In section 3, the influence of split-gate terminal voltage is analyzed, focusing on the on-resistance, breakdown voltage and capacitances of the device. The achieved results are compared with those of a conventional device, having a continuous gate contact. In section 4, hot-carrier degradation is investigated and the influence of a separate split-gate contact is evaluated. Finally, in section 5, the main achievements of the paper are summarized in the conclusions.

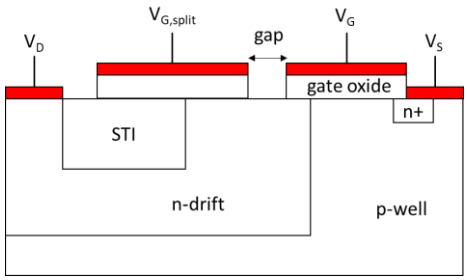

Fig. 1: Schematic view of an n-type split-gate LDMOS. A gap region (not in scale) is introduced in order to control by means of different terminals the channel region (V_G) and the field-plate region ($V_{G,split}$).

2. Experimental

The device under test is a 40V n-type LDMOS integrated in 90 nm Bipolar-CMOS-DMOS (BCD) technology by STMicroelectronics. Two different topologies have been investigated: a "conventional" structure with a continuous gate contact; a "split-gate" structure with two accessible gate contacts, adopted to bias the channel and drift regions separately, as shown in the schematic view reported in Fig. 1.

Hot-carrier degradation is investigated by stressing the device with a constant large drain voltage while the gate voltage is selected to maximize the impact ionization (*ii*), representing the worst-case scenario as it is periodically experienced during the switching processes in a power application. The quantification of wear-out is done by measuring the on-resistance in linear region (V_{DS} = 0.1V) at a large gate voltage (V_{GS} = 5V). Capacitance-voltage measurements are performed by applying a constant bias, between the considered terminals, and by superimposing a small signal with 50mV of amplitude and 1MHz of frequency. All the analyses are performed at room temperature.

IV and CV measurements are carried out by means of Agilent 4156B parameter analyzer and Agilent E4980A LCR meter, respectively.

3. Performance of fresh devices

The transfer characteristics of the split-gate LDMOS are reported in Fig. 2 for different value of the split-gate voltage $V_{G,split}$. The increase of $V_{G,split}$ leads to an increase of the drain current and hence to a reduction

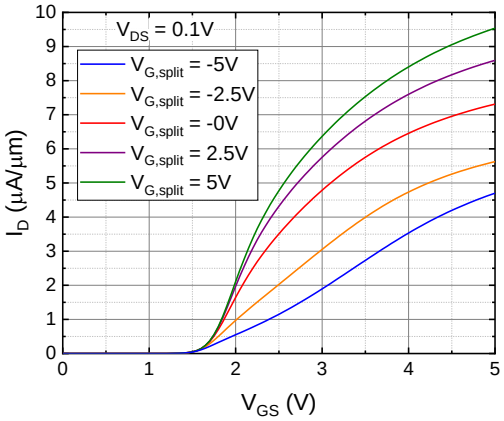

Fig. 2: Trans-characteristics at V_{DS}=100mV as a function of split-gate voltage.

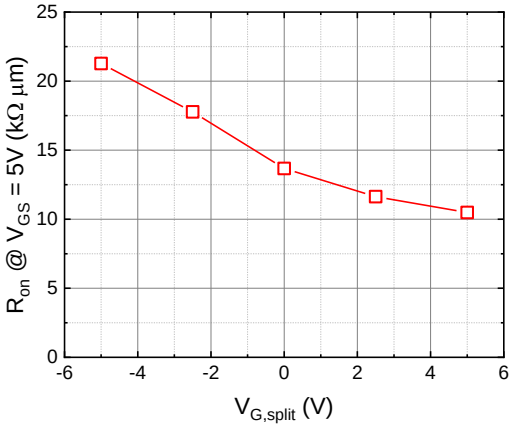

Fig. 3: R_{on} evaluated at V_{GS}=5V and V_{DS}=100mV as a function of split-gate voltage.

of on-resistance, R_{on}, as shown in Fig. 3. This is due to the accumulation of electrons in the drift region. The breakdown voltage is evaluated in Fig. 4 as a function of $V_{G,split}$. In this case, the influence of split-gate voltage is limited, unless a large negative voltage is applied.

In Fig. 5, the transfer characteristics of a conventional device is compared with that of a split-gate device in which gate and split-gate terminals are short-circuited. A larger transconductance is observed in the case of conventional device. Therefore, R_{on} is worsened in the case of split-gate structure because of the space region between the gate terminal and field-plate region.

The gate-to-channel capacitance (C_G) is reported in Fig. 6. This capacitance represents the input capacitance of the device and is representative of the driving capability of the device. Hence, a lower value is desirable also to minimize driving losses. The

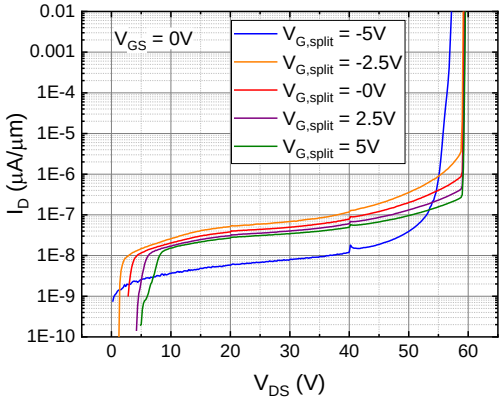

Fig. 4: Breakdown voltage at V_{GS}=0V as a function of split-gate voltage.

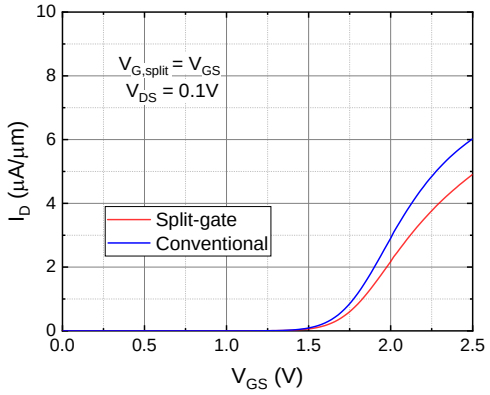

Fig. 5: Trans-characteristics at V_{DS}=100mV for split-gate device with $V_{G,split}$=V_{GS} and a conventional device. The conventional device exhibits a larger transconductance, meaning that the presence of the gap negatively affects the transport within the channel.

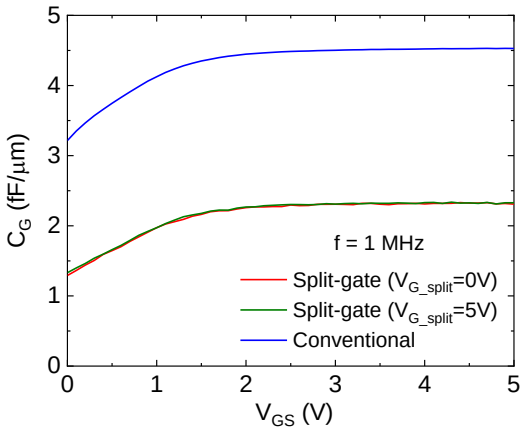

Fig. 6: Gate-to-channel capacitance as a function of the gate voltage. Split-gate device allows significantly reducing the input capacitance.

capacitance is measured between gate and source/drain terminals. During the measurement the split-gate voltage is kept at a constant voltage (as reported in Fig. 6), while source, drain and substrate are biased to 0V. The split-gate device exhibits roughly half of the gate capacitance, compared to the conventional device. Moreover, this value is independent of the split-gate voltage.

The drain-to-gate capacitance (C_{DG}) is reported in Fig. 7. In the case of split-gate device, this capacitance includes both values of gate and split-gate regions. Source, substrate and gate terminals are biased to 0V, while the split-gate terminal is biased to 0V or 5V. C_{DG} is a relevant parameter affecting the switching performance of the device. From fig. 7, a similar value is observed for both device, while the biasing of the split-gate device leads to a shift of the CV curve. It is worth noting that, the small difference, between conventional and split-gate device, is comparable with the accuracy of the instrument and cannot be considered relevant.

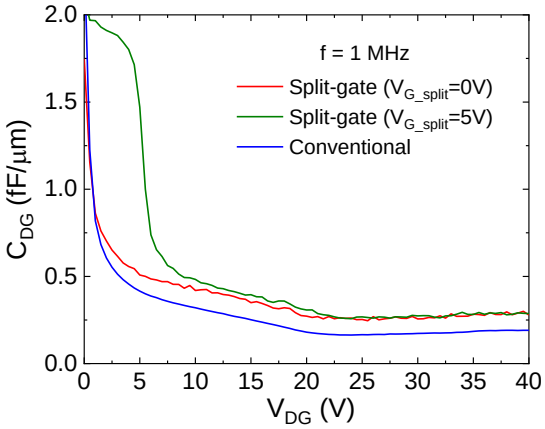

Fig. 7: Drain-to-Gate capacitance as a function of the drain voltage. Similar capacitance is observed in both conventional and split-gate structure.

4. Hot-carrier-induced degradation

A comparison between HCD in split-gate and conventional devices, at V_{DS}=40V, is reported in Fig. 8. The split-gate device is biased with $V_{G,split}$=V_{GS}, during both measure and stress phases, so that its behavior is as close as possible to the one of a conventional device. As a result, the observed HCD is very similar for both structures.

It is well known as the level of degradation due to HC is related to the impact ionization process. Therefore, it is important to estimate the value of the gate voltage at which the peak of *ii* occurs, typically with a gate over-drive voltage ranging between 0.5V and 1V [8]. Fig. 9 reports the analysis of R_{on} degradation as a function of the gate voltage, considering V_{DS}=40V and $V_{G,split}$=V_{GS}. HCD appears to be poorly dependent on the gate voltage in the range of V_{GS} comprised between 2.0V and 2.6V. This result suggests that the peak of the electric field is localized close to the drain side, where the gate and split-gate voltages have a lower impact [1]. The dependence of the drain stress voltage on the on-resistance degradation is reported in Fig. 10. In order to predict the lifetime of the device, an increase of R_{on} of 10% is considered as a failure criterion. By assuming a simple power law fitting for V_{DS}=40V (i.e. the nominal operating voltage of the device), a lifetime of $3.95 \cdot 10^6$ seconds, which is longer than 1000 hours, is achieved. However, this kind of fitting typically leads to an overestimation of the lifetime, while other models, accounting for the long-term saturation effects [7], may be used to better predict the device lifetime.

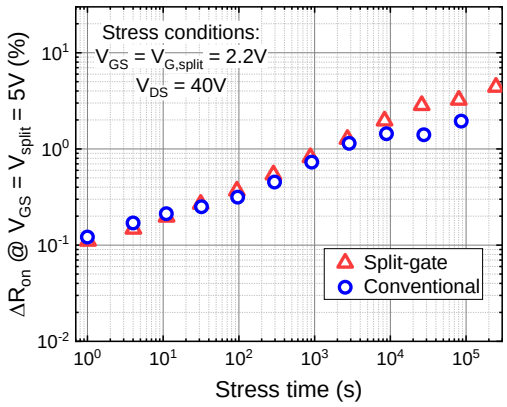

Fig. 8: R_{on} degradation after HC stress for split-gate and conventional structures.

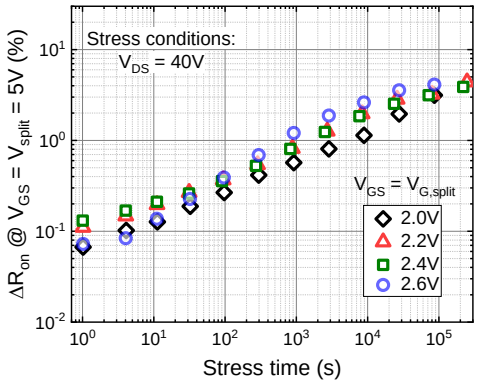

Fig. 9: R_{on} degradation as a function of the gate voltage. Split-gate voltage is kept constant during this analysis.

In Fig. 11, split-gate devices have been stressed with different $V_{G,split}$, ranging from 0 to 5V, and V_{DS}=40V.

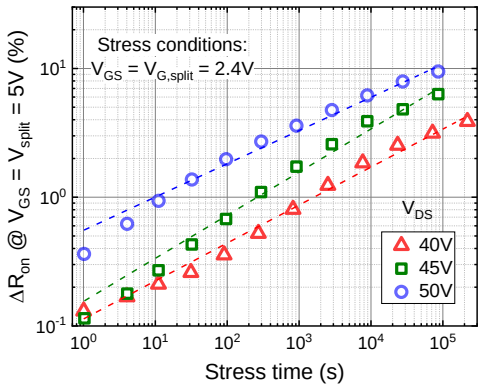

Fig. 10: R_{on} degradation after HC stress for split-gate devices as function of the drain stress voltage.

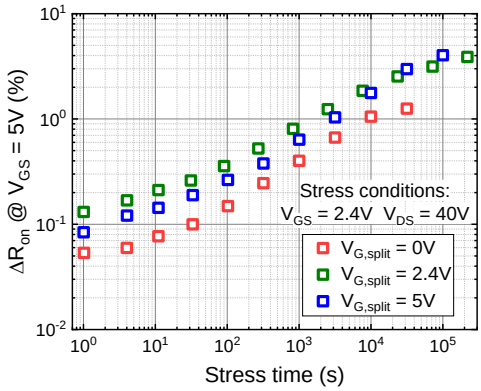

Fig. 11: R_{on} degradation after HC stress (V_{DS} = 40V) as a function of the split-gate voltage.

By keeping $V_{G,split}$=0V, a lower degradation is observed, suggesting that the peak of the electric field underneath the STI region is minimized.

4. Conclusions

In this work, a split-gate LDMOS structure has been investigated. With respect to a conventional device, the field-plate region is controlled with a separate terminal. Because of this solutions, the input capacitance is significantly reduced (halved with respect to the conventional device) while the C_{DG} is almost unchanged.

The adoption of a large $V_{G,split}$ allows reducing the on-resistance of the device, because of electrons accumulation in the drift region, while the impact on the breakdown voltage is limited. On the other hand, considering HC stress at V_{DS}=40V, lower values of $V_{G,split}$ allow slightly reducing the R_{on} degradation. Hence, a tradeoff between performance and reliability can be identified.

In comparison to a conventional structure, the wear-out of R_{on} during HC stress seems to be comparable in split-gate devices. However, the gate capacitance to be driven is smaller, allowing better high-frequency performance.

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