

“Limiting Power Cycling Stress in Power MOSFETs by Active Thermal Control”

P. Magnone, H. Abedini, A. Petucco

University of Padova, Department of Management and Engineering, Vicenza, Italy

ABSTRACT

In this work we propose a system which is able to actively control the temperature of a power MOSFET, in order to limit the temperature swing and hence to reduce the power/thermal cycling effect. To this purpose a dedicated driving circuit, allowing to control the gate voltage of the switching device under investigation, is used in a synchronous buck converter. Therefore, power losses can be modulated in order to reach the desired temperature through self-heating effects. The implemented control system is able to compensate the non-linear relationship between the gate voltage and the on-resistance. Moreover, to improve the response of the system, a predictor has been implemented, having the capability of on-line tuning the thermal resistance of the device. Experimental results are reported to demonstrate the suitability of this solution to control the temperature in the semiconductor device. The reduction of temperature swing under power and thermal cycling is also demonstrated.

I. INTRODUCTION

In modern power converters, the reliability of the system is significantly limited by the failure of semiconductor devices [1]. One of the main mechanisms of failure is the thermal/power cycling. It has been demonstrated that the lifetime of power devices is strongly affected by the temperature swing, while the average temperature has a lower impact [2, 3]. Based on this idea, several solutions have been proposed in literature, aimed at limiting the temperature swing in power devices [4-10]. To achieve this goal, the temperature of the device is actively controlled by modulating the losses in the device. Hence, due to the self-heating effects, the junction temperature can be increased to the desired value. The gate resistance, gate voltage, switching frequency or gate transient shaping are typically controlled in order to modulate the switching losses in the device.

In this work, we propose a solution in which the temperature of a power MOSFET is actively controlled by changing the gate voltage level during the conduction phase. The conduction losses can be then modulated by increasing the on-resistance (R_{on}) of the device. This parameter is strongly related to the gate voltage and can easily reach values ten times higher than the nominal value. However, the relationship between the on-resistance and the gate voltage (V_G) is significantly non-linear, especially when approaching close to the threshold voltage. The control system is based on an experimental R_{on} - V_G look-up table, whose values are used to compensate the output of the regulator and to obtain a closed-loop response independent of the considered operating point. Moreover, a feedforward system is implemented to predict the drain voltage (and hence the on-resistance), during the conduction phase, to achieve the desired reference temperature. In order to improve the effectiveness of the predictor, the thermal resistance is tuned during the real-time operation of the system. Target applications for this kind of methodology could be switch-mode power supplies, in which low voltage devices are adopted. For sake of simplicity the solution reported in this paper is based on discrete components, but the actual target could be a driver integrated in the power device.

The paper is organized as follows. In section II, we describe the developed board and the experimental setup adopted in order to test the proposed methodology. Moreover, the active thermal control approach is introduced. In section III, we discuss the control strategy adopted to accurately set the temperature inside the device and hence to limit the power/thermal cycling phenomenon. In section IV, we report the experimental validation of the developed system and the simulations results in which we analyze the choice of controlling the case temperature rather than the junction temperature. Finally, in section V, the main achievements of this work are summarized.

II. EXPERIMENTAL SETUP AND ACTIVE THERMAL CONTROL APPROACH

In order to validate the proposed methodology, we considered a synchronous buck with a switching frequency of 20kHz, a nominal input voltage of 12V and an output voltage of 6V. A schematic representation is reported in Fig. 1. The low-side switch (Q4) is an n-MOSFET, while the high-side (Q3) switch is a p-MOSFET. In this work the active thermal control is implemented in the high-side switch, even if the same methodology can be applied to the other switch as well. A current sensor LEM LTSR 15-NP is placed in series to the inductor to measure the output current and an optically isolated voltage amplifier (TLP7820) is used to measure the V_{DS} of the p-MOSFET. A Texas Instruments microcontroller (TMS320F28377S) is adopted to acquire the feedback signals, to implement the controller and to generate the control signals. A type K thermocouple is fixed on the p-MOSFET package in order to estimate

the temperature of the device. Hence, in this work the case temperature t_c will be controlled. Although a larger junction temperature is expected, the dynamics of junction and case temperatures are supposed to be the same. Under this hypothesis, a reduction of the case temperature swing will lead to a minimization of the junction temperature swing. It is worth noting that, in the case of fast power cycling phenomena, this assumption cannot be assumed anymore. This issue will be discussed in more details in the section IV.C.

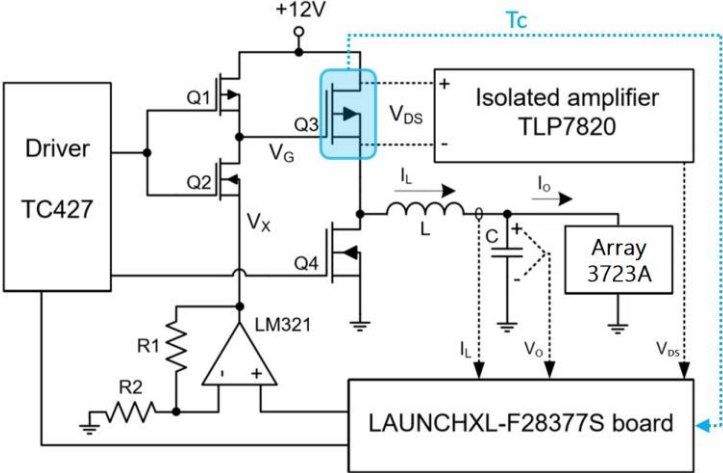


Figure 1. Schematic representation of synchronous buck converter with dedicated driving circuit to control the gate voltage of p-MOSFET transistor (Q3). An electronic load is connected to the converter output to change the load conditions and hence to generate a power cycling.

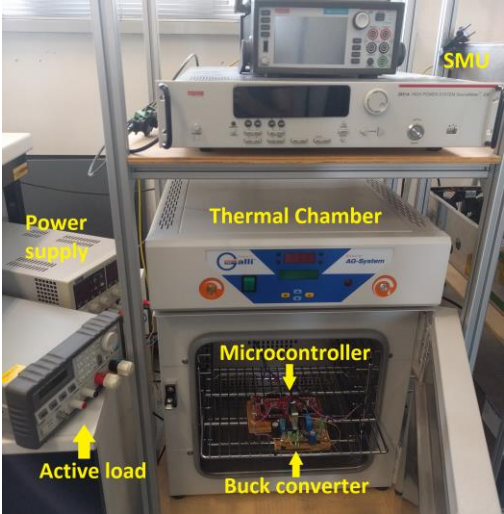


Figure 2. A picture of the experimental setup.

An electronic load (ARRAY 3723A) is connected to the output of the converter in order to emulate the effect of power cycling. The converter is also placed in a thermal chamber in order to evaluate the impact of thermal cycling. A picture of the developed board and of the experimental setup is reported in Fig. 2. Source measure units (SMUs) are adopted for the initial assessment of the static characteristics of the analyzed power MOSFET.

Referring to Fig. 2, the couple of transistors Q1-Q2 are used to drive the high-side switch. When the output of the TC427 driver is low, Q1 is turned-on and $V_G = 12V - |V_{TH1}|$, where V_{TH1} is the threshold voltage of Q1. In this case, the high-side switch Q3 is turned-off. On the other hand, if the output of the driver is high, Q2 transistor allows to obtain $V_G = V_X$, where V_X is a voltage level arbitrary generated by the microcontroller and the op-amp amplifier. The high-side switch is then turned-on but its on-resistance can be increased by controlling the V_X voltage.

In fig. 3 it is reported the on-resistance of the considered power MOSFET as a function of both the temperature and the driving voltage. The semiconductor device is placed in a thermal chamber by using a proper test fixture and SMUs are adopted to measure the on-resistance. Therefore, no internal power is dissipated in the device during this experiment. Consequently, the case and junction temperatures can be assumed to be the same. While R_{on} is about 20m Ω at room temperature and $|V_{GS}| = 10V$, its value can be increased above 200 m Ω if a gate voltage lower than 3V is applied. Moreover, the reduction of gate voltage is expected to increase the switching losses as well, since the switching time is expected to increase by reducing the gate voltage.

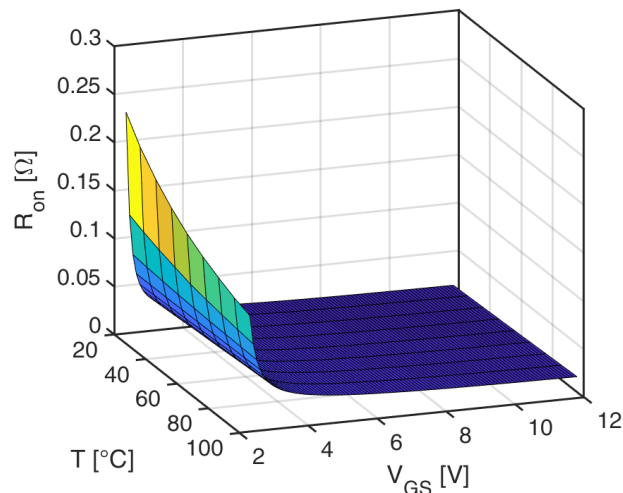


Figure 3. On-resistance as a function of the operating temperature and gate voltage. The semiconductor device is placed in a thermal chamber and SMUs are used to measure the IV curves. R_{on} can be significantly modified by modulating the gate voltage level. The temperature has also a relevant impact on R_{on} . The case and junction temperatures are assumed to be the same for the considered test.

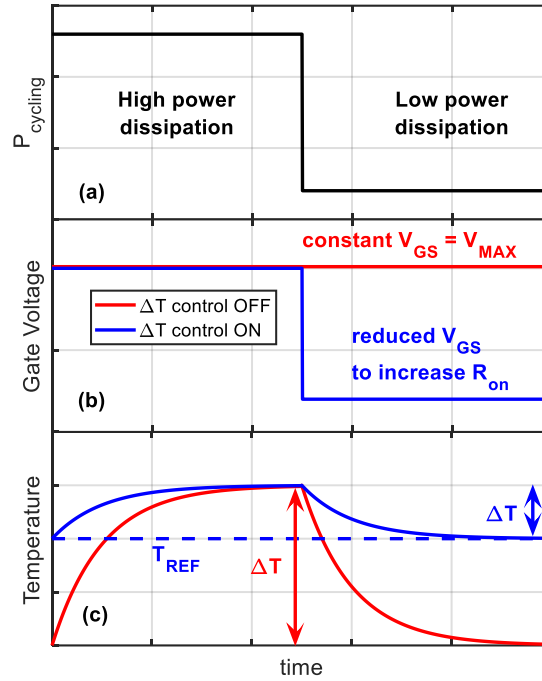


Figure 4. Basic approach for active thermal control: (a) ideal power cycling; (b) gate voltage; (c) temperature cycling. The behavior of the device with (blue) or without (red) the use of active thermal control is considered. In the case of active thermal control enabled, by reducing V_{GS} (hence increasing R_{on}), the self-heating of the component allows reducing the thermal cycling effects.

The active thermal control approach is illustrated in Fig. 4, considering an ideal power cycling effect. A reference temperature T_{REF} is defined, determining the minimum temperature of the device. When the temperature overcomes this value, the gate voltage is increased (to its maximum value) in order to minimize R_{on} and hence the self-heating effects. On the other hand, when the temperature tends to be lower than the reference value, the gate voltage is reduced (to increase R_{on}) allowing to keep the desired temperature. Thanks to this strategy, ΔT swing is reduced with respect to the case of no active thermal control.

III. CONTROL SCHEME

The goal of the control system is to keep a constant temperature in the semiconductor device. To this purpose, the control scheme reported in Fig. 5 has been implemented in the microcontroller. Two loops can be identified: an outer (temperature) loop based on the case temperature feedback and an inner (voltage) loop based on the drain-source voltage feedback. $S_e(s)$ and $S_t(s)$ are the electrical and thermal systems, respectively, of the power MOSFET to be controlled.

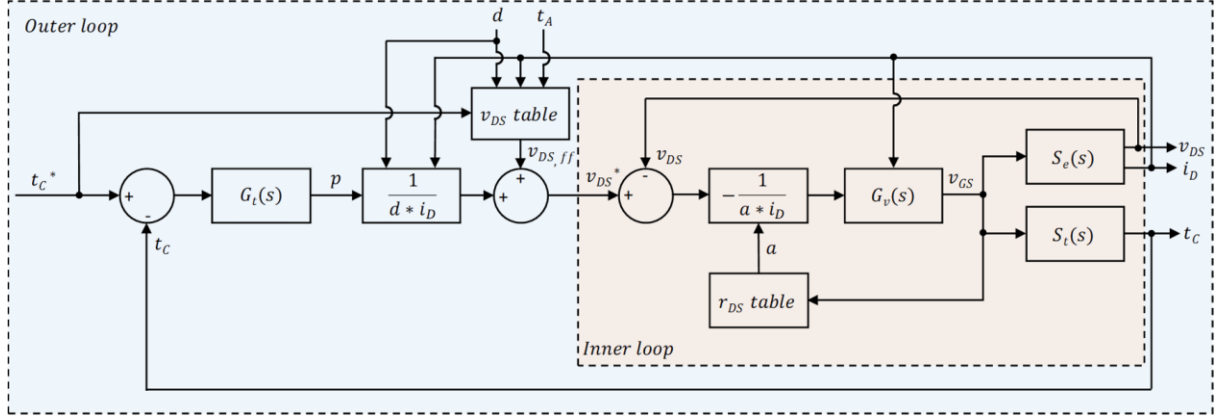


Figure 5: Control scheme implemented to limit power and thermal cycling phenomena.

The relationship between the drain voltage/current and the gate voltage is highly non-linear, as illustrated in Fig. 3. For this reason, a specific procedure to drive the inner loop is introduced. Eq. (1) represents the linearized relationship between v_{ds} and v_{gs} around the operating point q for a given operating temperature and drain current i_D :

$$v_{ds} = \underbrace{-a \cdot v_{gs}}_{r_{ds}} \cdot i_D \Big|_q \quad (1)$$

Where $a = |dr_{DS}/dv_{GS}|$ is a parameter experimentally evaluated, at different temperatures and gate voltages, and implemented as a look-up table in the microcontroller. Therefore, the electrical system $S_e(s)$ can be described as:

$$S_e(s) = \frac{v_{ds}}{v_{gs}} = -a \cdot i_D \Big|_q \quad (2)$$

The variable gain of the electrical system is a limitation for a proper design of the controller. To eliminate this problem, the term $\frac{-1}{a \cdot i_D}$ is added before the controller in order to compensate this dependency around the operating point q . A proportional-integral (PI) controller is then implemented for $G_v(s)$ allowing to reach a crossover frequency equal to 3.18 kHz.

The outer loop allows controlling the case temperature t_c and it is based on another PI controller $G_t(s)$. As a first approximation, we assume that conduction losses are dominant in the power device and that the current ripple can be neglected. In this case the temperature increase (with respect to the ambient temperature) can be expressed as:

$$\Delta T = R_{TH} \cdot P \approx R_{TH} \cdot d \cdot V_{DS} \cdot I_D \quad (3)$$

where R_{TH} is thermal resistance of the device, d is the duty cycle, P is the average power dissipation, I_D and V_{DS} are the average drain current and voltage, respectively, during the conduction phase. The output of the controller is then the required power p , which is multiplied by $(d i_D)^{-1}$ term in order to obtain the reference v_{DS} for the inner voltage loop. $G_t(s)$ is designed as a PI controller having a crossover frequency equal to 0.0239 Hz. In order to improve the performance of the regulator, and to reduce the long response time, a voltage predictor is also implemented in the control system. The signal $v_{DS,ff}$ is generated according to the following equation, which is strictly related to the assumption reported in eq. (3):

$$v_{DS,ff} = (t_c^* - t_A) / (R_{TH} \cdot d \cdot i_D) \quad (4)$$

where t_A and t_c^* are the ambient and the reference temperatures, respectively. The proper operation of the predictor relies on the accurate calibration of thermal resistance. Moreover, the assumptions of the model in eq. (3), further limit the accuracy of the predictor reported in eq. (4). For these reasons, an automatic tuning algorithm to calculate the thermal resistance is implemented within the microcontroller. The thermal resistance is calculated as:

$$R_{TH}(I_D, \Delta T, d) = \frac{\Delta T}{d \cdot V_{DS} \cdot I_D} \quad (5)$$

Ideally the thermal resistance should be independent of the drain current and duty cycle, and lightly affected by the device temperature. In our case, these dependences account for inaccuracies introduced by eq. (3) in the evaluation of the power dissipation (assumed to be due only to conduction losses). Hence, the v_{DS} table reported in Fig. 5, contains a look-up table in which R_{TH} is function of the drain current, the duty cycle and $\Delta T = t_c - t_A$. This table is updated every time a new steady-state condition is reached (only in the case the new operating point is significantly different

from those already stored in the memory). The predictor can then calculate the drain voltage from eq. (4), by interpolating the value of R_{TH} for the actual operating point.

In the analysis of the operation of this kind of active thermal control, some intrinsic limitations must be considered. First, if the output current is small or zero there is no possibility to warm-up the device, therefore t_C^* cannot be achieved. Second, the system cannot be cooled down, hence if a large current is drained from the load, t_C will be higher than t_C^* .

IV. RESULTS AN DISCUSSION

IV.A THERMAL MODEL

As a first step, the open-loop thermal response of the power MOSFET under investigation is analyzed. A typical temperature transient, in the case of multiple output current steps, is reported in Fig. 6, where the case temperature has been directly measured by means of a thermocouple installed on the case of the device. The slow transient reported in Fig. 6 can be correctly modeled as a first order system having a time constant in the order of 100s. In Fig. 7 the junction to case equivalent thermal network of the component under investigation is reported. The network is derived from the thermal transient reported in the datasheet of the component. As expected, the time constants are much lower with respect to the one represented in Fig. 6. This means that only in the case of relatively slow power/thermal cycling, the minimization (or cancellation) of the case temperature cycling will lead to a minimization (or cancellation) of the junction temperature cycling.

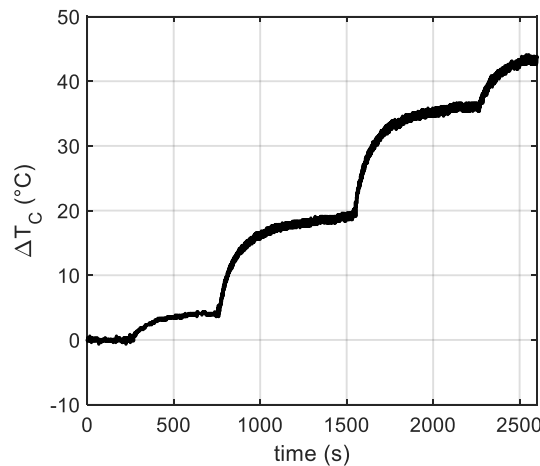


Figure 6: Case temperature (T_C) increases in response to multiple output current steps.

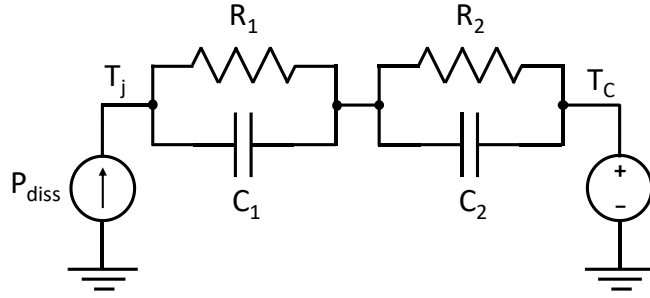


Figure 7: Junction to case thermal equivalent network. Following data are considered: $R_1 = 1.5 \text{ K/W}$, $R_2 = 1 \text{ K/W}$, $C_1 = 2.3 \text{ mJ/K}$, $C_2 = 50 \text{ mJ/K}$.

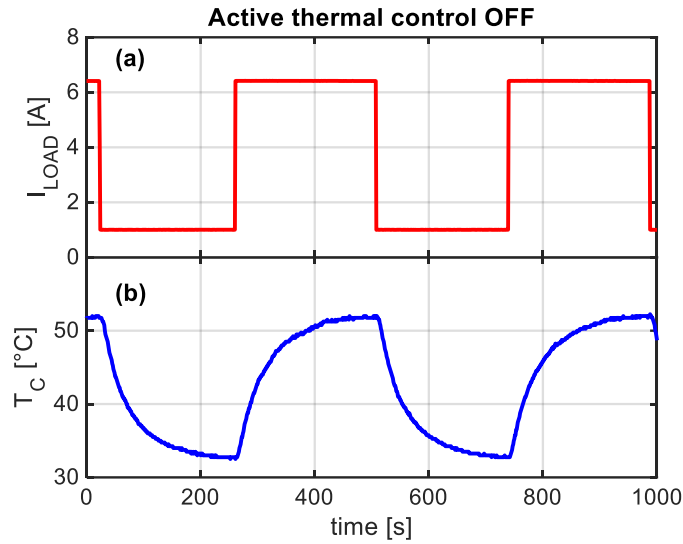


Figure 8: Case temperature (T_c) cycling due to the output current (I_{LOAD}) change. Without using the thermal control, a temperature variation of about 20°C is observed.

IV.B EXPERIMENTAL RESULTS

In this section experimental results aimed at demonstrating the proper operation of the developed system are reported. Fig. 8 shows an example of the power cycling effect in the device operating without the active thermal control. Considering a cycling of the load current from 1A to 6.5A, we observe a case temperature swing of about 20°C . The same load conditions are considered in Fig. 9, with the adoption of the active thermal control. When the output current reaches the minimum level (1A), V_{GS} is reduced, leading to $R_{on} > 200\text{m}\Omega$ and $t_c \approx t_c^* = 50^\circ\text{C}$. It is worth noting that, in order to keep a constant temperature, the on-resistance is increased by a factor of about 10, hence increasing significantly the power dissipation. Moreover, the reduction of V_{GS} leads to a further increase of the switching losses in the device. Overall, the temperature swing is reduced to a few degrees. It is important to highlight that, if the current

is reduced too much, the system will not be able to generate enough internal losses and the target of constant temperature cannot be achieved.

In order to evaluate the response of the proposed system to a thermal cycling, the chamber temperature (and hence the ambient temperature) is ranged between 25°C and 42°C under a constant load current (1A). As reported in Fig. 10, the system is able to keep t_c constant to the reference value (50°C).

The impact of the on-line R_{TH} tuning algorithm is evaluated considering the experimental results reported in Fig. 11. In this case multiple power cycles are considered for the device. During the first cycle ($t < 600s$), R_{TH} is based on an initial guess value. As a consequence, on-resistance oscillates during the transient of I_{LOAD} from 4A to 1A. This leads to an overtemperature of about 2°C with respect to the reference temperature, and to an increase of the transient time. After the first cycle, the implemented on-line algorithm allows tuning the value of R_{TH} . Therefore, the second transient of I_{LOAD} , from 4A to 1A, shows much better performance: on-resistance oscillations are significantly limited and the case temperature is basically kept constant.

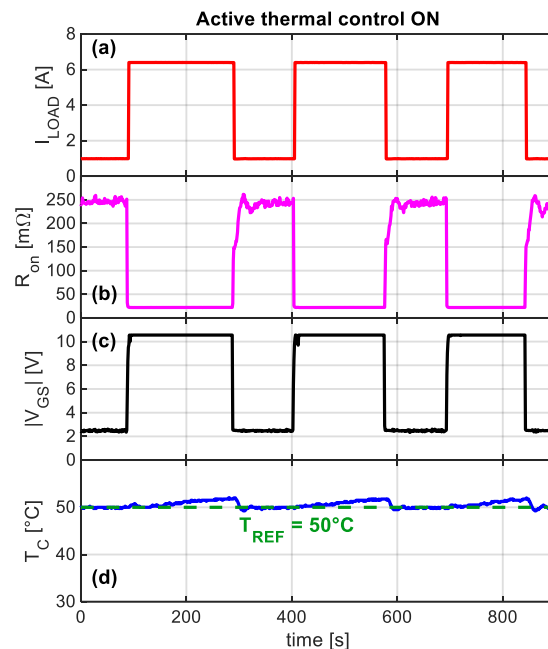


Figure 9: Case temperature (T_C) profile due to the output current (I_{LOAD}) cycling. The active thermal control allows minimizing the temperature swing.

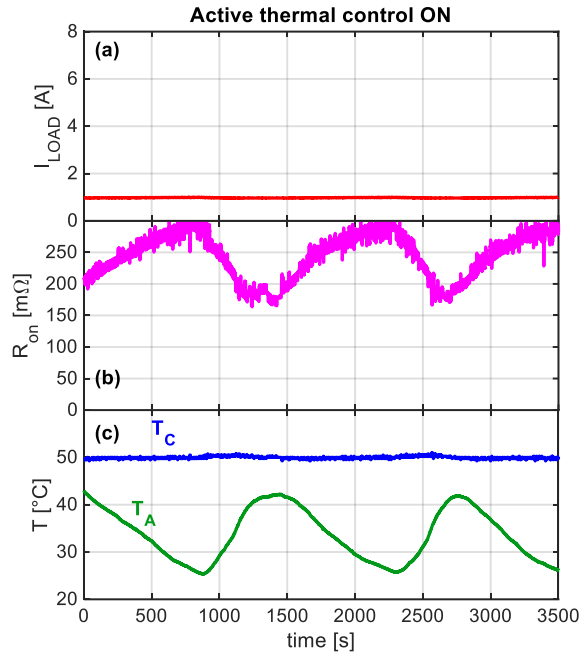


Figure 10: Case temperature (T_C) profile in the case of thermal cycling due to the ambient temperature (T_A) cycling.

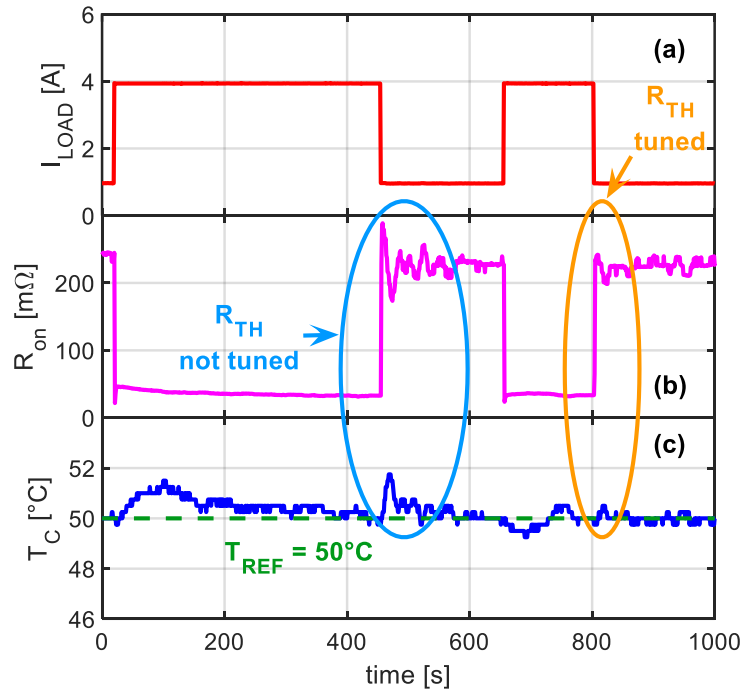


Figure 11: Effect of the feedforward and tuning algorithm of R_{TH} . The calibration of R_{TH} allows improving the transient response of the system.

IV.C SIMULATIONS OF JUNCTION TEMPERATURE CONTROL

In the section IV.B, an active control based on the sensing of the case temperature is considered. Even if this is a suitable solution in the case of relatively slow changes of the junction temperature, we need to keep into account that the load can also exhibit fast changes. In this case, according to the thermal model reported in the section IV.A, the junction thermal transient can significantly deviate from that of the case temperature. This section aims at demonstrating the suitability of the proposed system also in the case of the junction temperature control. To this purpose, simulations have been carried out with PLECS.

Besides the simulation of the active thermal control and of the electrical behavior of the semiconductor device, a proper thermal coupling is considered. In particular, the junction temperature model reported in Fig. 7 is simulated, while conduction losses are considered as the main source of the power dissipation. The control system is essentially the same of that reported in Fig. 5 with the following modifications. (i) The predictor has been omitted, since the considered model corresponds to the one of the conduction losses. (ii) Both the feedback and the reference signals are referred to the junction temperature. (iii) Parameters of the G_t and G_v controllers have been slightly modified in order to increase the bandwidth for both of controllers and hence to obtain a faster transient of the controlled temperature. The simulation results, reported in Fig. 12, are based on a load current cycling with a period of 0.1s and a duty cycle of 5% (Fig. 12a). Considering the behavior of the semiconductor device without any thermal control (Fig. 12b), the junction temperature exhibits a thermal cycling effect, which can be quantified in about 3°C. On the other hand, the case temperature is essentially constant, given the fast cycling of the load current. The activation of the thermal control (Fig. 12c) demonstrates the capability of the system to limit the junction temperature cycling phenomenon.

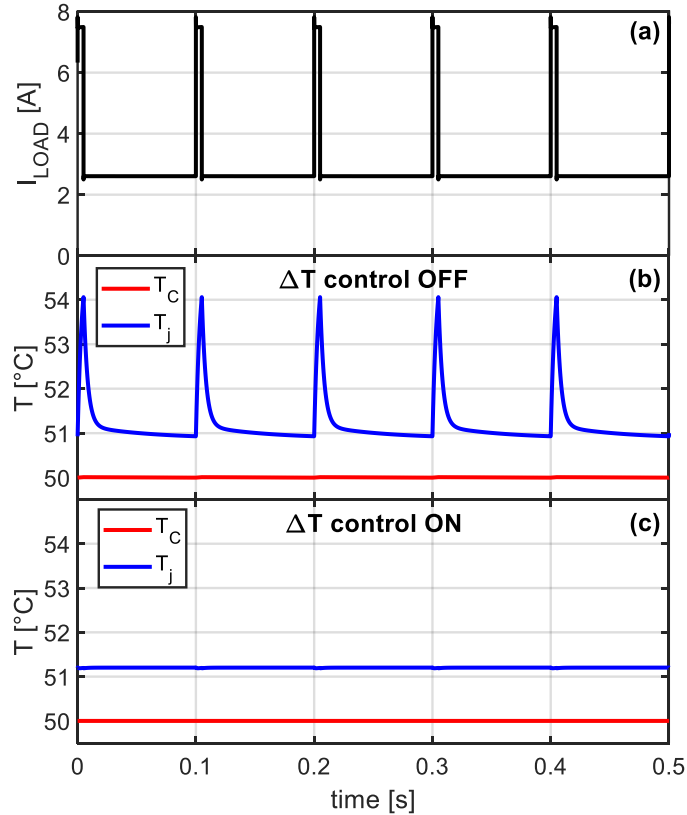


Figure 12. Simulated temperature profiles: (a) fast current cycling; (b) temperature profiles without using the active thermal control; (c) temperature profiles with the active thermal control. In the case of fast load current cycling, the case temperature does not exhibit any temperature cycling effect. The active thermal control allows suppressing the junction temperature cycling phenomenon.

V. CONCLUSIONS

This paper demonstrates the capability to actively control the temperature of a power MOSFET adopted in a buck converter. The developed control system is based on the possibility of modifying the gate driving voltage of the switching device by means of a dedicated circuit. The case temperature, drain-source voltage and output current are measured in order to properly control the temperature in the semiconductor device. Experimental results have demonstrated that the system is able to keep the temperature constant, or to limit the temperature swing, in the case of power and thermal cycling phenomena. The control system is based on a double loop approach: an inner voltage loop allowing to regulate the gate voltage according to the desired drain voltage; and outer temperature loop allowing to regulate the drain voltage in order to minimize the error between the case and the reference temperature. The adoption of a feedforward, based on an on-line thermal resistance tuning algorithm, allows to significantly improve the transient

response of the system. However, when considering fast power cycling phenomena, the junction temperature cycling can significantly differ from that of the case temperature. This is a limitation of the considered sensing system for the device temperature. Nevertheless, it is demonstrated, by means of simulations, that the control system can be equally adopted to control the junction temperature and to limit the associated thermal cycling.

REFERENCES

- [1] H. Wang, M. Liserre, F. Blaabjerg, "Toward Reliable Power Electronics: Challenges, Design Tools, and Opportunities", *IEEE Ind. Electron. Mag.*, vol. 7, no. 2, pp.17-26, 2013.
- [2] M. Held, P. Jacob, G. Nicoletti, P. Scacco, M. H. Poech, "Fast Power Cycling Test for IGBT Modules in Traction Application", *IEEE PEDS*, 1997.
- [3] L. R. GopiReddy, L. M. Tolbert, and B. Ozpineci, "Power Cycle Testing of Power Switches: A Literature Survey," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2465-2473, 2015.
- [4] D. A. Murdock, J. E. Ramos Torres, J. J. Connors, R. D. Lorenz "Active Thermal Control of Power Electronic Modules", *IEEE Trans. Ind. Appl.*, vol. 42, no. 2, pp. 552-558, 2006.
- [5] H. Luo, F. Iannuzzo; K. Ma, F. Blaabjerg, W. Li, X. He, "Active Gate Driving Method for Reliability Improvement of IGBTs via Junction Temperature Swing Reduction", *IEEE PEDG*, 2016.
- [6] P. K. Prasobhu, G. Buticchi, S. Brueske, M. Liserre, "Gate Driver for the Active Thermal Control of a DC/DC GaN-based Converter", *IEEE ECCE*, 2016.
- [7] P. K. Prasobhu, V. Raveendran, G. Buticchi, M. Liserre, "Active thermal control of a DC/DC GaN-based converter", *IEEE APEC*, 2017.
- [8] M. Andresen, K. Ma, G. Buticchi, J. Falck, F. Blaabjerg, M. Liserre, "Junction Temperature Control for More Reliable Power Electronics", *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 765-776, 2018.
- [9] M. Andresen, G. Buticchi, M. Liserre, "Study of reliability-efficiency tradeoff of active thermal control for power electronic systems", *Microelectron. Reliab.*, vol. 58, 119–125, 2016.
- [10] A. Soldati, F. Dossena, G. Pietrini, D. Barater, C. Conconi, F. Iannuzzo, "Thermal stress mitigation by Active Thermal Control: Architectures, models and specific hardware", *IEEE ECCE*, 2017.