Resistive-Capacitive Output Impedance Shaping for Droop-Controlled Converters in DC Microgrids with Reduced Output Capacitance

Guangyuan Liu, *Student Member, IEEE,* Paolo Mattavelli, *Fellow, IEEE,* and Stefano Saggini

***Abstract*—In dc microgrids, droop control is widely employed in power converters interfacing distributed energy resources and common dc bus for automatic power sharing. In order to limit the dc bus voltage variations even during load transient conditions, it is necessary to shape the output impedance of droop-controlled converters to be always lower than the dc resistive value. A commonly used way is to install bulky output capacitance, which not only increases the system cost, size and weight, but also generates higher short-circuit fault currents. In order to avoid large output capacitance, this paper proposes a design approach for droop-controlled converters, including the selection criterion of the output capacitance and the design of the droop coefficient. Herein, the required output capacitance is calculated based on the dc droop coefficient and the voltage control bandwidth. The droop coefficient is designed as a frequency-dependent term instead of a constant value. As a result, resistive-capacitive output impedance can be obtained with a much smaller output capacitance. The proposed design strategy is applied to buck and boost converters and validated by experimental results performed on a buck-based and a boost-based dc microgrid prototype, respectively.**

***Index Terms*—DC microgrids; droop control; design guideline; resistive-capacitive output impedance; reduced output capacitance.**

I. Introduction

DISTRIBUTED Energy Resources (DERs) such as photovoltaic and energy storage systems have seen a vigorous development in recent years. Various DERs can be grouped in the form of dc microgrids together with local customer loads [1], as shown in Fig. 1. Droop control is a decentralized control strategy widely used in dc microgrids, allowing proportional power sharing among parallel DER converters without communication [2], [3]. Based on droop control, the static dc bus voltage varies in an allowable range according to load conditions, that is, the bus voltage stays at a high level with light load while it stays at a low level with heavy load.

The performance of basic droop method has been studied and improved in different respects [4]. By adjusting the droop coefficients and the voltage set points through secondary control, the dc bus voltage can be restored to its nominal value and power sharing can be guaranteed regardless of cable impedance [5], [6]. Coordinated power management among DERs with different characteristics is also investigated. For instance, to balance the State-of-Charge (SoC) of batteries, batteries with higher SoC should deliver more power or absorb less power. [7], [8]. Additionally, in order to supply a reliable bus voltage to customer loads, it is essential to attain tight dc bus voltage regulation when facing load variations, which is the focus of this paper.

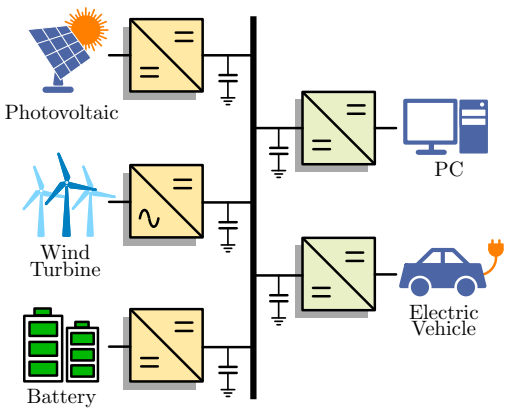

Fig. 1. An example of dc microgrid.

The behavior of bus voltage under load changes can be reflected by the total dc bus impedance. In general, the dc bus impedance is dominated by the output impedance of source converters [9], i.e., droop-controlled DER converters. The output impedance of a droop-controlled DER converter is determined by the droop resistance r_d at low frequency and by the output capacitance C_o at high frequency. At medium frequency, the output impedance depends on many factors like the control performance and may exhibit different shapes. The desired output impedance is purely resistive at low and medium frequency and is capacitive at high frequency, as shown in Fig. 2(a). In this case, when there is a nominal step change in the output current, the output voltage smoothly slides to a new level, holding the first-order low-pass characteristic, as illustrated in Fig. 2(b). However, the typical output impedance may present higher magnitude at medium frequency than r_d [10], [11], as depicted in Fig. 2(a). As a result, a step change of the output current, which contains medium-frequency disturbances, leads to dynamic voltage

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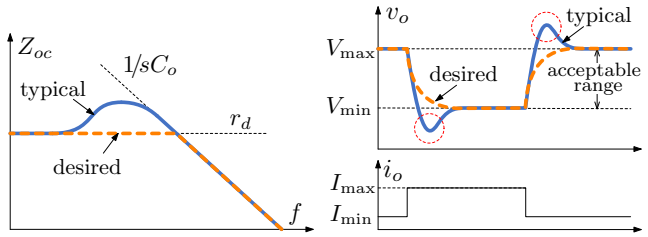


Fig. 2. (a) The output impedance $Z_{oc}(s)$ of a droop-controlled DC/DC DER converter. (b) The associated output voltage variations under nominal load step changes.

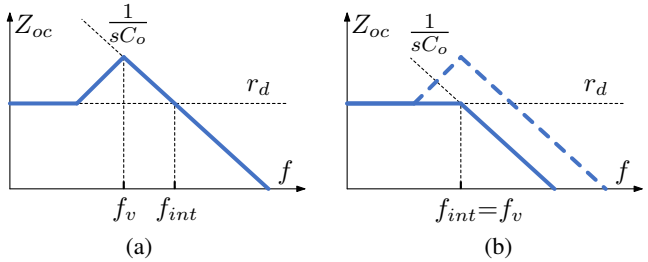


Fig. 3. Simplified diagram of the output impedance of droop-controlled converters to select proper output capacitance. (a) With inadequate output capacitance; (b) With reasonable output capacitance.

variation which is greater than the static voltage change, as highlighted in Fig. 2(b). Obviously, the output voltage exceeds the upper/lower limitations during transient.

To suppress the magnitude of output impedance, a straightforward solution is to choose relatively bulky output capacitors for DER converters [12]. By doing so, even at medium frequency, the output impedance is dominated by the output capacitance, obtaining the desired shape. Consequently, the dc bus voltage is so stiff that the bus voltage sags and surges during load changes are small enough or even negligible. Obviously, large output capacitance increases the system weight and size, which is critical in applications like aircrafts and ships [13]. Moreover, massive output capacitance means a great amount of energy stored on the bus. In case of a dc bus short-circuit fault, a high fault current can be generated, which makes fault isolation difficult [14].

Besides of hardware modifications, the output impedance can be also shaped by means of control solutions. In [15] and [16], an additional output voltage feedback path is added for the voltage control loop according to Mason's gain formula, so that the output impedance can be effectively shaped while preserving the voltage loop bandwidth. Voltage regulator modules, which are mainly buck converters serving as power supplies for microprocessors, are designed to have almost constant output impedance by means of tuning the parameters of voltage regulators [17]–[19]. In addition, the so-called Virtual-Capacitor (VC) control, which is also named as integral droop control or virtual inertia control, is capable of providing virtual output capacitance for converters, thus diminishing the peak of output impedance [20]–[26]. The VC control is basically realized by an output current feedback path through an integral gain. The functions of this approach include mitigating the harmonics in output currents/voltages of inverters [21], [22], enhancing the system damping and stability [23], and smoothing the output power flow of devices like batteries [24]–[26]. Combing the concept of VC control, an admittance-type droop controller is proposed in [27], achieving resistive-capacitive output impedance. However, this controller is developed for specific converters with LC output filters (like buck converters). Also, the design of virtual capacitance and the selection criterion for the physical output capacitance are still missing. Recently, a design guideline for buck-type droop-controlled converters is presented in [28] to accomplish resistive-capacitive output impedance, including the design of output capacitance and droop control parameters.

This paper, as an extension of [28], generalizes the analytical derivation, further simplifies the design of droop impedance to a uniform shape, and performs additional experiments on a boost-based dc microgrid prototype. The objective is to achieve resistive-capacitive output impedance without using large output capacitance. The main contributions can be summarized as:

1) the design methodology for droop controllers is proposed, so that resistive-capacitive output impedance can be obtained on a general DC/DC converter;
2) a simplified version of the proposed design method is introduced, which has a uniform format regardless of converter topologies, easing the procedure of implementation;
3) the selection criterion of the output capacitance of droop-controlled converters is provided.

The remainder of this paper is organized as follows. Section II gives the selection criterion of the output capacitance. Section III analyzes the output impedance of a general droop-controlled DER converter and introduces the design method for droop controllers to attain resistive-capacitive output impedance. Further, the design method is simplified, so that it is independent of converter topologies. In Section IV, the feasibility of proposed design method is validated by experimental results referring to a buck-based and a boost-based dc microgrid prototype.

II. Selection of Output Capacitance

This section provides an initial estimation of the output capacitance, by investigating the effect of the output capacitance on the output impedance.

In order to choose a reasonable output capacitance, the simplified shape of output impedance $Z_{oc}(s)$ is studied. Fig. 3(a) presents the diagram of $Z_{oc}(s)$ with inadequate output capacitance. The structure of $Z_{oc}(s)$ can be roughly divided into three parts. Well below the output voltage control bandwidth f_v, $Z_{oc}(s)$ can be shaped to be r_d by means of control methods [29]. When the frequency approaches the control bandwidth, $Z_{oc}(s)$ becomes closer to the open-loop output impedance, and its magnitude rises gradually until dominated by $1/sC_o$ at high frequency. As can be observed, $Z_{oc}(s)$ is lower than r_d

again when the frequency is over f_{int}, which is the intersection frequency of $1/sC_o$ and r_d:

$$f_{int} = 1/(2\pi \cdot C_o \cdot r_d) \tag{1}$$

To have resistive-capacitive output impedance, the output capacitance should be selected in such a way that f_{int} matches f_v, as illustrated in Fig. 3(b). Thus, the value of the output capacitance C_o can be expressed as:

$$C_o = 1/(2\pi \cdot r_d \cdot f_v) \tag{2}$$

This equation is easy to understand. For a converter with a certain power capacity, a smaller r_d means a narrower voltage tolerance band, which, in turn, requires larger C_o and higher f_v. In practical design, the voltage control bandwidth f_v can be firstly estimated according to system parameters such as the switching frequency and the control delay. Afterwards, the output capacitance C_o can be calculated by (2). It should be noticed that the output capacitance is obtained based on the simplified output impedance and is not highly accurate, so it can be adjusted accordingly in the following design procedures. Nevertheless, it could still facilitate the design process.

III. Design of Droop Controller

After having an initial value for the output capacitance, the power stage of a DER converter is already settled. Then, let us move to the design of the droop controller.

The control scheme of a general droop-controlled DC/DC converter is shown in Fig. 4(a). The droop controller consists of an inductor current loop, an output voltage loop, and a droop loop. It is worth mentioning that the implementation of droop control strategy can be categorized into two types, the voltage-current (*V-I*) droop and the current-voltage (*I-V*) droop [30]–[32]. The *V-I* droop method generates the output voltage reference v_o^* based on the sampled output current i_o and the droop coefficient. The *I-V* droop control calculates the output current reference i_o^* according to the measured output voltage v_o and the droop coefficient. In this paper, only the design methodology for the *V-I* droop approach is analyzed.

In terms of the controller design, in general, based on the required crossover frequencies and stability margins, the current regulator $G_i(s)$ can be designed firstly, followed by the voltage regulator $G_v(s)$ [33]. PI controllers are usually used for $G_i(s)$ and $G_v(s)$ to zero steady-state errors. At the end, the droop loop is closed to set the output voltage reference v_o^*:

$$v_o^* = V_0 - i_o \cdot Z_d(s) \tag{3}$$

where V_0 is the output voltage set point under no load condition and $Z_d(s)$ is the generalized droop impedance. The design method of the droop controller is straightforward. Firstly, on the basis of the small-signal model of the droop-controlled converter, the transfer function of the closed-loop output impedance $Z_{oc}(s)$ is derived, which can be regarded as a function of $Z_d(s)$. Then, by solving the equation $Z_{oc}(s) = r_d$, $Z_d(s)$ can be deduced.

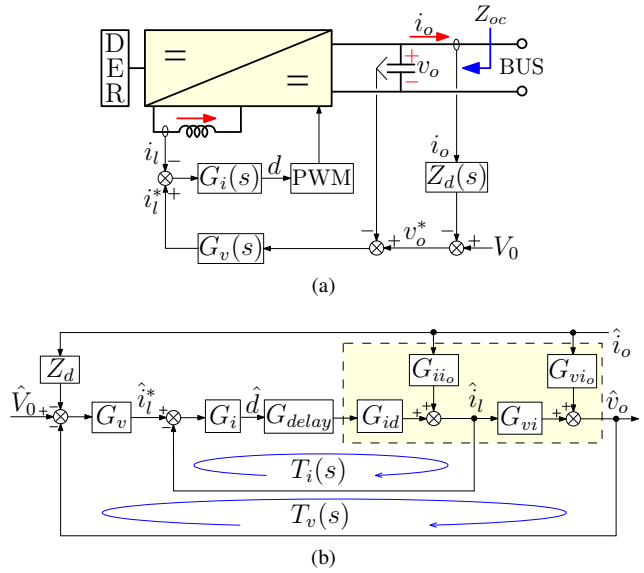


Fig. 4. A general droop-controlled DC/DC converter. (a) The control scheme. (b) The linearized model. The power stage is represented by blocks inside the dashed rectangle.

A. Proposed droop impedance

Under an operation condition, the power stage of the droop-controlled converter can be linearized as:

$$\hat{i}_l = G_{id}(s) \cdot \hat{d} + G_{ii_o}(s) \cdot \hat{i}_o \tag{4}$$

$$\hat{v}_o = G_{vd}(s) \cdot \hat{d} - Z_o(s) \cdot \hat{i}_o \tag{5}$$

where the diacritic mark $\hat{}$ indicates the ac small-signal, $G_{id}(s)$ is the transfer function from $\hat{d}$ to $\hat{i}_l$, $G_{ii_o}(s)$ is the transfer function from $\hat{i}_o$ to $\hat{i}_l$, $G_{vd}(s)$ is the transfer function from $\hat{d}$ to $\hat{v}_o$, and $Z_o(s)$ is the open-loop output impedance. By substituting $\hat{d}$ with $\hat{i}_l$ and $\hat{i}_o$, (5) can be rewritten as:

$$\begin{aligned}\hat{v}_o &= \frac{G_{vd}(s)}{G_{id}(s)} \cdot \hat{i}_l + \left[-Z_o(s) - \frac{G_{vd}(s) \cdot G_{ii_o}(s)}{G_{id}(s)}\right] \cdot \hat{i}_o \\ &= G_{vi}(s) \cdot \hat{i}_l + G_{vi_o}(s) \cdot \hat{i}_o\end{aligned} \tag{6}$$

Finally, the power stage can be represented by (4) and (6). The resulted linearized control block diagram of the droop-controlled converter is displayed in Fig. 4(b).

For the current loop, its open-loop transfer function $T_i(s)$ and its closed-loop transfer function $T_{iCL}(s)$ are given as:

$$T_i(s) = G_i(s) \cdot G_{delay}(s) \cdot G_{id}(s) \tag{7}$$

$$T_{iCL}(s) = T_i(s)/[1 + T_i(s)] \tag{8}$$

For the voltage loop, its open-loop transfer function $T_v(s)$ and its closed-loop transfer function $T_{vCL}(s)$ are given as:

$$T_v(s) = G_v(s) \cdot T_{iCL}(s) \cdot G_{vi}(s) \tag{9}$$

$$T_{vCL}(s) = T_v(s)/[1 + T_v(s)] \tag{10}$$

With the current loop, the voltage loop, and the droop loop

closed, the output impedance $Z_{oc}(s)$ can be deduced as:

$$Z_{oc}(s) = -\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{V}_0=0} = \frac{Z_d(s)T_v(s) - G_{ii_o}(s)G_{vi}(s)/[1+T_i(s)] - G_{vi_o}(s)}{1+T_v(s)} \tag{11}$$

Since the open-loop output impedance $Z_o(s)$ can be expressed as:

$$Z_o(s) = -\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{d}=0} = -G_{vi_o}(s) - G_{ii_o}(s)G_{vi}(s) \tag{12}$$

(11) can be rewritten as:

$$\begin{aligned} Z_{oc}(s) &= Z_d(s)T_{vCL}(s) + \frac{Z_o(s) + G_{ii_o}(s)G_{vi}(s)T_{iCL}(s)}{1+T_v(s)} \\ &= Z_o(s)[1 - T_{vCL}(s)] + \left[Z_d(s) + \frac{G_{ii_o}(s)}{G_v(s)}\right] T_{vCL}(s) \end{aligned} \tag{13}$$

It can be inferred from (13) that, in order to achieve resistive output impedance at low and medium frequency [i.e., $Z_{oc}(s) = r_d$], control parameters should be carefully designed. For simplicity, this paper performs on the droop impedance $Z_d(s)$, but one can also select the voltage regulator $G_v(s)$ as the tuning target, as was done in [17]. Herein, the droop impedance $Z_d(s)$ should be designed as:

$$Z_d(s) = r_d/T_{vCL}(s) - Z_o(s)/T_v(s) - G_{ii_o}(s)/G_v(s) \tag{14}$$

where r_d is the droop resistance. Within the voltage control bandwidth ω_v (i.e., $\omega < \omega_v$), $T_{vCL}(j\omega)$ and $T_{iCL}(j\omega)$ can be approximately considered as a unit gain. Hence, combining (9) and (12), (14) can be simplified as:

$$\begin{aligned} Z_d(j\omega) &\approx r_d + \frac{G_{vi_o}(j\omega) + G_{ii_o}(j\omega)G_{vi}(j\omega)}{G_v(j\omega)G_{vi}(j\omega)} - \frac{G_{ii_o}(j\omega)}{G_v(j\omega)} \\ &= r_d + \frac{G_{vi_o}(j\omega)}{G_v(j\omega)G_{vi}(j\omega)}, \quad \omega < \omega_v \end{aligned} \tag{15}$$

It can be found that $Z_d(s)$ is related not only to r_d but also to $G_{vi_o}(s)$, $G_{vi}(s)$ and the voltage regulator $G_v(s)$. Therefore, $Z_d(s)$ depends on the topology of DER converters due to the presence of $G_{vi_o}(s)$ and $G_{vi}(s)$.

To numerically verify the feasibility of the proposed design method, two representative examples of DC/DC DER converters are studied herein: a buck-type converter and a boost-type converter. It should be noted that this design method is generic and it can be also applied to other converters like buck-boost, Cuk, Sepic, and Zeta.

1) Buck-type converter: The control scheme of a buck-type droop-controlled DER converter is shown in Fig. 5. Under an operation point, the linearized equations of the buck converter are given as follows:

$$sL \cdot \hat{i}_l = V_{in} \cdot \hat{d} - \hat{v}_o \tag{16}$$

$$sC_o \cdot \hat{v}_o = \hat{i}_l - \hat{i}_o \tag{17}$$

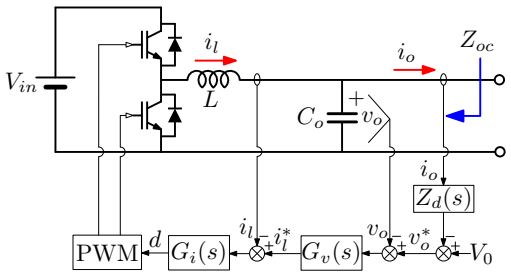


Fig. 5. Control scheme of an example buck-type droop-controlled converter.

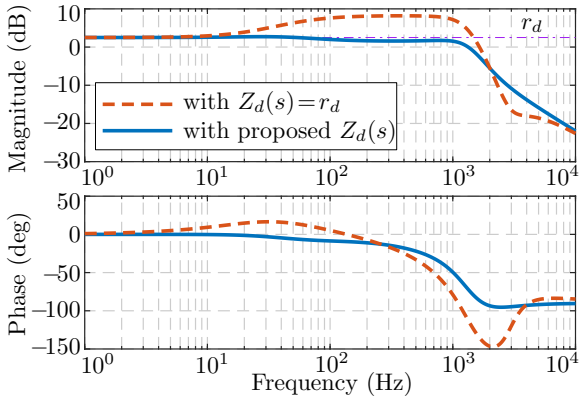


Fig. 6. Bode diagram of the output impedance $Z_{oc}(s)$ of the buck-type droop-controlled converter shown in Fig. 5, using different $Z_d(s)$. With the proposed $Z_d(s)$ [see (20)], resistive-capacitive output impedance is achieved.

Then, by combining (16) and (17), the state variables $\hat{i}_l$ and $\hat{v}_o$ can be expressed as:

$$\hat{i}_l = \underbrace{\frac{sC_oV_{in}}{s^2LC_o+1}}_{G_{id}(s)} \cdot \hat{d} + \underbrace{\frac{1}{s^2LC_o+1}}_{G_{ii_o}(s)} \cdot \hat{i}_o \tag{18}$$

$$\hat{v}_o = \underbrace{1/sC_o}_{G_{vi}(s)} \cdot \hat{i}_l + \underbrace{(-1/sC_o)}_{G_{vi_o}(s)} \cdot \hat{i}_o \tag{19}$$

The entire block diagram of the linearized droop-controlled buck converter is displayed in Fig. 4(b).

The system parameters used in this example are: $V_{in} = 380\,\text{V}$, $V_o = 200\,\text{V}$, $P_n = 3\,\text{kW}$, $L = 1.6\,\text{mH}$, $C_o = 200\,\mu\text{F}$, $f_s = 12.5\,\text{kHz}$, $r_d = 1.33\,\text{V/A}$. As discussed in Section II, the output capacitance C_o can be selected based on the voltage control bandwidth f_v and the droop resistance r_d. For example, f_v herein is expected to be $600\,\text{Hz}$, which is $1/20$ of the switch frequency f_s, so C_o is calculated as $200\,\mu\text{F}$ according to (2). Based on these parameters, the current loop $T_i(s)$ [see (7)] and the voltage loop $T_v(s)$ [see (9)] are designed to have zero crossings at $1.2\,\text{kHz}$ and $600\,\text{Hz}$, respectively. It is worth mentioning that the voltage control bandwidth is exactly designed at its expected value. As for the droop loop, the design of $Z_d(s)$ follows (15), resulting in:

$$Z_d(s) = r_d - 1/G_v(s) \tag{20}$$

The bode diagram of $Z_{oc}(s)$ is plotted in Fig. 6, with $Z_d(s)$ designed in the conventional way [i.e., $Z_d(s) = r_d$] and in the proposed way [see (20)]. As can be seen, in both cases, $Z_{oc}(s)$

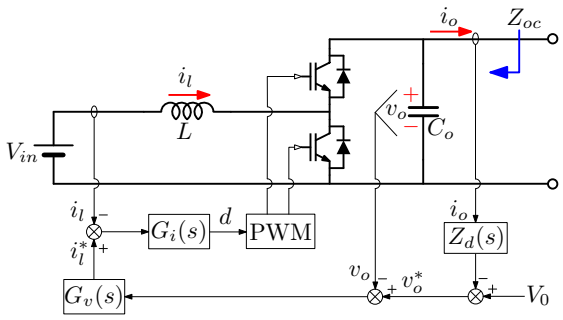


Fig. 7. Control scheme of an example boost-type droop-controlled converter.

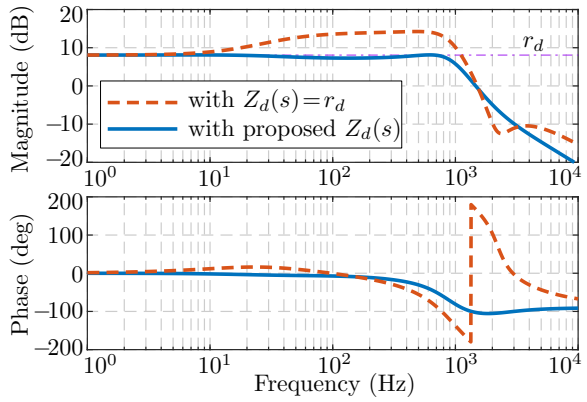


Fig. 8. Bode diagram of the output impedance $Z_{oc}(s)$ of the boost-type droop-controlled converter shown in Fig. 7, using different $Z_d(s)$. With the proposed $Z_d(s)$ [see (25)], resistive-capacitive output impedance is achieved.

is equal to r_d at low frequency. However, with $Z_d(s)$ being r_d, $Z_{oc}(s)$ shows high magnitude, which is about 1.9 times of r_d, in medium frequency range. This $Z_{oc}(s)$ actually suggests an output voltage overshoot/undershoot of 90 %. To restrict the voltage fluctuation to a lower level, for instance, 10 %, the output capacitance should be approximately increased to 9 times of the original value, that is, 1.8 mF. Whereas, with the proposed $Z_d(s)$ implemented, $Z_{oc}(s)$ is nearly constant until 1 kHz. Above this frequency, $Z_{oc}(s)$ is dominated by the output capacitance. As a result, the design target is achieved.

2) Boost-type converter: The Buck converter is a specific case because its small-signal model is not influenced by the operation point. Differently, for many other converters, their small-signal models change with the operation point. From this perspective, this paper aims to verify the feasibility of the proposed design method for this kind of converter by providing an example of boost converters. The control scheme of an boost-type converter is shown in Fig. 7. Under an operation point, the circuit of the boost converter can be linearized as follows:

$$sL \cdot \hat{i}_l = -(1-D_p) \cdot \hat{v}_o + V_{op} \cdot \hat{d} \tag{21}$$

$$sC_o \cdot \hat{v}_o = (1-D_p) \cdot \hat{i}_l - I_{lp} \cdot \hat{d} - \hat{i}_o \tag{22}$$

where V_{op} is the static output voltage, I_{lp} is the static inductor current, and D_p is the static duty cycle. In steady state, the input voltage V_{in} equals $(1-D_p)\cdot V_{op}$, and the static output current I_{op} equals $(1-D_p)\cdot I_{lp}$. Then, by combining (21) and

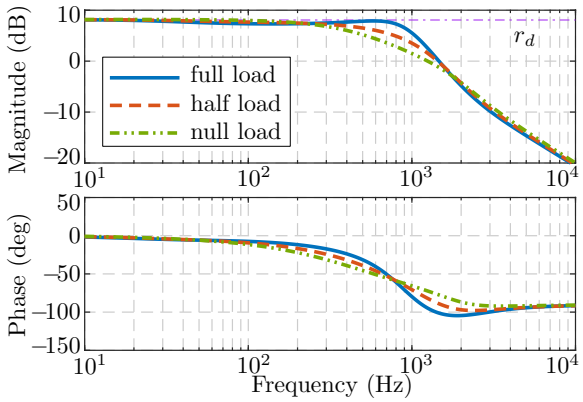


Fig. 9. Bode diagram of the output impedance $Z_{oc}(s)$ of the boost-type droop-controlled converter shown in Fig. 7, under different operation points.

(22), the state variables $\hat{i}_l$ and $\hat{v}_o$ can be expressed as:

$$\hat{i}_l = \underbrace{\frac{sC_oV_{op}+I_{op}}{s^2LC_o+(1-D_p)^2}}_{G_{id}(s)} \cdot \hat{d} + \underbrace{\frac{1-D_p}{s^2LC_o+(1-D_p)^2}}_{G_{ii_o}(s)} \cdot \hat{i}_o \tag{23}$$

$$\hat{v}_o = \underbrace{\frac{-sLI_{lp}+V_{in}}{sC_oV_{op}+I_{op}}}_{G_{vi}(s)} \cdot \hat{i}_l + \underbrace{\frac{-V_{op}}{sC_oV_{op}+I_{op}}}_{G_{vi_o}(s)} \cdot \hat{i}_o \tag{24}$$

For the complete block diagram of the linearized droop-controlled boost converter, one can refer to Fig. 4(b).

The system parameters are listed as follows: $V_{in} = 200\,\text{V}$, $V_o = 380\,\text{V}$, $P_n = 3\,\text{kW}$, $L = 1.6\,\text{mH}$, $C_o = 160\,\mu\text{F}$, $f_s = 12.5\,\text{kHz}$, $r_d = 2.53\,\text{V/A}$. Since the boost converter is a non-minimum phase system with a right-half-plane zero (at 2.1 kHz) in the voltage control loop, the voltage loop bandwidth f_v is expected to be 400 Hz, which is about 1/5 of the frequency of the right-half-plane zero. Then, C_o is calculated as 160 µF according to (2). Based on these parameters, the current loop $T_i(s)$ [see (7)] and the voltage loop $T_v(s)$ [see (9)] are designed to have zero crossings at 1.2 kHz and 400 Hz, respectively. Afterwards, following (15) and neglecting the right-half-plane pole introduced by $G_{vi}(s)$ since it is not causal, the droop impedance $Z_d(s)$ of the boost-type DER converter can be expressed as:

$$Z_d(s) = r_d - 1/[(1-D_p)G_v(s)] \tag{25}$$

The bode diagram of $Z_{oc}(s)$ is plotted in Fig. 8, with $Z_d(s)$ designed in the conventional way [i.e., $Z_d(s) = r_d$] and in the proposed way [see (25)]. When $Z_d(s)$ is designed as pure resistance, $Z_{oc}(s)$ is greater than r_d from 10 Hz to 1 kHz. Remarkably, with the proposed $Z_d(s)$, $Z_{oc}(s)$ is almost resistive at low frequency. Hence, the proposed design method is compatible with non-minimum phase systems. satisfying the design requirement. Furthermore, Fig. 9 shows the output impedance under different operation points while keeping control parameters the same. It can be seen that resistive-capacitive output impedance is ensured in a wide range of operating conditions.

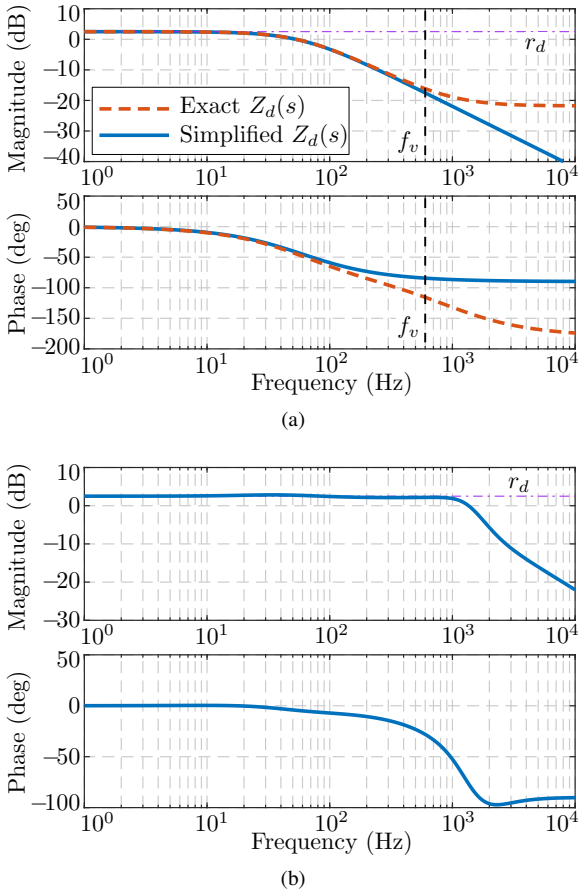


Fig. 10. (a) The droop impedance $Z_d(s)$, for the buck-type converter shown in Fig. 5, based on the exact model in (20) and its simplified version in (26). (b) The output impedance $Z_{oc}(s)$ with the simplified $Z_d(s)$.

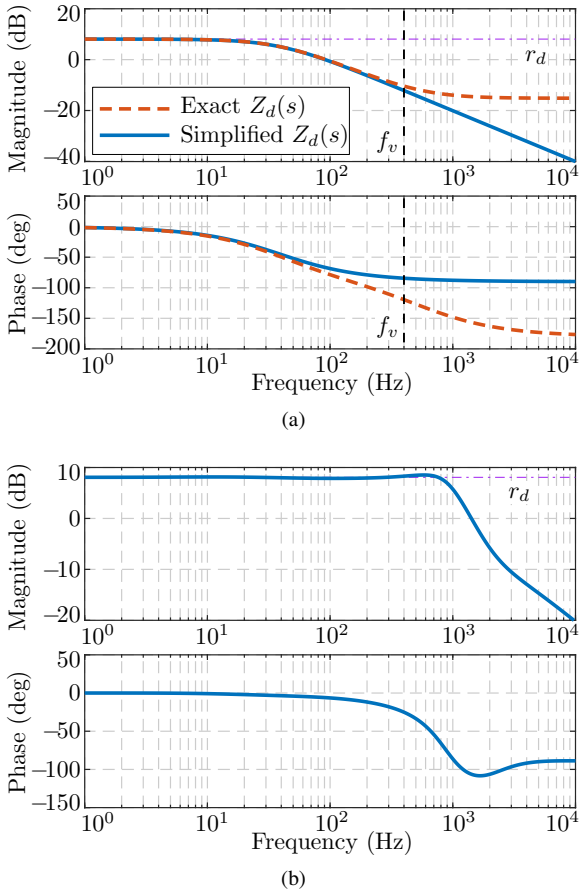


Fig. 11. (a) The droop impedance $Z_d(s)$, for the boost-type converter shown in Fig. 7, based on the exact model in (25) and its simplified version in (26). (b) The output impedance $Z_{oc}(s)$ with the simplified $Z_d(s)$.

B. Simplification of the proposed droop impedance

When the proposed droop impedance $Z_d(s)$ shown in (15) is applied to a general droop-controlled converter, the transfer function $G_{vi_o}(s)$ and $G_{vi}(s)$ should be calculated for every kind of the converter topology. Although the calculation may not bring too much difficulty, a concise droop impedance $Z_d(s)$, which is independent of converter topologies, is still more appreciated.

Fig. 10(a) depicts bode diagram of the droop impedance $Z_d(s)$ implemented in the example of buck-type converter. In fact, as the droop controller is only responsible for the output impedance up to the voltage control bandwidth f_v, the design of $Z_d(s)$ can be simplified as long as it is precise until f_v. Therefore, in this example, by performing curve fitting, the simplified version of the proposed $Z_d(s)$ is introduced as follows:

$$Z_d(s) = \frac{r_d}{s/\omega_{\text{zv}} + 1} \tag{26}$$

where ω_{zv} is the zero of the voltage regulator $G_v(s)$. Fig. 10(a) also plots the bode diagram of the simplified $Z_d(s)$. Clearly, within the voltage loop bandwidth, the difference between the exact $Z_d(s)$ and its simplified version is minor. With the simplified $Z_d(s)$ adopted, Fig. 10(b) shows the bode diagram of the corresponding output impedance $Z_{oc}(s)$. As expected, $Z_{oc}(s)$ is nearly resistive in the low and medium frequency range, presenting a satisfactory shape. Similarly, for the boost-type converter, the proposed exact $Z_d(s)$ and its simplified version, which is also expressed by (26), are shown in Fig. 11(a). It can be seen that the exact $Z_d(s)$ and its simplified form are close in shape below f_v. Consequently, the corresponding output impedance $Z_{oc}(s)$ presented in Fig. 11(b) is resistive at low frequency, verifying the effectiveness of the simplified design method.

Most importantly, the simplified $Z_d(s)$ is uniform for both buck-type and boost-type converters and is only related to the control parameters, so it can be easily extended to DER converters with different topologies. Also, Fig. 10(a) and Fig. 11(a) clearly indicate the low-pass characteristic of the proposed droop impedance. In such a case, low-pass filters, which are exploited in the droop loop to reject high-frequency noises [34], can be omitted.

In summary, for a droop-controlled DER converter shown in Fig. 4(a), in order to obtain a resistive output impedance, the design should follow the steps below.

- In the beginning, taking account of control parameters like the switching frequency and the control delay (including computation time and PWM delay), a reasonable voltage control bandwidth f_v can be set;

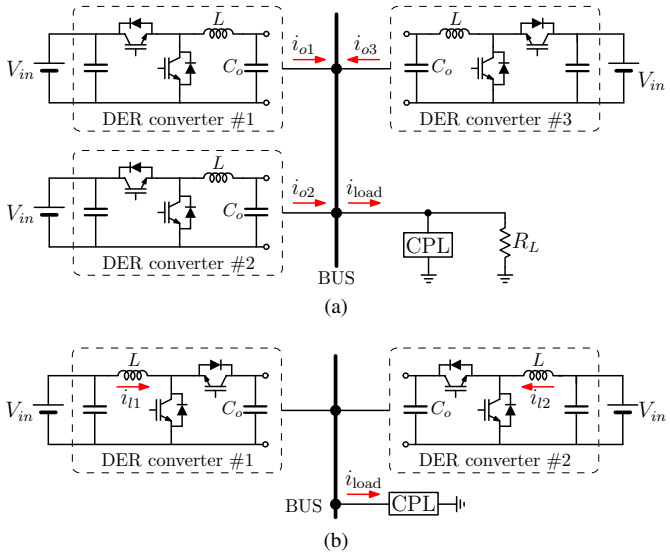


Fig. 12. Schematic diagrams of two laboratory-scale dc microgrid prototypes. (a) Buck-based dc microgrid; (b) Boost-based dc microgrid.

- At the converter circuit level, based on the predicted f_v, the output capacitance C_o is selected according to (2);
- Then, at the controller level, the current regulator $G_i(s)$ and the voltage regulator $G_v(s)$ can be designed on the basis of the current loop gain $T_i(s)$ and the voltage loop gain $T_v(s)$, respectively. The current control bandwidth can be set at, for example, $1/10$ of the switching frequency, and the voltage control bandwidth can be set at the expected value f_v;
- The droop loop is installed on top of inner current and voltage loops. The proposed droop impedance $Z_d(s)$ can be derived from (15) and further simplified by performing curve fitting.

In the end, it is necessary to perform an overall check of the resulted closed-loop output impedance by analytical expressions or by simulation results.

So far, only constant droop resistance is discussed. If nonlinear droop resistance is implemented [10], the design process should be repeated for different load conditions, and control parameters including the voltage regulator and the droop impedance should be adaptively tuned online.

IV. Experimental Results

To experimentally verify the proposed design method, two laboratory-scale dc microgrid prototypes are set up, as shown in Fig. 12. One prototype includes three buck-type droop-controlled DER converters, and the other one includes two boost-type droop-controlled DER converters. Constant power load, which is a typical scenario of microgrids, is also considered and is emulated by dc electronic load. The system parameters are reported in Table I.

A. Buck-based dc microgrid

The proposed design approach is firstly applied to the buck-based dc microgrid prototype shown in Fig. 12(a). The control

TABLE I
DER Converter Parameters

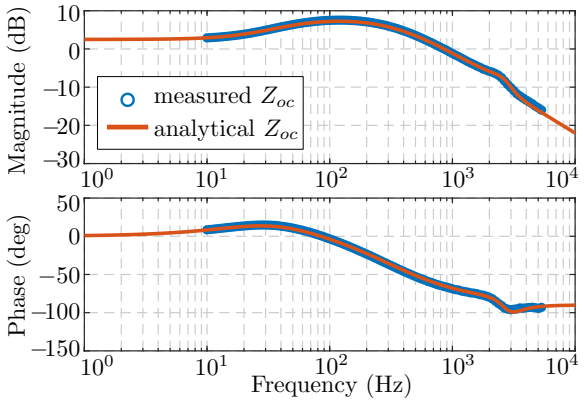
Parameter	Symbol	Buck	Boost
Input voltage	V_{in}	380 V	200 V
Nominal bus voltage	V_o	200 V	380 V
Nominal Power	P_n	3 kW	3 kW
Inductance	L	1.6 mH	1.0 mH
Output capacitance	C_o	200 µF	130 µF
Switching frequency	f_s	12.5 kHz	20 kHz
Droop resistance	r_d	1.33 V/A	2.53 V/A

structure of every buck-type DER converter is shown in Fig. 5. Specifically, in the experimental implementation, the inductor current, which equals the output current in steady state, is taken as the feedback signal in the droop loop. In terms of the design of droop controller, considering that the switching frequency f_s is 12.5 kHz and the control delay is one switching cycle, the voltage control bandwidth is estimated at 600 Hz, that is, around $1/20$ of f_s. Following the design procedure, the output capacitance is selected as 200 µF according to (2). The current loop has a crossover frequency of 1.2 kHz and a phase margin of 55°. The voltage loop has a crossover frequency of 600 Hz and a phase margin of 60°. The current regulator $G_i(s)$ is $0.03+5.7/s$ and the voltage regulator $G_v(s)$ is $0.7+267/s$.

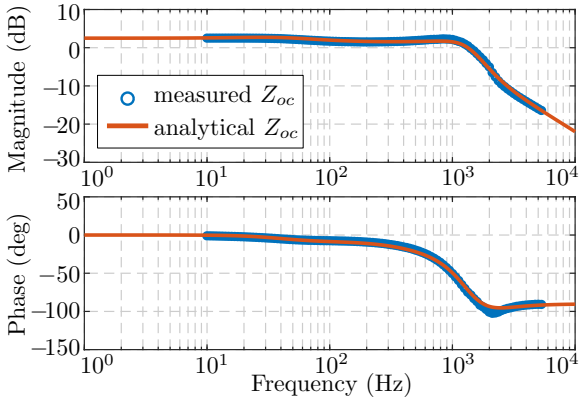
1) Output impedance measurement: The actual output impedance of one DER converter is experimentally measured by frequency sweep. Under an steady-state operation point, another converter injects sinusoidal small-signal perturbations into the dc microgrid. Meanwhile, the converter under measurement collects its output current and output voltage signals. Finally, the output impedance of the converter can be calculated by performing the fast Fourier transform on the collected data. The output impedance measurement can be automatically completed by the Software Frequency Response Analyzer (SFRA) functions embedded in the Texas Instruments digital controllers [35].

Fig. 13 shows the measured output impedance with different design principles. The actual output impedance is marked by a series of circles from 10 Hz to 5 kHz, and the analytical output impedance is represented by the solid line. As can be seen, the measured output impedances almost follow the analytical ones up to 5 kHz, proving the accuracy of the modeled output impedances.

Moreover, with $Z_d(s)$ being r_d, the peak magnitude of $Z_{oc}(s)$ is about 1.9 times of r_d, as shown in Fig. 13(a). Herein, only $Z_d(s)$ is designed in the classical way, while the output capacitance and the voltage loop are appropriately designed by following the proposed design procedure. In principle, the magnitude of $Z_{oc}(s)$ can be even higher if system parameters are not properly chosen, for example, smaller output capacitance is used. On the other hand, if $Z_d(s)$ is designed in the form of (15), the magnitude of the resulted $Z_{oc}(s)$ is successfully suppressed, presenting resistive characteristics at low and medium frequency, as displayed in Fig. 13(b). Similarly, with the simplified $Z_d(s)$ [see (26)], resistive-capacitive output impedance is also obtained, as presented in



(a)



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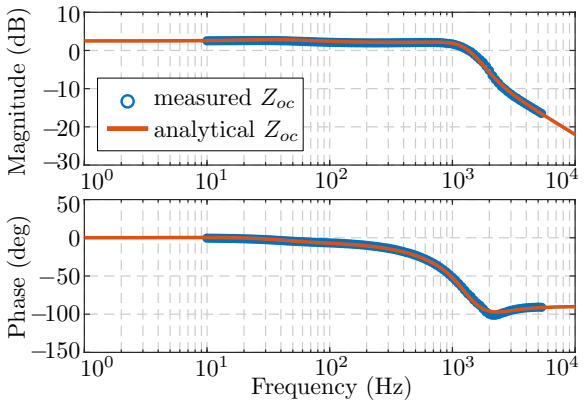
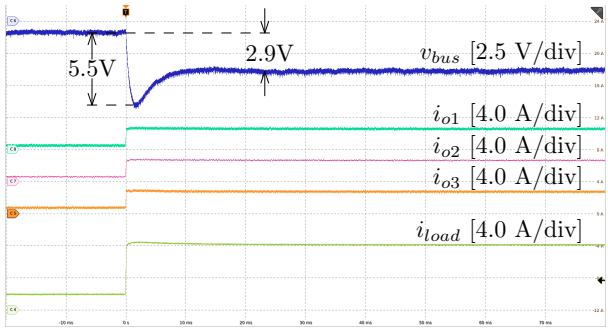


(c)

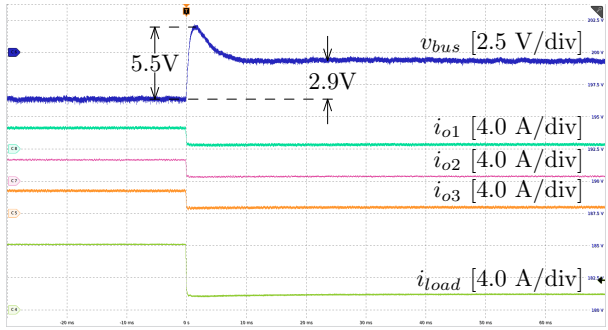
Fig. 13. The measured and theoretical output impedance $Z_{oc}(s)$ of one buck-type droop-controlled converter, with the droop controller designed in different ways. (a) $Z_d(s)$ is r_d; (b) The proposed $Z_d(s)$ is implemented in the form of (15); (c) The simplified $Z_d(s)$ is employed in the form of (26).

Fig. 13(c).

2) Voltage variations under load changes: In this test, several experiments are carried out to evaluate the dc bus voltage variations under load changes. In every experiment, all converters are designed in the same way, either all in the traditional way or all in the proposed way. Fig. 14 shows the dynamic experimental results under a constant power load step, with all droop controllers designed in the conventional way (i.e., $Z_d(s) = r_d$). As can be seen from Fig 14(a), when



(a)



(b)

Fig. 14. Experimental results under a step change of constant power load in buck-based microgrid, with $Z_d(s)$ being r_d. (a) 1.2 kW load step up. (b) 1.2 kW load step down. In both cases, the dc bus voltage shows large undershoot and overshoot during transient. v_{bus} offset: 200 V. Time: 10 ms/div.

the load steps up, the bus voltage presents a significant sag of 5.5 V during transient. When the load steps down, similar result can be found in Fig 14(b). Compared to the 2.9 V steady-state voltage changes, which are caused by the droop function, the dynamic voltage variations are almost doubled.

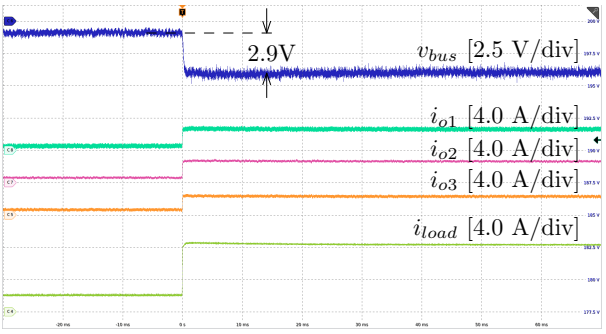
Fig. 15 depicts the experimental results under the same load changes, with all droop controllers designed in the proposed way [i.e., $Z_d(s)$ follows (15)]. Remarkably, the bus voltage undershoot and overshoot are successfully eliminated, verifying the feasibility of the proposed design method.

Fig. 16 displays the experimental results under the same load changes, with all droop controllers designed in the simplified way [i.e., $Z_d(s)$ follows (26)]. In this experiment, DER converter #3 is purposely designed with a different voltage loop bandwidth, that is, 300 Hz. According to the proposed design procedure, its output capacitance is increased to 400 µF. Notably, the bus voltage is still tightly regulated. Thus, the simplified design method is effective for converters of different bandwidths.

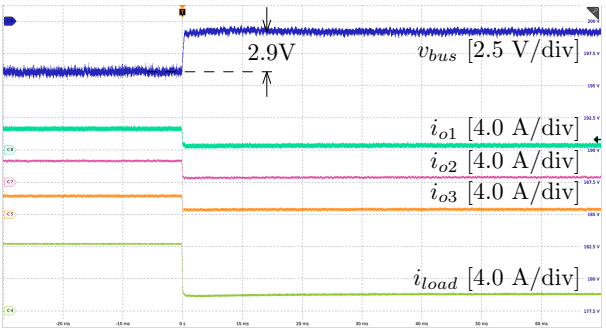
Indeed, as the total dc bus impedance is the parallel result of source output impedance and load input impedance, the decrease of the output impedance of DER converters results in the reduction of the bus impedance. Eventually, the dynamic response of dc bus voltage is enhanced [9].

B. Boost-based dc microgrid

The proposed design approach is also applied to the boost-based dc microgrid prototype shown in Fig. 12(b). The control

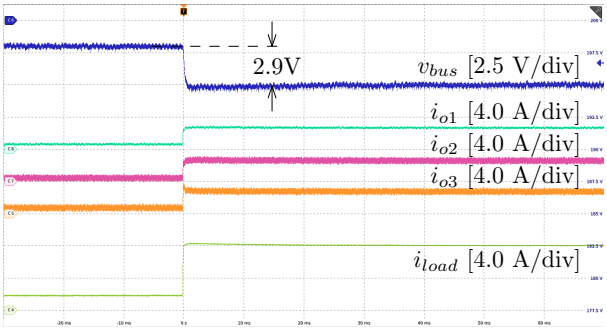


(a)

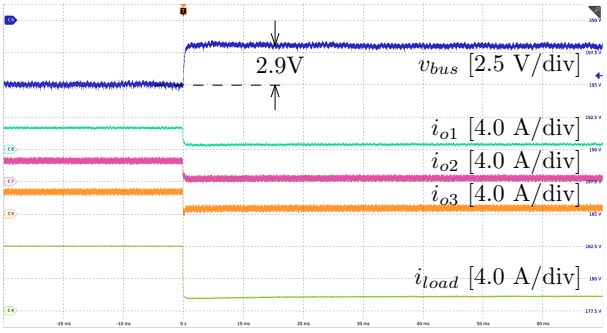


(b)

Fig. 15. Experimental results under a step change of constant power load in buck-based microgrid, with the proposed $Z_d(s)$ expressed as (15). (a) 1.2 kW load step up. (b) 1.2 kW load step down. In both cases, the dc bus voltage is tightly regulated inside the droop range. v_{bus} offset: 200 V. Time: 10 ms/div.



(a)



(b)

Fig. 16. Experimental results under a step change of constant power load in buck-based microgrid, with the simplified $Z_d(s)$ expressed as (26). (a) 1.2 kW load step up. (b) 1.2 kW load step down. In both cases, the dc bus voltage is tightly regulated inside the droop range. v_{bus} offset: 200 V. Time: 10 ms/div.

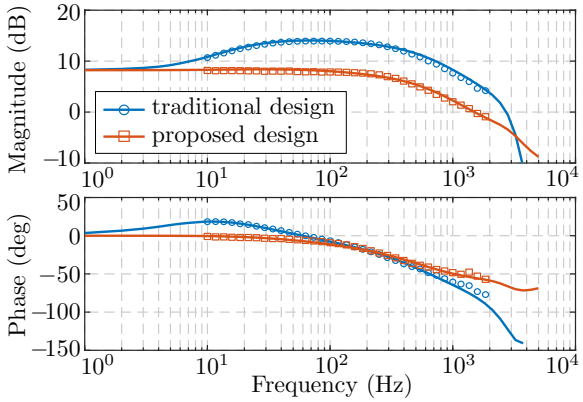


Fig. 17. The measurement results (circles and squares) and theoretical (solid lines) output impedance $Z_{oc}(s)$ of one boost-type droop-controlled converter, with the traditional [$Z_d(s) = r_d$] and proposed [see (26)] design.

structure of every boost-type DER converter is shown in Fig. 7. Since the switching frequency f_s is 20 kHz and the control delay is one switching cycle, the voltage control bandwidth is predicted at 550 Hz in this test. Subsequently, the output capacitance is chosen as 130 µF according to (2). The current loop has a crossover frequency of 2 kHz and a phase margin of 50°. The voltage loop has a crossover frequency of 550 Hz and a phase margin of 65°. The current regulator $G_i(s)$ is $0.034 + 32/s$ and the voltage regulator $G_v(s)$ is $0.75 + 77/s$.

The output impedance $Z_{oc}(s)$ of one boost-type droop-controlled converter is experimentally measured. Fig. 17 shows the measurement results with different design strategies. With the traditional design [$Z_d(s) = r_d$], $Z_{oc}(s)$ shows higher magnitude than r_d at medium frequency. Whereas, with the proposed design [see (26)], $Z_{oc}(s)$ is shaped to be resistive at low and medium frequency and to be capacitive at high frequency, meeting the design target.

Furthermore, the dynamic experiments under load changes are carried out, as shown in Fig. 18. With the traditional design, the dc bus voltage shows an unexpected dip of 6.5 V during transient, while the voltage change in steady state is only 4 V. Differently, with the proposed design, the dc bus voltage moves to the new level without any undershoot, demonstrating the advantage of the proposed design method.

C. Discussions

The overall impedance of a DER converter is the sum of the converter output impedance and the transmission cable impedance. Cable impedance can potentially induce additional voltage drop when facing load variations, and it can deteriorate power sharing performance, though these phenomena are not observed in the tests presented above. To tackle these issues, a smaller dc droop resistance should be considered in the design process, or secondary control should be installed to adjust the control parameters. Besides, droop control inherently leads to the deviation of dc bus voltage from its nominal value according to load conditions. It is necessary to add secondary control if dc bus voltage restoration is required.

Another point worth remarking is that the dc bus voltage shows sudden changes in case of load steps in experimental

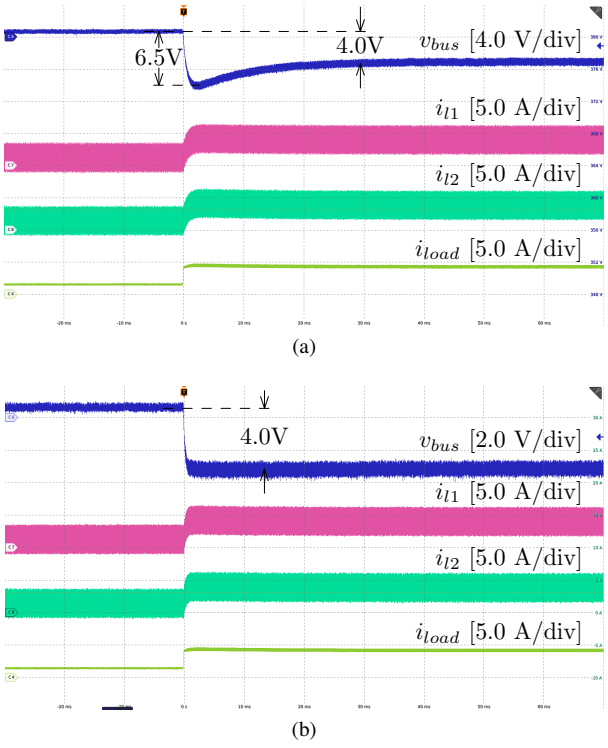


Fig. 18. Experimental results under a step-up change of constant power load in boost-based microgrid. (a) $Z_d(s)$ is r_d; (b) $Z_d(s)$ is designed in the proposed form as (26). v_{bus} offset: 380 V. Time: 10 ms/div.

results, challenging the system stability. To slow down the rate of change of dc bus voltage, the possible ways include *i)* increasing the physical output capacitance, *ii)* pushing the voltage loop bandwidth. Apart from these two ways, other control methods, for example, shaping the output impedance as a large virtual capacitance, can hardly further smooth the output voltage. This is because these control methods function as expected only if the frequency is well below the voltage loop bandwidth. In this case, although the output impedance can be reduced at low frequency, a magnitude peak that is determined by the output capacitance inevitably appears around the control bandwidth, causing dramatic voltage change when load steps.

V. Conclusion

This paper presents the design approach for droop-controlled DC/DC DER converters in dc microgrids towards resistive-capacitive output impedance, including the selection criterion of output capacitance and the design of droop impedance. In particular, the output capacitance is chosen according to the voltage control bandwidth and the dc droop resistance. The droop impedance is designed in the form of proposed transfer functions instead of a pure resistance. Following this design methodology, resistive-capacitive output impedance can be obtained on a general DC/DC converter. Consequently, the bus voltage is strictly limited in the acceptable range in case of load changes, without using bulky output capacitance. The effectiveness of the proposed design method has been verified by experimental results performed on a buck-based and a boost-based laboratory-scale dc microgrid prototype, respectively.

References

[1] H. Kakigano, Y. Miura, and T. Ise, "Low-voltage bipolar-type dc microgrid for super high quality distribution," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 3066–3075, Dec 2010.

[2] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna, and M. Castilla, "Hierarchical control of droop-controlled ac and dc microgrids–a general approach toward standardization," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 158–172, Jan 2011.

[3] L. Meng, Q. Shafiee, G. F. Trecate, H. Karimi, D. Fulwani, X. Lu, and J. M. Guerrero, "Review on control of dc microgrids and multiple microgrid clusters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 3, pp. 928–948, Sep. 2017.

[4] T. Dragicevic, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC microgrids-part I: A review of control strategies and stabilization techniques," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4876–4891, July 2016.

[5] S. Anand, B. G. Fernandes, and J. Guerrero, "Distributed control to ensure proportional load sharing and improve voltage regulation in low-voltage dc microgrids," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1900–1913, April 2013.

[6] X. Lu, J. M. Guerrero, K. Sun, and J. C. Vasquez, "An improved droop control method for dc microgrids based on low bandwidth communication with dc bus voltage restoration and enhanced current sharing accuracy," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1800–1812, April 2014.

[7] X. Lu, K. Sun, J. M. Guerrero, J. C. Vasquez, and L. Huang, "State-of-charge balance using adaptive droop control for distributed energy storage systems in dc microgrid applications," *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2804–2815, June 2014.

[8] Q. Wu, R. Guan, X. Sun, Y. Wang, and X. Li, "Soc balancing strategy for multiple energy storage units with different capacities in islanded microgrids based on droop control," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 1932–1941, Dec 2018.

[9] H. Abdollahi, S. Arrua, T. Roinila, and E. Santi, "A novel dc power distribution system stabilization method based on adaptive resonance-enhanced voltage controller," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5653–5662, July 2019.

[10] F. Chen, R. Burgos, D. Boroyevich, J. C. Vasquez, and J. M. Guerrero, "Investigation of nonlinear droop control in dc power distribution systems: Load sharing, voltage regulation, efficiency, and stability," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9404–9421, Oct 2019.

[11] G. Liu, T. Caldognetto, P. Mattavelli, and P. Magnone, "Suppression of second-order harmonic current for droop-controlled distributed energy resource converters in dc microgrids," *IEEE Trans. Ind. Electron.*, vol. 67, no. 1, pp. 358–368, Jan 2020.

[12] Y. Liu, T. C. Green, J. Wu, K. Rouzbehi, A. Raza, and D. Xu, "A new droop coefficient design method for accurate power-sharing in vsc-mtdc systems," *IEEE Access*, vol. 7, pp. 47 605–47 614, 2019.

[13] B. Sarlioglu and C. T. Morris, "More electric aircraft: Review, challenges, and opportunities for commercial transport aircraft," *IEEE Trans. Transport. Electrific.*, vol. 1, no. 1, pp. 54–64, June 2015.

[14] D. Salomonsson, L. Soder, and A. Sannino, "Protection of low-voltage dc microgrids," *IEEE Trans. Power Del.*, vol. 24, no. 3, pp. 1045–1053, July 2009.

[15] A. Aldhaheri and A. H. Etemadi, "Stabilization and performance preservation of dc-dc cascaded systems by diminishing output impedance magnitude," *IEEE Trans. Ind. Appl.*, vol. 54, no. 2, pp. 1481–1489, March 2018.

[16] L. Cao, K. H. Loo, and Y. M. Lai, "Systematic derivation of a family of output-impedance shaping methods for power converters-a case study using fuel cell-battery-powered single-phase inverter system," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5854–5869, Oct 2015.

[17] K. Yao, M. Xu, Y. Meng, and F. C. Lee, "Design considerations for vrm transient response based on the output impedance," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1270–1277, Nov 2003.

[18] M. Lee, D. Chen, K. Huang, C. Liu, and B. Tai, "Modeling and design for a novel adaptive voltage positioning (avp) scheme for multiphase vrms," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1733–1742, July 2008.

[19] A. Borrell, M. Castilla, J. Miret, J. Matas, and L. G. de Vicua, "Control design for multiphase synchronous buck converters based on exact constant resistive output impedance," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4920–4929, Nov 2013.

[20] E. Unamuno and J. A. Barrena, "Design and small-signal stability analysis of a virtual-capacitor control for dc microgrids," in *European Conference on Power Electronics and Applications (ECCE Europe)*, Sept 2017, pp. P.1–P.10.
[21] X. Wang, Y. W. Li, F. Blaabjerg, and P. C. Loh, "Virtual-impedance-based control for voltage-source and current-source converters," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7019–7037, Dec 2015.
[22] Q. C. Zhong and Y. Zeng, "Control of inverters via a virtual capacitor to achieve capacitive output impedance," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5568–5578, Oct 2014.
[23] L. Guo, S. Zhang, X. Li, Y. W. Li, C. Wang, and Y. Feng, "Stability analysis and damping enhancement based on frequency-dependent virtual impedance for dc microgrids," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 338–350, March 2017.
[24] P. Lin, P. Wang, J. Xiao, J. Wang, C. Jin, and Y. Tang, "An integral droop for transient power allocation and output impedance shaping of hybrid energy storage system in dc microgrid," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6262–6277, July 2018.
[25] Y. Gu, W. Li, and X. He, "Frequency-coordinating virtual impedance for autonomous power management of dc microgrid," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 2328–2337, April 2015.
[26] Q. Xu, X. Hu, P. Wang, J. Xiao, P. Tu, C. Wen, and M. Y. Lee, "A decentralized dynamic power sharing strategy for hybrid energy storage system in autonomous dc microgrid," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5930–5941, July 2017.
[27] Z. Jin, L. Meng, R. Han, J. M. Guerrero, and J. C. Vasquez, "Admittance-type rc-mode droop control to introduce virtual inertia in dc microgrids," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct 2017, pp. 4107–4112.
[28] G. Liu, P. Mattavelli, and S. Saggini, "Design of droop controllers for converters in dc microgrids towards reducing bus capacitance," in *European Conference on Power Electronics and Applications (ECCE Europe)*, Sep. 2018, pp. P.1–P.9.
[29] K. Yao, Y. Ren, and F. C. Lee, "Critical bandwidth for the load transient response of voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1454–1461, Nov 2004.
[30] F. Gao, S. Bozhko, A. Costabeber, C. Patel, P. Wheeler, C. I. Hill, and G. Asher, "Comparative stability analysis of droop control approaches in voltage-source-converter-based dc microgrids," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2395–2415, March 2017.
[31] Z. Jin, L. Meng, and J. M. Guerrero, "Comparative admittance-based analysis for different droop control approaches in dc microgrids," in *IEEE Second International Conference on DC Microgrids (ICDCM)*, June 2017, pp. 515–522.
[32] H. Wang, M. Han, R. Han, J. M. Guerrero, and J. C. Vasquez, "A decentralized current-sharing controller endows fast transient response to parallel dcdc converters," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 4362–4372, May 2018.
[33] G. Liu, T. Caldognetto, P. Mattavelli, and P. Magnone, "Power-based droop control in dc microgrids enabling seamless disconnection from upstream grids," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2039–2051, March 2019.
[34] S. D'Arco and J. A. Suul, "Equivalence of virtual synchronous machines and frequency-droops for converter-based microgrids," *IEEE Trans. Smart Grid*, vol. 5, no. 1, pp. 394–395, Jan 2014.
[35] Texas Instruments software frequency response analyzer (sfra) library user's guide. [Online]. Available: http://www.ti.com/tool/SFRA

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