Power-Based Droop Control in DC Microgrids Enabling Seamless Disconnection from Upstream Grids

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***Abstract*—This paper proposes a local power-based droop controller for distributed energy resource converters in dc microgrids that are connected to upstream grids by grid-interface converters. During normal operation, the grid-interface converter imposes the microgrid bus voltage and the proposed controller allows power flow regulation at distributed energy resource converters output. On the other hand, during abnormal operation of the grid-interface converter (e.g., due to faults in the upstream grid), the proposed controller allows bus voltage regulation by droop control. Notably, the controller can autonomously convert from power flow control to droop control, without any need of bus voltage variations detection schemes or communication with other microgrid components, which enables seamless transitions between these two modes of operation. Considering distributed energy resource converters employing the power-based droop control, the operation modes of a single converter and of the whole microgrid are defined and investigated herein. The controller design is also introduced. Furthermore, the power sharing performance of this control approach is analyzed and compared with that of classical droop control. The experimental results from a laboratory-scale dc microgrid prototype are reported to show the final performances of the proposed power-based droop control.**

***Index Terms*—DC microgrids, droop control, power flow control, islanding, seamless transition, power sharing.**

I. Introduction

In recent years, distributed energy resources (DERs) such as distributed generators (DGs) based on renewable sources (e.g., photovoltaic, wind) and energy storage systems (ESSs) (e.g., batteries, super capacitors) have seen a widespread diffusion. An effective way to integrate different types of DERs and loads in distribution grids is to aggregate them in the form of microgrids [1]–[3], which potentially improves energy management, conversion efficiency and grid reliability. DERs are typically interfaced with the distribution system by means of power electronic converters (PECs). Due to the intrinsic dc nature of the most of DERs and loads (e.g., electric vehicles, consumer electronics, LED lighting, etc.), there is a strong interest towards the development of dc microgrids [4]. Compared to their ac counterparts, dc microgrids can potentially achieve higher energy conversion efficiency and lower system costs, mainly by minimizing the number of dc/ac and ac/dc conversion stages. Moreover, dc operation removes any reactive power or frequency control issue, making the control easier and more effective [5]. Generally, a grid-interface (GI) converter is utilized to link a dc microgrid with an upstream grid (e.g., the utility, high-level dc microgrids). An example of generic layout of a dc microgrid is represented in Fig. 1.

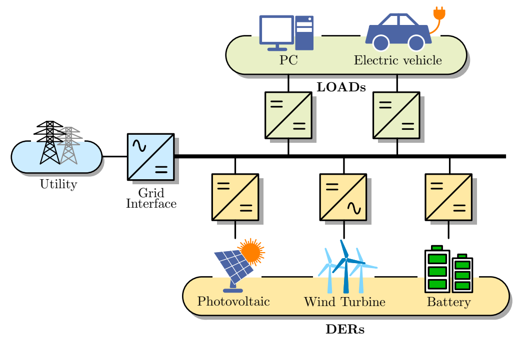

Fig. 1. An example of dc microgrid layout.

The primary control targets in dc microgrids are the distribution bus voltage and the power exchanged by DERs. Many control approaches have been investigated from this perspective. Among them, droop control is a common decentralized solution to implement primary level control, where the bus voltage is employed to convey the loading condition of the microgrid. With the droop control method, the droop curves of the microgrid elements are properly designed to obtain prioritized power management strategies [6], [7]. However, classical droop method often employs fixed droop curves, making power contributions from DERs determined by loads power absorption. This behavior limits the power control flexibility at the output of DERs and makes it difficult to apply power management strategies in which DERs act as power sources [8], [9]. To address this problem, an additional power flow controller, operating in parallel with the droop controller, can be used [10]. In such a case, DERs converters regulate their output power by means of the power flow controller when the bus voltage is imposed by the GI converter, and they regulate the bus voltage by means of the droop controller

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when the GI converter fails (e.g., due to faults or output power limitations). Unfortunately, switching between these two controllers usually requires time-critical communications between microgrid components or the implementation of bus voltage variations detection techniques, which increase system complexity and decrease reliability [11]. Similar issues, dealt with, for example, in [12]–[14], can be found in ac microgrids.

Power sharing is a key issue in dc microgrids due to the parallel operation of many DERs. Although all the parallel converters share a common dc bus, the bus voltages at specific points of connection are not exactly the same because of the interconnection cable impedances. Indeed, load distribution within dc microgrids applying conventional droop control, with constant droop characteristics, is significantly affected by cable impedances [15]. For converters employing the voltage-current (*V-I*) type droop method, since the droop coefficients can be approximately regarded as virtual output impedances [16], load distribution depends on the ratio between droop coefficients and cable impedances. With particular cable impedances, higher droop coefficients ensure better power sharing but result in wider bus voltage ranges. To cope with this trade-off, a nonlinear droop control method is presented in [17]. Under an equal voltage range, the droop coefficient is increased with the increase of the load power, attaining a more proportional power sharing under heavy loading conditions. In [18], low-bandwidth communication (LBC) is used to restore the consequent voltage derivations. Hence, relatively larger droop coefficients can be selected with less concerns on bus voltage constrains. In [19], a small ac signal whose frequency is related to the bus voltage is injected onto the dc bus. Based on this frequency, which is uniform within the microgrid, the load can be distributed proportionally regardless of cable impedances. Active compensation of mismatch currents is another way to guarantee proportional power sharing. By considering the difference between the average output current and the actual converters output currents, a correction term can be added into the droop function through LBC, either to shift droop curves [15], [20], [21] or to adjust droop coefficients [22], [23]. Alternatively, for DERs converters equipped with power flow controllers, the load can also be allocated in a proportional manner through LBC [24].

Aiming at achieving power flow control and enhancing system reliability, this paper proposes a local power-based droop controller for DERs converters by unifying the power flow controller and the droop controller. During normal operation, DERs track the given power references and the GI converter imposes the bus voltage, while, during abnormal operation of the GI converter, DERs ensure bus voltage regulation with droop control. The advantages of the proposed controller include *i)* regulation of DERs active power when the GI converter is operating normally, accurately accomplishing specific power sharing configurations through LBC, regardless of cable impedances and loading conditions, *ii)* smooth transitions from power flow control to droop control in the event of the GI converter inability in maintaining the bus voltage (e.g., due to power limitation or faults in the upstream grid), without using bus voltage variations detection schemes or communications with other microgrid elements.

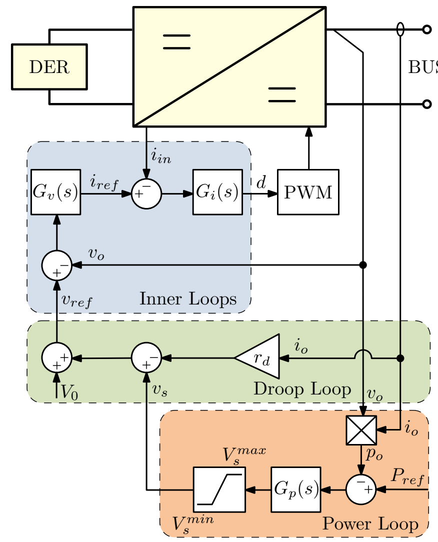

Fig. 2. Scheme of the proposed control method.

The remaining part of the paper is organized as follows. The control scheme of the proposed control method is presented in Sec. II. Then, the operation modes of a single DERs converter considered individually and those of the whole microgrid are analyzed in Sec. III. Sec. IV discusses the controller design. The power sharing performance of the proposed control method is discussed and also compared with that of traditional droop control in Sec. V. Finally, Sec. VI reports the experimental results relevant to the steady-state and transient behaviors of the proposed control method, showing its feasibility and effectiveness.

II. Control Scheme

The power-based droop controller, which is designed for DERs converters, is a combination of a droop controller and a power flow controller [25]. Fig. 2 shows the scheme of this control approach, which mainly consists of three parts: inner voltage and current loops, droop loop and power loop.

1) Inner voltage and current loops: the inner voltage and current loops are the bases of the control structure. The inner voltage regulator $G_v(s)$ generates the current reference i_{ref} by regulating the difference between the voltage reference v_{ref} and the output voltage v_o. The current regulator $G_i(s)$ takes i_{ref} and the inner current i_{in} to produce the duty cycle d.

2) Droop loop: the voltage-current (*V-I*) droop control is adopted here. The voltage reference is calculated as:

$$v_{ref} = (V_0 + v_s) - r_d \cdot i_o \tag{1}$$

where V_0 is the voltage set point under no load condition, r_d is the droop coefficient, v_s is the voltage offset determined by the power loop and i_o is the output current. In traditional droop control, v_s should be zero. In our solution, it is utilized to shift the droop curve upwards or downwards. It is worth mentioning that a voltage-power (*V-P*) droop can be implemented as well [26].

3) Power loop: outside the droop loop, an external bounded power loop is added to track a given power reference P_{ref}

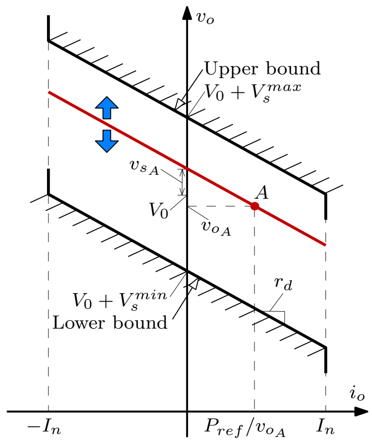

Fig. 3. Operation principle of a DER converter in power regulation mode.

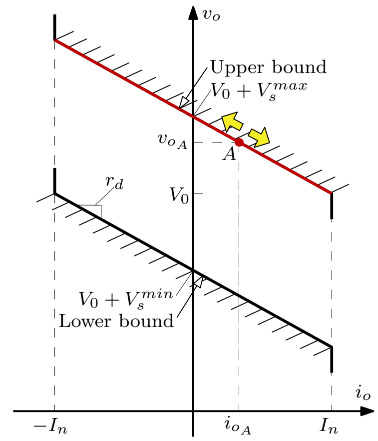

Fig. 4. Operation principle of a DER converter in bus regulation mode.

which can be defined by a microgrid supervisor using non-critical communications. $G_p(s)$ is employed to regulate to zero the difference between the power reference P_{ref} and the output power p_o. The offset v_s is generated by $G_p(s)$ to shift the droop curve, enabling, in this way, power flow regulation:

$$v_s = (P_{ref} - p_o) \cdot G_p(s) \tag{2}$$

It should be noted that the upper and lower saturation levels of v_s, namely, V_s^{max} and V_s^{min}, play a fundamental role in the controller. These two levels should be large enough to allow DERs to reach their nominal power. On the other hand, once the regulator v_s is saturated, the proposed controller turns into a classical droop controller.

III. Operation modes

This section firstly describes the operation modes of a single DER converter. Then, the concept is extended to the microgrid level.

A. Operation modes of a single DER converter

From the standpoint of each individual DER converter, the operation modes can be classified into *power regulation mode* and *bus regulation mode*.

1) Power regulation mode: in power regulation mode, the DER converter exchanges the desired power P_{ref} with the microgrid, while other converters regulate the bus voltage. For example, Fig. 3 shows the operation principle of a DER converter in power regulation mode. Let us assume that the bus voltage is regulated at v_{o_A}, with v_{o_A} not necessarily equal to V_0. To achieve power flow control, the offset v_{s_A}, which is produced by the power regulator $G_p(s)$, is added to V_0. Then, the droop curve of the controller is shifted upwards by v_{s_A}, forcing the converter to operate at point A and to have an output current i_{o_A} equal to P_{ref}/v_{o_A}. Correspondingly, if the bus voltage stands at V_0, v_s is equal to $r_d \cdot P_{ref}/V_0$.

2) Bus regulation mode: in bus regulation mode, the DER converter contributes in ensuring bus voltage regulation. In this case, its output power p_o depends on load power demand and it is not equal, in general, to its given power reference P_{ref}. If p_o is larger than P_{ref}, the power regulator $G_p(s)$ saturates v_s at its lower level V_s^{min} and the droop curve leans against its lower bound. Conversely, if p_o is smaller than P_{ref}, v_s reaches its higher level V_s^{max} and the droop curve leans against its upper bound, as depicted in Fig. 4. The operation point of the DER converter stays on the lower or upper bound in a way that depends on the specific loading conditions. The resulting behavior at the converters output terminals is similar to that obtained with conventional droop control.

3) Transition mechanism: seamless transition from power regulation mode to bus regulation mode is an important feature of the proposed controller. This process actually consists in the transition of $G_p(s)$ from unsaturated state to saturated state. The following example is considered here to explain the principle of this operation. A DER converter switches from power regulation mode to bus regulation mode when the GI converter stops the transfer of power from the upstream grid to the microgrid. This process can be divided into three stages, as presented in Fig. 5 and discussed in the following.

- Stage 1: assume the DER converter operating at a generic original operation point $A(V_0, i_{o_A})$, where i_{o_A} equals P_{ref}/V_0. After losing the support from the GI converter, the lost power contribution from the GI naturally redistributes to the droop controlled DER converter, which guarantees, in this way, the instantaneous power balance. Due to the control law (1) the bus voltage decreases and the operation point of the DER converter slides from A to B along the droop curve. As the outer power loop is usually designed to have a slower response than the droop loop, the effect of power loop, that is, the change of v_s, can be neglected in this stage. According to the control scheme, the following equation can be derived:

$$\Delta v_{o_1} = -r_d \cdot (i_{o_B} - i_{o_A}) + \Delta v_{s_1} \approx -r_d \cdot (i_{o_B} - \frac{P_{ref}}{V_0}) \tag{3}$$

where Δ refers to variations of variables, the subscript 1 indicates the change occurring in the first stage and i_{o_B} is the output current at operation point B. Noticeably, in this stage, the output power p_o increases to compensate the lost contribution from the GI and moves away from the power reference P_{ref}. Consequently, the error between p_o and P_{ref} becomes larger and v_s increases. On the contrary, the rate

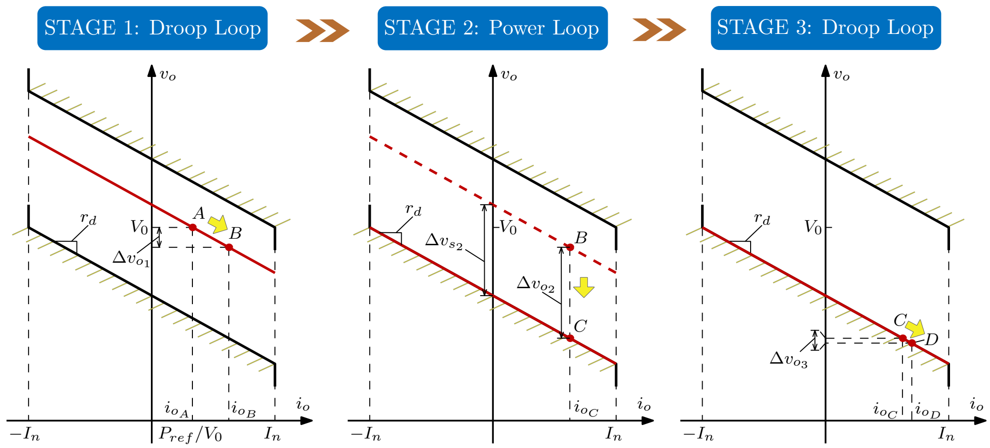

Fig. 5. Transition from power regulation mode to bus regulation mode.

of change of v_o decreases as the power deficit reduces.

- Stage 2: once v_s changes at the same pace as v_o, the transition process steps into the second stage, where the power loop takes effect. The power regulator $G_p(s)$ completes the transition from the unsaturated state to the saturated state and the operation point of the DER converter moves from B to C. The variation of the bus voltage Δv_{o_2} can be expressed as:

$$\Delta v_{o_2} = \Delta v_{s_2} = V_s^{min} - r_d \frac{P_{ref}}{V_0} \tag{4}$$

where the subscript 2 indicates that the change occurs in the second stage. In this stage, the bus voltage deviates together with the droop curve and the output current approximately remains unchanged.

- Stage 3: the third stage begins when v_s hits its lower saturation level V_s^{min}. The droop curve reaches its lower bound and the power regulator is inhibited. The bus voltage is then determined again by the droop loop and the operation point of the DER converter changes from C to D:

$$\Delta v_{o_3} = -r_d \cdot (i_{o_D} - i_{o_C}) \tag{5}$$

where the subscript 3 indicates that the change occurs in the third stage and i_{o_D} is the output current at operation point D. As can be seen, the bus voltage continues to decrease until the power balance is obtained. Finally, the microgrid enters another steady state.

B. Operation modes of microgrid

The operation of a dc microgrid with all the converters adopting the power-based droop controllers is now considered. The following operation modes can be identified.

1) Mode I: in this mode the GI converter compensates the power surplus or deficit within the microgrid through its connection with the upstream grid and maintains the bus voltage fixed at V_0, behaving as a grid-forming device. The DERs converters operate in power regulation mode, tracking their own power references and behaving as grid-following devices. ESSs can be charged or discharged according to the desired targets and renewable energy resources can be operated at their maximum power points. The equivalent microgrid model is shown in Fig. 6a.

2) Mode II: this mode occurs when the GI converter is incapable of controlling the bus voltage. There are two possible causes for this mode: the upstream grid is unavailable or the required power flow exceeds the GI converter availability (e.g., maximum converter's ratings). In these cases, the output power of the GI converter is fixed, and it can be represented as a constant power source. Meanwhile, DERs converters automatically reconfigure their operation status. For each DER converter, if the output power p_o is not equal to the power reference P_{ref}, the output of the power regulator $G_p(s)$ deviates and eventually saturates. In this condition, the droop curve is fixed at the upper or lower bound, and the converter works with droop control, operating in bus regulation mode to support the bus voltage. On the other hand, if p_o is equal to P_{ref}, the converter keeps on operating in power regulation mode. It should be noted that, in practical cases, the sum of DER converters power references differs from the load power, thus, there is at least one DER converter operating in bus regulation mode.

To clearly explain the possible operation modes in *Mode II*, the example of a microgrid composed of two equal DERs converters is now referred to. Let us assume $P_{ref_1} > P_{ref_2}$. The following situations can occur as a function of the load absorbed power P_L.

- Situation 1: Converter #1 and #2 are in bus regulation mode. Both of the droop curves of these two converters are saturated:
  - at the upper bound if:

$$P_{ref_1} > P_{ref_2} > \frac{P_L}{2} \tag{6}$$

  - at the lower bound if:

$$\frac{P_L}{2} > P_{ref_1} > P_{ref_2} \tag{7}$$

In this situation, the converters share the load equally if cable impedances are negligibly small. The equivalent microgrid model in this case is shown in Fig. 6b. Since the lower and upper bounds of the droop curves are designed to

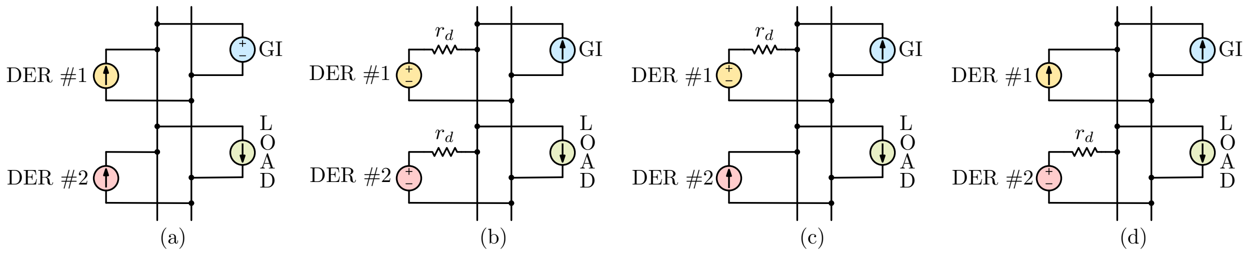

Fig. 6. Equivalent models of dc microgrid in different operation conditions. (a) in mode I; (b) in mode II, situation 1; (c) in mode II, situation 2; (d) in mode II, situation 3.

have no intersections, the case that the droop curves of two converters are saturated at different bounds cannot happen (this aspect is specifically addresses in Sec. IV).

- Situation 2: Converter #1 is in bus regulation mode while converter #2 is in power regulation mode. Converter #2 tracks its power reference P_{ref_2} and converter #1 supplies the remaining power demand, that is, $P_L - P_{ref_2}$. The droop curve of converter #1 is saturated at the upper bound. This situation occurs when:

$$P_{ref_1} > \frac{P_L}{2} > P_{ref_2} \quad \& \quad P_{ref_1} + P_{ref_2} > P_L \tag{8}$$

The equivalent microgrid model in this case is shown in Fig. 6c.

- Situation 3: Converter #1 is in power regulation mode while converter #2 is in bus regulation mode. Similar to situation 2, the droop curve of converter #2 is saturated at the lower bound. The relationship between P_{ref_1}, P_{ref_2} and P_L in this situation can be expressed as:

$$P_{ref_1} > \frac{P_L}{2} > P_{ref_2} \quad \& \quad P_{ref_1} + P_{ref_2} < P_L \tag{9}$$

The equivalent microgrid model in this case is shown in Fig. 6d.

It can be found that, the operation modes of DERs converters are actually determined by factors like the load power, droop coefficients and power references. With the non-critical communication within the microgrid, appropriate power references can be chosen for DERs converters to pursue specific operation situations.

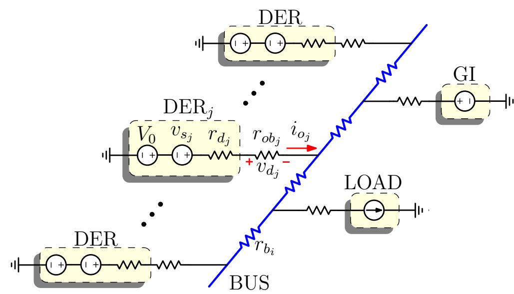

Fig. 7. Equivalent model of a dc microgrid with cable impedances r_{ob} and r_b.

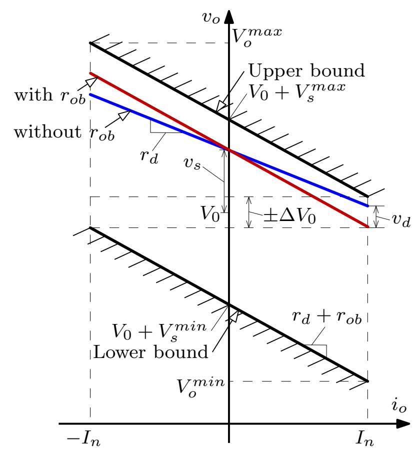

Fig. 8. Equivalent droop function with cable impedances r_{ob}.

IV. Controller design

According to the operation principle, the controller design is presented in this section, with distributed cable impedances taken into consideration. The current regulator $G_i(s)$, the voltage regulator $G_v(s)$, and the power regulator $G_p(s)$ should be designed considering different operation modes [27]. The focus herein is, in particular, on the selection of droop coefficient r_d and saturation levels of power regulator $G_p(s)$, V_s^{max} and V_s^{min}, which is an aspect that deserves adequate investigation.

A. Current delivery capacity

When the microgrid is in *Mode I*, all DERs converters operate in power regulation mode. In this condition, DERs converters should be able to generate or absorb their nominal currents. For *V-I* type droop methods, the droop coefficients r_d can be regarded as virtual output impedances of DERs converters, as shown in Fig. 7. In addition, the output-to-bus impedances r_{ob} of the cables that link DERs to the dc bus can be considered as extra output impedances. Thus, for a DER converter, its total output impedance is $r_d + r_{ob}$ and its output voltage v_o can be expressed as

$$v_o = (V_0 + v_s) - (r_d + r_{ob}) \cdot i_o \tag{10}$$

This equivalent droop function is reported in Fig. 8. After considering the output-to-bus impedances r_{ob}, the droop curve shows a larger droop slope, resulting in an additional voltage drop v_d, which limits the actual current capacity that can be exploited. Besides, although the output voltage of the GI converter is imposed at V_0, the bus voltage fluctuates from $V_0 - \Delta V_0$ to $V_0 + \Delta V_0$ due to distributed dc bus impedances

r_b, that is

$$V_0 - \Delta V_0 \leqslant v_o \leqslant V_0 + \Delta V_0 \tag{11}$$

Then, by combining (10) and (11), the output current i_o of each DER can be shown as

$$\frac{v_s - \Delta V_0}{r_d + r_{ob}} \leqslant i_o \leqslant \frac{v_s + \Delta V_0}{r_d + r_{ob}} \tag{12}$$

It can be found that the output current range is determined by the range of variation of v_s, namely, from V_s^{min} to V_s^{max}. To allow the exploitation of the full nominal current I_n of DERs, that is, to allow the current i_o to assume all the values in the interval $[-I_n, I_n]$, the limitations of V_s^{max} and V_s^{min} should be defined as

$$\begin{cases} V_s^{max} \geqslant I_n(r_d + r_{ob}) + \Delta V_0 \\ V_s^{min} \leqslant -I_n(r_d + r_{ob}) - \Delta V_0 \end{cases} \tag{13}$$

The requirement of rated current capacity gives a lower limitation for V_s^{max} and an upper limitation for V_s^{min}, respectively.

B. Bus voltage range

While in *Mode II* (i.e., autonomous mode), some DERs operate in bus regulation mode and regulate the bus voltage. When these DERs absorb the respective nominal current and their v_s are located at the upper saturation level V_s^{max}, the highest output voltage V_o^{max} is obtained. Similarly, when the DERs deliver nominal current and their v_s are located at the lower saturation level V_s^{min}, the output voltage reaches its lowest level V_o^{min}:

$$\begin{cases} V_o^{max} = V_0 + V_s^{max} + I_n(r_d + r_{ob}) \\ V_o^{min} = V_0 + V_s^{min} - I_n(r_d + r_{ob}) \end{cases} \tag{14}$$

If the acceptable bus voltage range is defined as $V_0 \pm \Delta V_b$, then $V_o^{max} \leqslant V_0 + \Delta V_b$ and $V_o^{min} \geqslant V_0 - \Delta V_b$ must be satisfied. Accordingly, the limitations for V_s^{max} and V_s^{min} can be written as

$$\begin{cases} V_s^{max} \leqslant \Delta V_b - I_n(r_d + r_{ob}) \\ V_s^{min} \geqslant -\Delta V_b + I_n(r_d + r_{ob}) \end{cases} \tag{15}$$

The requirements on bus voltage range give an upper and a lower limitation, respectively, for V_s^{max} and V_s^{min}.

C. Parameters selection

By combining (13) and (15), the available ranges of V_s^{max} and V_s^{min} can be found as

$$\begin{cases} I_n(r_d + r_{ob}) + \Delta V_0 \leqslant V_s^{max} \leqslant \Delta V_b - I_n(r_d + r_{ob}) \\ -\Delta V_b + I_n(r_d + r_{ob}) \leqslant V_s^{min} \leqslant -I_n(r_d + r_{ob}) - \Delta V_0 \end{cases} \tag{16}$$

According to (16), a restriction for r_d can be derived:

$$r_d \leqslant \frac{\Delta V_b - \Delta V_0 - 2 I_n r_{ob}}{2 I_n} \tag{17}$$

Since larger droop coefficient can bring benefits, such as higher power sharing accuracy, r_d should be chosen as large as possible. Additionally, for parallel DERs converters, their droop coefficients should be inversely proportional to their nominal currents to attain a proportional load distribution. In this case, let us define a maximum acceptable voltage drop V_d^{max} on the output-to-bus cables r_{ob}. For any DER converter in the dc microgrid, it is required that the product of its rated current I_n and its output-to-bus cable impedance r_{ob} is less than V_d^{max}. Then, the droop coefficient r_d can be selected as

$$r_d = \frac{\Delta V_b - \Delta V_0 - 2V_d^{max}}{2 I_n} \tag{18}$$

Further, V_s^{max} and V_s^{min} are set as

$$\begin{cases} V_s^{max} = \dfrac{\Delta V_b + \Delta V_0 - 2V_d^{max}}{2} \\ V_s^{min} = -\dfrac{\Delta V_b + \Delta V_0 - 2V_d^{max}}{2} \end{cases} \tag{19}$$

It can be seen that V_s^{max} and V_s^{min} are constants, so that all the DERs converters share the same saturation levels. As a result, under no load condition, there is no circulating current among DERs converters operating in bus regulation mode. It is also possible to find that the upper bounds do not intersect with the lower bounds at any voltage level, which means that DERs converters operating in bus regulation mode must have droop curves saturated at the same level.

D. Design Method

In summary, the design method adopted herein for the power-based droop controller shown in Fig. 2 consists in the design of the following control blocks.

1) Current regulator $G_i(s)$: according to the desired performances, $G_i(s)$ can be designed on the basis of the open-loop current-control transfer function $T_{i_1}(s)$ or $T_{i_2}(s)$, which are reported in (A.1) and (A.2) of the Appendix. Herein, the common choice of adopting a PI compensator for $G_i(s)$ is made, with a target crossover frequency equal to $1/10$ the switching frequency and phase margin of $60°$.

2) Voltage regulator $G_v(s)$: similarly to the previous stage, the regulator $G_v(s)$ can be designed on the basis of the open-loop voltage-control transfer function $T_v(s)$, which is reported in (A.3) of the Appendix. A PI compensator can be adopted for $G_v(s)$ too. In this case, the crossover frequency is typically set significantly smaller than the inner current control loop (e.g., $1/10$ the current loop crossover frequency).

3) Droop coefficient r_d and the power loop saturation levels V_s^{max} and V_s^{min}: firstly, the acceptable bus voltage fluctuation range ΔV_b, the maximum voltage drop V_d^{max} on the output-to-bus cable impedance r_{ob}, and the voltage drop ΔV_0 along the dc bus impedance r_b should be specified, taking into account the relevant constrains discussed above. Then, according to (18) and (19), r_d, V_s^{max}, and V_s^{min} can be computed.

4) Power regulator $G_p(s)$: depending on the aimed dynamic performance of the power loop, either a PI controller or a pure integrator can be chosen as $G_p(s)$. The regulator $G_p(s)$ can be designed to achieve the desired crossover frequency and phase margin by referring to the open-loop power-control transfer function $T_p(s)$, which is reported in (A.4) of the Appendix. It is worth mentioning that, since the power loop is actually used to adjust the droop function, the crossover frequency of

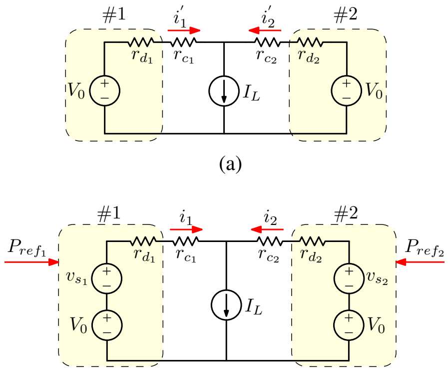

Fig. 9. Equivalent circuit of dc microgrids based on (a) traditional droop control; (b) power-based droop control.

the power loop should be much smaller than that of the droop loop (e.g., few hertz).

The numerical parameters computed by the design methodology described above and adopted in the presented validation of the approach are reported in Sec. VI and listed in Tab. I. While for steps 1) and 2) it is possible to refer to standard design procedures adopted for dc/dc converters for dc microgrids applications, the design steps 3) and 4) pertain to the control approach proposed in this paper.

V. Power sharing performance

With the proposed controllers, when the microgrid is in *Mode I*, DERs converters operate in power regulation mode. Through LBC, converters power references can be set in proportion to converters ratings. In this case, despite the existence of cable impedances, proportional power sharing can be accomplished precisely. However, when the dc microgrid operates in *Mode II*, power sharing accuracy degrades due to cable impedances. In the following, load distribution among parallel converters in the two operating modes is discussed and compared with that of traditional droop control. A microgrid including two DERs converters is considered in the comparison.

A. Droop controlled converters

The equivalent circuit with DERs converters employing droop controllers is shown in Fig. 9a. The output currents i_1' and i_2' can be derived as

$$\begin{cases} i_1' = \dfrac{r_{d_2}+r_{c_2}}{r_{d_1}+r_{c_1}+r_{d_2}+r_{c_2}} I_L \\ i_2' = \dfrac{r_{d_1}+r_{c_1}}{r_{d_1}+r_{c_1}+r_{d_2}+r_{c_2}} I_L \end{cases} \tag{20}$$

where I_L is the load current and r_c is the cable impedance including the corresponding output-to-bus impedance r_{ob} and the bus impedance r_b. The mismatch $\Delta i'$ between the relative currents is defined as

$$\Delta i' = \frac{i_1'}{I_{n_1}} - \frac{i_2'}{I_{n_2}} = \frac{I_L}{I_{n_1} I_{n_2}} \frac{(r_{d_2}+r_{c_2})I_{n_2} - (r_{d_1}+r_{c_1})I_{n_1}}{r_{d_1}+r_{c_1}+r_{d_2}+r_{c_2}} \tag{21}$$

where I_{n_1} and I_{n_2} are the nominal output currents of converter #1 and #2, respectively. Only if $(r_{d_1}+r_{c_1})I_{n_1}$ equals $(r_{d_2}+r_{c_2})I_{n_2}$, there is no mismatch current and an exactly proportional load sharing is obtained.

B. Power-based droop controlled converters

When power-based droop controllers are used in DER converters, the equivalent circuit of the dc microgrid can be presented as in Fig. 9b. The output of the power loop, v_s, can be regarded as an adjustable voltage source in series with the constant voltage source V_0.

The output currents, i_1 and i_2, of converter #1 and #2 can be calculated as

$$\begin{cases} i_1 = \dfrac{(r_{d_2}+r_{c_2})I_L + (v_{s_1}-v_{s_2})}{r_{d_1}+r_{c_1}+r_{d_2}+r_{c_2}} \\ i_2 = \dfrac{(r_{d_1}+r_{c_1})I_L - (v_{s_1}-v_{s_2})}{r_{d_1}+r_{c_1}+r_{d_2}+r_{c_2}} \end{cases} \tag{22}$$

the mismatch Δi of relative currents between these two converters results

$$\Delta i = \frac{i_1}{I_{n_1}} - \frac{i_2}{I_{n_2}} = \frac{I_L}{I_{n_1} I_{n_2}} \Bigg[\frac{(r_{d_2}+r_{c_2})I_{n_2} - (r_{d_1}+r_{c_1})I_{n_1}}{r_{d_1}+r_{c_1}+r_{d_2}+r_{c_2}} + \frac{(v_{s_1}-v_{s_2})(I_{n_1}+I_{n_2})/I_L}{r_{d_1}+r_{c_1}+r_{d_2}+r_{c_2}} \Bigg] \tag{23}$$

C. Comparison of power sharing performance

A comparison of power sharing performance between the power-based droop control and the droop control is discussed here. Generally, the droop coefficient of a converter is inversely proportional to its nominal output current, that is, $r_{d_1} I_{n_1} = r_{d_2} I_{n_2}$. Hence, the ratio K_{mis} of Δi and $\Delta i'$ is derived as

$$\begin{aligned} K_{mis} = \frac{\Delta i}{\Delta i'} &= 1 + \frac{(v_{s_1}-v_{s_2})(I_{n_1}+I_{n_2})}{(r_{d_2}+r_{c_2})I_{n_2} - (r_{d_1}+r_{c_1})I_{n_1}} \frac{1}{I_L} \\ &= 1 + \frac{(v_{s_1}-v_{s_2})(1/r_{d_1}+1/r_{d_2})}{r_{c_2}/r_{d_2} - r_{c_1}/r_{d_1}} \frac{1}{I_L} \end{aligned} \tag{24}$$

If $|K_{mis}|$ is smaller than 1, the load is better distributed (i.e., in a way that is closer to the exact proportional sharing) with the power-based droop control. Otherwise, the traditional droop control method shows a better power sharing performance.

Since the saturation levels of v_{s_1} and v_{s_2} are the same, that is, $V_{s_1}^{min} = V_{s_2}^{min}$ and $V_{s_1}^{max} = V_{s_2}^{max}$, $|K_{mis}|$ is analyzed as follows.

1) $v_{s_1} = v_{s_2}$: it indicates the case that converter #1 and #2 are both in bus regulation mode. v_{s_1} and v_{s_2} are saturated at the same level, either the upper level or the lower one. $|K_{mis}|$ is equal to 1 in this case, traditional droop control and power-based droop control show the same power sharing accuracy.

2) $v_{s_1} \neq v_{s_2}$: it suggests the situation that one converter is in bus regulation mode while the other one is in power regulation mode. Therefore, the power loop brings additional uncertainty for power sharing.

If v_{s_1} is larger than v_{s_2}, there are two possible operation cases for these two converters. In the first case, converter #1 operates in bus regulation mode, with v_{s_1} saturated at the

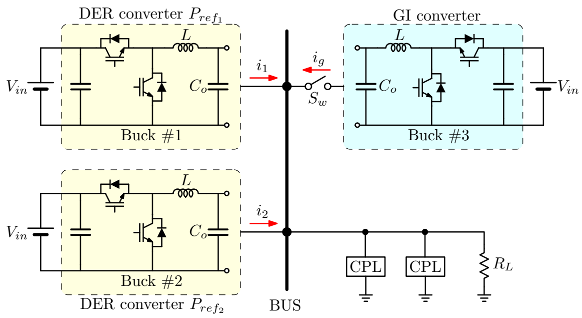

Fig. 10. Schematic of the laboratory-scale dc microgrid.

upper level, while converter #2 operates in power regulation mode. In the second one, converter #1 operates in power regulation mode, while converter #2 operates in bus regulation mode, with v_{s_2} saturated at the lower level. The indicator of power sharing performance, $|K_{mis}|$, is calculated as below

- $|(v_{s_1} - v_{s_2})(1/r_{d_1} + 1/r_{d_2})| < 2\,|(r_{c_2}/r_{d_2} - r_{c_1}/r_{d_1})I_L|$ & $r_{c_2}/r_{d_2} < r_{c_1}/r_{d_1} \Rightarrow |K_{mis}| < 1$
- otherwise $\Rightarrow |K_{mis}| > 1$

If v_{s_1} is smaller than v_{s_2}, similarly, the power-based droop control attains a higher power sharing accuracy if $|(v_{s_1} - v_{s_2})(1/r_{d_1} + 1/r_{d_2})| < 2\,|(r_{c_2}/r_{d_2} - r_{c_1}/r_{d_1})I_L|$ and $r_{c_2}/r_{d_2} > r_{c_1}/r_{d_1}$.

In summary, when a dc microgrid is operating in *Mode I*, the power-based droop control method is able to distribute the load proportionally. When operating in *Mode II*, by coordinating DERs power references, the power-based droop control method is able to improve the load distribution among sources.

VI. Experimental results

The actual operation of the proposed controller has been thoroughly tested by means of a laboratory-scale dc microgrid testbed. The testbed configuration considered herein is shown in Fig. 10. It is composed of three parallel buck converters of 3kW rated power, buck converter #1 and #2 play the role of DERs converters and are controlled by the proposed power-based droop control, buck converter #3 plays the role of GI converter. All the converters are powered by a dc power source. System parameters are listed in Table I. Here, the acceptable bus voltage fluctuation is $\pm 15\%$ of the nominal value, that is $\pm\Delta V_b = \pm 30\,\mathrm{V}$, the maximum voltage drop V_d^{max} on the output-to-bus cables impedances r_{ob} is $5\,\mathrm{V}$, and the voltage drop ΔV_0 along the dc bus impedances r_b is neglected. According to (18) and (19), the droop coefficients for two DERs converters are $0.67\,\mathrm{V/A}$, and power regulators upper and lower saturation levels are $10\,\mathrm{V}$ and $-10\,\mathrm{V}$. Besides, the transfer functions used to design the current regulator $G_i(s)$, the voltage regulator $G_v(s)$, and the power regulator $G_p(s)$ are reported in Appendix. The yielded parameters for these three regulators are shown in Table I. The resulted bandwidths of the current loop, the voltage loop, and the power loop are $1000\,\mathrm{Hz}$, $300\,\mathrm{Hz}$, and $3.5\,\mathrm{Hz}$, respectively.

In the following, the basic functionality of the proposed control approach is firstly shown. Secondly, the achievable power sharing performance with cable impedances included are evaluated.

TABLE I
System Parameters

Parameter	Symbol	Value
Converters		
Input voltage	V_{in}	$380\,\mathrm{V}$
Nominal bus voltage	V_{bus}	$200\,\mathrm{V}$
Nominal power	P_n	$3\,\mathrm{kW}$
Inductance	L_{in}	$1.6\,\mathrm{mH}$
Output capacitance	C_o	$110\,\mu\mathrm{F}$
Switching frequency	f_{sw}	$12.5\,\mathrm{kHz}$
Inner Current and Voltage Loops		
Current regulator	$G_i(s)$	$0.025 + 12.1/s$
Voltage regulator	$G_v(s)$	$0.16 + 395/s$
Droop Loop		
Voltage set point	V_0	$200\,\mathrm{V}$
Droop coefficient	r_d	$0.67\,\mathrm{V/A}$
Power Loop		
Upper saturation level	V_s^{max}	$10\,\mathrm{V}$
Lower saturation level	V_s^{min}	$-10\,\mathrm{V}$
Power regulator	$G_p(s)$	$0.067/s$

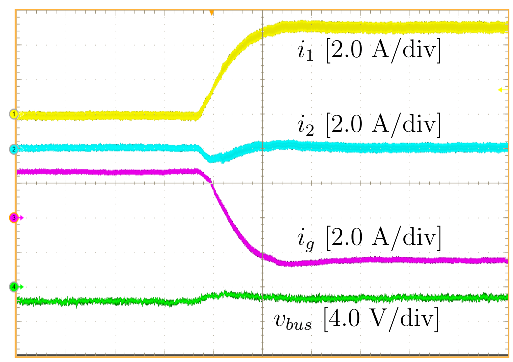

Fig. 11. Transient response of P_{ref_1} step: $0\,\mathrm{kW} \rightarrow 1\,\mathrm{kW}$, with $P_{ref_2} = 0\,\mathrm{kW}$ and $R_L = 70\,\Omega$. v_{bus} offset: $200\,\mathrm{V}$. Time: $100\,\mathrm{ms/div}$.

A. Basic functionality

The controller basic functionalities are evaluated while the microgrid operating in the two possible operation modes described in Sec. III-B.

When the microgrid operates in *Mode I*, buck #1 and #2 operate in power regulation mode and the GI converter dominates the bus voltage. A step change from $0\,\mathrm{kW}$ to $1\,\mathrm{kW}$ is applied to P_{ref_1}. The resulting dynamic performance is displayed in Fig. 11. The output current i_1 rises smoothly from $0\,\mathrm{A}$ to $5\,\mathrm{A}$, with the delivered output power correspondingly increasing up to $1\,\mathrm{kW}$. Accordingly, i_g reduces by $5\,\mathrm{A}$ to maintain the power balance. In the same operation case, the transient response with a load step from $70\,\Omega$ to $30\,\Omega$ is also shown in Fig. 12. The power deficit is compensated by the GI converter, while buck #1 and #2 keep injecting their power references in steady-state.

The transition of the microgrid from *Mode I* to *Mode II* is performed by opening the switch S_w, that is, by disconnecting the GI converter. As discussed in Sec. III-B and summarized in Fig. 6, under different situations of power references and loading conditions, different microgrid operations may establish during *Mode II*. The acquisitions displayed in Fig. 13 refer to microgrid operation in situation 1, with two DERs converters operating in bus regulation mode. Whereas, Fig. 14 refers to a transition to *Mode II* in situation 2, where buck #1

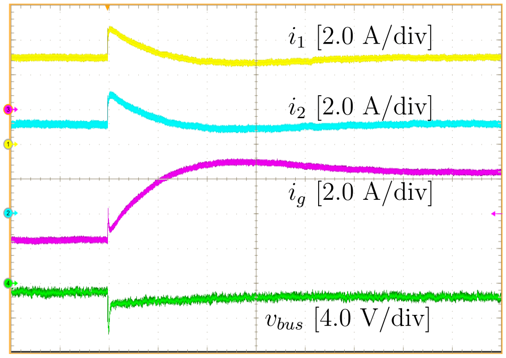

Fig. 12. Transient response of load step: $70\,\Omega \rightarrow 30\,\Omega$, with $P_{ref_1} = 1\,\mathrm{kW}$ and $P_{ref_2} = 1\,\mathrm{kW}$. v_{bus} offset: 200 V. Time: 40 ms/div.

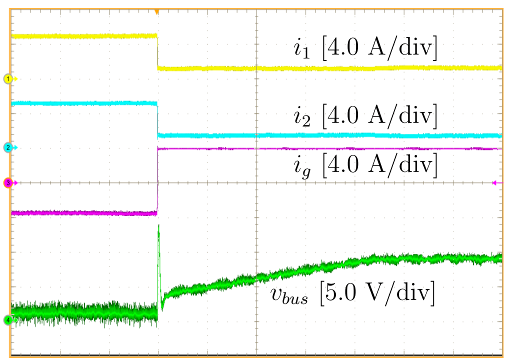

Fig. 13. Transition from *Mode I* to *Mode II*, with $P_{ref_1} = 1\,\mathrm{kW}$, $P_{ref_2} = 1\,\mathrm{kW}$, and $R_L = 70\,\Omega$. i_g offset: -4 A, v_{bus} offset: 200 V. Time: 25 ms/div.

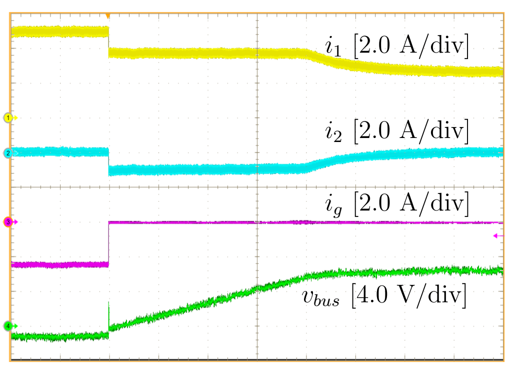

Fig. 14. Transition from *Mode I* to *Mode II*, with $P_{ref_1} = 1\,\mathrm{kW}$, $P_{ref_2} = 0\,\mathrm{kW}$, and $R_L = 70\,\Omega$. v_{bus} offset: 200 V. Time: 100 ms/div.

operates in bus regulation mode and buck #2 operates in power regulation mode. In both the cases, the transition processes are achieved smoothly, which validates the effectiveness of the proposed control method. Moreover, two programmable electronic loads (ARRAY 3711A) are connected to the dc bus to emulate constant power loads. The results obtained in the transition from *Mode I* to *Mode II* are displayed in Fig. 15. Notably, the transition process occurs smoothly, even in presence of constant power loads connected to the dc bus.

Load step is implemented when the microgrid operates in *Mode II*. In Fig. 16, both DERs converters operate in bus regulation mode before and after the load step. The total load power is increased by 800 W and each DER converter outputs

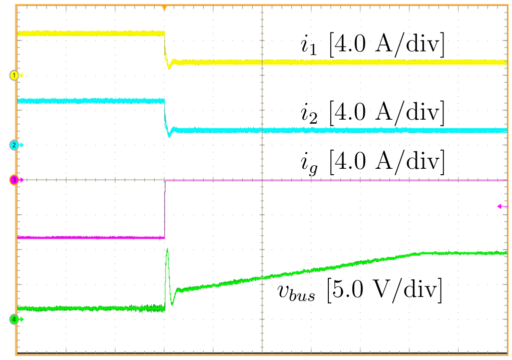

Fig. 15. Transition from *Mode I* to *Mode II*, with $P_{ref_1} = 1\,\mathrm{kW}$, $P_{ref_2} = 1\,\mathrm{kW}$, and $R_L = 150\,\Omega$. Two constant power loads, absorbing 0.2 kW each, are connected to the dc bus. v_{bus} offset: 200 V. Time: 25 ms/div.

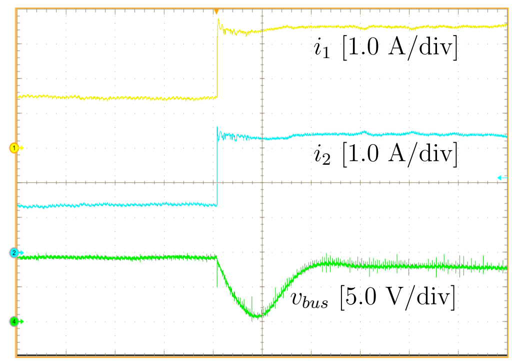

Fig. 16. Transient response of load step: $70\,\Omega \rightarrow 30\,\Omega$, with $P_{ref_1} = 1\,\mathrm{kW}$ and $P_{ref_2} = 1\,\mathrm{kW}$. v_{bus} offset: 200 V. Time: 1 ms/div.

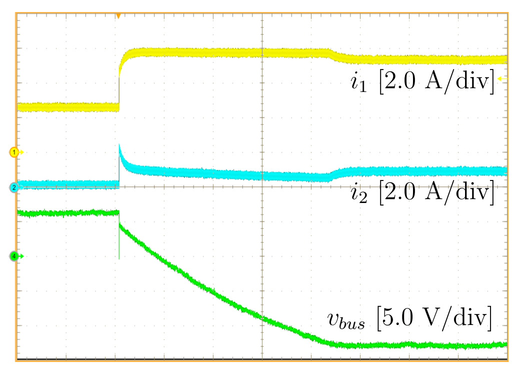

Fig. 17. Transient response of load step: $70\,\Omega \rightarrow 30\,\Omega$, with $P_{ref_1} = 1\,\mathrm{kW}$ and $P_{ref_2} = 0\,\mathrm{kW}$. v_{bus} offset: 200 V. Time: 500 ms/div.

400 W more, that is, about 2 A of their currents. As a result, bus voltage decreases by 1.4 V, due to the droop function. Besides, different power references and load steps may load to different microgrid states. As presented in Fig. 17, buck #1 switches from bus regulation mode to power regulation mode, while buck #2 undergoes a reverse process during this transient.

B. Power sharing performance

A resistor r_b, with value $0.5\,\Omega$, is placed at the output terminal of buck #1 to emulate cable impedance. In this way, the power sharing performances of traditional droop control as compared to power-based droop control are evaluated.

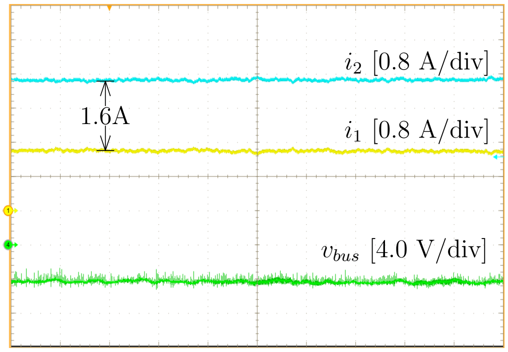

Fig. 18. Power sharing performance of the traditional droop control, with $R_L = 30\,\Omega$. i_1 offset: 1 A, i_2 offset: 1 A, v_{bus} offset: 200 V. Time: 4 ms/div.

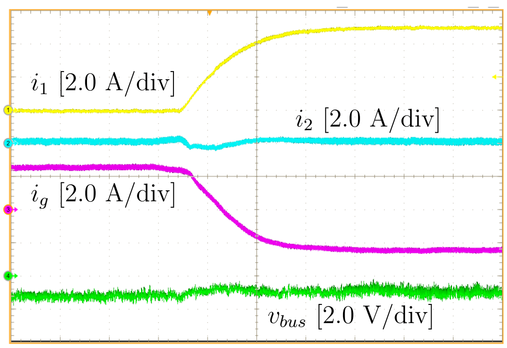

Fig. 19. Power sharing performance of the proposed control method under P_{ref_1} step: 0 kW → 1 kW, with $P_{ref_2} = 0$ and $R_L = 70\,\Omega$. v_{bus} offset: 200 V. Time: 100 ms/div.

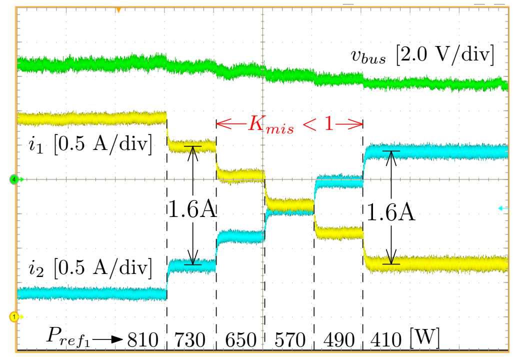

Fig. 20. Power sharing performance of the proposed control method under different P_{ref_1} (W), with $P_{ref_2} = 0$ kW and $R_L = 30\,\Omega$. i_1 offset: 1.5 A, i_2 offset: 1.5 A, v_{bus} offset: 180 V. Time: 5 s/div.

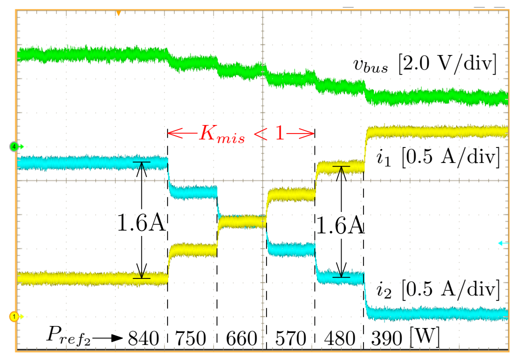

Fig. 21. Power sharing performance of the proposed control method under different P_{ref_2} (W), with $P_{ref_1} = 1.5$ kW and $R_L = 30\,\Omega$. i_1 offset: 2 A, i_2 offset: 2 A, v_{bus} offset: 200 V. Time: 5 s/div.

1) With traditional droop control: in this test, converters #1 and #2 employ conventional droop controllers. Since these two converters have the same power rating, an equal load distribution is expected. However, due to bus impedance r_b, a mismatch current of 1.6 A can be observed in Fig. 18, with a load current of about 6.7 A.

2) With power-based droop control: in this test, converters #1 and #2 employ the proposed power-based droop control. Fig. 19 shows the transient response with a step variation of the power reference P_{ref_1}, when the microgrid operates in *Mode I*. Since the bus voltage is imposed by the GI converter, converter #1 tracks its power reference precisely and the power sharing accuracy is preserved regardless of the bus impedance.

When the microgrid operates in *Mode II*, the power sharing performance is tested with different power references. Fig. 20 presents the result with converter #1 operating in power regulation mode and converter #2 operating in bus regulation mode. It can be seen that, by selecting proper power references, the mismatch current can be reduced or even totally eliminated. A similar result is obtained when converter #1 operates in bus regulation mode and converter #2 operates in power regulation mode, as shown in Fig. 21. As a consequence, compared to the traditional droop control method, power sharing accuracy is enhanced with the proposed approach.

VII. Conclusion

This paper presents a power-based droop controller for DERs in dc microgrids that are connected to upstream grids by a GI converter. During normal operation, the GI converter regulates the bus voltage and the proposed controller allows distributed converters to track given power references. If the GI converter is not able (e.g., due to disconnection or faults) to provide bus voltage regulation, the proposed controller seamlessly transits to bus regulation mode, allowing to stabilize the bus voltage by droop control. Moreover, by applying proper power references, the proposed control method allows better power sharing performances among parallel DERs as compared to conventional droop control methods. These features are attained by means of a bounded power loop on top of a traditional droop controller. In the paper, the design criteria of droop coefficient and saturation levels of the power control loop are also discussed, satisfying the requirements of output current capacity and bus voltage regulation. Finally, the power-based droop control method has been implemented on a laboratory-scale dc microgrid testbed and its performance, in all the relevant operation modes, is experimentally verified and reported.

Appendix

The design procedure of the regulators $G_i(s)$, $G_v(s)$, and $G_p(s)$, in Fig. 2, used in the proposed control method is presented herein. Fig. A.1a shows the implementation of the proposed control method referring to a buck-type DER converter. The equivalent models of the DER converter in bus regulation mode and power regulation mode are also illustrated

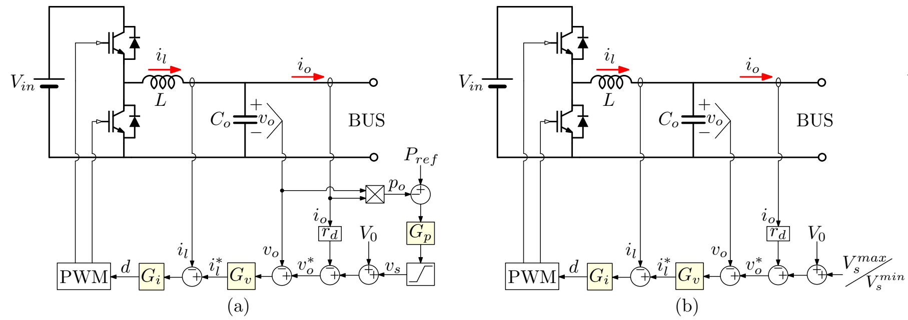

Fig. A.1. The implementation of the proposed control method on an example buck-type DER converter. (a) the control scheme; (b) the converter model in bus regulation mode; (c) the converter model in power regulation mode.

in Fig. A.1. In bus regulation mode, the DER converter is controlled as a voltage source. In this case, the output of the power regulator $G_p(s)$, that is, v_s, is saturated at its upper level V_s^{max} or lower level V_s^{min}, explained in Sec. III and shown in Fig. A.1b. On the other hand, in power regulation mode, the bus voltage is imposed at V_0 by the GI converter and the DER converter behaves as a power source. Since the voltage control bandwidth of the GI converter is much higher than the power control bandwidth of the DER converter, the GI converter can be modeled as an ideal voltage source. Then, the output voltage v_o is also set at V_0 and the output capacitance C_o can be neglected, as shown in Fig. A.1c.

At first, the current control loop is considered to design the current regulator $G_i(s)$. In bus regulation mode, the open loop transfer function $T_{i_1}(s)$ from duty cycle d to the inductor current i_l is derived as:

$$T_{i_1}(s) = \frac{\hat{i}_l}{\hat{d}} = \frac{sC_oV_{in}}{s^2LC_o + 1} \cdot e^{-\tau s} \qquad \text{(A.1)}$$

where τ is the control delay. In power regulation mode, the open loop transfer function $T_{i_2}(s)$ from duty cycle d to the inductor current i_l is expressed as:

$$T_{i_2}(s) = \frac{\hat{i}_l}{\hat{d}} = \frac{V_{in}}{sL} \cdot e^{-\tau s} \qquad \text{(A.2)}$$

Generally, the current loop is expected to have high crossover frequency. In this frequency range, $T_{i_1}(s)$ and $T_{i_2}(s)$ are similar to each other. Hence, the current regulator $G_i(s)$ can be designed based on either $T_{i_1}(s)$ or $T_{i_2}(s)$.

The voltage regulator $G_v(s)$ allows the output voltage v_o to track the voltage reference v_o^*. As v_o is clamped to V_0 in power regulation mode, $G_v(s)$ should be designed according to the transfer function derived for the bus regulation mode. In bus regulation mode, the open loop transfer function $T_v(s)$ from the current reference i_l^* to the output voltage v_o is derived as:

$$T_v(s) = \frac{\hat{v}_o}{\hat{i}_l^*} = \frac{1}{sC_o} \cdot \frac{T_{i_1}(s) \cdot G_i(s)}{1 + T_{i_1}(s) \cdot G_i(s)} \qquad \text{(A.3)}$$

Then, $G_v(s)$ can be designed according to $T_v(s)$.

The power regulator $G_p(s)$ should be designed on the basis of the transfer function derived in power regulation mode, because the output of $G_p(s)$ is saturated in bus regulation mode. In power regulation mode, the open loop transfer function $T_p(s)$ from the voltage offset v_s to the output power p_o is given as:

$$T_p(s) = \frac{\hat{p}_o}{\hat{v}_s} = \frac{V_0 \cdot G_v(s) \cdot T_{i_2}(s) \cdot G_i(s)}{1 + T_{i_2}(s) \cdot G_i(s) \cdot (1 + G_v(s) \cdot r_d)} \qquad \text{(A.4)}$$

Finally, the power regulator $G_p(s)$ can be designed on the basis of $T_p(s)$.

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