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A fast trigger processor for limited streamer tubes

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Abstract

An electronic device has been realized which provides the total number of firing limited streamer tubes (LST) in different sectors as well as in the whole detector. These numbers are available a few microseconds after the read-out of the LST front-end electronics and can be used for trigger purposes.

1. Introduction

Limited streamer tubes (LST) [1] are now widely used in physics experiments. As tracking devices they can easily recognize tracks, as well as provide a measurement of the total energy deposited in the detector. Both informations are very useful even at the trigger level, allowing the selection of the interesting events on the basis of the track multiplicity and/or energy release.

The electronic device, described in the following, has been realized in order to compute on line the number of channels hit in a streamer tube detector in pre-selected sections (partial sums) as well as in the whole detector (global sum).

The LST data are usually stored in digital form in a shift register implemented in the front end electronic cards, which are serially connected in a daisy chain line (bus) for the read out. The partial sums are obtained grouping properly the buses through a CAMAC programmable selection. Acceptance windows can be introduced, via CAMAC, for each partial as well as for the total sum. Thus a trigger or a reset signal is generated, in a few μs, whether or not all the computed sums are contained in their preset acceptance windows.

The system was designed for the N–$\bar{N}$ experiment [2] which was designed to search for neutron–antineutron oscillations at the high flux reactor of the Institute Laue-Langevin in Grenoble. It was intended to operate jointly with a controller especially designed for the read-out of the streamer tubes front end electronics (STROC) [3], working at 5 MHz frequency.

In the following the system lay-out is described (Section 2), and details are given on the processing cycle and the CAMAC functions (Section 3); then some concluding remarks on its performance and use are given.

2. System lay-out

The system is composed of two different types of modules: the pre-adder (PA) cards and the master adder (MA) module, see Fig. 1.

The PA is designed as a single slot CAMAC module which can handle up to 16 buses, each one 1024 channel long. It computes the total hit activity over the single buses. To allow a fully parallel computation each PA contains 16 8-bit counters, in a one to one correspondence with the front-end buses.

The information from the front-end cards is obtained during their shift-out by spying the status of the cluster memories of the STROC. An ECL-TTL adapter board, plugged into the rear STROC connector, interfaces the read-out controller and the PAs. It delivers to the PA the STROC gate and read-out clock signals, together with the hit activity of each connected bus.

The MA is a programmable device which computes the partial and the global sums out of the single bus sums. It is responsible for the final trigger decision. With the present configuration it can handle up to 7 PAs by means of an external common bus realized with a 34 wire flat cable. This corresponds to a maximum of 114 688 digital channels.

In the present design, according to the requirements of the N–$\bar{N}$ experiment, the partial and global sums have a dynamic range of 12 bit.

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3. The processor cycle

The processor cycle is composed of two distinct phases: during the first one the PAs accumulate the sum over the single buses in parallel with their readout, in the second one the MA computes the partial and global sums and takes the trigger decision.

3.1. The PA cycle

The block diagram of PA unit is shown in Fig. 2. The STROC read-out gate (STROBE) is used to automatically reset the PAs through the capacitor C1 and to start a new processing cycle.

The detection of an active channel during the gate strobes the read-out clock signal to the ck line of the corresponding bus counter. In this way at the end of the read-out each counter will contain the total number of hit channels on the corresponding bus. It has to be noted that the real structure of the computation is highly parallel: to perform this cycle a time is required: 205 μs maximum, 155 μs for the N–$\bar{N}$ experiment, which corresponds to the time needed to read out the LST buses.

Usually bus crowding indicates discharges in the detector or other kind of bus failures. So the 8-bit dynamic range of the bus counters, corresponding to an occupation of 25% of the maximum allowed bus length, is not a limitation: in any case the buses presenting an overflow will be discarded from the computation (see below).

3.2. The MA cycle

The logical structure of the MA computing cycle is summarized by the flow chart diagram of Fig. 4 while the MA module block diagram is shown in Fig. 3.

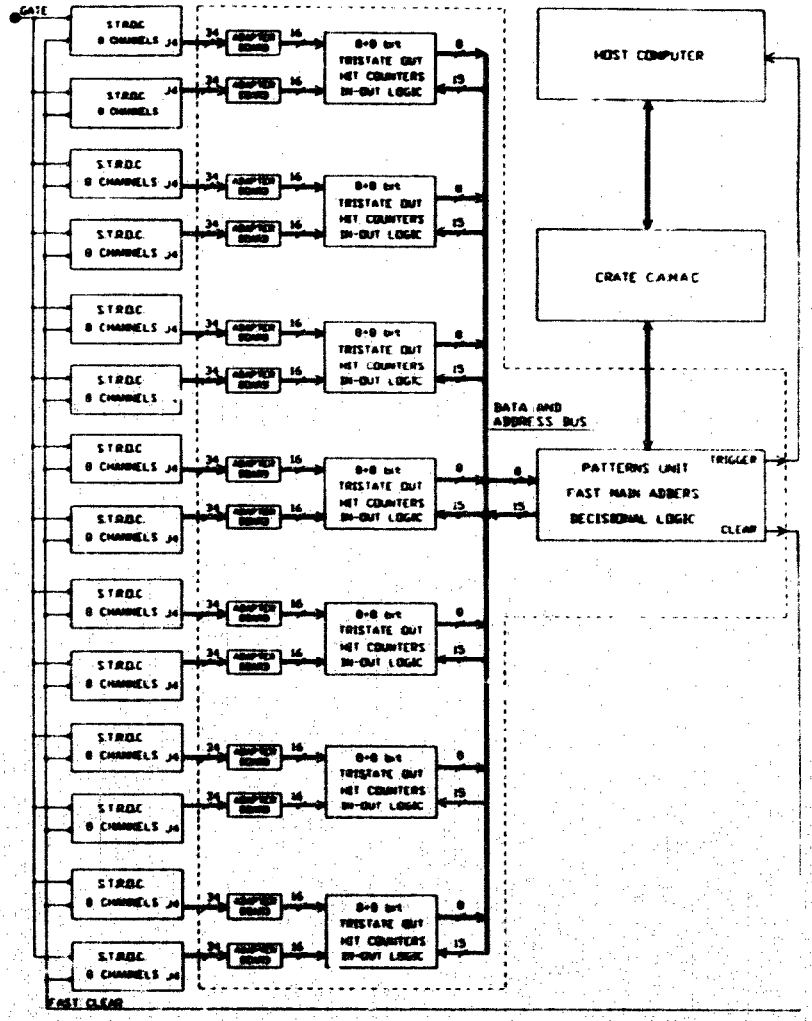

Fig. 1.

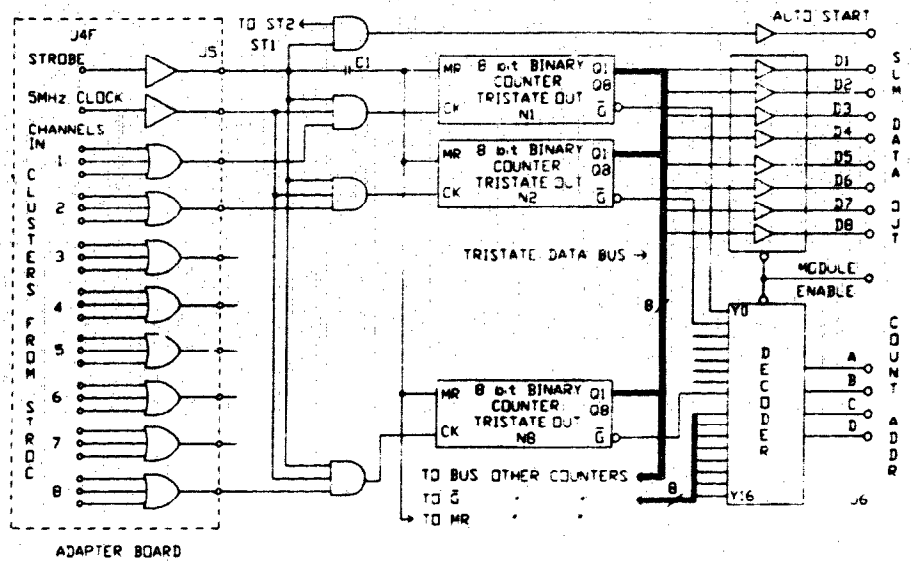

Fig. 2.

When the last STROC releases the gate line an automatic START of the MA cycle is generated. The MA starts clocking at 10 MHz an 8 bit RAM (PATTERN UNIT) containing the addresses of the programmed sequence of buses. It drives the COUNT ADDRESS lines (bit 0–3) and through the decoder A (bit 4–6) the PA address. The most significant bit (7) signals the end of a group of buses, while the 8th output of the decoder

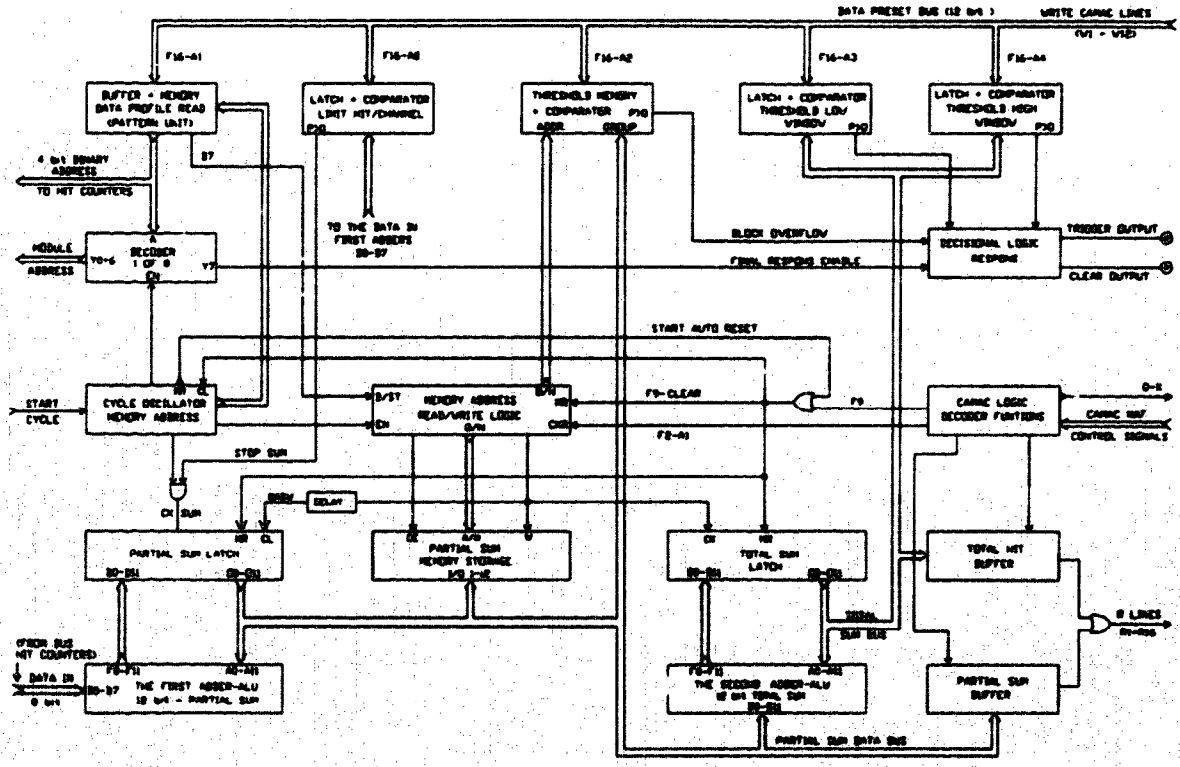

Fig. 3.

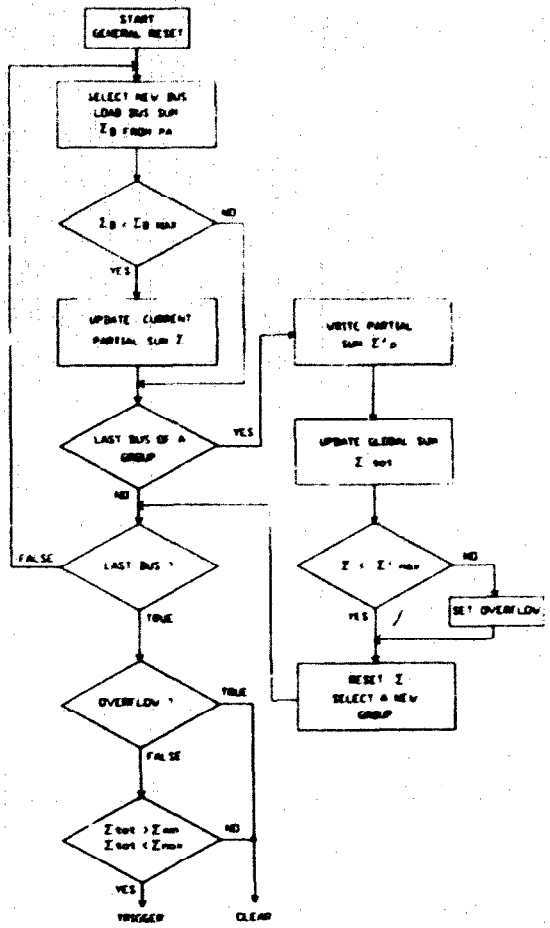

Fig. 4.

generates the STOP of cycle. Bus grouping is initially done by CAMAC according to the required physical informations. With the present system up to 16 groups of buses can be defined.

The selected PA forces on the data lines the content Σ_B of the addressed bus counter. The new value of the current partial sum, Σ, updated by the partial sum adder ALU, is latched only if Σ_B is below the CAMAC preset bus upper threshold to discard the crowded buses.

If an end of group is detected the memory address R/W logic writes the current value of Σ in the corresponding partial sum memory (12 bit RAM), latches the updated global sum (Σ_{tot}) out of the total sum adder ALU and, with a delay of 20 ns, resets the partial sum latch. At the same time a comparator sets a block overflow flip-flop, if Σ exceeds the maximum allowed value.

When the last bus is processed the final decision logic is enabled: if the value Σ_{tot} stored in the global sum latch is contained in its preset acceptance window and no block overflow has occurred a trigger signal is generated, otherwise a clear signal is issued. The signals are available a few μs (11 μs maximum) after the completion of PA cycle. For the N–$\bar{N}$ experiment the total time required to take this decision after the latch of the LST cards was 166 μs.

Table 1
List of the implemented CAMAC functions

NAF	Action
F16-A0	Write the maximum meaningful number of hit/bus (0–255)
F16-A1	Store the pattern of buses for the various groups
F16-A2	Write the upper thresholds for each group of buses
F16-A3	Write the global lower threshold
F16-A4	Write the global upper threshold
F2-A0	Read the global sum (bit 0–11), the trigger status bit (12) and the overflow bit (14)
F2-A1	Read the partial sums
F9	Reset
F26	Enable START input
F24	Inhibit START input
F25	Inhibit CLEAR output

3.2.1. CAMAC functions

To allow an easy change of the thresholds and the composition of groups of buses the set of CAMAC functions listed in Table 1 has been implemented. The computed sums are also CAMAC readable till the next cycle and the read-out can be carried out via a single DMA Q-Scan, ECA mode, operation.

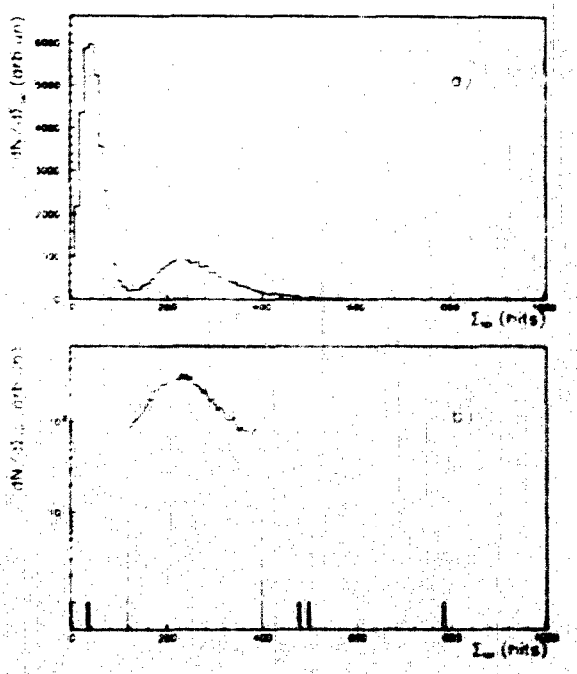

Fig. 5.

4. Conclusions

An electronic system has been realized which is able to provide a trigger or a fast clear signal on the basis of the total and partial hit activity in a LST detector. The signal is available a few μs after the read-out of the LST buses.

This fast processor was originally designed to suppress the beam related spurious triggers in the N–$\bar{N}$ experiment at Grenoble [2,4]. Fig. 5 is an example of its action. It shows a typical histogram of the total hit activity in the detector for events collected without (a) and with (b) this trigger processor: the beam related fake triggers, corresponding to the low activity peak, were efficiently eliminated at the trigger level without increasing the electronic dead time [2,4]. The upper cut of 400 hits is applied as a matter of example: during the data taking it was fixed to 2500 hits.

A system with 7 PAs was used without failures for approximately two years in the N–$\bar{N}$ experiment at Grenoble, showing its complete reliability. The same device exhibited good performances also in the Fenice experiment at Frascati where it was also adopted [5].

References

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