# A Two-Stage Twin-Bus Buck Converter for Battery Charging Applications

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***Abstract*—The paper describes and shows the operation of a two-stage isolated dc-dc converter for battery charging in electric-vehicle applications, where high efficiency is needed over a wide range of battery voltages. The proposed converter combines a first two-output isolation stage with CLLC resonant structure and a second two-input buck post-regulator. The post-regulator presents a twin-bus buck structure that allows low conversion losses even with output voltages that vary over a wide range, thanks to reduced voltage stresses across the switching devices. The isolation stage is constantly operated at resonance as a dual-output dc-transformer (DCX), thus ensuring high efficiency. The conversion structure, analysis, and design considerations are outlined considering an experimental prototype rated 10 kW, with input-bus voltage at 800-V and output-bus voltage ranging from 250 V to 500 V, which is suitable for electric-vehicles battery-charging applications.**

***Index Terms*—Battery charger, CLLC, dc-dc, dc-transformer, post-regulator, soft-switching, two-input buck converter.**

## I. Introduction

DC-DC converters with galvanic isolation are important components for the development of effective electric-vehicle (EV) battery-charging systems [1]–[3]. The resonant LLC converter is commonly adopted in many applications for its simple structure and efficient power conversion. However, performance significantly degrades at input or output voltages that do not allow near-resonance operation [2], [4]–[6]. To overcome the limitations of the frequency-modulated LLC converter, the LLC stage is often operated at its resonant frequency (i.e., DCX operation), which ensures high efficiency [7], [8]. This configuration, called isolated DCX-LLC resonant converter, is widely used in applications, including power supply, energy storage, data centers, and solid-state transformers, because it can efficiently interface two dc buses while providing galvanic isolation [7], [8]. Instead, output voltage regulation is obtained in other configurations, like those discussed in [9]–[13], by using a subsequent additional stage. These multi-stage solutions show potential advantages to accommodate wide operating voltage ranges for applications like in Fig. 1, at the cost of a higher number of components, which, on the other hand, may impact the overall power density [13]–[15].

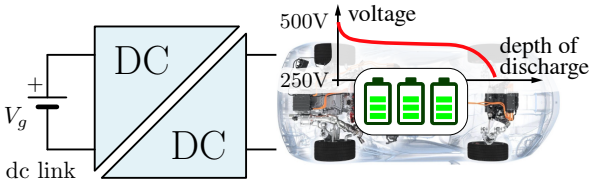


Fig. 1: EV-charging application.

To improve the performance of the LLC resonant dc-dc converter in a wide output-voltage range, this paper describes, analyzes, and evaluates experimentally a two-stage conversion structure in which the second stage performs the post-regulation of the output voltage. Such a multi-stage solution shows potential advantages in accommodating a wide range of operating voltages for the application displayed in Fig. 1, at the cost of a higher number of components with respect to the basic LLC topology, but with potential advantages in terms of overall conversion efficiency for wide ranges of operating voltage. Moreover, the described solution presents reduced voltage stresses on the switching devices, allowing low conversion losses even when working with a wide range of input or output voltages. Hence, the losses of the post-processing stage have only a marginal impact on the overall efficiency of the converter.

The conversion circuit is represented in Fig. 2. The post-regulator, herein referred to as twin-bus buck (TBB), is connected to an intermediate dc-link, which is supplied through the two secondary windings of a high-frequency transformer and subsequent rectifier. The principle is to operate the main converter at the operating condition that ensures maximum efficiency, namely, at resonance, and exploit the post-regulation stage working at lower voltage stress to perform the output voltage regulation. Despite the additional post-regulation stage, its parallel structure allows additional flexibility for output voltage regulation while preserving high overall efficiency. The merits of the solution and the related efficiency improvements are outlined in this work and demonstrated by

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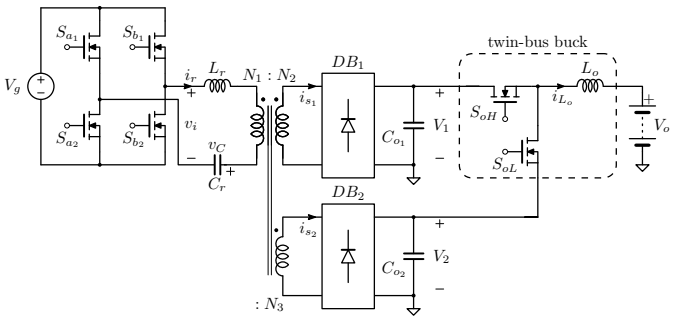



Fig. 2: Simplified schematic of the considered two-stage twin-bus buck converter.

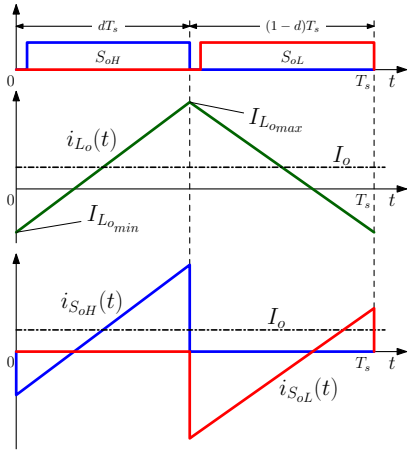



Fig. 3: Main waveforms of TBB stage shown in Fig. 2.

measurements on an experimental prototype.

In the following, the topology is described in Sect. II. The DCX stage design is discussed in Sect. III and Sect. IV reports the obtained experimental results considering a 10- kW rated prototype. Conclusions are reported in Sect. V.

## II. Converter Structure and Operation

### A. Two-Stage Converter Configuration

Different configurations of two-stage dc-dc converters exploiting a voltage post-regulator are described in the literature [16]–[18]. As shown in Fig. 2, the proposed converter consists of a first isolation stage based on an LLC resonant converter implementing a high-efficiency dual-output DCX converter and a second conversion stage for post-regulation connected to the load. Such a second stage supplied by the DCX converter presents a two-input buck structure [19], called herein twin-bus buck (TBB), and it is responsible for output voltage regulation. Referring to Fig. 2, the voltage stress of the post-regulator, namely, $V_1 - V_2$, is lower that the output voltage $V_o$, which allows switching devices with smaller on-resistance as well as lower switching losses.

### B. Twin-Bus Buck Converter and Main Waveforms

The proposed dual-input post-regulator is shown in Fig. 2, with key waveforms displayed in Fig. 3. The post-regulator is based on a dual-input buck topology [19], [20], designed to operate in quasi-square wave, that is, with a peak-to-peak inductor current ripple higher than twice the average load current. This allows the zero voltage turn-on of the switches $S_{oH}$ and $S_{oL}$. The TBB is responsible for the output voltage regulation of the whole converter, shown in Fig. 2. The output voltage $V_o$ is a function of the input voltages of the TBB, $V_1$ and $V_2$ with $V_1 > V_2$, and the duty-cycle of the upper switch (i.e., $S_{oH}$):

$$V_o = V_2 + d(V_1 - V_2) \tag{1}$$

For fixed input voltages $V_1$ and $V_2$, the minimum and maximum output voltages are:

$$\begin{aligned} V_o^{\min} &= d^{\min} V_1 + (1 - d^{\min}) V_2 \\ V_o^{\max} &= d^{\max} V_1 + (1 - d^{\max}) V_2 \end{aligned} \tag{2}$$

with $d^{\min}$ and $d^{\max}$ indicating the minimum and maximum duty-cycles of $S_{oH}$, and corresponding to $V_o^{\min}$ and $V_o^{\max}$ in Table I, respectively. Then, the needed input voltages $V_1$ and $V_2$ provided by the DCX stage, can be calculated from (2) as:

$$\begin{aligned} V_1 &= \frac{V_o^{\max}(1 - d^{\min}) - V_o^{\min}(1 - d^{\max})}{d^{\max} - d^{\min}} \\ V_2 &= \frac{V_o^{\min} d^{\max} - V_o^{\max} d^{\min}}{d^{\max} - d^{\min}} \end{aligned} \tag{3}$$

By using (3), the maximum voltage stress of the switches $V_1 - V_2$, can be expressed as:

$$V_1 - V_2 = \frac{V_o^{\max} - V_o^{\min}}{d^{\max} - d^{\min}} \tag{4}$$

which is always lower than the voltage stress of the switches of a single-stage converter that requires a supply voltage higher than the maximum output voltage. The only effective way to minimize such voltage stress, and the related switching loss, is to maximize the duty-cycle excursion $d^{\max} - d^{\min}$, for example, imposing $d^{\min} = (1 - d^{\max}) = 5\%$. In such extreme conditions, ZVS can also be achieved by a proper selection of the output inductor value and the switching frequency (refer, for example, to [21], [22]). In general, the main advantage of this converter solution is that the voltage stress $V_1 - V_2$ of the switches is lower than the input voltages, allowing the choice of MOSFETs with lower voltage ratings and potentially lower losses [14], [15].

## III. Design of LLC Stage Operated as DCX

When the LLC resonant tank is operated exactly at resonance, the voltage conversion ratio becomes virtually independent from the actual load. In this operating condition, the LLC behaves as a dc-transformer and presents maximum efficiency [15]. From (3), with $d^{\min} = (1 - d^{\max}) = 5\%$, the transformer turns ratio can be calculated as $n_1 = N_2/N_1 = 0.642$ and $n_2 = N_3/N_1 = 0.295$ to make the LLC converter operate at the resonant frequency $f_s$ at input voltage $V_g = 800$ V and output voltages ranging from 250 V to 500 V.

### A. Transformer Design

In the design of the main magnetic element, both winding and core losses must be considered. The transformer design procedure adopted herein is based on [23].

Once the magnetic core is selected, with given magnetic volume $V_c$, window winding area $W_a$, core cross-sectional area $A_c$, Steinmetz parameters $K_c$, $\alpha$ and $\beta$, and maximum window filling factor $k_u$ (typ., assume $k_u \leq 40\%$), it is possible to calculate the winding losses as:

$$P^{\text{cond}} = RF(f_s)\rho_w V_w k_u J_0^2 \tag{5}$$

where $\rho_w$ is the copper resistivity, $V_w$ is the total windings volume, $RF(f_s) = R^{\text{ac}}/R^{\text{dc}}$ is the resistivity factor for the selected litz wire at fundamental frequency $f_s$ [23] and $J_0$ is the current density. The last parameter is calculated as:

$$J_0 = \frac{\sum VA}{K_v f_s k_f B_{\max} k_u A_p} \tag{6}$$

where $\sum VA$ is the power rating of the transformer, $K_v$ is the waveform factor, $B_{\max}$ is the peak flux density, $k_f$ is core stacking factor, and $A_p = A_c W_a$ is the area product of the core.

The core losses can be estimated using the Steinmetz equation:

$$P^{\text{core}} = V_c K_c f_s^{\alpha} B_{\max}^{\beta} \tag{7}$$

where $K_c$, $\alpha$ and $\beta$ are the Steinmetz parameters for the considered material, while $V_c$ is the core volume. The total transformer dissipated power is then computed as the sum of (5) and (7) and it must be lower than the thermal dissipation capability of the component at the desired operating temperature, which can be estimated during the design phase. Fig. 4 reports the results of the calculated transformer losses, showing a total loss of 24 W at nominal conditions, namely, $V_1 = 514$ V and $V_2 = 236$ V, and $P_o = 10\,k$W. According with Fig. 4, the selected design point is more conservative in terms of core losses with respect to the optimal point, this is due to a trade-off between the desired magnetizing inductance and the conductor sections. Fig. 5 depicts the winding layout of the designed transformer of Fig. 6a. The designed transformer presents turns ratio $n_1 = 0.625$ and $n_2 = 0.292$, current density $J_0 = 5$ A/mm$^2$, number of turns per winding $N_1 = 24$, $N_2 = 15$, $N_3 = 7$.

### B. Resonant Tank Design

For what concerns the design of the resonant $L_r C_r$ tank, the transformer leakage inductance can be exploited for the implementation of the inductive part. Given the DCX operation mode of the LLC, low values of $L_m$ can be used, which is beneficial in terms of transformer design, losses, and resonant capacitor voltage stress. With the aimed DCX operation, the value of the magnetizing inductance $L_m$ is typically chosen to ensure a sufficiently high magnetizing current to allow ZVS for all the switches of the main converter. A classical design for a DCX-LLC with voltage ratings of Table I (see, for example, [8], [15]) requires a magnetizing inductance of about 200 µH.

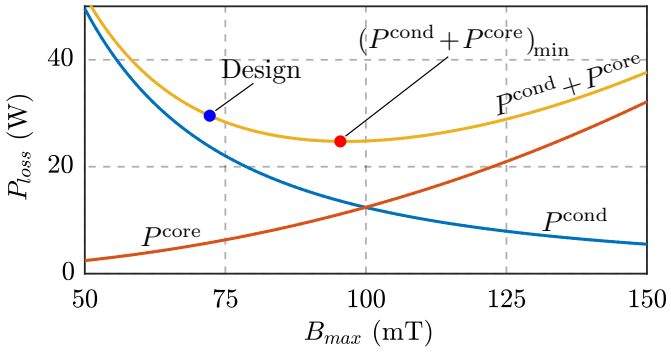



Fig. 4: $P$-$B$ plot for transformer design at $V_o = 400$ V and $P_o = 10$ kW.

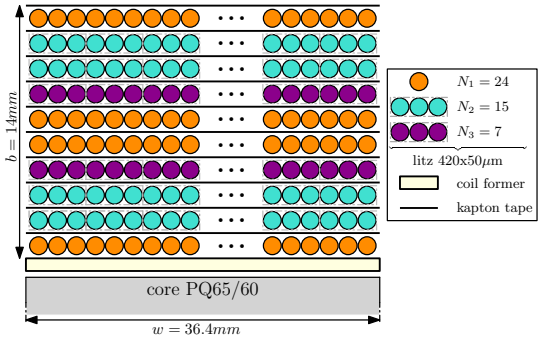
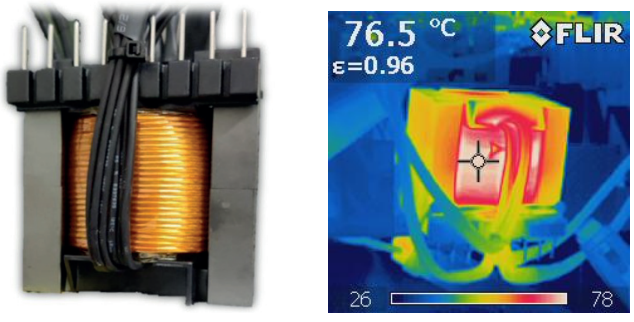



Fig. 5: Winding arrangement at the design point in Fig. 4.

The designed transformer in Fig. 6a achieves the design target, with a magnetizing inductance of about 215 µH.

The capacitive part of the resonant tank can be selected on the basis of the desired resonant frequency (i.e., converter switching frequency at DCX-LLC operation). The winding arrangement of the designed transformer in Fig. 4 is shown in Fig. 5. The interleaving of the primary and secondary-side windings is an effective solution to limit the leakage inductance and winding losses [24]. The experimental prototype in Fig. 6a, which results from the design in Fig. 4 and winding arrangement in Fig. 5, presents values of leakage inductances $L_{r_1} = 795$ nH, $L_{r_2} = 445$ nH, and $L_{r_3} = 271$ nH for the




(a) (b)

Fig. 6: (a) Transformer prototype, and (b) thermography at the design point in Fig. 4 (natural convection).

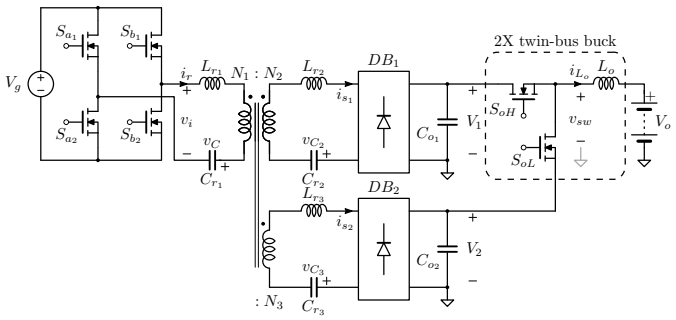



Fig. 7: Overall circuit schematic of the solution described herein, composed of a DCX-CLLC stage plus two interleaved twin-bus buck stages.

input, high-voltage, and low-voltage windings, respectively. The secondary windings leakage inductances $L_{r_2}$ and $L_{r_3}$ affect the overall resonance frequency proportionally to the normalized conduction interval of the respective diode bridge rectifier. In fact, these inductances come into play only when the corresponding rectifying diodes are conducting, and these intervals are related to the duty-cycle of the TBB stage, as well as to the load current. To remove such a dependence of the resonance frequency from the load, two additional resonant capacitors are connected in series with the two output ports of the transformer, as shown in Fig. 7. At resonance, the capacitive part of each of the series-resonant impedances $L_{r_i}C_{r_i}$ cancels out with the corresponding inductive part. $C_{r_1} = 796\,n\text{F}$, $C_{r_2} = 1.42\,\mu\text{F}$ and $C_{r_3} = 2.34\,\mu\text{F}$ are then calculated as proper values for the resonant capacitances in order to achieve a continuous resonant current operation of the converter. The proposed post-regulated converter is then shown in Fig. 7.

## IV. Experimental Results

The implemented prototype of a 10- kW module is shown in Fig. 9. Parameters are reported in Table I. Figs. 8 show the experimental waveforms of the implemented solution in Fig. 7 at output current $I_o = 25$ A and output voltages in the range 250 - 500 V. In particular, Figs. 8(a), (c), (e) show the measured resonant currents at the transformer ports, and Figs. 8(b), (d), (f) show the switching node voltage of the TBB and the inductor current. The switching frequency of the DCX-CLLC is set to $f_s = 200\,k\text{Hz}$ and dead-time to $t_d = 260\,\text{ns}$. If needed, additional refinements to match the true resonance frequency may be performed by adjusting the values of the resonant capacitors or the used operating frequency in the controller [8], [25], [26].

Figs. 8(a), (b) show the converter waveforms at minimum output voltage $V_o = 250$ V and output current $I_o = 25$ A. The duty-cycle of the TBB is set to 7%, the switching frequency to the lower limit of $f_{s_o} = 50\,k\text{Hz}$. Such a lower limit comes from a trade-off between the dc-link capacitances and the output voltage ripple. The conversion efficiency in such an operating point is about 97.6% (power and efficiency measurements performed by a Keysight PA2203A herein). For

TABLE I: Converter parameters.

| **Parameter** | **Symbol** | **Value** | |
|---|---|---|---|
| Input voltage | $V_g$ | 800 | V |
| Output voltage | $V_o$ | 250 - 500 | V |
| Nominal output voltage | $V_o^{\text{nom}}$ | 400 | V |
| Maximum output current | $I_o^{\text{max}}$ | 25 | A |
| Nominal power | $P_o^{\text{nom}}$ | 10 | $k$W |
| Switching frequency of CLLC | $f_s$ | 200 | $k$Hz |
| Switching frequency of TBB | $f_{s_o}$ | 50 - 400 | $k$Hz |
| Turns ratio $N_2/N_1$ | $n_1$ | 0.625 | - |
| Turns ratio $N_3/N_1$ | $n_2$ | 0.292 | - |
| Intermediate bus $V_1$ | $V_1$ | 500 | V |
| Intermediate bus $V_2$ | $V_2$ | 234 | V |
| Magnetizing inductance | $L_m$ | 215 | µH |
| Leakage inductances | $L_{r_1}$ | 795 | $n$H |
| | $L_{r_2}$ | 445 | $n$H |
| | $L_{r_3}$ | 271 | $n$H |
| TBB inductor | $L_o$ | 30 | µH |
| Transformer | Core: PQ65/60, Material: N87 | | |
| Inductor | Core: PQ40/40, Material: N97 | | |
| Resonant capacitances | $C_{r_1}$ | 796 | $n$F |
| | $C_{r_2}$ | 1.42 | µF |
| | $C_{r_3}$ | 2.34 | µF |
| $S_{a_1}$, $S_{a_2}$, $S_{b_1}$, $S_{b_2}$ | G3R30MT12K, SiC MOSFETs | | |
| $S_{oH}$, $S_{oL}$ | LMG3422R030, GaN FET | | |
| Output Rectifier $DB_1$ | UJ3D06560KSD, SiC diodes | | |
| Output Rectifier $DB_2$ | STTH100W04CW | | |

$V_o = 250$ V, ZVS conditions are not satisfied for average output currents higher than about 10 A. Figs. 8(c), (d) show the converter waveforms at nominal output voltage $V_o = 400$ V and output current $I_o = 25$ A. The duty-cycle of TBB is set to 65% and the switching frequency of the TBB is $f_{s_o} = 73\,k\text{Hz}$ in order to achieve ZVS. The conversion efficiency in such a point is about 98.4%. Figs. 8(e), (f) show the converter waveforms at maximum output voltage $V_o = 500$ V and output current $I_o = 25$ A. The duty-cycle of the TBB is set to 95%, the switching frequency to the lower limit of $f_{s_o} = 50\,k\text{Hz}$. The conversion efficiency in such a point is about 98.5%. For $V_o = 500$ V ZVS conditions are not satisfied for output currents higher than about 10 A. Remarkably, the loss of ZVS in heavy load conditions and extreme duty-cycles is the direct consequence of the selected inductance $L_o$. It is worth remarking that the selected inductance of the post-regulator, $L_o$, results from a trade-off between the inductor losses and the losses of the output switches $S_{oH}$-$S_{oL}$. Then, the switching frequency $f_{s_o}$ of the output switches is modulated in the range 50 - 400 kHz. Further optimizations in the selected inductance will be carried out in future works, after an accurate loss-breakdown of the considered converter implementation.

Fig. 10 shows the converter efficiency measured at the minimum, nominal, and maximum output voltage. The measured peak efficiency at minimum output voltage is 97.8%, while at nominal output voltage is 98.51%, which is very close to the absolute maximum efficiency of 98.63% measured at maximum output voltage conditions.

Fig. 11 shows the responses of the output voltage, $v_o$, and

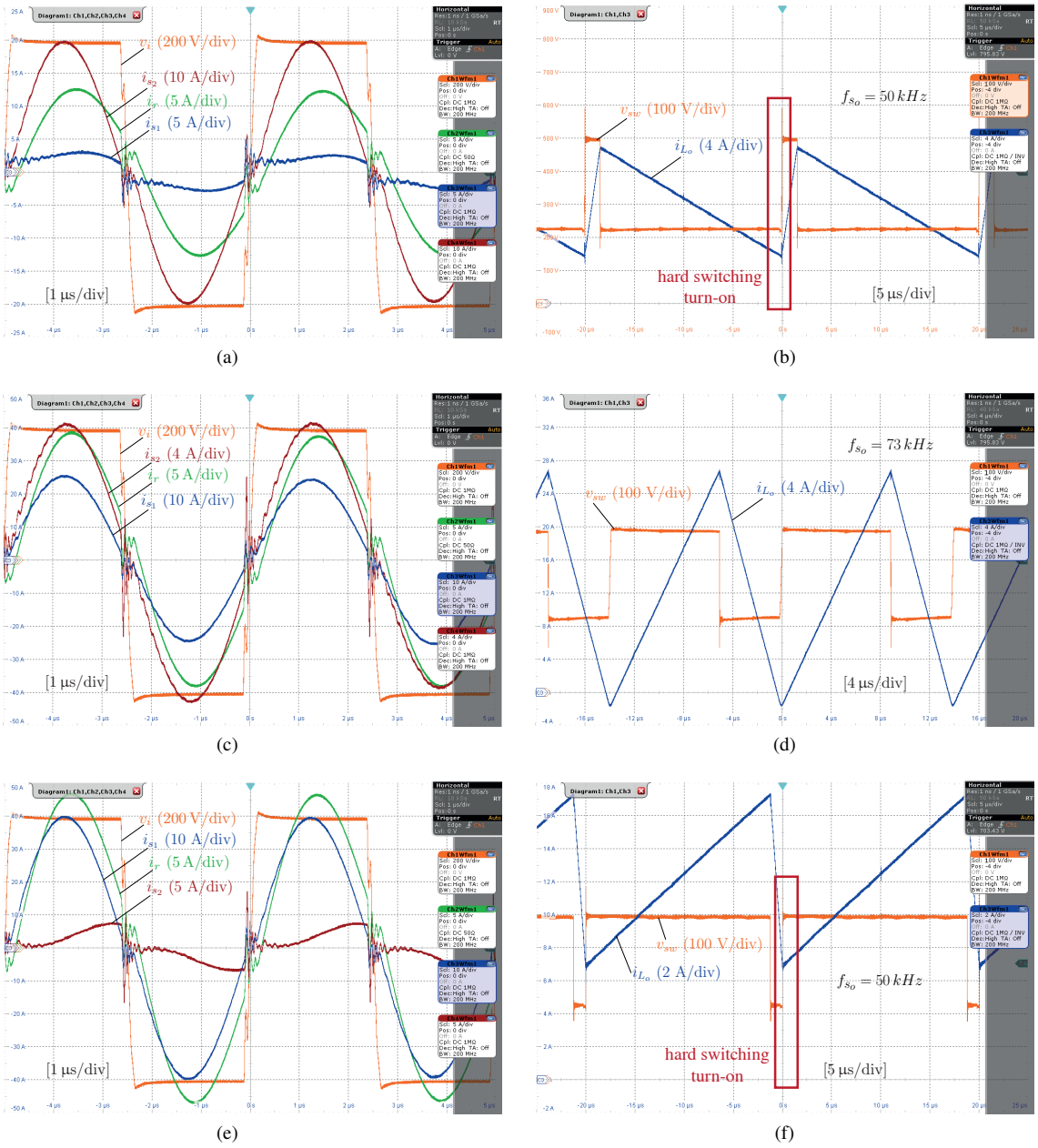



Fig. 8: Experimental results of the proposed converter in Fig. 7 at $I_o = 25$ A. (a),(b) $V_o = 250$ V; (c),(d) $V_o = 400$ V; (e),(f) $V_o = 500$ V.

inductor current of the TBB, $i_{L_o}$, after a step variation of the duty-cycle $d$. The load is set to a constant resistance $R_L = 90\,\Omega$, and duty-cycle $d$ steps from $40\,\%$ to $45\,\%$. The measured dynamics match the expectations from the simulation models. Further studies will be performed for the modeling and control of the converter as future developments of this work.

Finally, possible efficiency improvements can be obtained in the whole range of operation after an accurate losses investigation, through a better design of the magnetic elements, more efficient rectification stages, or through some parameters optimization.

## V. Conclusions

A two-stage converter composed of a DCX-CLLC and a post-regulator for battery charging applications is proposed, designed, and demonstrated in this work. The DCX-CLLC converter always operates at its optimal operating point and the additional post-regulator based on a dual-input buck converter is used to regulate the output voltage. In such a post-regulator, the stress of the switches is a fraction of the rated voltages; hence the efficiency can be improved. The considered topology is presented, showing experimental results considering a 10 kW prototype. Conversion performances covering the whole power and voltage ranges have been reported

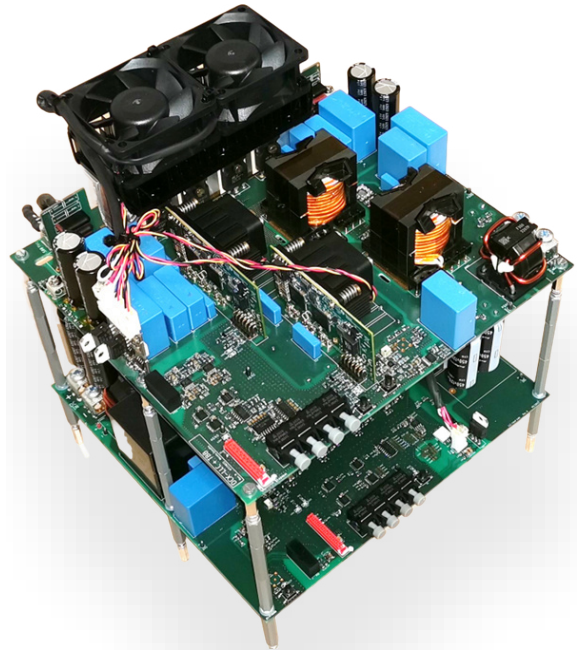


Fig. 9: DCX-CLLC + twin-bus buck converter prototype.

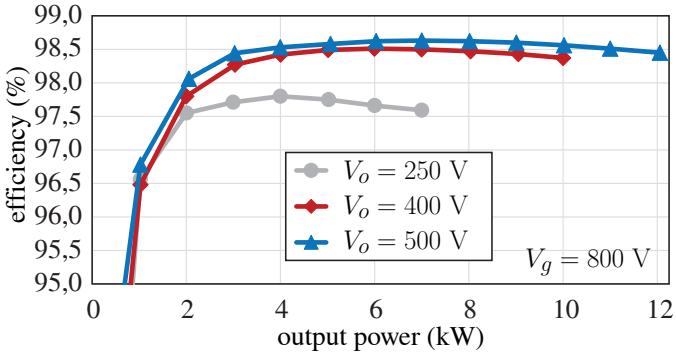



Fig. 10: Measured efficiency at minimum, nominal and maximum output voltage.

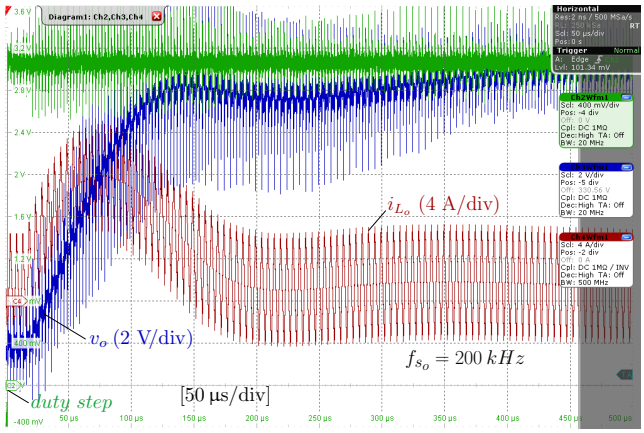



Fig. 11: Output voltage and inductor current response from a step perturbation of the duty-cycle. Step perturbation from $d = 40\,\%$ to $d = 45\,\%$. Resistive load $R_L = 90\,\Omega$.

experimentally, showing high efficiency over a wide range of operating conditions, recording a peak efficiency of 98.63% at 500 V output voltage and 7 kW transferred power.

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