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High-bandwidth droop-based controllers for DC and AC microgrids

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I would like to dedicate this thesis to my loving parents ...

Acknowledgements

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Abstract

Due to the reduction in the transmission and distribution losses, the overall system costs and the CO_2 emissions, distributed power generation based on sustainable and green resources, such as photovoltaic and wind have been exploited over the past decades. Grouping several mentioned power resources together with some loads as well as some energy storage systems is so-called a microgrid environment. Also, in microgrids, as the sources are near the loads, the power quality, efficiency, and reliability will be significantly increased. Microgrids are also a smart choice for remote locations that are not reachable by the main grid.

Microgrids have three different architectures, DC, ac, and hybrid. DC microgrids bring some advantages over their AC counterpart. For instance, the inductive voltage drop is removed in a DC system. But still, AC microgrid is more compatible with the nature of many DERs such as wind and electric motors load. These facts make it valuable to consider both AC and DC microgrids for research activities.

Sharing loads automatically between parallel resources in microgrids is an important aspect. A primary level control like the droop control solution can be used to share the power among parallel resources without any communication. Droop control is a simple approach that mostly applies to parallel DERs to ensure their stability. In AC systems, it generates the output reference voltage magnitude and voltage frequency of the DG units based on their reactive (Q–V) and active power (P–F) values and in DC systems, It functions by introducing virtual resistance in line to equalize current sharing or by controlling voltage magnitude based on active power (P–V).

This dissertation focuses on performance improvement of droop-controlled converters, mainly in the following three aspects: i) a novel Dual-Edge (DE) PWM suitable for DC/AC and DC/DC converters with reduced modulation delay, and a graphical-based analysis for its dynamic behavior, and its effect on output impedance and stability; ii) reduction of DC bus capacitance while maintaining tight DC bus voltage regulation in DC microgrids; iii) Per-Phase Power Controller in AC Microgrids with smooth transfer from the power flow control to droop control, allowing AC microgrids to seamlessly disconnect from upstream grids;

First: With rising environmental concerns, the installation of distributed generating systems creating microgrids in power systems has recently gained a lot of attention. This cure, however, is not without its own set of problems. Examples include the delay in digital control systems, grid impedance changes in weak grids, and the interaction between paralleled converters in a microgrid, which might risk the expected performance of microgrids. The smallest feasible delay in a control loop is crucial for optimizing the controller's bandwidth and achieving high robustness against grid impedance fluctuations, as well as eliminating negative virtual impedance and signal aliasing. In power electronics applications, the PWM module acts as the principal interface between the hardware and the controller. These modules will often have a delay; for example, a triangle carrier PWM will have a delay equal to half of the sampling frequency. To address this issue, a novel PWM approach known as DE-PWM is devised and implemented on a field-programmable gate array with a shorter modulation delay. The specifics including the generation of driving signals for power switches at various sampling frequencies within a switching cycle, small signal analysis, and its influence on output impedance, are presented.

Second: Having smaller DC bus capacitance in resource converters paralleled in DC microgrids, will provide better conditions considering the voltage surges and sags during load changes. A way to reduce the output capacitance is to use high bandwidth controllers like hysteresis or new PWM methods to eliminate the delay existing in normal PWM methods. This is because, given a certain output voltage tolerance band, a faster dynamic response controller will allow larger voltage dynamic variations, so that smaller output capacitance can be used. Herein, An over-sampled hysteresis modulation with resistive output impedance shape of droop-controlled boost converters in DC microgrids is implemented on digital signal processors and details like the effect of non-negligible computation time, are presented.

Third: When paralleled EPCs are operating islanded in microgrids, they should sustain the bus voltage by output power adaption using droop laws. In any case, microgrids can operate in two modes: isolated or connected to the upstream grid. When connected to the grid, EPCs should set the output power to a preset value to allow power control. It is also critical to provide seamless transition between the two operational modes. Remarkably, the use of the traditional droop control scheme for per-phase power control in AC systems would lead to unequal frequencies among the phase voltages, which is not acceptable. Per-phase power control is crucial for several services in modern smart power networks, like demand-response and distributed unbalance compensation. Here a droop-based controller for grid-tied three-phase inverters is presented. The controller allows regulating the inverter output power while operating grid-tied, to support the local grid voltage while operating islanded, and to seamlessly transition into this latter mode of operation. Instead, the proposed controller

allows independent power references tracking at each of the phases of a three-phase inverter while grid-tied and a proper transition into the islanded operation. The stability analysis of the whole control system and outlines a procedure for the design of the involved regulators, plus, simulation and experimental results considering a laboratory-scale prototype are reported and discussed to validate the proposed controller.

All of the above-mentioned proposals are verified by relevant experimental results performing on different laboratory-scale DC and AC microgrid prototypes. Imperix software and hardware's great flexibility for prototyping aided in the experimental validation of power converter control strategies discussed in the dissertation.

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Nomenclature

Acronyms / Abbreviations

AC Alternating Current

ADC Analog-to-digital Converter

BESS Battery Energy Storage System

VSI Current Source Inverter

DC Direct Current

DE Dual-edge

DEPWM Dual-Edge Pulse Width Modulation

DER Distributed Energy Resource

DF Describing Function

DFT Discrete Fourier Transform

DG Distributed Generation

DPWM Digital Pulse Width Modulation

DSP Digital Signal Processor

EMS Energy Management System

EPC Electronic Power Converter

FPGA Field Programmable Gate Array

FPU Floating Point Unit

DC Low Voltage Direct Current

MG Microgrid

DC Medium Voltage Direct Current

PCC Point of Common Coupling

PLL Phase Locked Loop

PR Proportional-Resonant

PWM Pulse Width Modulation

RHP Right Half Plane

S/H Sample And Hold

SEMS Smart Energy Management System

SISO Single-Input Single-Output

TTE Trailing-Triangular Edge

UPS Uninterrupted Power Supply

VRM Voltage Regulation Modules

VSI Voltage Source Inverter

Chapter 1

Introduction

This chapter deals with microgrids and gives a brief introduction to the background under three aspects: Microgrid Motivation, Microgrid Architecture and Microgrid Control. Finally, the challenges and goals of this dissertation are outlined.

1.1 Why Microgrids?

The world as a whole is on the path to fossil fuel depletion [11]. When this inevitable depletion is reached, which could be towards the end of this century, the electrical energy consumed by civilization will have to come from renewable resources, which means that the sophisticated on-demand electricity to which we have become accustomed will be lost [19]. Much research has already been done in the field of renewable energy. In particular, research on the potential of renewable energy in a particular location is urgently needed to promote the diffusion of renewable energy [6, 30, 93]. Studies such as [29, 67, 42] that look at large countries' renewable energy mix, remark the importance of renewable energy potential, and policy aspects that are urgently needed to inform renewable energy decisions [66, 80]. Apart from this, due to seasonal variations and intermittency characteristics of renewable energy,

Fig. 1.1 General scheme of a microgrid.

accurate forecasting of various renewable energy resources is crucial [5, 78]. Distributed generation systems have gained importance and renewable energy sources are taking an increasingly larger share of electricity generation [48]. This has promoted the deployment of renewable energy microgrids that support various hybrid energy configurations and energy storage systems [63, 107, 56].Among all renewable energy sources, photovoltaic is considered one of the most important renewable sources [28]. All mentioned advantages, as well as lower distribution losses and higher stability, will be possible in microgrids and the use of microgrid can effectively solve the problem of new energy consumption issues.

1.2 Types of Microgrids

Local sources, the upstream grid, and consumers are the key elements of a microgrid (shown in Fig. 1.1). Within a microgrid, these four types of entities are connected to one or more common power buses via power electronic converters. Depending on the type of common bus, microgrid architectures generally fall into three categories: Ac, dc and hybrid Hybrid (AC/DC) microgrids.

1.2.1 AC microgrids

An AC bus system connects the different energy producing sources and loads in an ac microgrid's network. AC microgrids are often made up of dispersed generating sources like renewables and traditional power generation sources like engine-based generators. These distributed generators are linked to an energy storage medium, such as a battery energy storage system (BESS), through an AC bus system. Solar panels, wind turbines, and other renewable sources provide DC output. Through power electronic-based converters, this output may be transformed to AC.

AC microgrid systems using renewable-based DG units have been explored and deployed in many nations, according to the literature. A lot of researchers have explored the viability of their operation. Smart energy management systems (SEMS) to maximize the microgrid's economic operation is provided in [88, 36]. [49] describes a preplanned switching and fault occurrence that leads to distribution subsystem islanding and the development of a microgrid. Furthermore, [38] address the parallel functioning of DG unit inverters without communication signals utilizing resistive output impedance. In [43], a review of control techniques is presented, along with a consideration of the issues that arise when the ESSs are integrated into AC microgrids. The authors also report on research of power converter management and protection techniques for grid-connected microgrid systems using renewable-based DG units

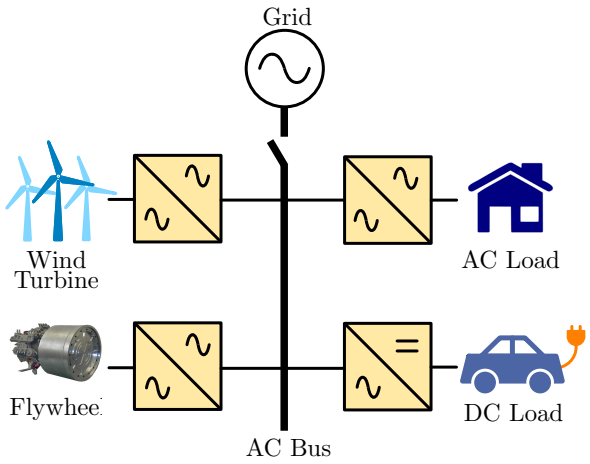


Fig. 1.2 An example of AC microgrid.

in [51, 8]. An example of an AC microgrid is the Sendai Microgrid 950kw in Japan, which combines 50 KW of solar energy with 700 KW of gas/diesel and 200 KW of fuel cell [33].

AC microgrids are adaptable due to their ability to link with standard utility grids or operate in islanded mode. They are also compatible with commonly used alternating current (AC) equipment such as motors and other alternating current-based loads that. Power protection systems are cost-effective in an AC system. Anyway, reduced conversion efficiency and the high cost of converters such as DC-AC converters are typical issues in AC systems. Controllability is challenging due to frequency, voltage regulation, and imbalance correction. Lower power supply reliability can stymie the performance of equipment that demands a high-performance power source, and transmission efficiency is lower than that of their DC counterparts.

AC microgrids are practical with both renewable and non-renewable energy sources, according to the literature reviewed above. They are used in a variety of settings, including distant places, commercial buildings, and as power supply backups, and they help to increase the efficiency and dependability of current power system infrastructure.

1.2.2 DC microgrids

DC microgrids work in a similar way to their AC equivalents. The fundamental distinction is that the DC bus network interconnects the dispersed generators and loads in the network, whereas the AC bus interconnects the distributed generators and loads in the network. The operating voltage of these DC buses is usually between 350 and 400 volts. To meet the low voltage needs for electronics-based loads, the primary DC bus can be split into multiple low voltage buses. By increasing low voltage power sources like solar modules (usually 20-45V)

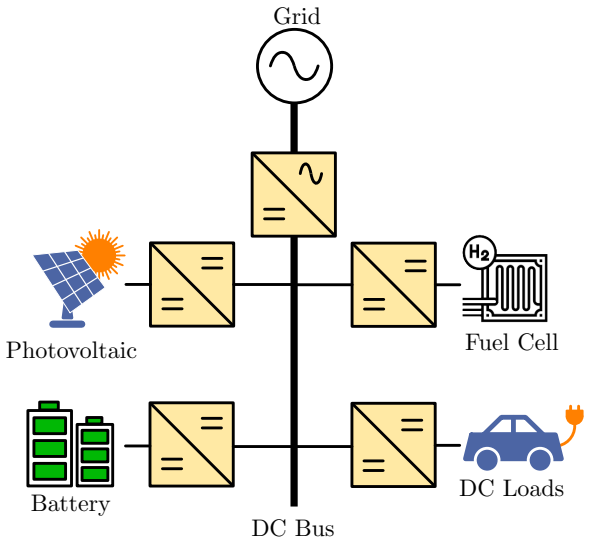


Fig. 1.3 An example of DC microgrid.

to the high voltage DC bus, high voltage gain DC-DC converters in DC-type microgrids enhance the practicality of connecting them to the high voltage DC bus. The amount of their voltage gain/power handling operation may be used to classify these converters.

Sweden and Japan have both built DC microgrid structures with a capacity of 5 MW. Both of these microgrids provide direct current (DC) electricity to data centers in their respective nations. Another example is a New Zealand DC microgrid, which likewise provides DC power to data centers but works at a 220-V LVDC level rather than the MVDC level used in prior examples. Sweden's DC microgrid runs at 380 V, but Japan's microgrid operates at 400 V [77].

Because of DC MGs superior conversion efficiency, they are an ideal solution for powering high-performance electrical devices. Aside from the cost reductions provided by renewable energy, lower-cost converter systems can provide further savings. Because there is no reactive current, the transmission efficiency is better, and the cabling is comparatively small owing to the high voltage at low amperage. The power supply is more reliable even in remote areas. It is significantly easier to control a system that does not produce problems such as synchronization, harmonics, reactive power management, and frequency control. Although, immature DC microgrid power protection systems might be an issue, particularly for sites with high electrical needs. Converting an existing AC system to DC adds complexity and cost. When there are no reactive power sources available, voltage drop issues are more likely, especially in larger systems. Lower AC load compatibility, proportional to the volume of AC-based loads, causes DC microgrids to be less well-known in the market.

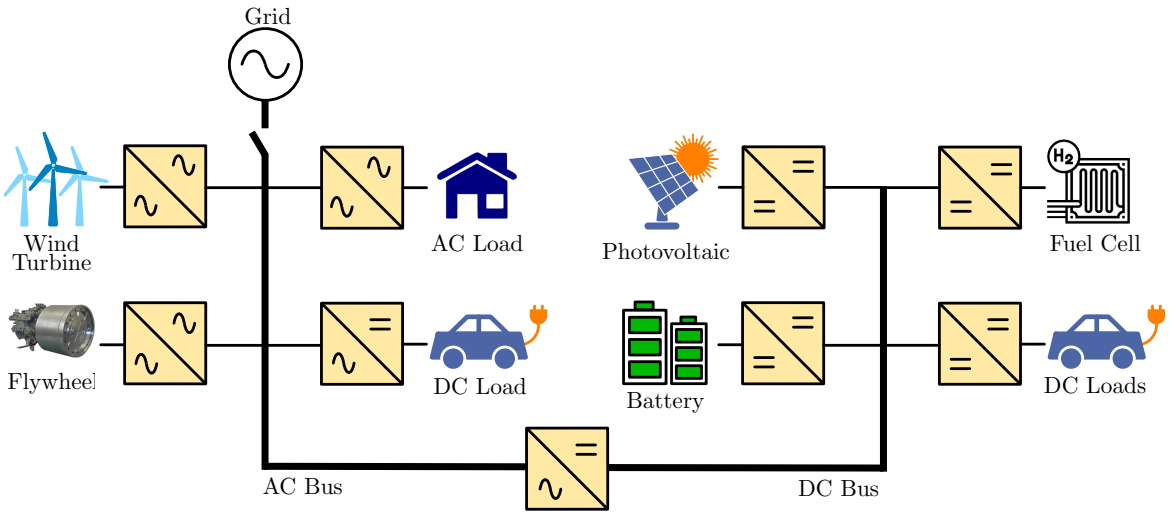


Fig. 1.4 An example of hybrid microgrid.

1.2.3 Hybrid microgrids

Hybrid microgrids are made up of both alternating current (AC) and direct current (DC) power distribution networks, as well as a microgrid central controller. The goals of building hybrid microgrids are to eliminate conversion stages, interface devices, boost dependability, and reduce energy expenditures, consequently enhancing the network's overall efficiency. A structure like this allows both alternating current and direct current power to be provided to a distribution network, while clients can utilize electricity as needed (AC or DC). power electronic converters are often in charge of decoupling the alternating current and direct current components of a microgrid [45, 99].

The Boeing 787's electrical system is an example of a hybrid AC/DC microgrid used to save weight and maintenance costs. A primary 230 V AC distribution system distributes power from six generators totaling 1450 kVA to three subsystems: a 115 V AC system, a 270 V DC system, and a 28 V DC system in this system [65]. Another example is the hybrid system erected on Graciosa Island, which combines a 4-MW battery storage system with wind, solar, and diesel power generating. Since its installation in November 2012, a 3-MW battery storage system has enabled grid operators to absorb 9 MW of wind energy while reducing diesel imports by 8 million gallons. When the wind does not blow for extended periods of time, diesel generators continue to meet demand [34].

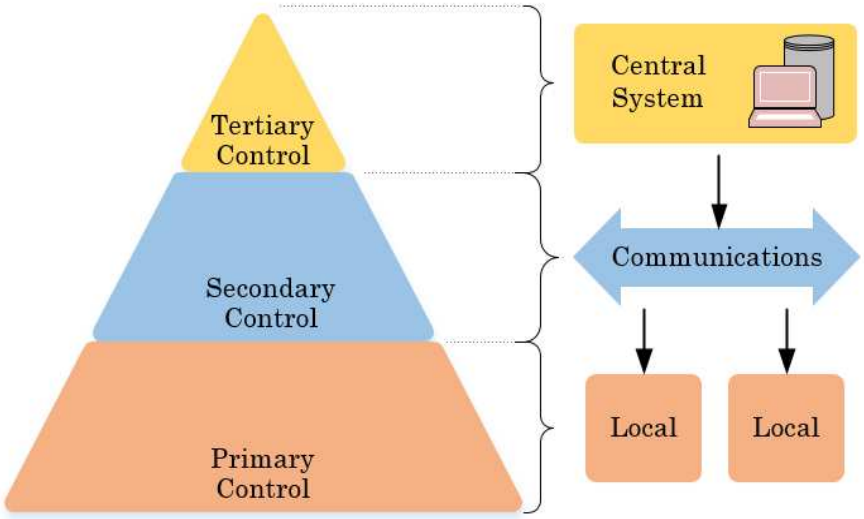


Fig. 1.5 Hierarchical layers of a microgrid control system [95].

1.3 Microgrid control layers

The most essential control objectives of the MG control system in a microgrid include DGs output voltage and current control, active and reactive power balancing and frequency (in AC or hybrid MGs) and voltage regulation. As well as demand-side management, economic dispatch, and transition between operating modes. Whereas in the grid-connected operating mode, the key problem is the interaction with the main grid, while dependability and control difficulties are more important in the islanded operation mode because to the low inertia of the MG [9]. The aforementioned objectives may be met using a hierarchical control scheme represented in Fig. 1.5 that consists of three control levels: primary, secondary, and tertiary. These control levels differ in terms of reaction time and infrastructure needs (e.g., communication requirements) [74].

1.3.1 Primary layer

The primary or local control level is concerned with the inner voltage and current control loops to control inverter outputs (which are sometimes overlooked in modeling analyses due to their speed of reaction), as well as frequency regulation in AC systems and power-sharing, which are referred to as primary control goals [25]. These themes are highlighted in the following sections.

Inverter output control

Due to their uses, inverters' output currents or output voltages must be adjusted in order to match certain reference wave forms. The control of electronically connected DER units in microgrids has received a lot of attention in technical literature. [74] provides an overview of grid-side converter controllers. In a wide range of switching inverter applications, the hysteresis approach is employed as controller. While the popular PWM technique requires a PI/PID regulator to modulate the error, which may result in an unavoidable delay [73], hysteresis current control has a fast dynamic response and does not require any information about the system parameters, which increases its robustness [50]. The deadbeat algorithm is another sort of control that is employed when a precisely determined and short period is required to attain the system's steady state. Dead-beat controllers are classified into two types: compensation controllers with no access to state variables and state controllers having access to state variables. Because of its ease of development, the first type of controller is commonly employed in SISO systems [53]. Another sort of controller is predictive control, which is dependent on the correctness of both the system model and the reference prediction.

To achieve zero steady-state error at fundamental frequency in AC systems or to regulate other frequencies than zero, a Proportional-Resonant (PR) controller is utilized instead of the traditional PI controller. Also, controllers based on the dq synchronous reference frame have been widely employed in the control of three-phase systems. The sinusoidal signals under control can be represented as DC values in an orthogonal dq frame, spinning synchronously at the observed grid fundamental frequency, using the Park transformation [16].

Power sharing control

After ensuring that the inverter output is controlled, the next stage is to regulate the inverter's power. For this reason, the droop technique is the most well-established option, initially described in [18] for use in AC systems. Active power in an inductive dominant distribution network is heavily reliant on the power angle, which is dynamically regulated by the frequency in droop control, while reactive power is mostly governed by the AC voltage. Similarly, in DC systems, the droop principle has been used successfully. Unlike with AC systems, the idea of "reactive power" does not apply, and only active power may be delivered. The DC voltage defines the amount of active power transmitted in the DC network. As a result, in DC systems, a comparable droop control may be developed by establishing a connection between active power and DC voltage and modifying the voltage to accomplish the appropriate load sharing. Load sharing can also be accomplished by incorporating a "virtual resistance" into the existing system [35]. The "virtual resistance" is an ideal value that is unaffected by its

working conditions, such as temperature, and produces no "real" power loss, but the "real resistance" is not a set number that may fluctuate with environmental circumstances and produces "real" power losses that should be minimized. Droop gain, droop constant, or droop coefficient are all names for this virtual resistance.

1.3.2 Secondary layer

The secondary control, as a communication-based solution for parallel construction of DGs, enables power sharing and adjusts for voltage and frequency variations caused by load fluctuation and local control operation. In order to isolate the dynamics and make the design of the control settings easier, the secondary layer often functions at a slower reaction speed than the primary layer. Other auxiliary control objectives, such as voltage profile adjustment, reactive power sharing, and voltage imbalance removal at PCC, can be accomplished at the secondary layer. Secondary control layer techniques are often classed based on the communication system's topology (or absence of) [37, 44].

1.3.3 Tertiary layer

The tertiary layer, also known as the Central/Emergency Control layer, is responsible for power dispatching and aims to optimize it in terms of cost and efficiency. Because of the nature of the controlled variables, the process can be performed in time increments of many seconds or minutes [3]. It plays an especially essential function in the islanded operating mode. It functions as an MG energy management system (EMS), monitoring the MG's local and secondary controllers. It is also in charge of detecting islanding and connecting/disconnecting from the main grid, as well as emergency control and general protection programs [91].

1.4 Challenges and Research Objectives

In this chapter, microgrids are investigated from a variety of angles, including architecture and control, to offer readers a comprehensive view. Because primary control maintains the fundamental operation of converters in DC and AC microgrids, having well-designed primary control is crucial to assuring the stable operation of whole microgrids. This dissertation investigates several aspects of primary control for power converters in DC and AC microgrids, with a focus on droop control.

1.4.1 The delay introduced by the PWM module

Challenge: The employment of a digital signal processor to implement the controllers will cause a delay in completing the waveform measurement and calculating the references. Because of the fast clock rate and short sample duration, it is often assumed that these delays have no effect on the compensation process's effectiveness. Anyway, the references, or control signals, require PWM technique to be introduced to the switches in order to control the hardware, and this PWM technology will also create extra delays. This delay will result in non-ideal compensation, which implies that the system's ability to adapt for dynamic changes will be compromised (where the reference is deliberately delayed and the output won't be in phase with desirable reference [55]). Above the cross-over frequency of an inner control loop, these delays also may cause harmonic instability [98].

Objective: Examining the dynamic behavior and small signal models of the DE-DPWM graphically, as well as synchronism correction techniques, to reduce modulation delay and its effect on stability.

1.4.2 Reduction of DC bus capacitance in DC microgrids

Challenge: Saving money, increasing power density, and decreasing short-circuit fault current are all advantages of having a smaller output capacitance for each DER DC-DC converter in a DC microgrid. However, in DC microgrids, a certain value of capacitor on the DC bus is required to supply transient power and stabilize the DC bus voltage. As a result, the DC bus capacitance is designed to be as low as feasible while maintaining an acceptable DC bus voltage throughout the transient.

Objective: Improving the design of droop control for high-band DC-DC power converters using hysteresis controllers, such that their output capacitance may be lowered while the output voltage remains within the tolerance band during load changes.

1.4.3 Per-phase power controller in AC microgrids

Challenge: Per-phase power regulation is critical for a variety of services in advanced smart power networks, including demand response and distributed imbalance compensation. However, in islanded operating mode, using the typical droop control approach for per-phase power regulation would result in uneven frequencies among the phase voltages, which is unacceptable. In addition, the inverter controller should be able to regulate the inverter output

power while it is grid-tied, and as mentioned support the local grid voltage when it is islanded, and seamlessly transition into this latter mode of operation.

Objective: Develop a controller that allows independent power reference tracking for each phase of a three-phase inverter when grid-tied, as well as a smooth transition into islanded operation, and supports the local grid voltage while islanded under droop laws.

1.5 Dissertation Outline

Chapter 2 proposes a simplified graphical analysis approach for modeling the small-signal behavior of DPWM implemented with a double-edge carrier. This graphical technique has the benefit of being relatively simple and allowing for instant physical interpretation of the produced data. The results show that the DE-DPWM can significantly enhance the closed-loop phase margin. This improvement is most noticeable in the *double-update* operation, when the modulator has almost no phase delay.

Chapter 3 describes an extension of digital hysteresis modulation for droop controlled DER converters in DC microgrids. The major goal is to shape the output converter impedance such that it is practically resistive within the controller bandwidth, without amplification of the output impedance over the whole frequency range. This is also accomplished with a very low output capacitor, because the suggested digital hysteresis technique provides fast dynamic response by avoiding any inherent delay of the PWM modulator and shows an inherent derivative action.

Chapter 4 proposes and experimentally evaluates a controller for three-phase four-wire inverters capable of *i*) independent output power control for each phase while operating grid-connected, *ii*) smooth transitions into the islanded operation, *iii*) operation in islanded conditions even when multiple parallel connected converters integrating the proposed controller are present.

Chapter 5 highlights the key findings of the research.

Chapter 2

A Dual-Edge Modulator for High-Switching Frequency Power Converters

2.1 Introduction

Conventional DPWM architecture exhibits non-negligible time-delays that can deteriorate the closed-loop performance of such power systems. Recent research efforts have been devoted to the development of new control strategies capable of reducing these delays and improving the performance of the controlled systems. One of the most remarkable solutions is the Dual-Edge PWM [81]. This PWM architecture can improve the overall dynamic performance of the controlled systems. Indeed, its small-signal frequency exhibits a phase-boost action, allowing the design of robust, wide-bandwidth control loops, while it reduces the large-signal delay over conventional solutions. In its digital implementation, it does not introduce any phase-boost action but reduces the modulation delay that is normally associated with conventional DPWM schemes. The analog DEPWM has been exhaustively and rigorously analyzed in [81]. However, the small-signal behavior of its digital implementation has yet to be analytically proven.

This chapter proposes a *graphical-based* approach to analyze the dynamic behavior of the DE-DPWM. As a further contribution, two effective synchronism correction strategies are developed. As a common practical case, a multi-loop output voltage control of a single-phase VSI is used to show the achievable advantages, resulting from the use of this architecture. The chosen case study is one of the most popular dc-ac topologies used in various applications like UPS. Moreover, the VSI is utilized to emulate an ac grid to supply other ac loads to show

the quality of its ac output voltage during transients and/or in presence of non-linear loads. The dynamic performance and the quality of the ac output voltage are strongly dependent on the chosen control strategy. Several fast dynamic control solutions have been proposed to shorten the transient period and to effectively reduce the distortions on the output voltage.

The easiest way to obtain a low distortion sinusoidal load voltage, requires a sine pulse width modulation scheme [106, 10]. Unfortunately, even this approach performs well with linear loads, not with non-linear. One of the most popular solutions to improve the dynamic performance that provides a low voltage distortion is the multi-loop control approach [92, 1]. This is a rather large field of research and countless solutions can be adopted. Some of the control strategies that ensure low output voltage distortion and excellent dynamic response are listed here: digital predictive controllers [14, 20], controllers that involve hysteric-based modulator [21, 87] and over-sampling DPWM based techniques [22, 76].

In principle, predictive controls allow for dead-beat control. Using them to implement the inner-current control loop can lead to advantages in terms of bandwidth available for the outer-voltage control loop. The main disadvantage of this approach is the high sensitivity to changes in controlled system parameters. Indeed, such controllers work by implementing control equations that generally depend on the parameters of the converter. Therefore, they are inherently more sensitive to changes in the latter. Hysteresis control techniques [4] provide very good performance in terms of dynamics. They are variable switching-frequency controls and can present stability problems depending on the nature of the loads. Finally, control techniques based on oversampled DPWM can also be extended to the DE-DPWM case. In this chapter, it is shown how it is possible to obtain advantages on the converter dynamic, by modifying the structure of the DPWM passing from the most common TTE based implementation of the proposed one.

2.1.1 Outline

The basic structure and operation of the DE-DPWM are discussed in Sect. 2.2. Since this is a variable switching frequency system, a synchronization mechanism to ensure proper sample acquisition is necessary. For this purpose, two synchronism corrections are presented in Sect. 2.3. Sect. 2.4 details the proposed graphical-based analysis technique. Sect. 2.6 will show the effect of this modulator on the output imprudence. Sect. 2.5 and Sect. 2.7 are related to simulation validation and experimental testing.

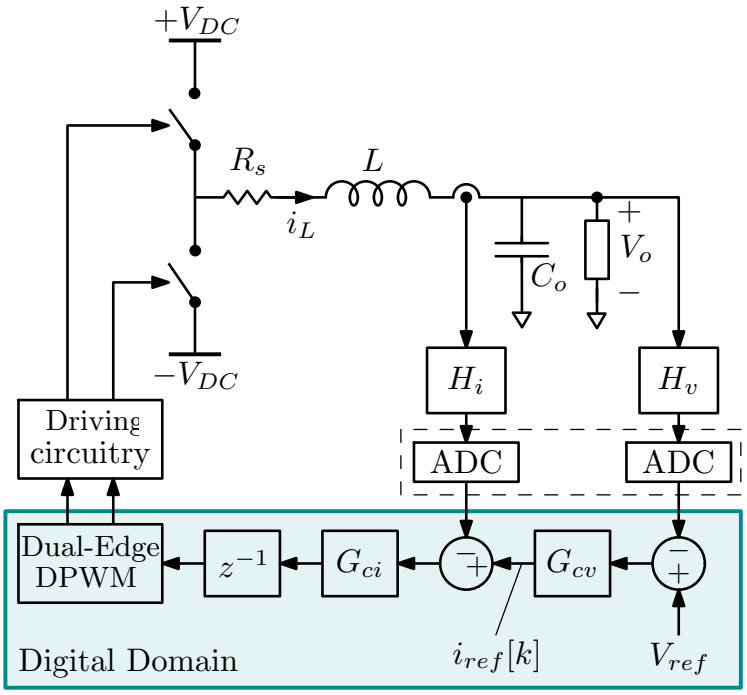


Fig. 2.1 Multi-loop output voltage control based on digital dual-edge PWM for single-phase VSI.

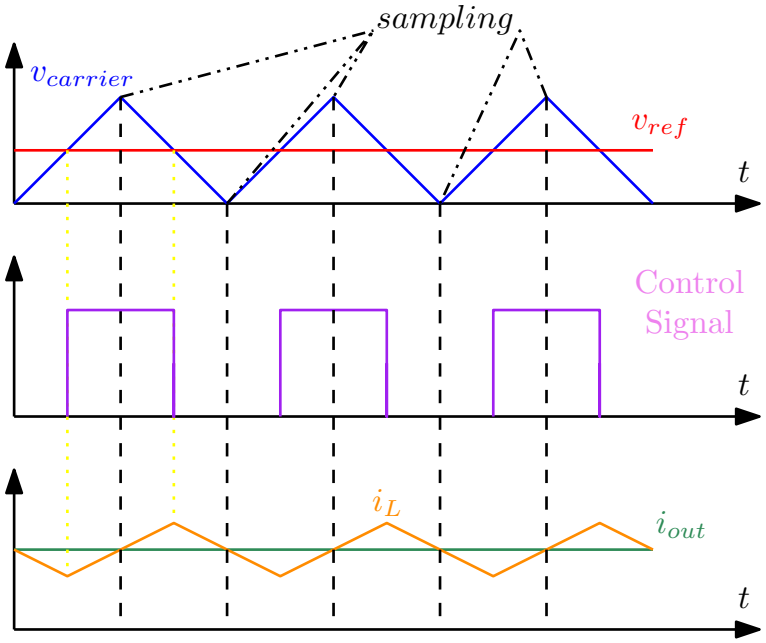


Fig. 2.2 Generic triangle wave carrier PWM architecture.

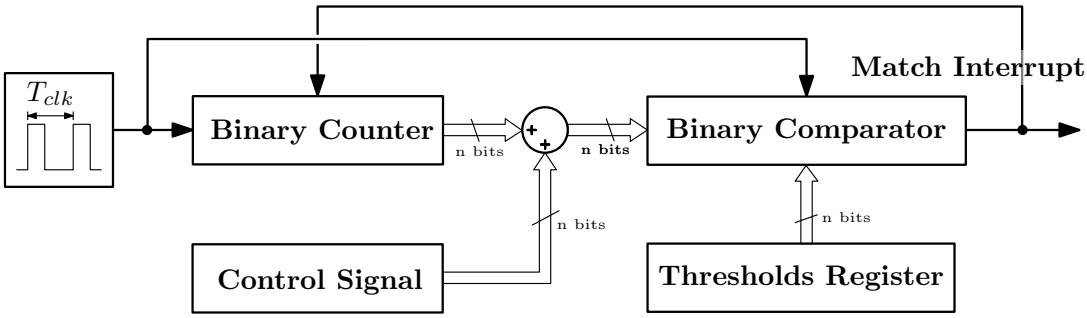


Fig. 2.3 Generic DE-DPWM architecture.

2.2 Digital Dual-Edge Modulator

Fig. 2.1 shows the single-phase VSI case study, where the performance of the DE-based DPWM modulator is analyzed and compared to the TTE based DPWM modulator. The analog dual-edge modulator is analyzed in [81], showing a leading phase in the high-frequency range. Here, the describing function approach is used to formally prove the modulator frequency response. The application of its digital version needs to address two main issues:

- determination of the sampling and control update instants.
- synchronisation with an external clock, usually needed when a three-phase system is adopted.

The DE-DPWM is analyzed concerning the chosen case study: *multi-loop output voltage and average inductor current-mode control in a single-phase VSI*. The comparison with a TTE based DPWM is fundamental since its implementation is simple, it naturally offers the sampling instant for the average current (Fig. 2.2), and it is widely used in many microcontrollers and DSPs. Indeed, the TTE modulator naturally provides the instants at the middle of switch turn-on and turn-off, i.e. the instants for sampling the average currents, being directly the minimum and the maximum of the triangular carrier. As is well-known, both single sampling, (i.e. sampling and control updating once per switching period), and double sampling digital modulators, are widely adopted. As shown in Fig. 2.3, this synchronism between average current and DE carrier is not naturally present unless specific provisions are used.

2.2.1 Organization and operation

A generic DE-DPWM implementation is shown on Fig. 2.3. The control signal is summed to the ramp generated by a binary counter clocked at frequency $f_{clk} = 1/T_{clk}$. When this sum is

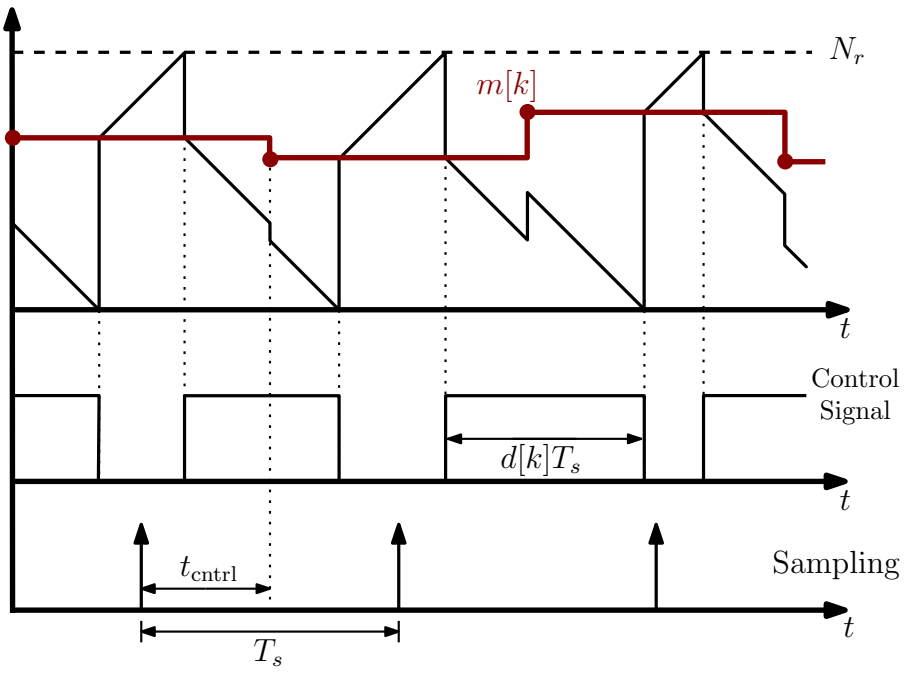


Fig. 2.4 Digital Dual-Edge waveforms with no synchronism correction

equal to the threshold value N_r (is presented in Fig. 2.4), the binary comparator generates the *match interrupt*. The match interrupt changes the gate signal level, resets the counter, and changes the sign of the counter. This generic implementation algorithm is used as a simple example to explain the proposed synchronization strategy.

The switching period T_s, in steady-state conditions, can be written as:

$$T_s = T_{clk} N_r, \tag{2.1}$$

while the duty cycle resolution q_D, (i.e. the smallest duty cycle variation), is:

$$q_D = \frac{1}{N_r}. \tag{2.2}$$

It is worth mentioning that the DE modulator exhibits constant switching frequency in steady-state conditions, while it is naturally variable under transients and synchronization. The next section describes the synchronism correction strategy between modulating signal and sampling instants.

2.3 Synchronism Correction

While the TTE based DPWM inherently allows to sample the average value of the inductor current and provide a post-sampling spectrum free from any high-frequency switching components (discussed in Sect. 2.2), in the DE based DPWM there is no reason why sampling events should always happen in the middle of the ON or the OFF phase. The sampling events are locked on turn-on rising edge with a delay to have them at $\frac{t_{off}}{2}$ or $\frac{t_{on}}{2}$, but this synchronization will be wasted due to load transients. To explain the proposed synchronization method, the *i*-th *synchronization-time error* is defined as the time difference between the sampling instant and the half of the on-phase. A simple method to compute this error is to count the number k of clock periods between the turn-on and the sampling event. Therefore, the synchronization-time error can be written as follows:

$$\varepsilon_s = t_{count} - \frac{dT_s}{2}, \tag{2.3}$$

being $t_{count} = kT_{clk}$.

This error can be used to vary the switching frequency slightly so that after a certain number of modulation periods, the error will be zero and as result, samplings will happen in the middle of the ON or the OFF phase. This control acts like a PLL control. In this chapter, two strategies are presented to modulate the switching frequency for the synchronization: the *threshold modulation* and the *slope modulation*.

2.3.1 Thresholds modulation

To translate the synchronization error into a switching frequency variation, one solution is to change threshold values in a weighted way, so that the duty cycle of the modified period remains constant during the synchronization. Precisely, for the *i*-th modulation cycle, the modified switching period $T_s'[i]$, on-time, and off-time can be presented as:

$$\begin{aligned} T_s &\rightarrow T_s'[i] = T_s + \varepsilon_s[i] \\ t_{on} &\rightarrow t_{on}'[i] = dT_s'[i] \\ t_{off} &\rightarrow t_{off}'[i] = (1-d)T_s'[i]. \end{aligned} \tag{2.4}$$

The described synchronism correction is exemplified in Fig.2.5.

In steady-state conditions, the upper threshold value $N_H[i]$ is equal to N_r and the lower threshold $N_L[i] = 0$. To perform the synchronization, this values will vary based on (2.4),

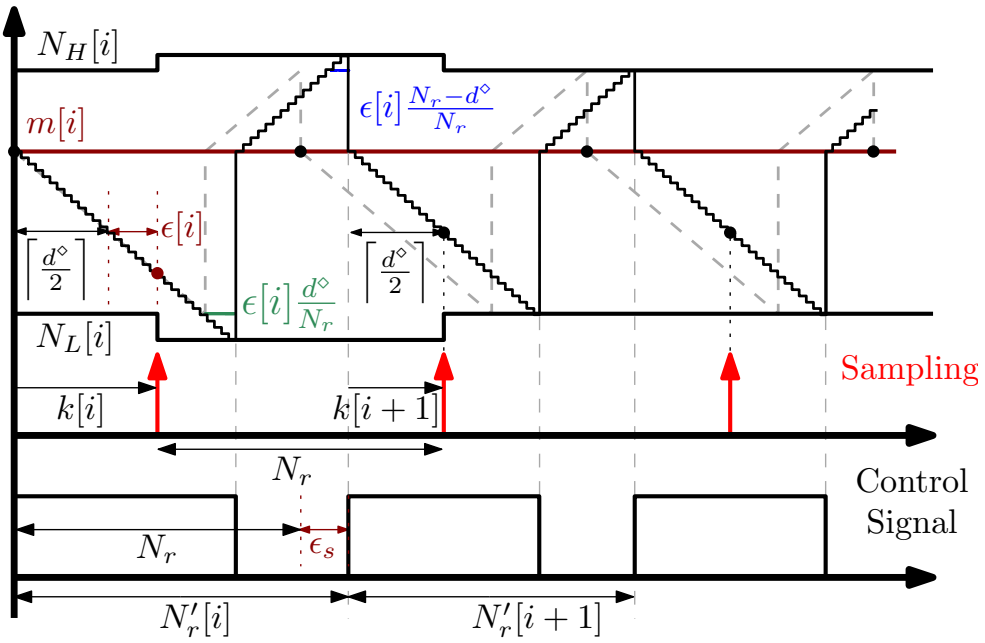


Fig. 2.5 Steady-state operation of the DE modulator with thresholds modulation synchronism correction.

explained in the following:

$$N_H[i] \triangleq N_r + \Delta N_H[i] \quad \text{and} \quad N_L[i] \triangleq \Delta N_L[i], \tag{2.5}$$

where $\Delta N_H[i]$ and $\Delta N_L[i]$ are the numerical threshold corrections at the i-th modulating cycle. The synchronization-time error defined in (2.3) can be represented in the numerical domain as:

$$\varepsilon[i] = k[i] - \left\lceil \frac{d^\diamond}{2} \right\rceil, \tag{2.6}$$

where $k[i]$ is the number of clock periods between the turn-on and the sampling event at the i-th modulation cycle and $d^\diamond$ is the numerical representation of the duty cycle. Threshold correction in (2.5) can be expressed as a function of the synchronization-time error:

$$\Delta N_L[i] = -\left\lceil \varepsilon[i]\frac{d^\diamond}{N_r} \right\rceil \quad \text{and} \quad \Delta N_H[i] = \left\lceil \varepsilon[i]\frac{N_r - d^\diamond}{N_r} \right\rceil. \tag{2.7}$$

Finally, the modified numerical threshold $N'_r[i]$ is given by:

$$N'_r[i] = N_H[i] - N_L[i] = N_r + \varepsilon[i] = N_r + k[i] - \left\lceil \frac{d^\diamond}{2} \right\rceil. \tag{2.8}$$

Therefore, the resulting switching period $T_s'[i]$ corresponding to the i-th modulation cycle is given by:

$$T_s'[i] = T_{clk}\left(N_r + k[i] - \left\lceil d\frac{N_r}{2}\right\rceil\right). \tag{2.9}$$

Quantization error

The described synchronism correction strategy results in a duty cycle resolution loss. This is due to the numerical space that is needed to change thresholds values. For instance, if the digital system operates with n bits, the positive integer full-scale [0 to $(2^{(n-1)}-1)$] cannot be used to describe the duty cycle in the digital domain. Indeed, the synchronization error (2.3) needs a margin to be applied. In other words, by indicating the maximum positive synchronization error as: $\varepsilon_{s_{MAX}}$, N_r must satisfy the following inequality:

$$N_r + \left\lceil \frac{\varepsilon_{s_{MAX}}}{T_{clk}} \right\rceil \leq 2^{(n-1)} - 1. \tag{2.10}$$

Therefore, if q_D in equation (2.2) increases, the duty cycle resolution will decrease. However, the following clarification must be noted, generally, the resolution loss is small enough not to be significant, since the synchronism control is normally programmed to correct synchronization error in several modulation periods. Thus, only small threshold variations are required, even in the presence of large control signal transients. One simple solution requires dividing the error by 4, which implies that in each modulation period only half of the measured error is corrected. By doing so, after m complete modulation periods, synchronization error will be:

$$\varepsilon_s[i+m] = \varepsilon_s[i]/4^m \tag{2.11}$$

Fig. 2.6 shows the synchronism correction operation, starting from a not synchronized condition. With the synchronization-time error divided by a factor of 4. the synchronized condition is achieved after around 7 switching periods by decreasing the frequency value.

The described synchronism correction has to be synchronous with the sampling clock and also requires the control signal value as inputs in order to compute new values N_L and N_H. With reference to the generic implementation in Fig. 2.3, the illustrated synchronization mechanism can be therefore summarized as in Fig. 2.7.

2.3.2 Slope modulation

A valid alternative to the synchronization mechanism presented in the previous section can be obtained with a weighted variation of DE carrier slopes. This method allows modulating

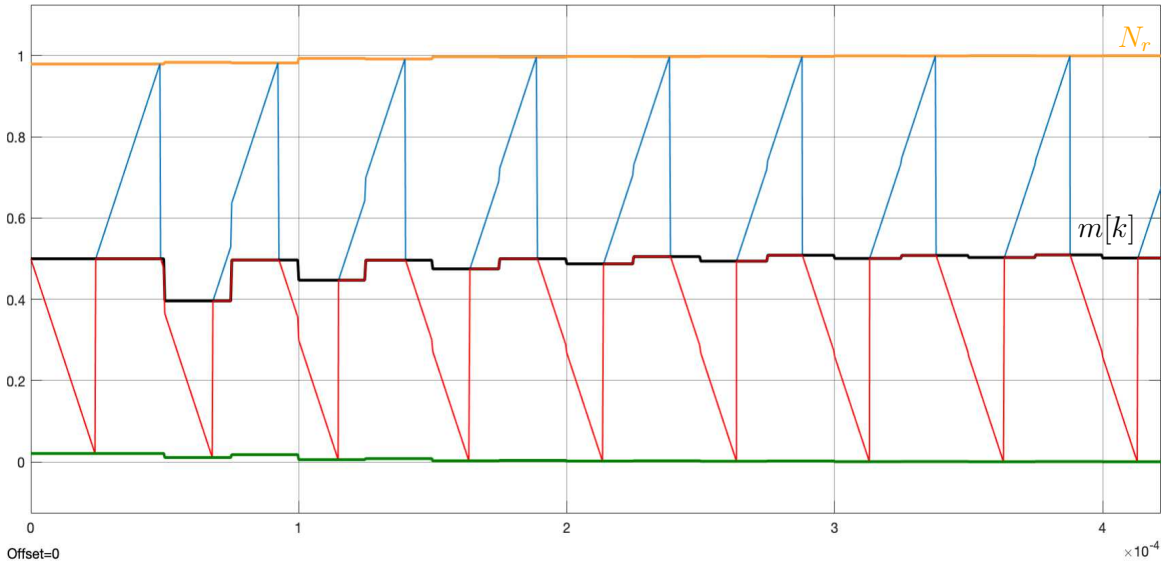


Fig. 2.6 DE-PWM Synchronism correction acting from a not synchronized condition.

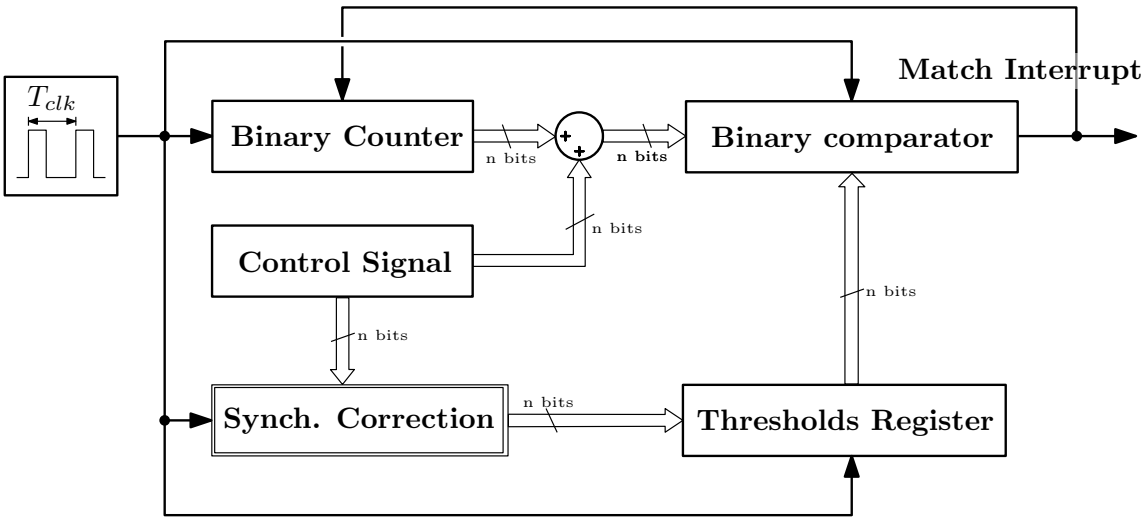


Fig. 2.7 Generic DE-DPWM architecture with the proposed thresholds modulation synchronism correction.

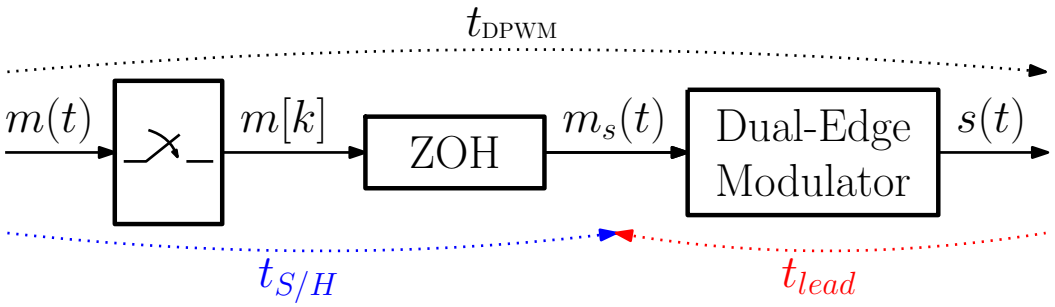


Fig. 2.8 Simplified block-diagram model of the Digital Dual-Edge PWM

the switching frequency without changing the duty cycle of the DPWM output signal. The slope modulation is a valid and straightforward alternative to the threshold modulation in the analog implementation. In digital systems, ramps are usually implemented by a binary counter which is a digital integrator with a certain integration step that is quite often equal to 1. To change the slope of a digital ramp, this integration step has to be changed. For example, one could use an integration step equal to the generic value $\nu > 1$ and then decrease or increase this step-in order to have the required variation. Since ν can only take integer values, fractional integration steps can be emulated by varying ν between two integer values across the required value. Clearly in doing so there would be a loss of resolution similar to that discussed in the previous case. In any case this strategy while being implementable in digital systems is certainly less intuitive and a bit more complex than the *thresholds modulation* strategy. This *slope modulation* approach is here introduced for completeness only and will not be further considered in this chapter.

2.4 Small-Signal Analysis

The frequency response of the proposed DE carrier-based modulator can be formally derived with the rigorous *Describing Function* approach as in [81] for the original analog counterpart. In this chapter an approximated but simpler approach is used.

To derive the small-signal model of the DE carrier-based DPWM, the general block diagram of a uniformly sampled PWM, sketched in Fig. 2.8, is used as a reference. The time delay associated with the S/H block can be generically referred as:

$$t_{S/H,N} = \frac{T_s}{2N} \tag{2.12}$$

where N is the number of samples per switching period. Moreover, the modulator transfer function is going to be easier to obtain when the input signal is a piecewise type of signal with

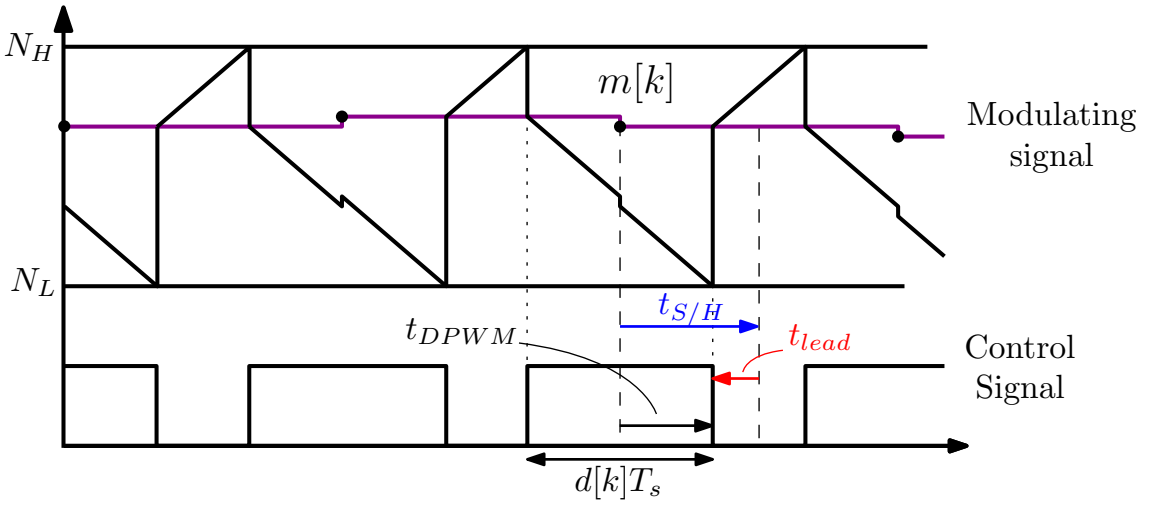


Fig. 2.9 Single update operation of a digital Dual-Edge PWM

precise instants of duty cycle update. Depending on where the modulating signal updates and on the number of updates per period, the small-signal transfer function changes, for this reason, the following cases are studied separately.

2.4.1 Single-update small-signal model

In single-update mode, the ADC samples the state variable (i.e., the inductor current) once per switching cycle. The sample is taken in the middle of the on (or off) phase. The single-sampling operation of the DE modulator is exemplified in Fig. 2.9. Referring to Fig. 2.8, the modulation delay t_{DPWM} for the *single-update* operation can be defined as the time distance between the i) sampling instant of the modulating signal $m(t)$ and ii) the instant where the duty cycle value of the modulator output signal is determined (i.e. the overall modulation delay is the time distance between the update of the control signal $m[k]$ and the turn-off edge of the gate signal shown in Fig. 2.9).

The modulation delay t_{DPWM} is shorter than the delay produced by the S/H unit equal to $T_s/2$, this phenomenon is due to the lead introduced by the Dual-Edge modulator with respect to the piecewise control signal $m_s(t)$. The lead introduced by the Dual-Edge modulator is equal to t_{lead}. Since the modulator is operating with the synchronization correction, the update instant is happening at $t_{on}/2$, which means that:

$$t_{DPWM} = \frac{t_{on}}{2}. \tag{2.13}$$

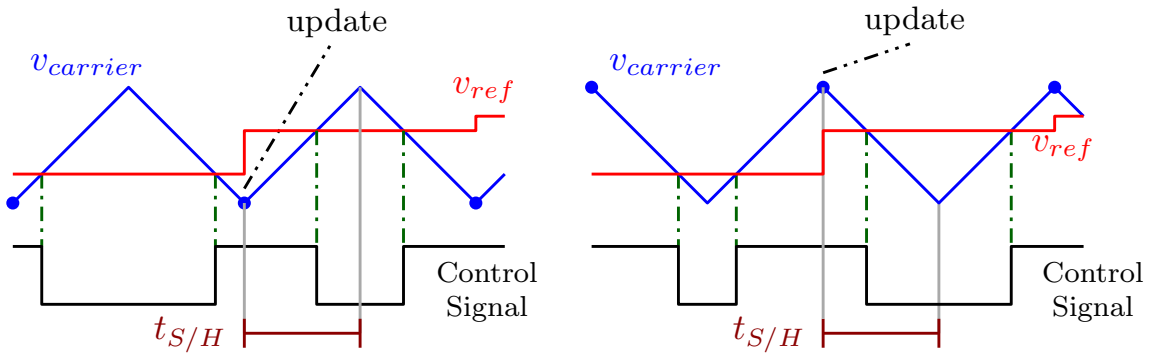


Fig. 2.10 TTE-DPWM delay for the single update at the valley (left) or the peak (right).

The time-lead introduced by the DE modulator is:

$$t_{lead} = t_{S/H,1} - t_{DPWM} = \frac{t_{off}}{2}. \tag{2.14}$$

Finally, the *single-update* DE-DPWM behaves as a system that introduces only a time-delay (introduced in (2.13)):

$$G_{DE_{single}}(s) \approx e^{-s\frac{t_{on}}{2}} \tag{2.15}$$

(2.15) shows that the DE-DPWM operating in single-update mode does not introduce a constant time delay and its transfer function depends on the operating point.

Note that applying the same methodology to the TTE carrier-based digital modulator, operating in *single-update*, results in a delay of $\frac{T_s}{2}$ that is equal to the S/H delay. Fig. 2.10 shows the modulating signal is generally updated on the peak (or on the valley) of the TTE carrier, and the final value of the pulse duration is completely known at the valley (or at the peak) of the carrier. Therefore, the delay for TTE-DPWM is equal to:

$$G_{TTE_{single}}(s) \approx e^{-s\frac{T_s}{2}} \tag{2.16}$$

By considering (2.15) and (2.16), it is clear that for a duty cycle close to 1 the time delay of the DE-DPWM is close to $\frac{T_s}{2}$, with no advantage with respect to the easier TTE based architecture.

Adaptive sampling

The DE-DPWM operating in single update mode has a good dynamic response for duty cycles less than 0.5. However, the advantages of this solution seem to be lost when the duty cycle exceeds the value of 0.5. This issue can be solved with the simple solution proposed here.

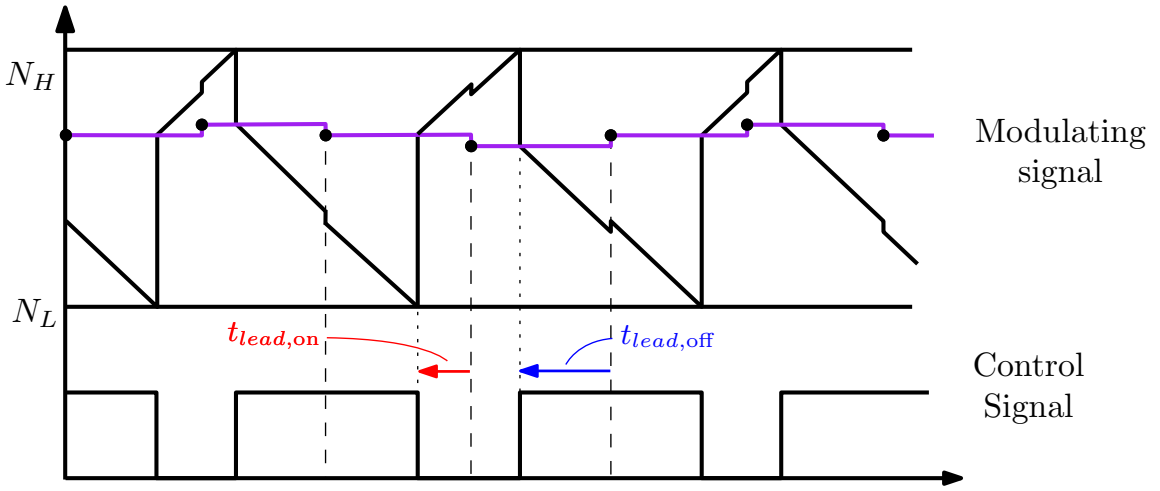


Fig. 2.11 Double update operation of a digital Dual-Edge PWM

The *adaptive sampling* technique moves the sampling instant in the middle of the on-time for duty cycles greater than 0.5, so that the updates happen at $\frac{t_{off}}{2}$ and the time delay is $t_{DPWM} = \frac{t_{off}}{2}$. By combining this with (2.15) the final small-signal transfer function for the single update DE-DPWM can be written as follows:

$$G_{DE_{single}}(s) \approx \begin{cases} e^{-s\frac{t_{on}}{2}} & \text{for } d \leq 0.5 \\ e^{-s\frac{t_{off}}{2}} & \text{for } d > 0.5 \end{cases} \tag{2.17}$$

The worst case is for $d = 0.5$, where $t_{DPWM} = \frac{T_s}{4}$. Of course, implementing this solution brings more complexity in synchronization, and also, frequency variation in ac systems at every zero crossing.

2.4.2 Double-update small-signal model

By sampling in the middle of both on time and off time during each switching period, the double-update mode is obtained. Thanks to the higher sampling rate, any transient on the state variables can be detected earlier, resulting in a faster response.

The DE modulator introduces a small-signal phase lead concerning the sampled control signal. For this double-update mode, in each switching cycle, two different *single-update* modulation leads can be measured: i) the on-time update and ii) the off-time update. The average between these two lead times is used to calculate the overall *double-update* modulation lead:

$$t_{lead} = \frac{1}{2}\left(t_{lead,off} + t_{lead,on}\right) = \frac{1}{2}\left(\frac{t_{on}}{2} + \frac{t_{off}}{2}\right) = \frac{T_s}{4}. \tag{2.18}$$

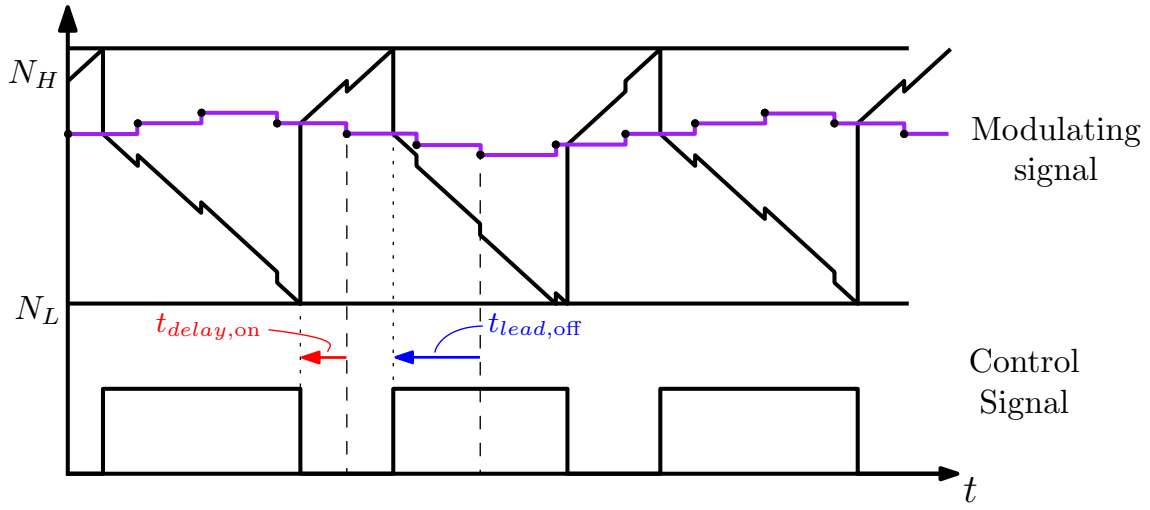


Fig. 2.12 Over-sampling operation of a digital Dual-Edge PWM.

Using (2.12) for the double update mode, the time delay associated with the S/H block is equal to $\frac{T_s}{4}$. This time is equal to the overall double-update modulation leading time t_{lead} in (2.18). by considering the mentioned facts, it is clear that the digital Dual-Edge modulator operating in *double-update*, introduces *zero* modulation delay, and the small-signal dynamic behavior remains constant for all operating points.

$$G_{DE_{double}}(s) \approx 1 \tag{2.19}$$

2.4.3 Oversampling small-signal model

From (2.12), oversampling is an efficient solution to mitigate the intrinsic delay introduced by the conventional DPWM. However, it remains to be understood whether there are any advantages in applying the oversampling approach to the DE-DPWM.

Fig. 2.12 shows the operation of the *over-sampling* DE-DPWM with $N = 4$. Using a similar methodology as used for the double-update case, modulation leads can be attributed at each update instant of *single-updates* and then perform a mean for all contributes to get the total modulation lead. Using Fig. 2.12 as a reference, there are one update during the t_{off} and 3 updates during the t_{on} for $d > 0.5$ and the contrary when $d < 0.5$. The update of the duty cycle during the off-time happens at $\frac{t_{off}}{2}$ thanks to proposed synchronism control. Therefore, the *single-update* time lead is:

$$t_{lead,off} = \frac{t_{on}}{2}. \tag{2.20}$$

For the three updates during the on-time, one update will happen in the middle of the on-time (i.e. at $\frac{t_{on}}{2}$), and the other two are symmetrically arranged. The mean value of these two is exactly $\frac{t_{on}}{2}$. Therefore, the time lead associated with this case has a weight equal to 3. the *single-update* time lead for on-time is:

$$t_{lead,on} = \frac{t_{off}}{2}. \tag{2.21}$$

The overall time lead is obtained by performing the mean of the 4 contributes:

$$t_{lead} = \frac{3.t_{lead,on} + t_{lead,off}}{4} \tag{2.22}$$

Thus, for the generic duty cycle:

$$t_{lead} = \begin{cases} \frac{T_s}{8} + \frac{t_{off}}{4} & \text{if } d > 0.5 \\ \frac{T_s}{8} + \frac{t_{on}}{4} & \text{if } d < 0.5 \end{cases} \tag{2.23}$$

Once again, to obtain the actual modulation delay, the time difference between the oversampled S/H (i.e., (2.12) for $N = 4$), and overall modulation lead in (2.23) is used:

$$t_{DPWM} = t_{S/H,4} - t_{lead} = \begin{cases} -\frac{t_{off}}{4} & \text{if } d > 0.5 \\ -\frac{t_{on}}{4} & \text{if } d < 0.5 \end{cases} \tag{2.24}$$

In DE-DPWM operating in oversampling mode, the modulation delay is negative, or in other words, the modulation exhibits a *phase-lead action*. For duty cycle $d = 0.5$ the time lead is $T_s/8$, but, as the duty cycle gets closer to 1 or 0, the lead drops to 0 with no small-signal improvement compared to the double-update operation.

2.4.4 Analog small-signal model

To further validate of the proposed *graphical-based* methodology, the continuous-time analog case is now briefly discussed. Results obtained with the proposed analysis are compared with the model developed in [81] through DF approach. Starting from the oversampling case, the analog case can be obtained by raising the number of samples per period to infinite.

A mean of the infinite contributes belonging to the on and off leading time are performed. The computation of these yields intuitively to:

$$t_{lead,on} = \frac{t_{off}}{2} \quad \text{and} \quad t_{lead,off} = \frac{t_{on}}{2} \tag{2.25}$$

To obtain the overall time lead weighted mean of $t_{lead,\text{on}}$ and $t_{lead,\text{off}}$ has to perform as:

$$t_{lead} = (1-d)\, t_{lead,off} + d\, t_{lead,on}. \tag{2.26}$$

The idea behind the assignment of the weights is that $(1-d)$ of all the infinite updates happen during the off-time and d during the on-time. As the S/H time delay for infinite sampling is equal to zero, the *continuous time modulation delay* is:

$$t_{DPWM} = t_{S/H,inf} - t_{lead} = -t_{lead} = -T_s(1-d)d \tag{2.27}$$

Therefore, the analog DE modulator transfer function can be written as:

$$G_{DE}(s) \approx e^{sT_s(1-d)d}. \tag{2.28}$$

Similar to the oversampling case, the modulation delay has a negative sign, which means that the modulator introduces a phase-lead action.

2.5 Simulation Validation

In this section, the DE-DPWM small-signal models obtained with the proposed analysis are compared with models simulated in MatLab/Simulink® environment. Before discussing results, the following lines summarize the procedure used to measure the frequency responses from simulations.

2.5.1 Frequency response measurement

In steady-state operation, with a constant input modulating signal M, the modulator output $s_{\text{steady}}(t)$ is a square wave having the duty cycle equal to:

$$D = \frac{M}{N_r} \tag{2.29}$$

where N_r denotes the difference between the lower and the upper thresholds. To measure the transfer function a sinusoidal perturbation $\hat{m}(t)$ is superimposed:

$$m(t) = M + \hat{m}(t) = M + \hat{m}_a \sin(\omega t + \varphi) \tag{2.30}$$

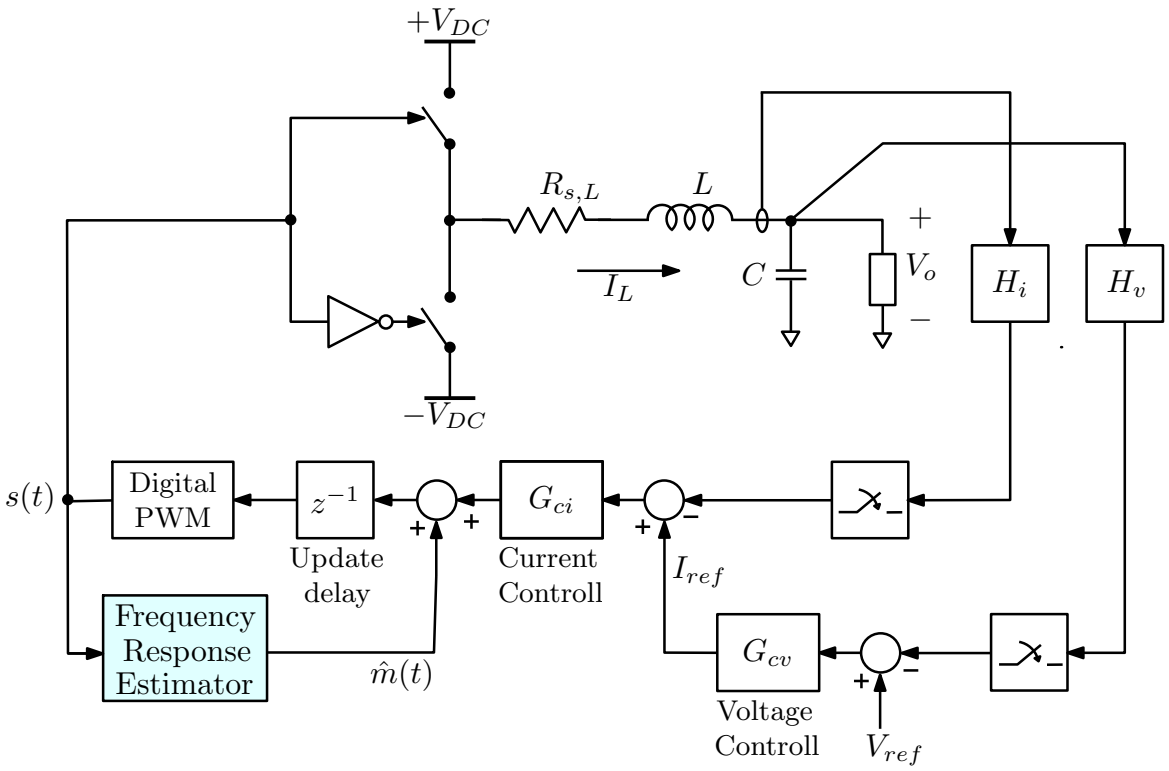


Fig. 2.13 Approximated model of the multi-loop controlled VSI.

which produces a corresponding perturbation $\hat{s}(t)$ in the output modulator command:

$$s(t) = s_{\text{steady}}(t) + \hat{s}(t). \tag{2.31}$$

The small-signal frequency response $G_{DPWM}(j\omega)$ is defined as the ratio between components $s(\omega_p)$ and $m(\omega_p)$ at the perturbation frequency ω_p:

$$G_{\text{DPWM}}(j\omega_p) \triangleq \lim_{\hat{m}_a \to 0} \frac{s(\omega_p)}{m(\omega_p)}. \tag{2.32}$$

Practically a small signal (5% amplitude in relative terms) is injected into the input of the modulator (2.30), and the transfer function of the modulator at frequency ω_p is measured and analyzed with the DFT. Repeating the procedure on a predefined set of frequencies allows deriving a graph where the measurement results are compared to the analytically calculated ones. Fig. 2.13 shows the approximated model of the multi-loop controlled VSI, plus the frequency estimator block, update delay is compensated from measurements.

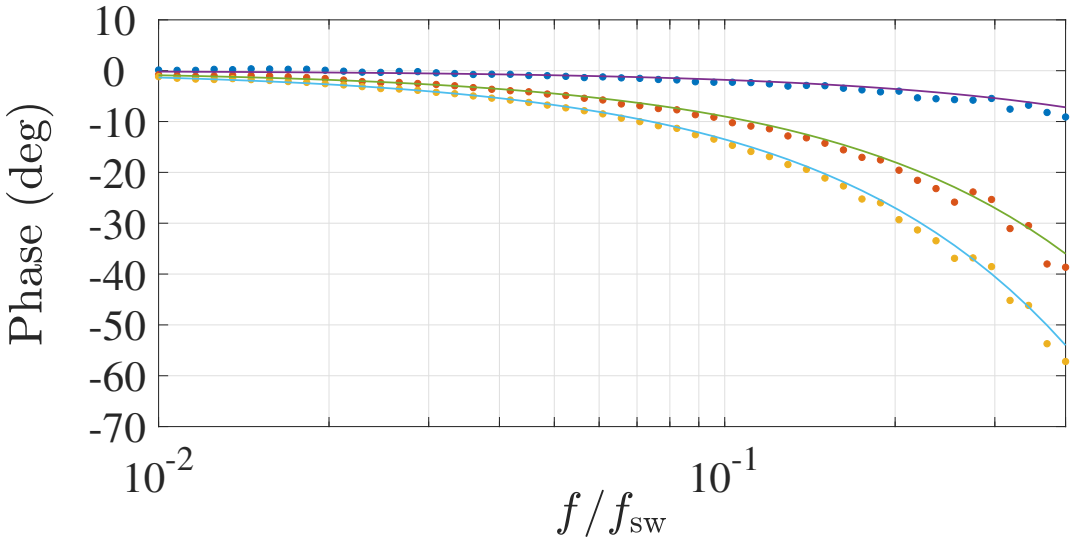


Fig. 2.14 Comparison between the phase-shift measured in MatLab/Simulink (dots) and the proposed analytical model (continuous lines) of the *single-update* DE-PWM VS the normalized switching frequency, for (from bottom to top) $d = 0.1$, $d = 0.75$ and $d = 0.5$.

2.5.2 Single update

Fig. 2.14 shows the comparison of the proposed analytical model of *single-sampling* DE carrier-based DPWM and the measurements from MatLab/Simulink® model. This test shows a very good match between the simulations and the proposed model throughout the frequency range up to $\frac{f_s}{2}$.

2.5.3 Double update

Fig. 2.15 shows the comparisons for small-signal models obtained with the proposed analysis of the *double-sampling* operation and the measurements from MatLab/Simulink® models. Also, in this case, the proposed simplified analysis succeeds in predicting the behavior obtained in simulation.

Simulations for the double-update DE-DPWM show that the phase delay introduced by this architecture is practically zero and constant over the frequency range of interest and different values of the duty cycle. This confirms what has been found analytically, i.e., the *double-update* DE-DPWM architecture provides zero phase delay.

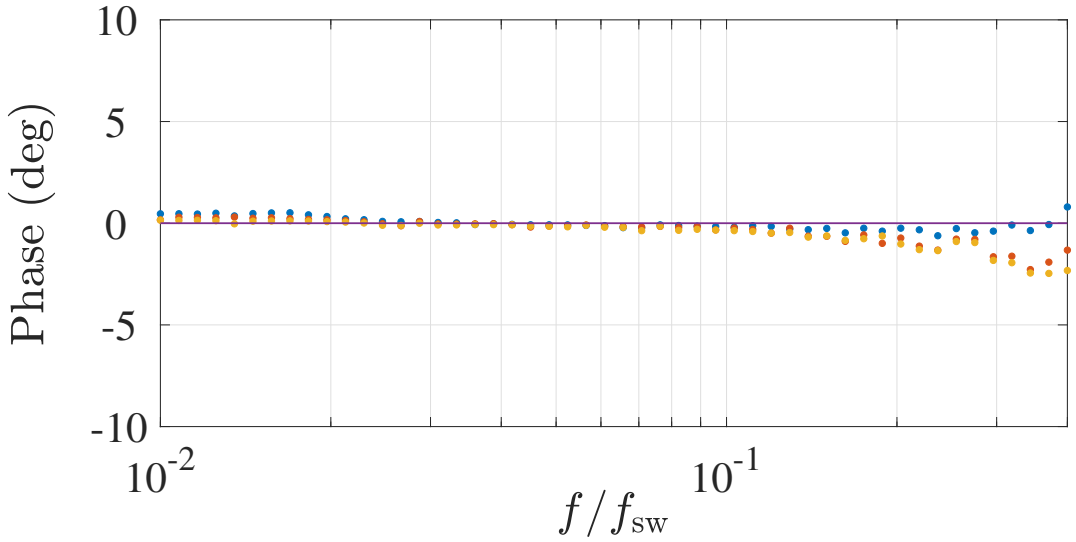


Fig. 2.15 Comparison between the phase-shift measured in MatLab/Simulink (dots) and the proposed analytical model (continuous lines) of the *double-update* DE-PWM VS the normalized switching frequency, for (from bottom to top) $d = 0.1$, $d = 0.75$ and $d = 0.5$.

2.5.4 Oversampling

The oversampling realization even shows how it is possible to use such an architecture to achieve a derivative action in the control loop without any additional implementation of a derivative term. This is certainly a remarkable result. For instance, such a modulator could be used for the realization of single voltage-loop control systems with a very fast dynamic response .Also, in this case (Fig. 2.16), the proposed simplified analysis succeed to predict the behavior obtained in simulation.

The simulations discussed in this section show that, although simplified, the proposed graphical-based analysis approach succeeds in capturing the behavior of the digital DE modulator architectures.

2.5.5 Analog

Fig. 2.17 shows the phase-shift comparison between the analytical model obtained with the proposed *graphical* approach and the measured results in MatLab/Simulink® for DE-DPWM.

These simulations are in a good match with the developed model. Note that, in Fig. 2.17 the comparison with the analytical model obtained in [81] has been omitted to avoid over-complicating the presentation of the results. The respective curves obtained starting

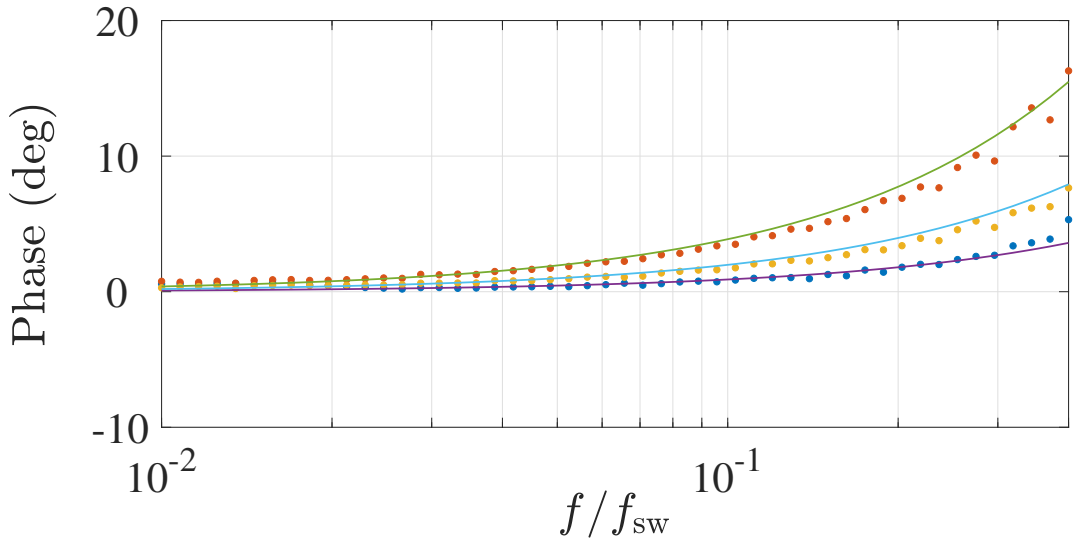


Fig. 2.16 Comparison between the phase-shift measured in MatLab/Simulink (dots) and the proposed analytical model (continuous lines) of the *oversampling* DE-PWM VS the normalized switching frequency, for (from bottom to top) $d = 0.1$, $d = 0.75$ and $d = 0.5$.

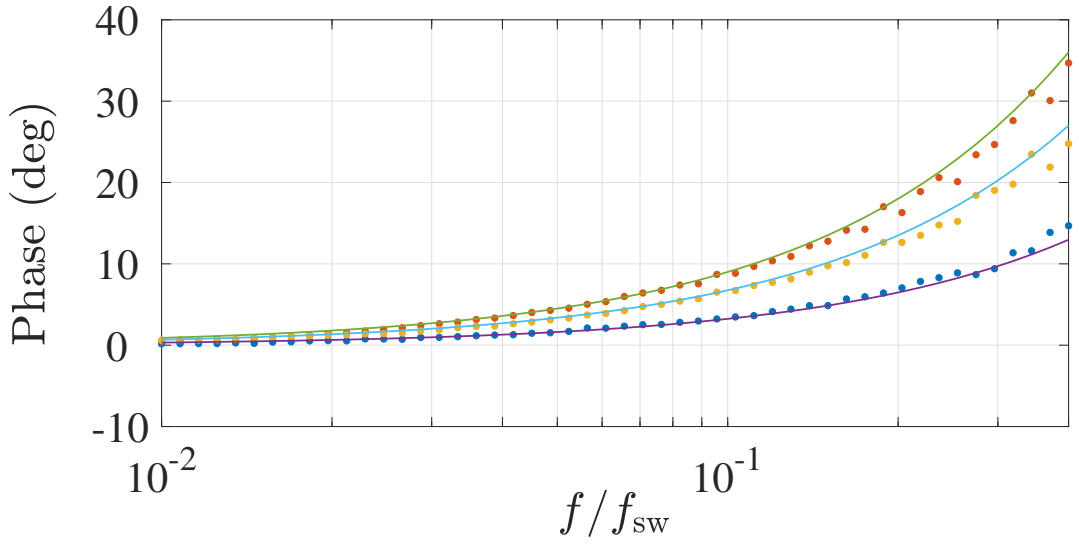


Fig. 2.17 Comparison between the phase-shift obtained from MatLab/Simulink simulations (dots) and the analytical model (continuous lines) of the analog DE-PWM, obtained with the proposed approach, VS the normalized switching frequency. Comparison for (from bottom to top) $d = 0.1$, $d = 0.75$ and $d = 0.5$.

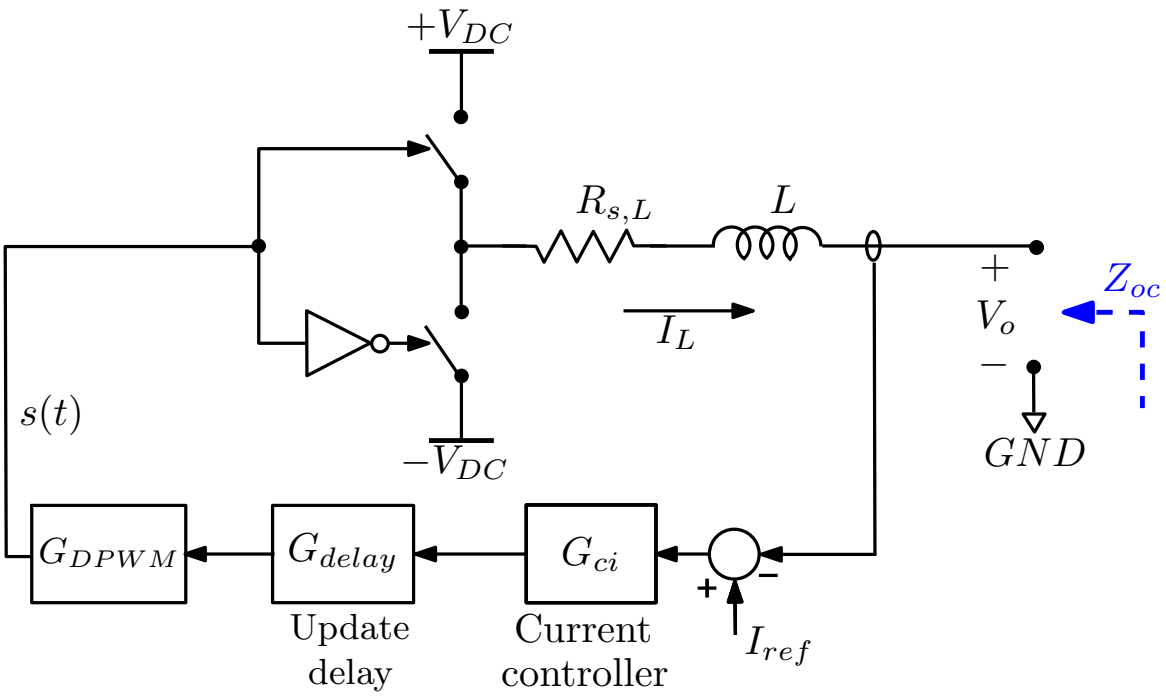


Fig. 2.18 Control scheme of single-loop controlled CSI.

from the two analytical models are always perfectly overlapped in the considered frequency range. This is further evidence of the effectiveness of the proposed *graphical-based* analysis approach.

2.6 Effect of Dual-Edge Modulator on Output Impedance

2.6.1 Current source inverter

Having inverters connected to the microgrids with passive output impedance will significantly increase the stability of the system. To have a passive output impedance it is important to have its phase between -90 and 90 degrees. To determine the closed-loop output impedance, a small signal model of the control and the power stage is needed. Following the example of the CSI shown in Fig. 2.18 and neglecting converter losses, the main transfer functions of the small-signal model can be expressed as:

$$\hat{v}_o(s) = \hat{d}(s) \cdot V_{DC} - \hat{i}_l(s) \cdot (R_{s,L} + Ls) \tag{2.33}$$

$$\hat{d}(s) = -G_{delay}(s) \cdot G_{DPWM}(s) \cdot G_{ci}(s) \cdot \hat{i}_l(s) \tag{2.34}$$

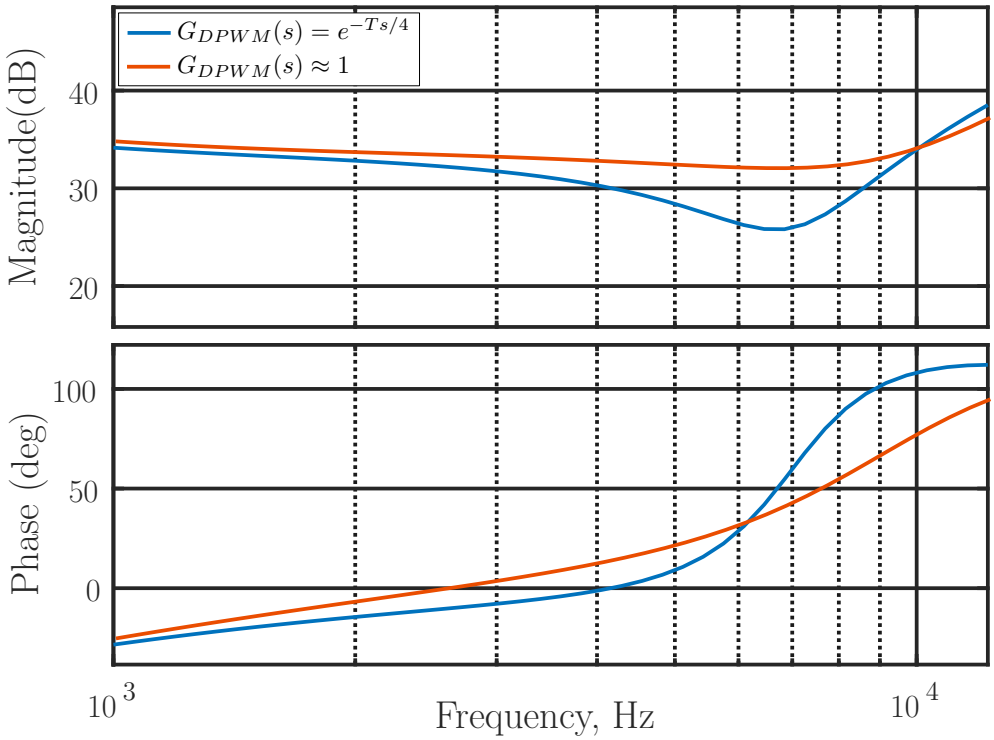


Fig. 2.19 Bode diagram of the output impedance of the CSI.

By considering the above equations, the small-signal model of the closed-loop output impedance will be:

$$\begin{aligned} Z_{oc}(s) &= -\left.\frac{\hat{v}_o(s)}{\hat{i}_l(s)}\right|_{\hat{I}_{ref}=0} \\ &= R_{s,L} + Ls + G_{delay}(s)\cdot G_{DPWM}(s)\cdot G_{ci}(s)\cdot V_{DC} \end{aligned} \tag{2.35}$$

Where $G_{delay}(s)$ is the transfer function of control signal update delay, this value is equal to sampling period, $G_{DPWM}(s)$ is the transfer function of digital PWM, and $G_{ci}(s)$ is the transfer function of the current controller that is PI regulator.

As the transfer function of *double-update* modulation discussed in subsection 2.4.2 is independent to the operation point, the *double-update* modulation is selected to compare the DE-based DPWM modulator to the TTE based DPWM modulator.

Fig. 2.19 shows the bode diagram of $Z_{oc}(s)$ with the $G_{DPWM}(s) = e^{-Ts/4}$ given by (2.18) and $G_{DPWM}(s) \approx 1$ given by (2.19). The parameters used are reported in Tab. 2.1. With the DE-based DPWM modulator, $Z_{oc}(s)$ is passive, while with $G_{DPWM}(s) = e^{-Ts/4}$, $Z_{oc}(s)$ is an active component after the frequencies around 8kHz.

Table 2.1 Current-source inverter parameters for the selected case study.

Parameter	Symbol	Value
Nominal Output Power	P_o	9.0 kW
Input voltage	V_{in}	$\pm$200 V
Nominal Output voltage	V_o	110 V(rms)
Switching frequency	f_s	25 kHz
Output Frequency	f_o	50Hz
Inductance	L	1.5mH
Inductance ESR	$R_{s,L}$	265mΩ
Death Time	Δt	0.5μs
Proportional gain of PI	kp	49.57
Integral gain of PI	ki	$1.5574236 * 10^5$

2.6.2 Droop-Controlled Converter

Droop control is commonly used in power converters linking dispersed energy resources and a common DC bus for automated power sharing in DC microgrids. To reduce DC bus voltage changes even under load transient situations, the output impedance of droop-controlled converters must always be lower than the dc resistive value (droop coefficient). Installing bulky output capacitance is one method for shaping the output impedance of droop-controlled converters, but it not only increases system cost, size, and weight, but it also leads in larger short-circuit fault currents. To avoid large output capacitance, [62] proposes a frequency-dependent droop coefficient design technique for droop-controlled converters that allows for resistive-capacitive output impedance with significantly reduced output capacitance. The effect of the DE-based DPWM on the anticipated output capacitance reduction in [62], for Buck-type converter will be studied in this section.

Following the example of the droop-controlled DC/DC converter shown in Fig. 2.20 and neglecting converter losses, the main transfer functions of the small-signal model can be expressed as:

$$\hat{i}_l = \underbrace{\frac{sC_oV_{in}}{s^2LC_o+1}}_{G_{id}(s)} \cdot \hat{d} + \underbrace{\frac{1}{s^2LC_o+1}}_{G_{ii_o}(s)} \cdot \hat{i}_o \tag{2.36}$$

$$\hat{v}_o = \underbrace{1/sC_o}_{G_{vi}(s)} \cdot \hat{i}_l + \underbrace{(-1/sC_o)}_{G_{vi_o}(s)} \cdot \hat{i}_o \tag{2.37}$$

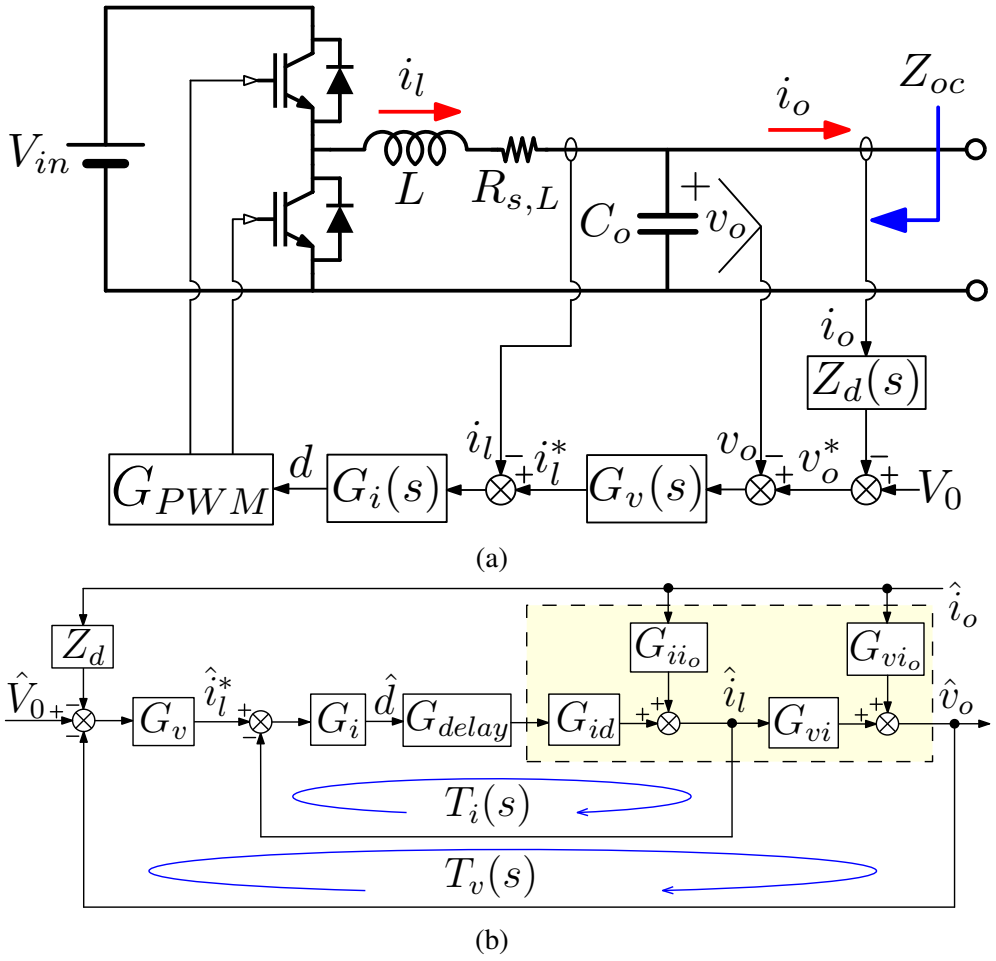


Fig. 2.20 A droop-controlled DC/DC converter in general. (a) The control strategy. The linearized model (b). Blocks within the dashed rectangle indicate the power stage. [62]

Table 2.2 Droop-controlled DC/DC converter parameters for the selected case study.

Parameter	Symbol	Value
Nominal Output Power	P_o	9 kW
Input voltage	V_{in}	400 V
Nominal Output voltage	V_o	200 V
Switching frequency	f_s	25 kHz
Inductance	L	1.5mH
Inductance ESR	$R_{s,L}$	265mΩ
Death Time	Δt	0.5µs
Droop resistance	r_d	1.33 V/A

The current loop's open-loop transfer function $T_i(s)$ and closed-loop transfer function $T_{iCL}(s)$ are defined as follows:

$$T_i(s) = G_i(s) \cdot G_{delay}(s) \cdot G_{id}(s) \tag{2.38}$$

$$T_{iCL}(s) = T_i(s)/[1 + T_i(s)] \tag{2.39}$$

The open-loop transfer function $T_v(s)$ and closed-loop transfer function $T_{vCL}(s)$ for the voltage loop are provided as follows:

$$T_v(s) = G_v(s) \cdot T_{iCL}(s) \cdot G_{vi}(s) \tag{2.40}$$

$$T_{vCL}(s) = T_v(s)/[1 + T_v(s)] \tag{2.41}$$

With the current, voltage, and droop loops closed, the output impedance $Z_{oc}(s)$ may be calculated as follows:

$$\begin{aligned} Z_{oc}(s) &= -\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{V}_0=0} \\ &= \frac{Z_d(s)T_v(s) - G_{ii_o}(s)G_{vi}(s)/[1+T_i(s)] - G_{vi_o}(s)}{1+T_v(s)} \end{aligned} \tag{2.42}$$

Where to have resistive-capacitive output impedance, $Z_d(s)$ for buck-type converter is presented in [62] as:

$$Z_d(s) = r_d - 1/G_v(s) \tag{2.43}$$

and C_o can be expressed as:

$$C_o = 1/(2\pi r_d f_v) \tag{2.44}$$

where f_v is the output voltage control bandwidth.

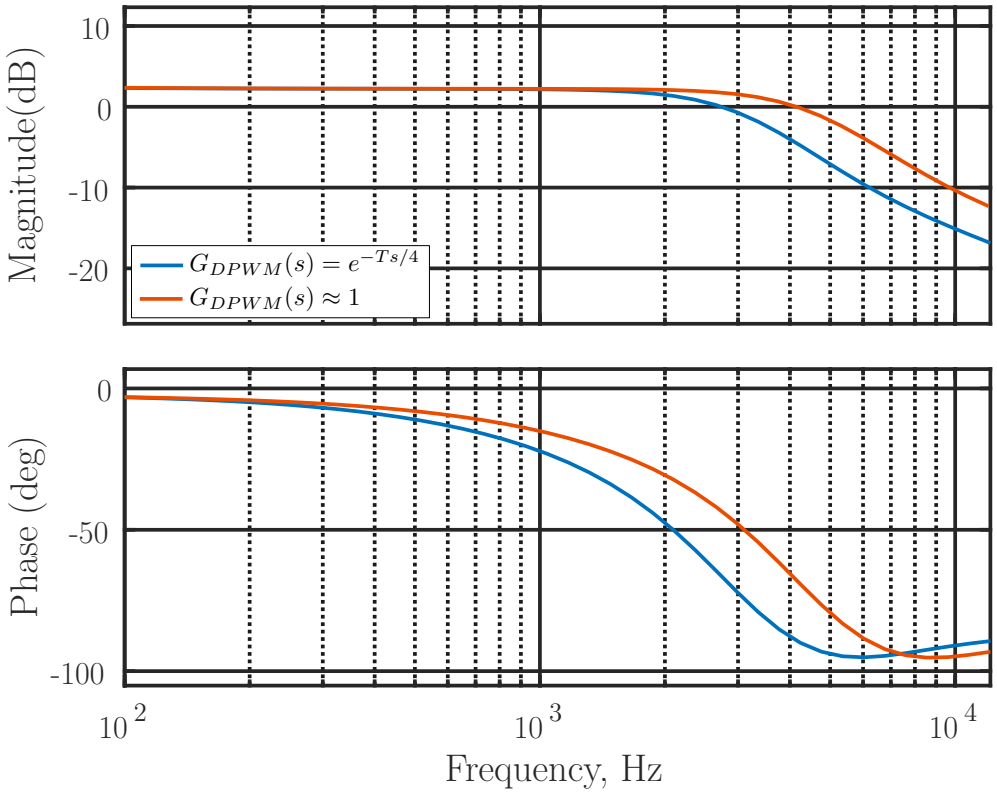


Fig. 2.21 Bode diagram of the output impedance of the buck-type droop-controlled converter.

Having reduced latency in the open loop transfer function allows for more bandwidth while mentioning the loop's gain and phase margins. Using equations (2.38) and (2.40) with the reasonable identical phase and gain margins around 10dB and 60deg for both situations of $G_{DPWM}(s) = e^{-Ts/4}$ given by (2.18) and $G_{DPWM}(s) \approx 1$ given by (2.19), we get a voltage loop bandwidth of 8.12 k rad/s and 12.3 k rad/s, respectively. Using the predicted bandwidths in (2.44), the output capacitors will be 90 µF and 60 µF in case of using the TTE-based DPWM modulator and the DE-based DPWM modulator, respectively. Fig. 2.21 shows the bode diagram of $Z_{oc}(s)$ for both cases. This chart clearly shows that utilizing this modulator will allow to significantly reduce output capacitance.

2.7 Experimental Results

The proposed graphical-based analysis approach is used to design the controllers exemplified in Fig. 2.1 and Fig. 2.18. This is implemented in a laboratory prototype to test the DE-DPWM and to highlight its advantages compared to the more traditional architecture based on TTE-DPWM. Precisely the 9kW single-phase VSI prototype operating at $f_s = 20$kHz, with

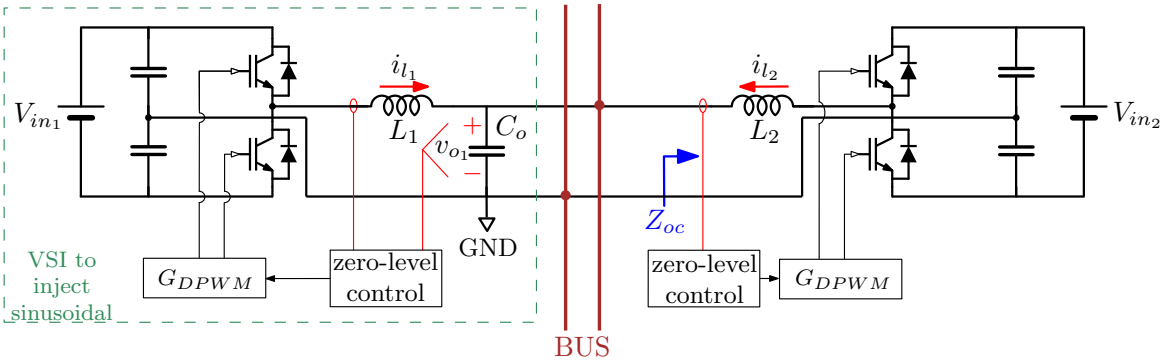


Fig. 2.22 General scheme of the output impedance measurement setup.

parameters in Tab. 2.3, is built and tested for load step variations, and other two prototypes operating at lower $f_s = 25$kHz, with parameters in Tab. 2.1 and Tab. 2.2 , are built to measure the out impudence.

Single-update and *double-update* implementations of the digital pulse-width modulators are used for the load step variations experimental tests and *double-update* for output impedance measurement. More details of this prototype can be found in Appendix B.

2.7.1 Output impedance measurement

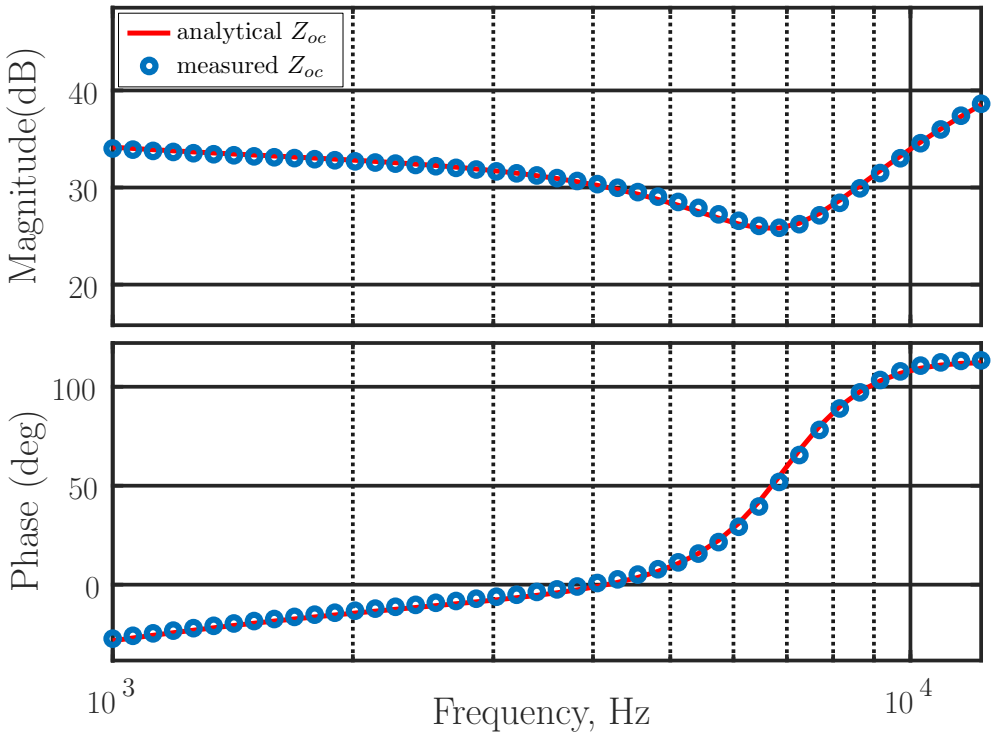
Current source inverter

The actual output impedance of CSI is experimentally measured by frequency sweep. Under a steady-state operation point, another VSI injects sinusoidal small-signal perturbations into the CSI (Fig. 2.22). The controllers of both inverters are implemented in a single processor, and meanwhile, it collects the inductor current and output voltage signals. Finally, the output impedance of the converter can be calculated by performing the Fast Fourier Transform (FFT) on the collected data. The output impedance measurement can be automatically completed by the Software Frequency Response Analyzer.

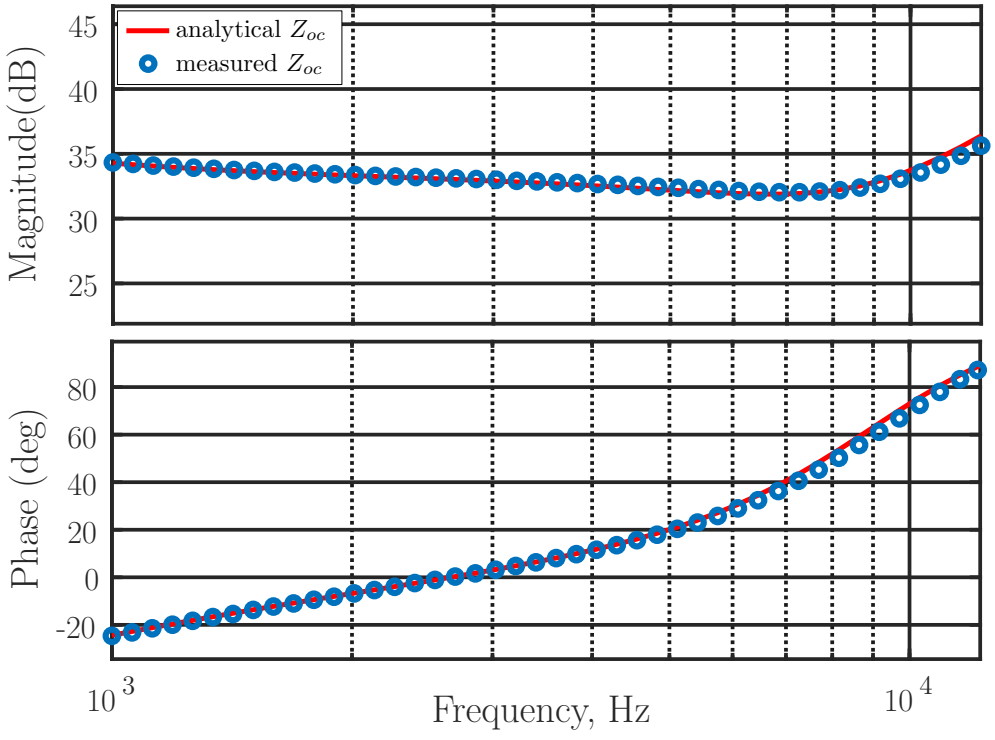
Fig. 2.23a shows the measured output impedance with different modulators. The actual output impedance is marked by a series of circles, and the analytical output impedance is represented by the solid line. As can be seen, the measured output impedances almost follow the analytical ones, proving the accuracy of the modeled output impedances.

Droop-Controlled Converter

Fig. 2.24 shows the measured output impedance with different modulators and the calculated output capacitors. A sequence of circles represents the actual output impedance, whereas



(a)



(b)

Fig. 2.23 Measured and analytical results for output impedance measurement: (a) TTE carrier based DPWM implementation and (b) DE carrier based DPWM implementation

Table 2.3 Voltage-source inverter parameters for the selected case study.

Parameter	Symbol	Value
Nominal Output Power	P_o	9.0 kW
Input voltage	V_{in}	$\pm$200 V
Nominal Output voltage	V_o	110 V(rms)
Switching frequency	f_s	20 kHz
Output Frequency	f_o	50Hz
Output capacitance	C_o	50 μF
Inductance	L	1.5mH
Inductance ESR	$R_{s,L}$	265mΩ
Nominal Output load	R_o	11Ω
Death Time	Δt	0.5μs
Current loop proportional gain of PI	kpi	0.13
Current loop Integral gain of PI	kii	400
Voltage loop Proportional gain of PI	kpv	$22.5 * 10^{-4}$
Voltage loop Integral gain of PI	kiv	7.5

a solid line represents the analytical output impedance. As noted, the measured output impedances almost exactly match the analytical ones, demonstrating the correctness of the predicted output impedances.

2.7.2 Load-step variation

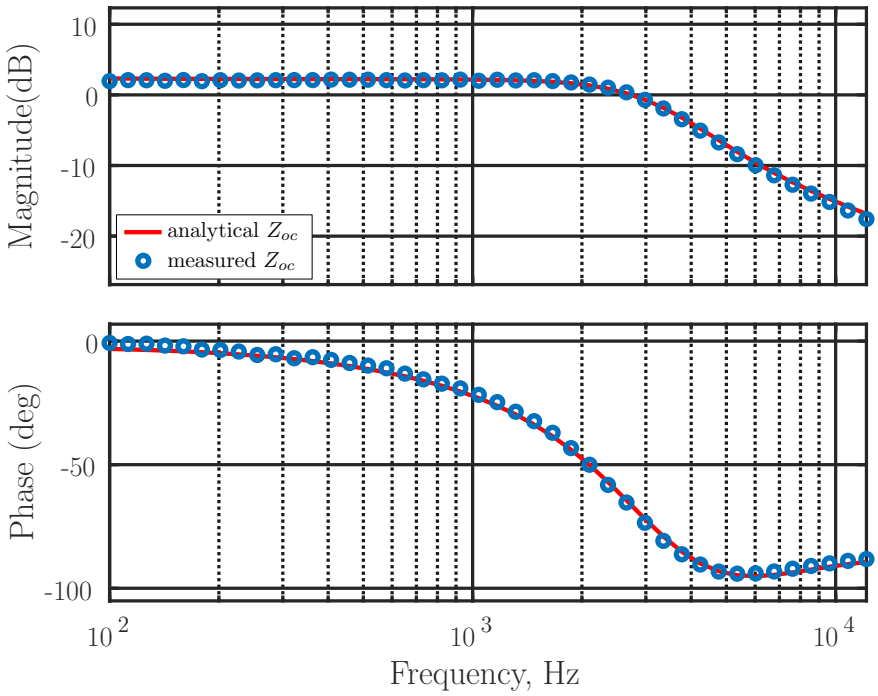
Single-sampling operation

The bandwidths and the phase margins of the inner inductor current control-loops for DE-DPWM and TTE-DPWM are respectively:

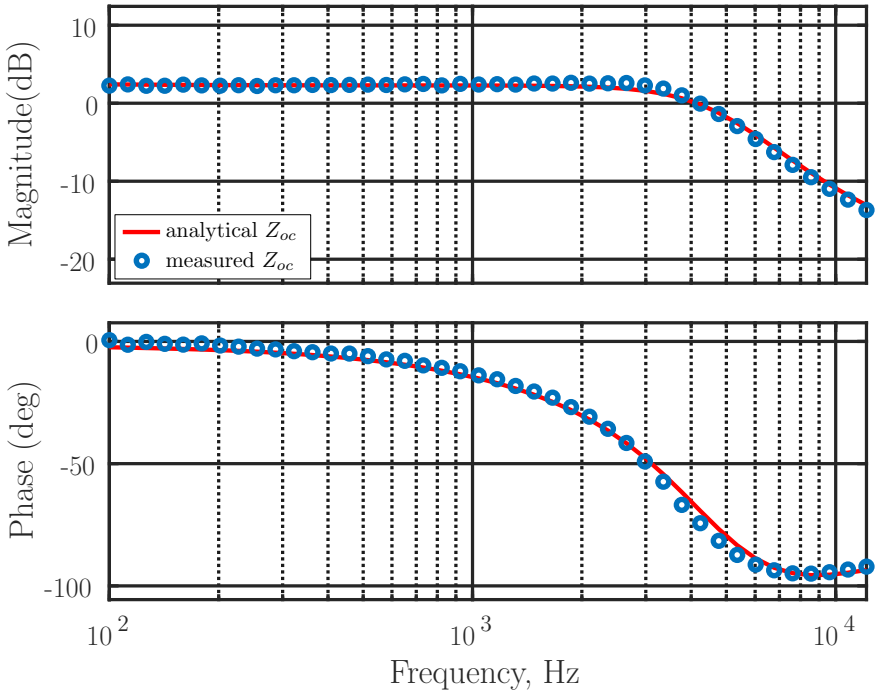
$$\begin{aligned} f_{c-\mathrm{DE}} &= 2.35\mathrm{kHz} \quad \text{with} \quad \phi_{m-\mathrm{DE}} = 50.5^o \\ f_{c-\mathrm{TTE}} &= 2.4\mathrm{kHz} \quad \text{with} \quad \phi_{m-\mathrm{TTE}} = 39.1^o, \end{aligned} \tag{2.45}$$

In both cases (DE-DPWM and TTE-DPWM), the same PI compensators are used for the control loops and voltage loops to have a clear comparison between these two cases.

Fig. 2.25 shows the experimental results for the *single-update* operation. In this test the load steps from the open circuit condition to the nominal-load (i.e., 11Ω),. The control that involves the DE-DPWM shows a dynamic response with less oscillations in the output voltage, confirming the slight gain achieved in the closed-loop phase margin.

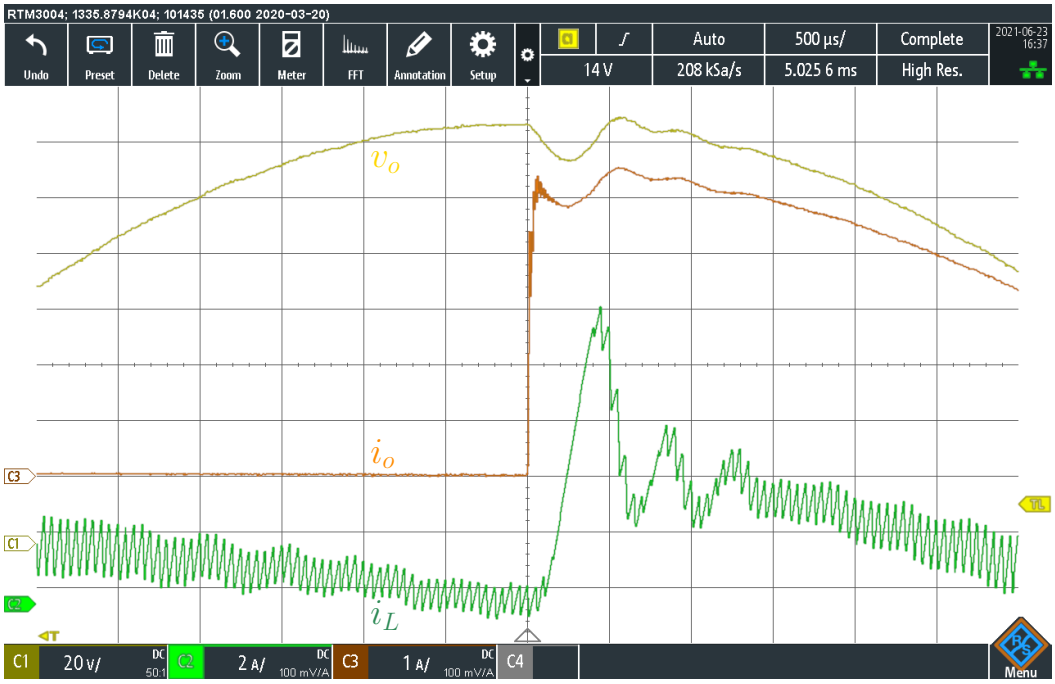


(a)

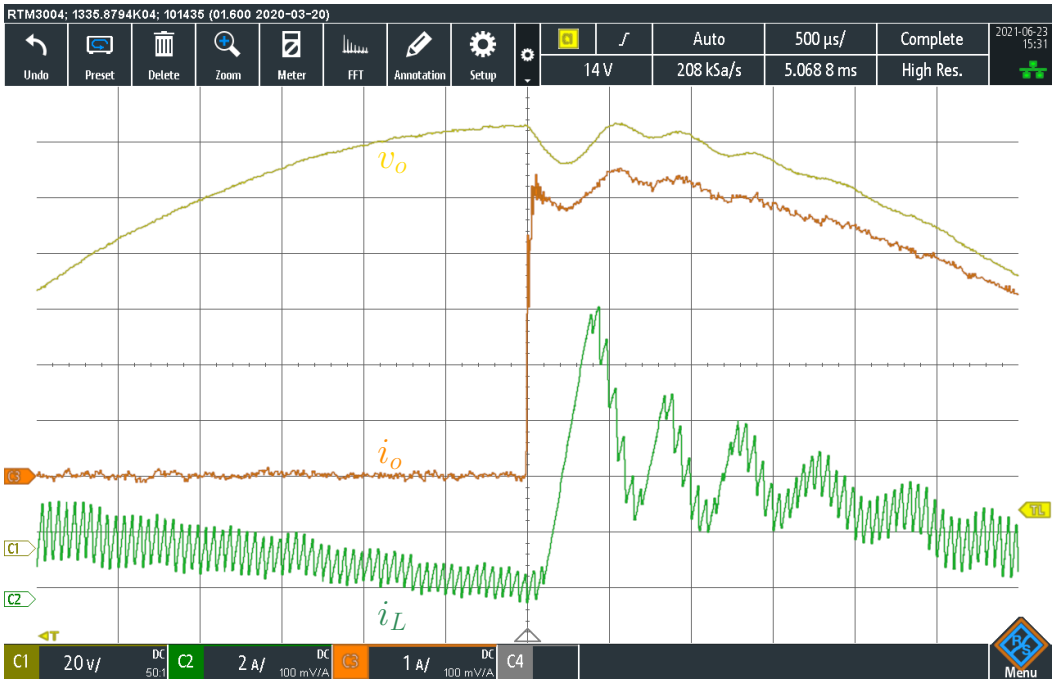


(b)

Fig. 2.24 Measured and analytical results for output impedance measurement: (a) TTE carrier based DPWM implementation with $C_o = 90\,\mu\text{F}$ and (b) DE carrier based DPWM implementation with $C_o = 60\,\mu\text{F}$.



(a)



(b)

Fig. 2.25 Experimental results for load-step variation: from no-load condition to nominal load. Results for (a) *single-update* DE carrier based DPWM implementation and (b) TTE carrier based DPWM implementation.

Double-update operation

Regarding the *double-update* case, the bandwidths are:

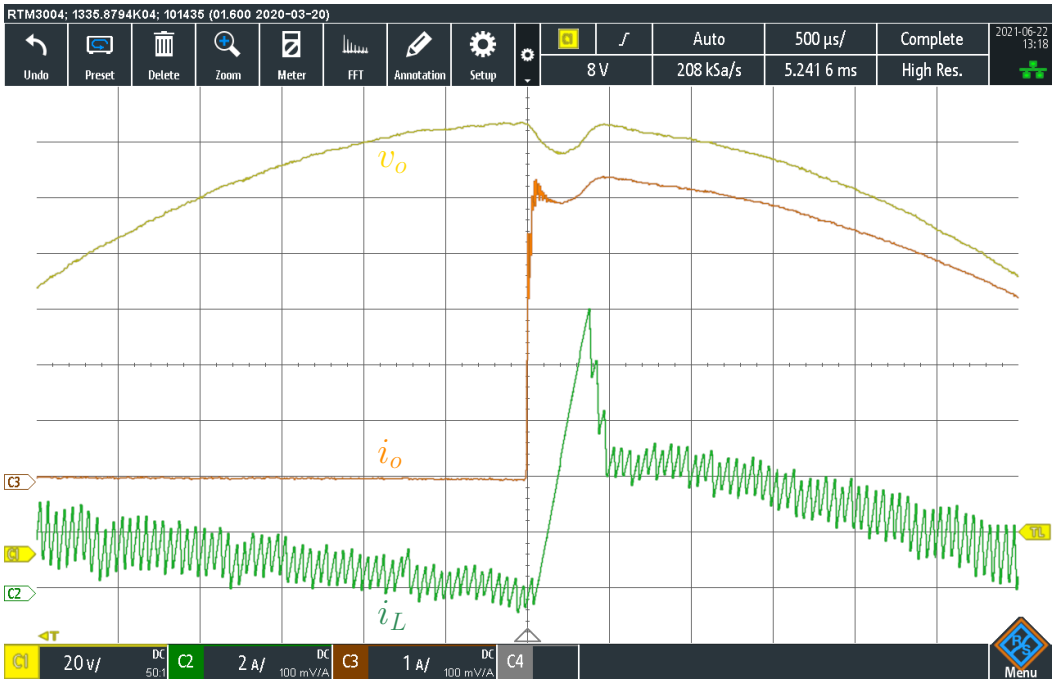
$$\begin{aligned} f_{c-\mathrm{DE}} &= 3.8\mathrm{kHz} \quad \text{with} \quad \phi_{m-\mathrm{DE}} = 51.05^{o} \\ f_{c-\mathrm{TTE}} &= 3.8\mathrm{kHz} \quad \text{with} \quad \phi_{m-\mathrm{TTE}} = 35.5^{o}. \end{aligned} \tag{2.46}$$

Fig. 2.26 shows the experimental results for the *double-update* operation during the same abrupt load-step changes above considered. In this case, the developed analytical DE-DPWM model predicts a phase-lead action. The DE-DPWM introduces almost no phase delay in this operating mode, practically eliminating the delay introduced by the modulator itself in the control loop. The final result is showing a better dynamic response of the DE-DPWM with respect to the traditional TTE architecture.

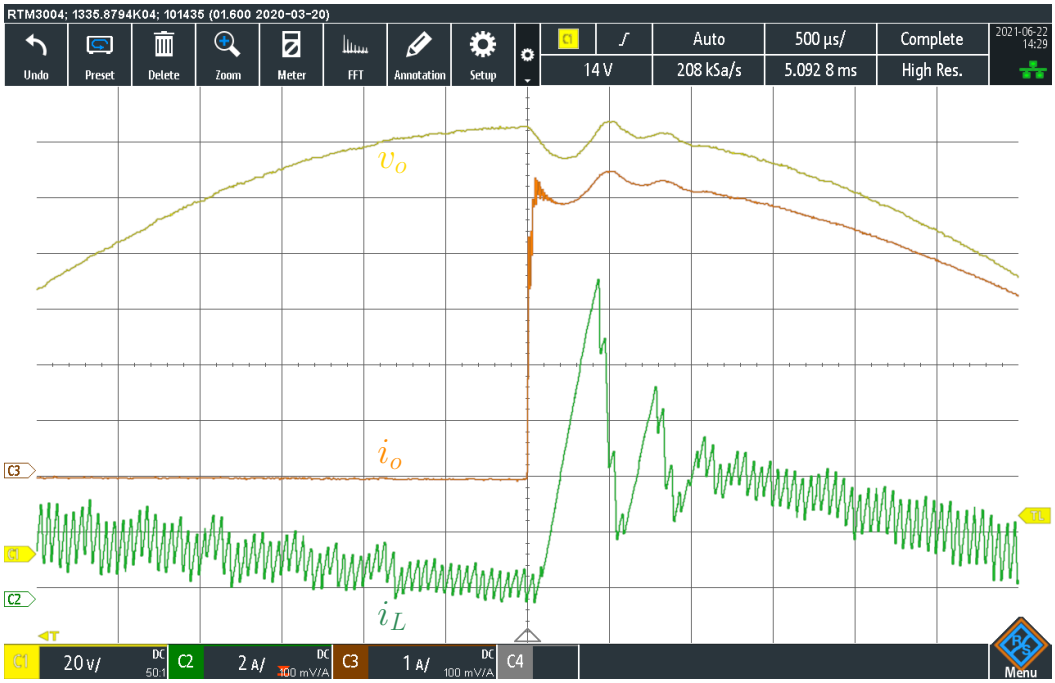
2.8 Summary

This chapter proposes a simplified analysis technique to model the small-signal behavior of the DPWM implemented with a double-edge carrier. Although less rigorous than the approach that employs describing functions, the developed methodology proved to be sufficiently accurate in predicting the DE-DPWM small-signal behavior. Moreover, the discussed graphical approach has the advantage of being very simple and allows to provide an immediate physical meaning of the obtained results. After validation by simulation, the proposed analytical model is used to design a multi-loop voltage control for a VSI. The case study summarized in Tab. 2.3 is implemented and tested in the laboratory.

The results highlight that the DE-DPWM can provide a significant improvement on the closed-loop phase margin. This improvement, already visible in the *single-update* case, is even more pronounced in the *double-update* operation, where the modulator has practically no phase delay. Experimental tests also show that the DE-DPWM provides real advantages over the classic solution based on the TTE carrier, and it it will increase the stability and decreases the costs.



(a)



(b)

Fig. 2.26 Experimental results for load-step variation: from no-load condition to nominal load. Results for (a) *double-update* DE carrier based DPWM implementation and (b) TTE carrier based DPWM implementation.

Chapter 3

Output impedance R-C shaping using hysteresis modulation

3.1 Introduction

In DER dc-dc converters that are forming a dc microgrid, saving cost, higher power density, and smaller short-circuit fault current are beneficial points that can be attained by having a smaller output capacitance for each converter. However, decreasing too much output capacitance can cause unacceptable output voltage spikes/dips during load changes. Considering the mentioned facts, a proper control technique allowing to have a resistive output impedance with smaller output capacitance is a better design solution for DER converters.

The Boost converter is an example of the topologies that their small-signal model is influenced by the operation point. Differently, for some other topologies like Buck converter, their small-signal model does not change with the operation point. From this perspective, this chapter aims to verify the feasibility of the proposed design method for more complicated case by providing an example of Boost converters, to complete the work presented in [60].

3.1.1 Droop control

Droop control is a widely used decentralized control strategy for proportional power-sharing among parallel DER converters without communication [40, 69]. The starting point for droop control is the basic droop method and it has been studied and improved in different aspects [27]. In a dc microgrid, the dc bus impedance is an important parameter for the performance of the system, and it is dominated by the output impedance of the droop-controlled DER converters connected to the dc bus in parallel [2]. At low-frequency droop resistance and at high-frequency, the output capacitance, are the dominating parameters to shape the output

impedance of a droop-controlled DER converter. But for the medium frequency, many factors like the control performance and parameters usually cause different shapes [61].

3.1.2 Relevance of R-C output impedance with small C

The reduction of the output capacitor in DER for DC micro-grids is an interesting feature, as it would enable a lower short-circuit current during bus short- circuit faults, making fault isolation easier [68] and, in more general terms, reducing the capacitive energy stored in the dc bus. On the other hand, it is important that the output voltage variations due to load variations are kept within a specific tolerance band. The undesired and desired cases are shown Fig. 3.1a and Fig. 3.1b, where undershoots and overshoots with respect to the steady-state bus voltage are present due to step load variations. The desired case is possible if the DER output impedance is purely resistive-capacitive [61], as widely studied in the past for VRM [102]. A resistive-capacitive output impedance may also reduce converter interactions among different converters and/or damp possible resonances in the dc bus, if located within the control bandwidth [2]. To obtain such behavior with small output capacitors, two main provisions are needed:

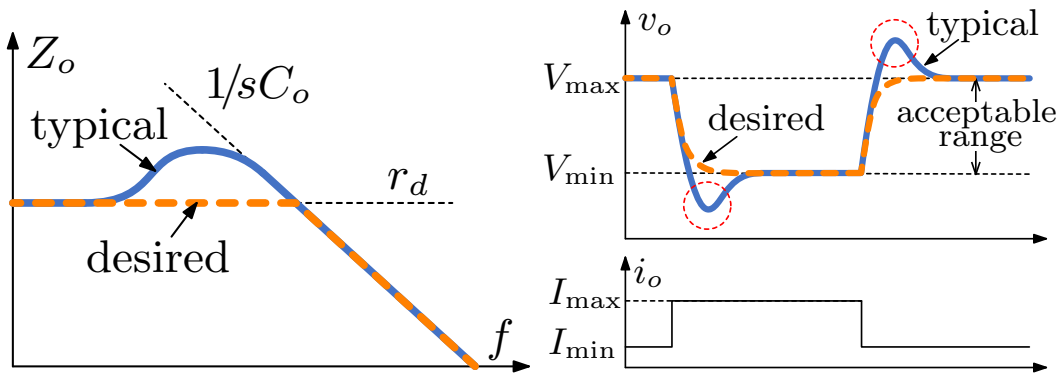
- shaping the output impedance by control design;
- adopt a very high bandwidth control as the minimum capacitor value is, under first-order approximation, inversely proportional to the control bandwidth [101]:

$$C_o = 1/(2\pi r_d f_v) \tag{3.1}$$

  For a converter with a certain power capacity, (3.1) shows that a smaller droop resistance r_d means a narrower voltage tolerance band, which, in turn, requires larger C_o or a higher output voltage control bandwidth f_v.

3.1.3 Outline

Based on the approach proposed in [61], [23], and [60], this chapter addresses the analysis and design of a droop controlled DER using a high performance oversampled hysteresis modulation in Sect. 3.2 , where the hysteresis modulation is applied to a combination of the sampled inductor current, the output voltage, and the output current. By properly design the controller parameters, the proposed solution enables the resistive behavior within the controller bandwidth and a reduction of the output capacitance due to high-bandwidth hysteresis modulation. To be continued, this chapter also addresses a simplified small-signal



(a) output impedance (b) output voltage transient

Fig. 3.1 Different output impedance of droop-controlled DER converters and corresponding dynamic output voltage waveforms during load changes.

analysis of the proposed solution, the design methodology, the frequency shaping of the droop coefficients in Sect. 3.3, and the selection criterion of the output capacitance of droop-controlled converters. The effectiveness of the proposed solutions is experimentally validated on 3kW Boost prototypes in Sect. 3.4.

3.2 Droop Control Based on Hysteresis Modulation

To have a resistive-capacitive output impedance with a small output capacitance, a fast voltage controller for DER dc-dc converters, is necessary. This chapter analyses a high bandwidth oversampled hysteresis controller for the droop controller of Boost converters. To complete the section, a design approach for hysteresis droop-controlled converters, including the design of frequency-dependent droop coefficients is also proposed.

3.2.1 Modified hysteresis modulation

The hysteresis regulator, as shown in Fig. 3.2, is constructed based on a hysteretic differentiator and a PI controller. These two elements are responsible for instant actions and zero steady-state error, respectively. More details are discussed below.

Hysteretic differentiator

The hysteretic differentiator, which is composed of a comparator and an integrator, is the heart of the proposed control method. The steady-state operation waveforms of the control of Fig. 3.2 are shown in Fig. 3.3. The ramp state $R(t)$ generated by the integrator is compared

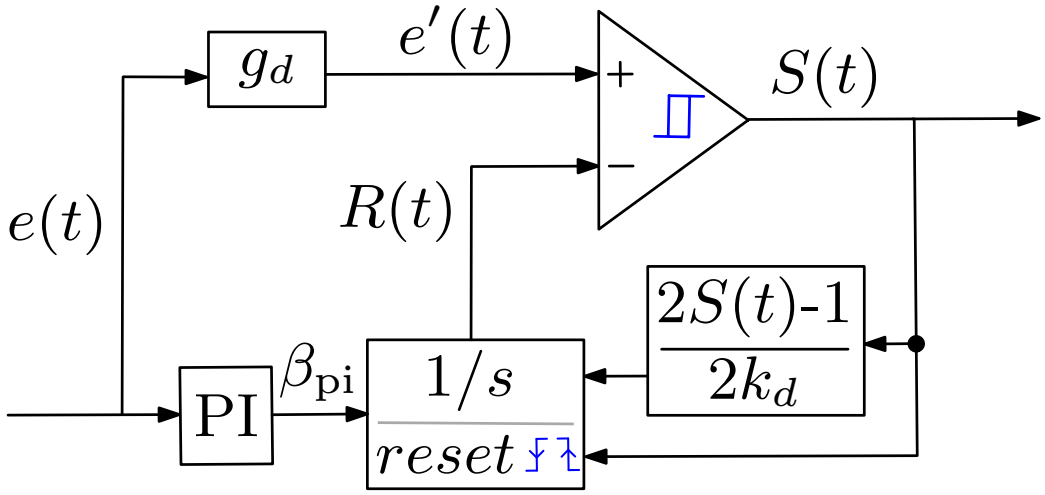


Fig. 3.2 Scheme of the hysteresis controller.

to the error signal $e'(t)$ by the comparator and the switching signal $S(t)$ is generated. $S(t)$ has two states, 0 and 1:

$$S(t) = \begin{cases} 0, & \text{if } e'(t) < R(t) \\ 1, & \text{else} \end{cases} \tag{3.2}$$

$S(t)$ restarts the integrator in any change of its state: if a rising edge is detected, $R(t)$ is shifted downward by $\beta + \beta_{\text{pi}}$ and, if a falling edge is detected, $R(t)$ is shifted upward by $\beta - \beta_{\text{pi}}$, being β is a constant value and β_{pi} is the output of the PI controller. The parameter β determines the switching period T_{sw}, as:

$$T_{sw} = 4\beta k_d, \tag{3.3}$$

being $1/2k_d$ the absolute value of the slope of $R(t)$. While the switching period T_{sw} varies during transient conditions, as in any hysteresis modulation, (3.3) shows that T_{sw} is constant in steady-state conditions.

An approximated small-signal model of the hysteretic differentiator is now derived. The first part is related to the effect of the PI controller on the duty cycle. Assuming $e(t)$ constant within the switching period and analyzing the waveform of Fig. 3.3, we have:

$$D = \frac{1}{2} \cdot (1 + \frac{\beta_{PI}}{\beta}). \tag{3.4}$$

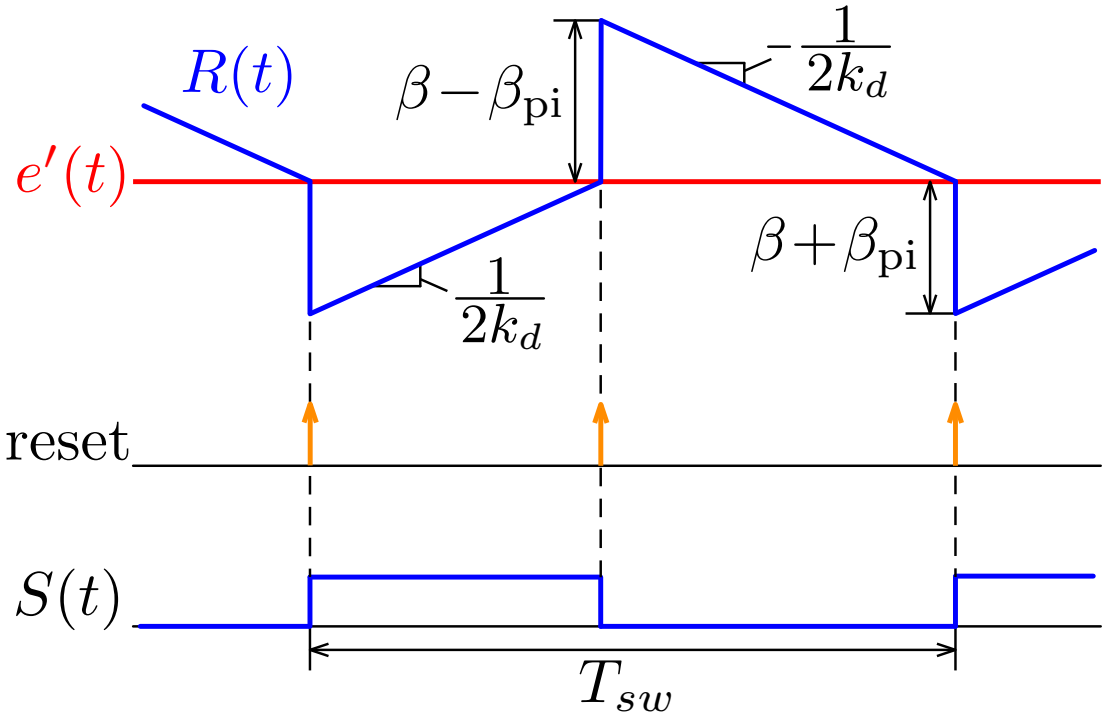


Fig. 3.3 Steady state operation principle of the hysteresis droop controller.

Thus, under perturbation of $\hat{\beta}_{PI}$, the following relation holds:

$$\hat{\delta}(s) = \frac{1}{2}\frac{\hat{\beta}_{PI}(s)}{\beta} = \frac{k_p + \frac{k_i}{s}}{2\beta}\hat{e}(s) \tag{3.5}$$

being k_p and k_i the PI controller coefficients. Moreover, as shown in [23], there is an intrinsic derivative effect on the hysteresis modulation of Fig. 3.4 . In fact, assuming a constant β_{PI}, it can be shown that [23] :

$$\hat{\delta}(s) \approx s(k_d.g_d) \tag{3.6}$$

Using (3.5) and (3.6) , the small-signal model of the hysteresis controller shown in Fig. 3.2, can be approximated as:

$$G_{hys}(s) = \frac{\hat{S}(s)}{\hat{e}(s)} \approx \frac{k_p + \frac{k_i}{s}}{2\beta} + s(k_d.g_d) \tag{3.7}$$

In (3.7), the constant gain g_d adds a degree of freedom in the designing the controller coefficients.

Thus, the proposed hysteresis modulation behaves, under the approximated small-signal analysis, as a PID controller. The proposed modulation maintains the nonlinear behavior of

the hysteresis modulation for large perturbations, thus providing a fast dynamic response under step load transients.

PI controller

A PI controller is used to force $e(t) = 0$ on the output voltage v_o in steady-state. Its output β_{pi} is used to adjust the duty cycle. For example, considering the case that $e(t)$ is positive, the output of the PI controller, β_{pi} increases. Then the position of $R(t)$ moves downward compared to the position of $e'(t)$, which means a higher duty cycle and as result, an increase on v_o.

3.2.2 Droop control with shaping of the output impedance

The control scheme of the droop-controlled dc-dc converter with the proposed hysteresis modulation is shown in Fig. 3.4. In general terms, the droop controller includes the output voltage v_o, inductor current i_L and the output current i_o sensing, both current sensing are not strictly needed since the output current i_o can be estimated from i_L and the duty-cycle δ. In Fig. 3.4 the inductor current sensing is used to attenuate the effect of the RHP zero in Boost or buck-Boost converters and $Z_{if}(s)$ is a high-pass filter with a properly designed gain to ensure stability and damped behavior, but zero dc gain. Other equivalent variations of the control architecture shown in Fig. 3.4 are, of course, possible.

Under these assumptions, the *V-I* droop method generates the output voltage reference v_o^* based on the sampled output current i_o and the droop impedance $Z_d(s)$, as follows:

$$v_o^* = V_0 - i_o \cdot Z_d(s), \tag{3.8}$$

where V_0 is the output voltage set point with $i_o = 0$, and $Z_d(s)$ is the shaped droop impedance, being $Z_d(j0) = r_d$, and r_d is the DER desired droop resistance. In Sect. 3.3 the transfer function $Z_d(s)$ is designed to ensure a resistive behavior within the controller bandwidth.

3.2.3 Digital implementation and current sampling

The theoretical analog waveforms of Fig. 3.3 shall be implemented in a digital platform. One example of the resulting waveforms is reported in Fig. 3.5, where the ramp waveform $R(t)$ and the error signal $e(t)$ is oversampled 10 times within the switching period T_{sw}. Moreover, the example shows the case of one sample delay, typically present in DSP implementations, as in the case of the experimental prototype described in Section 3.4. It is worth mentioning two relevant properties of digital implementation:

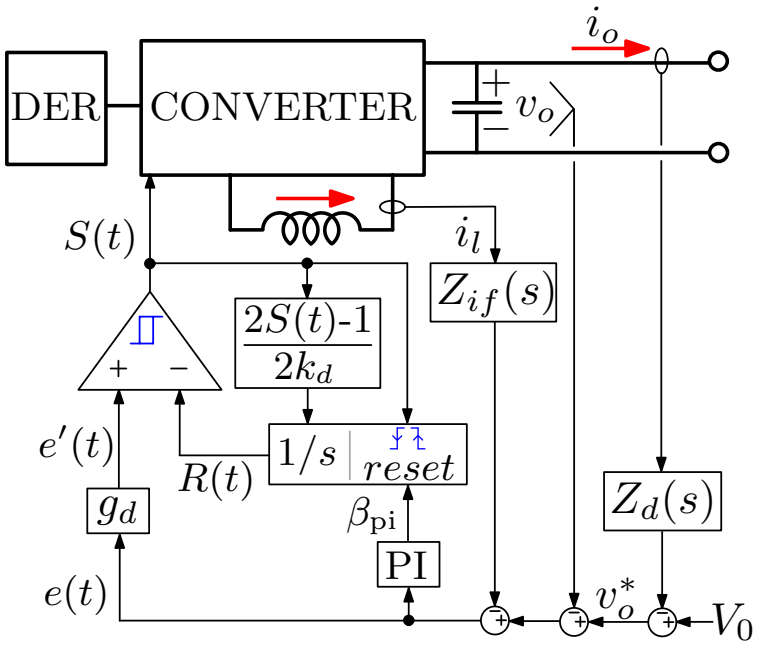


Fig. 3.4 General control scheme of the hysteresis droop controller.

- at each sampling time T_{sp}, the new value of $R(t)$ and $e(t)$ is obtained, and their difference is used to drive the Digital Pulse Width Modulator peripheral in the DSP. Thus, the time resolutions of the t_{on} and t_{off} sub-intervals are set by the Digital Pulse Width Modulator resolution and not by the oversampling period;
- while the output voltage is oversampled by a factor N, the current is sampled only at the middle of the on-time, reducing the possible filters in the control loop. The sampling is set as shown in (3.5), evaluating half of the t_{on} time based on the expected duty-cycle given by (3.4):

$$\frac{t_{on}}{2} = k_d.(\beta + \beta_{PI}). \tag{3.9}$$

3.3 Small-Signal Analysis

To determine the closed-loop converter output impedance, a small signal model of the control and of the power stage is needed. Following the example of the synchronous Boost converter shown in Fig. 3.6 and neglecting converter losses. Under an operation point, the circuit of the Boost converter can be linearized as follows:

$$sL \cdot \hat{i}_L = -(1 - D_{op}) \cdot \hat{v}_o + V_{op} \cdot \hat{d} \tag{3.10}$$

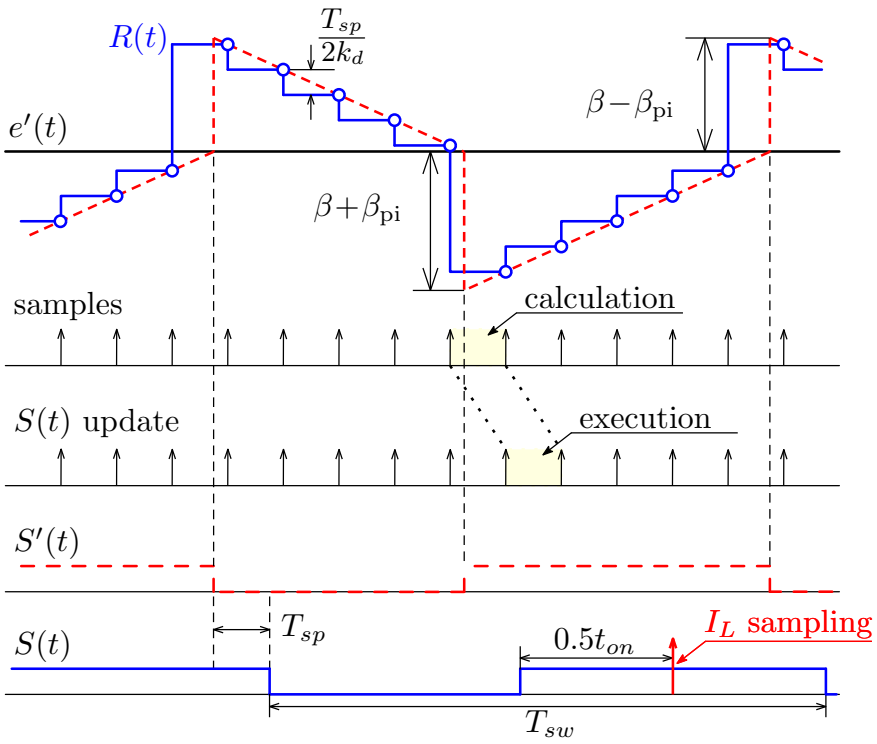


Fig. 3.5 Digital implementation with oversampled control and one-sample delay

$$sC_o \cdot \hat{v}_o = (1-D_{op}) \cdot \hat{i}_L - I_{Lp} \cdot \hat{d} - \hat{i}_o \tag{3.11}$$

Where I_{Lp} is the static inductor current, V_{op} is the static output voltage, and D_{op} is the static duty cycle. In steady-state, the input voltage V_{in} is equal to $(1-D_{op}) \cdot V_{op}$, and the static output current is $I_{op} = (1-D_{op}) \cdot I_{Lp}$. Then, by combining (3.10) and (3.11), the main transfer functions of the small-signal model can be expressed as:

$$\hat{i}_l = \underbrace{\frac{sC_oV_{op}+I_{op}}{s^2LC_o+(1-D_{op})^2}}_{G_{id}(s)} \cdot \hat{d} + \underbrace{\frac{1-D_{op}}{s^2LC_o+(1-D_{op})^2}}_{G_{ii_o}(s)} \cdot \hat{i}_o \tag{3.12}$$

$$\hat{v}_o = \underbrace{\frac{-sLI_{lp}+V_{in}}{sC_oV_{op}+I_{op}}}_{G_{vi}(s)} \cdot \hat{i}_l + \underbrace{\frac{-V_{op}}{sC_oV_{op}+I_{op}}}_{G_{vi_o}(s)} \cdot \hat{i}_o \tag{3.13}$$

where $G_{id}(s)$ is the transfer function from $\hat{d}$ to $\hat{i}_l$, $G_{ii_o}(s)$ is the transfer function from $\hat{i}_o$ to $\hat{i}_l$, $G_{vi}(s)$ is the transfer function from $\hat{i}_l$ to $\hat{v}_o$ and $G_{vi_o}(s)$ is the transfer function from $\hat{i}_o$ to $\hat{v}_o$. The parameters of the small-signal model depend on the converter operating point, denoting V_{op} the output voltage, I_{lp} the inductor current, and D_{op} the duty cycle of the operating point.

By considering the (3.12) and (3.13), the simplified small-signal model of the proposed modulator (3.7), the control block diagram of the hysteresis droop-controlled converter is displayed in Fig. 3.7. The evaluation of the control performance and the design of the PID control parameters of $G_{hys}(s)$ can be performed similarly to the multi-loop control.

For the inner loop, its open-loop transfer function $G_{it}(s)$ and its closed-loop transfer function $G_{iCL}(s)$ are given by:

$$G_{it}(s) = G_{hys}(s) \cdot G_{delay}(s) \cdot G_{id}(s) \tag{3.14}$$

$$G_{iCL}(s) = \frac{G_{it}(s)}{1 + G_{it}(s) \cdot Z_{if}(s)} \tag{3.15}$$

In (3.14), $G_{delay}(s)$ is included to consider the effect of one-sampling-period delay mentioned in Sect. 3.2.

For the outer voltage loop, its open-loop transfer function $T_v(s)$ and its closed-loop transfer function $T_{vCL}(s)$ are given as:

$$T_v(s) = G_{iCL}(s) \cdot G_{vi}(s) \tag{3.16}$$

$$\begin{aligned} T_{vCL}(s) &= \frac{T_v(s)}{1 + T_v(s)} \\ &= \frac{G_{hys}(s) \cdot G_{delay}(s) \cdot G_{id}(s) \cdot G_{vi}(s)}{1 + G_{hys}(s) \cdot G_{delay}(s) \cdot G_{id}(s) \cdot [G_{vi}(s) + Z_{if}(s)]} \end{aligned} \tag{3.17}$$

In (3.17), $Z_{if}(s)$ is a first-order high-filters given by:

$$Z_{if}(s) = R_{if} \frac{s}{s + \omega_h} \tag{3.18}$$

where R_{if} and ω_h are designed to reduce the effect of the RHP zero. For such purpose, we have designed $\omega_h = I_{op}/(V_{op} \cdot C_o)$ and $R_{if}/\omega_h = L \cdot I_{lp}/I_{op}$. In principle, the parameters may be adapted to the operating conditions, but, for simplicity, the parameters are designed at half of the load and at the nominal input/output voltages, and then kept constant during converter operation.

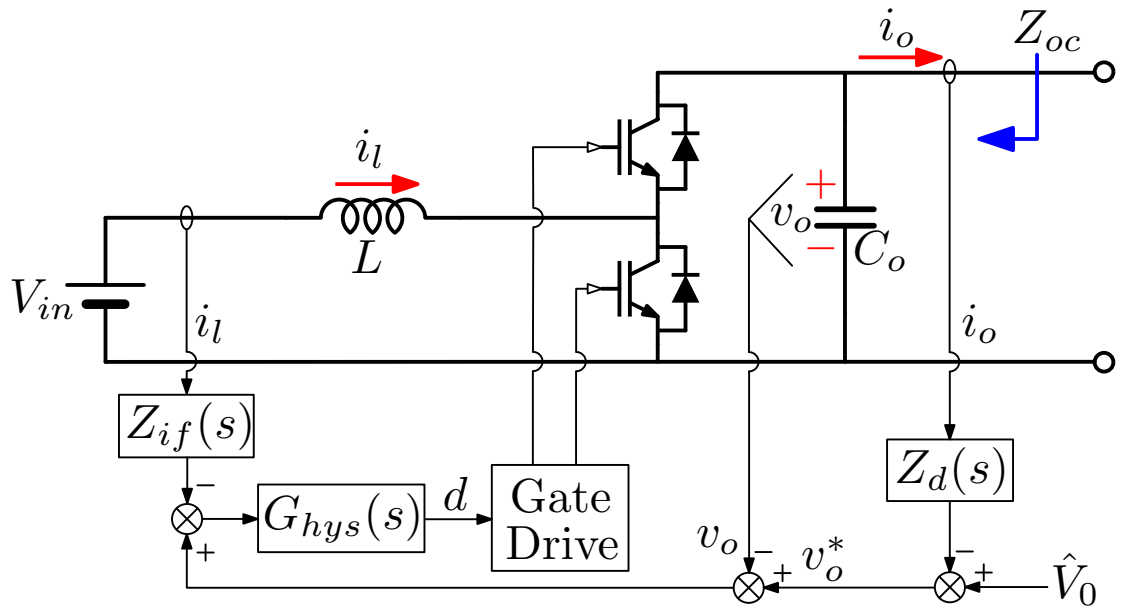


Fig. 3.6 Linearized model of the Boost-type hysteresis droop-controlled.

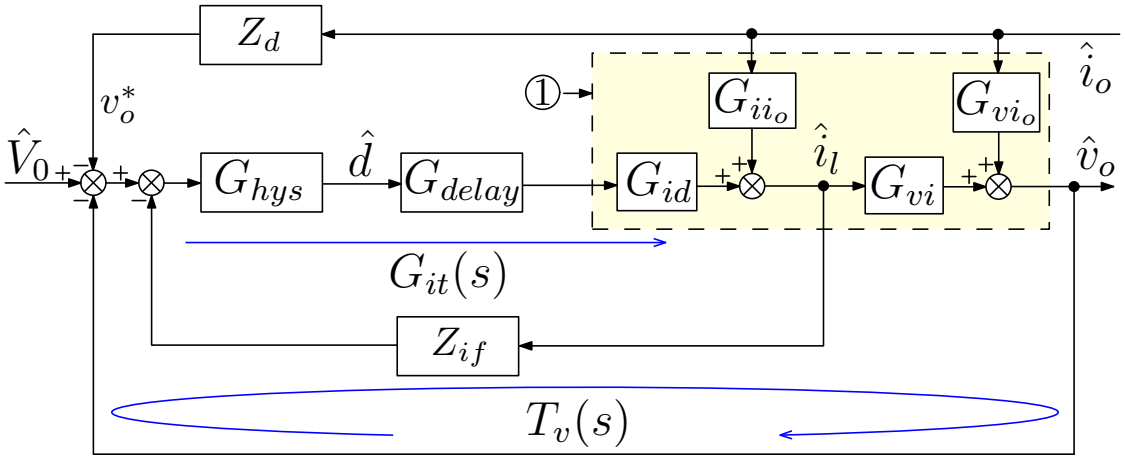


Fig. 3.7 The Boost-type hysteresis droop-controlled DER converter model.

3.3.1 Output impedance shaping

It is desired to have a resistive closed-loop output impedance $Z_{oc}(s)$ equal to r_d at low and medium frequency. Thus, $Z_d(s)$ can be evaluated by solving the equation $Z_{oc}(s) = r_d$. The transfer function of the closed-loop output impedance $Z_{oc}(s)$ is derived as:

$$\begin{aligned} Z_{oc}(s) &= -\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{V}_0=0} \\ &= \frac{Z_d(s)\cdot T_v(s) - \dfrac{G_{ii_o}(s)\cdot G_{vi}(s)}{1+G_{it}(s)\cdot Z_{if}(s)} - G_{vi_o}(s)}{1+T_v(s)} \end{aligned} \tag{3.19}$$

By considering $Z_{oc}(s) = r_d$ in (3.19) and combining it with (3.16) and (3.17), the droop impedance $Z_d(s)$ should be designed as:

$$\begin{aligned} Z_d(s) &= \frac{r_d}{T_{vCL}(s)} + \frac{\dfrac{G_{ii_o}(s)\cdot G_{vi}(s)}{1+G_{it}(s)\cdot Z_{if}(s)} + G_{vi_o}(s)}{T_v(s)} \\ &= \frac{r_d}{T_{vCL}(s)} + \\ &\quad \frac{G_{ii_o}(s)\cdot G_{vi}(s) + G_{vi_o}(s)[1+G_it(s)\cdot Z_{if}(s)]}{T_i(s)\cdot G_{vi}(s)} \end{aligned} \tag{3.20}$$

A set of approximations on (3.20) are used to derive a simpler, easier to be implemented $Z_d(s)$. Assuming that $T_{vCL}(j\omega) \approx 1$ and $1/G_{it}(s) \approx 0$ within the voltage control bandwidth (i.e., $\omega < \omega_v$), neglecting the RHP pole introduced by $G_{vi}(s)$ and combining (3.12), (3.13) and (3.14), (3.20) can be simplified as:

$$Z_d(s) \approx r_d - \frac{Z_{if}(s)}{1-D_{op}}, \quad \omega < \omega_v \tag{3.21}$$

where D_{op} is based on the nominal input and output voltage and it can be adapted to the operating conditions, if needed. Fig. 3.8 shows the bode diagram of $Z_{oc}(s)$ with the $Z_d(s)$ given by (3.21) and $Z_d(s) = r_d$. The parameters used are reported in Tab. 3.1. With the proposed design, $Z_{oc}(s)$ is almost resistive at low frequency, while with $Z_d(s) = r_d$, $Z_{oc}(s)$ is increased by almost 3.4dB respect to r_d.

Furthermore, Fig. 3.9 shows the $Z_{oc}(s)$ under different operating conditions while keeping the same control parameters. As can be seen, output impedance has a small variation from no-load condition to full-load condition.

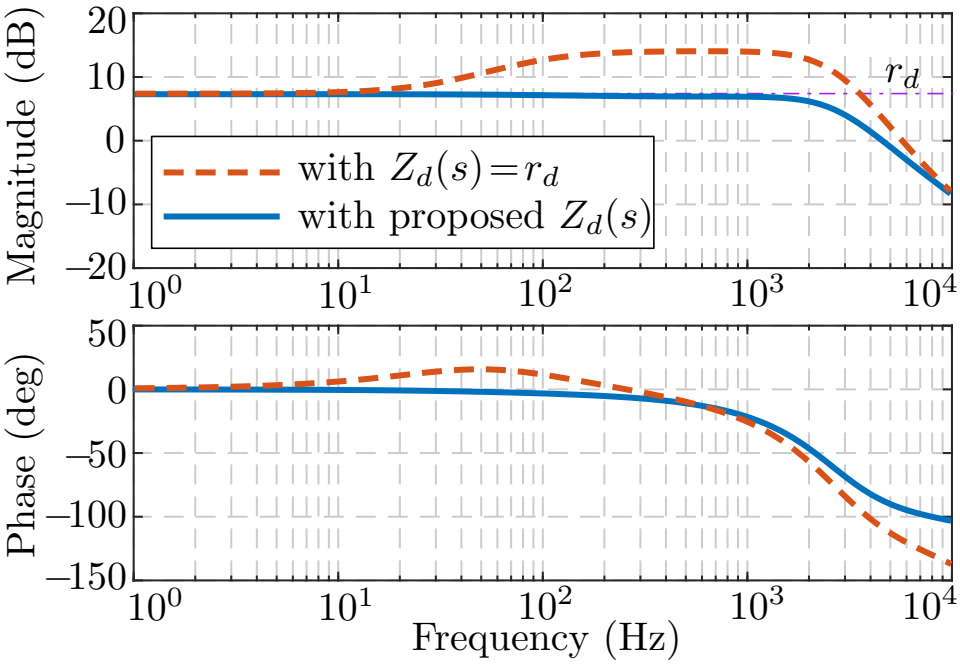


Fig. 3.8 Bode diagram of the output impedance of the Boost-type hysteresis droop-controlled converter with proposed $Z_d(s)$ and $Z_d(s) = r_d$.

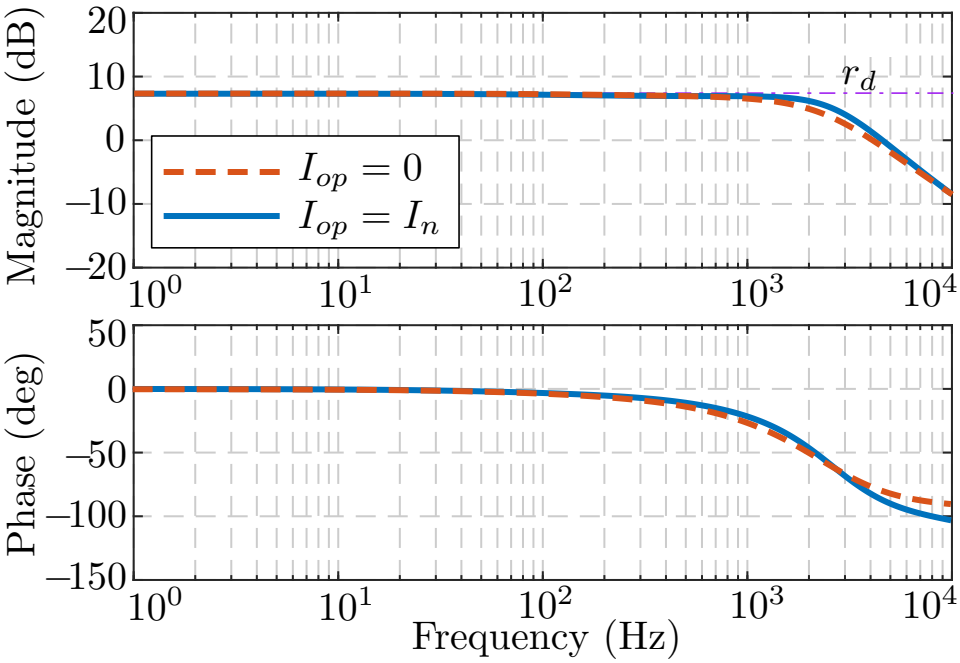


Fig. 3.9 Bode diagram of the output impedance of the Boost-type hysteresis droop-controlled converter under different operation conditions with proposed $Z_d(s)$.

Table 3.1 System Parameters

Parameter	Symbol	Value
Input voltage	V_{in}	200 V
Nominal bus voltage ($I_o = 0$)	V_o	380 V
Nominal Power	P_n	3.0 kW
Nominal output current	I_n	8.30 A
Inductance	L	1.0 mH
Output capacitance	C_o	50 µF
Switching frequency	f_{sw}	20 kHz
Update frequency	f_{up}	200 kHz
Oversampling factor	N	10
Droop coefficient	r_d	2.4 V/A
Cutoff frequency of Tif	ω_{h}	414 rad/s
Proportional gain of PI	k_p	1.31
Integral gain of PI	k_i	1500
Ramp slope	k_d	$2.25e^{-6}$
Derivative gain	g_d	10
Hysteresis window height	β	5.56

3.4 Experimental Results

To experimentally demonstrate the performance of the hysteresis droop controller, three 3 kW Boost-type DER converters are used. The system parameters are listed in Tab. 3.1. The schematic picture of the experimental prototypes is shown in Fig. 3.10, where converters n.1 and n.2 are used for droop control and converter n.3 is used as the perturbation unit for the impedance measurement. The DSP adopted in the prototypes is TMS320F28379D. More details of this prototype can be found in Appendix A.

The measured output impedances with $Z_d(s) = r_d$ and with $Z_d(s)$ given by (3.21) are shown in Fig. 3.11 and Fig. 3.12. As can be seen, the results are in a very good agreement with the analytical results and that the proposed implementation using (3.21). Using $Z_d(s) = r_d$, Fig. 3.13 and Fig. 3.14 are showing the output voltage transients due to a $3A$ step load variation obtained by the electronics load, while converters n.3 was turned off. The voltage variation is about $6.7V$ while the steady-state variation is $3.6V$. The improvements obtained with the proposed approach are shown in Fig. 3.15 and Fig. 3.16. As expected, the bus voltage variations never exceed the steady-state variation of $3.6V$.

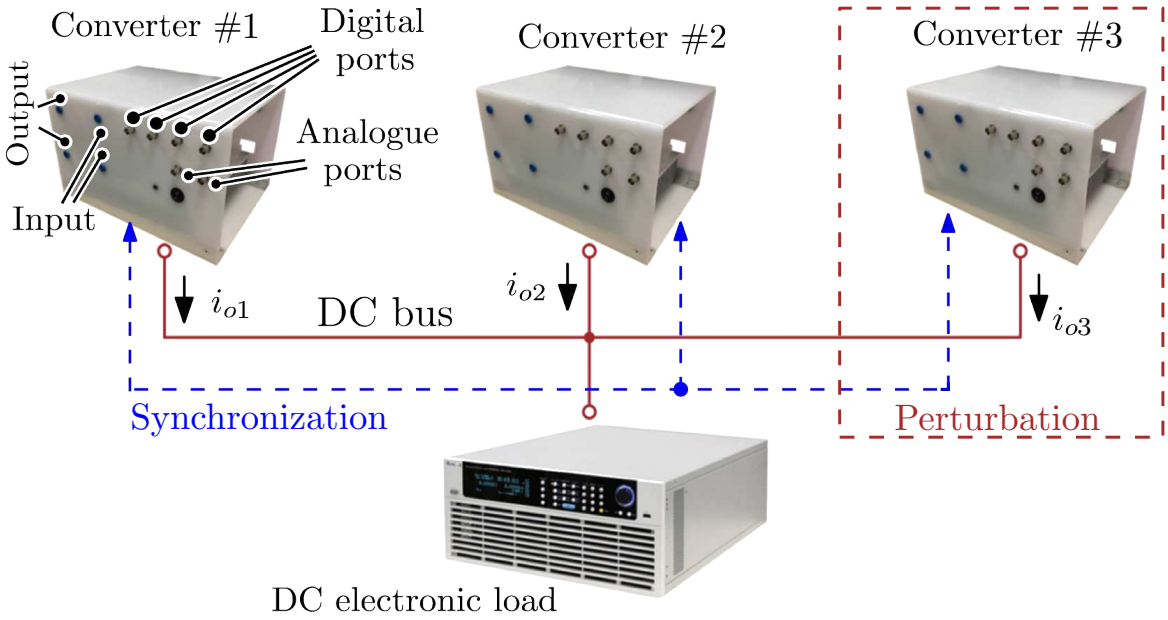


Fig. 3.10 Experimental setup

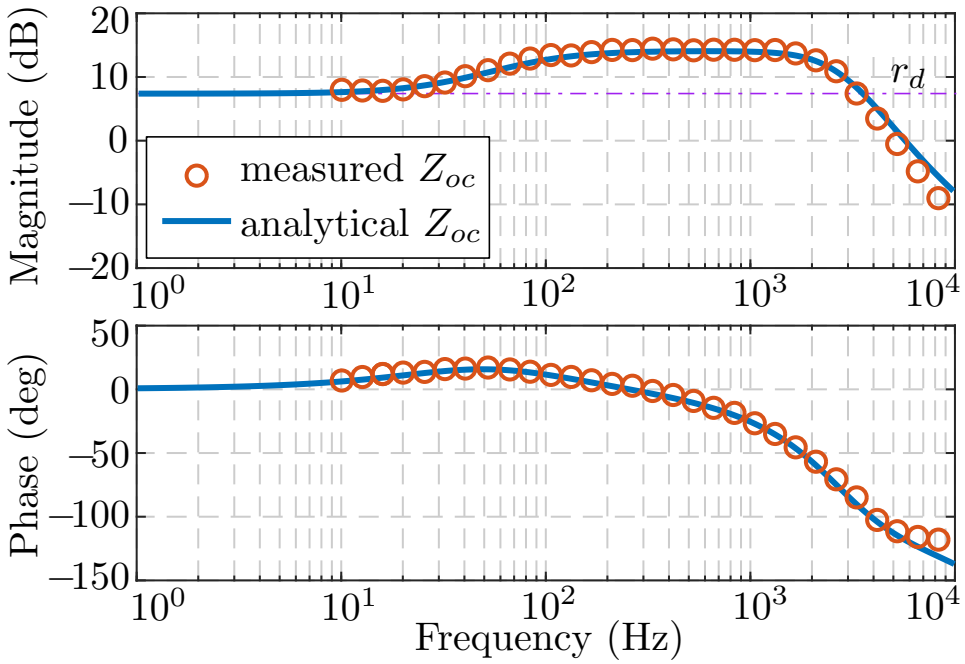


Fig. 3.11 The measured and theoretical output impedance $Z_{oc}(s)$ of one Boost-type hysteresis droop-controlled converter with $Z_d(s) = r_d$.

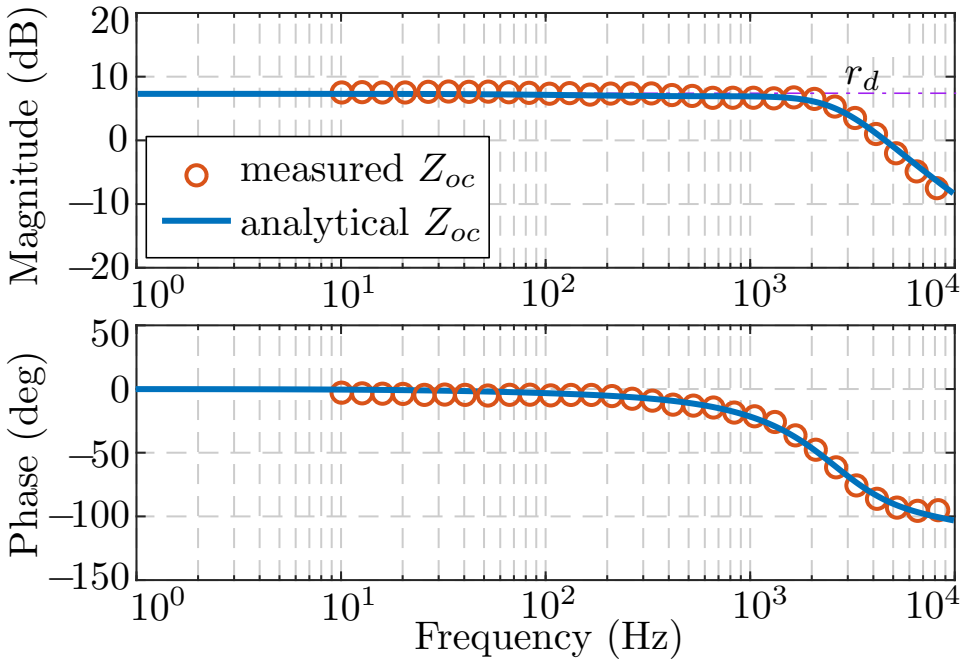


Fig. 3.12 The measured and theoretical output impedance $Z_{oc}(s)$ of one Boost-type hysteresis droop-controlled converter with proposed $Z_d(s)$.

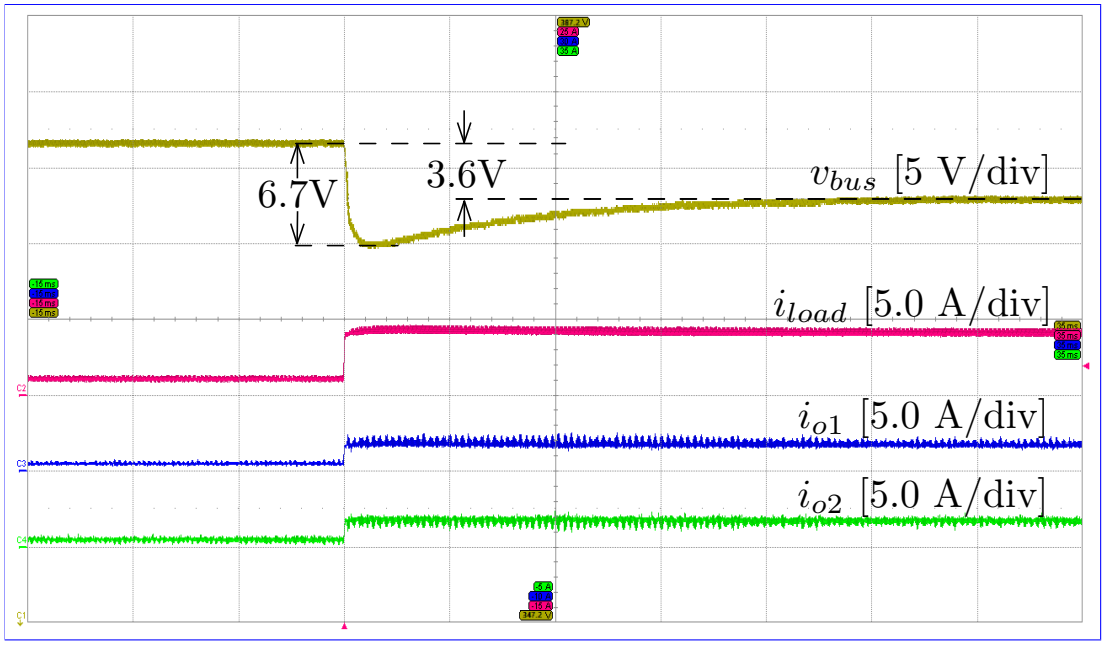


Fig. 3.13 Experimental results under a 3A step up load change of constant current load in Boost-based microgrid with $Z_d(s) = r_d$.

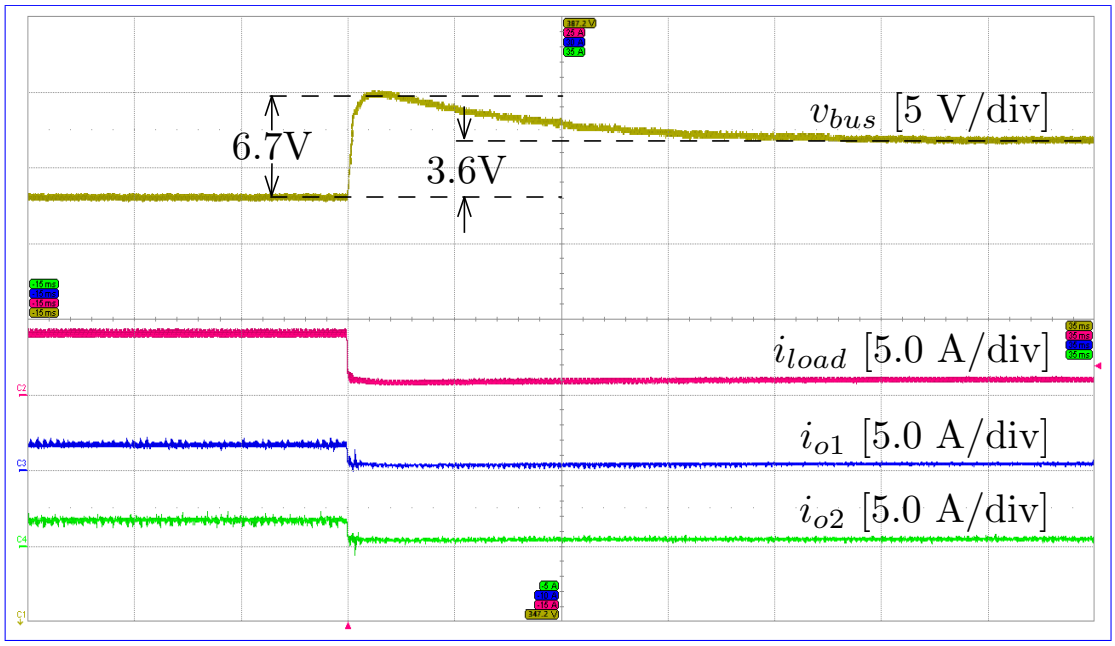


Fig. 3.14 Experimental results under a 3A step down, load change of constant current load in Boost-based microgrid with $Z_d(s) = r_d$.

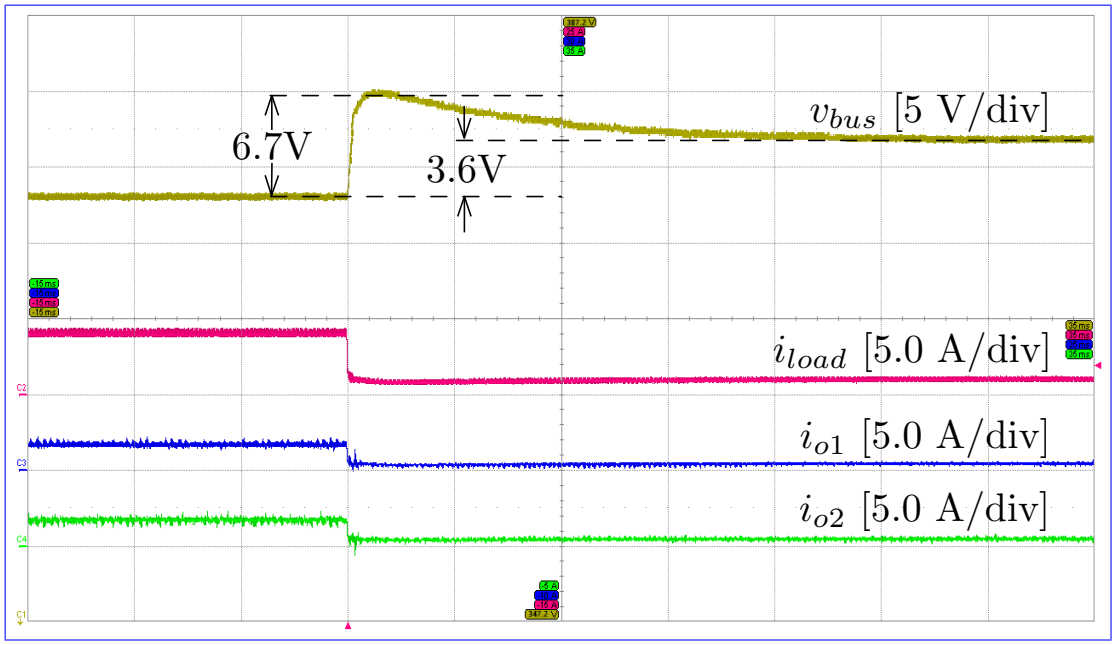


Fig. 3.15 Experimental results under a 3A step up load change of constant current load in Boost-based microgrid with proposed $Z_d(s)$.

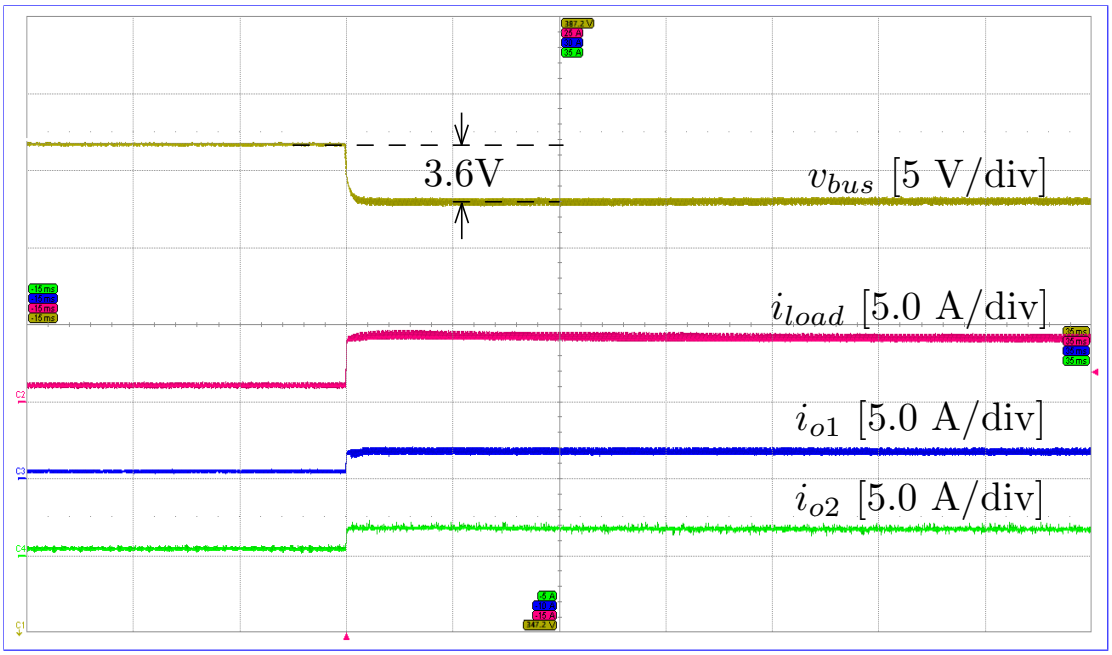


Fig. 3.16 Experimental results under a 3A step down load change of constant current load in Boost-based microgrid with proposed $Z_d(s)$.

3.5 Summary

The chapter presents an extension of a digital hysteresis modulation for droop controlled DER converters in DC microgrids. The main scope is to achieve the shaping of the output converter impedance so that it can be considered almost resistive within the controller bandwidth, without amplification of the output impedance in the whole frequency range. This is achieved also with a very small output capacitor, as the proposed digital hysteresis approach gives a fast dynamic response by avoiding any intrinsic delay of PWM modulator and exhibits an inherent derivative action. An approximated small-signal model is also used to design the controller parameters and to shape the closed-loop output impedance. Experimental results on two parallel Boost converters, having $P_n = 3$kW, $V_o = 380$V, and $f_{sw} = 20$kHz, verify the validity of the approach, showing a resistive-capacitive output impedance with $50\mu F$ output capacitance.

Chapter 4

A Per-Phase Power Controller for Smooth Transitions to Islanded Operation

4.1 Introduction

In chapter 2 a fast response hysteresis controller is proposed to have higher bandwidth for inner control loops, and in chapter 3, a DE-PWM is discussed, allowing to push significantly the bandwidth of the inner loop controllers. Having higher bandwidth for the inner loop controllers shown in Fig. 4.1 , makes it possible to have faster power control dynamics in ac or dc microgrids.

Low-voltage grids are steadily evolving to provide the advanced services that are required in the forthcoming energy scenario [46, 71]. Examples of crucial features are *i*) flexible power control, to allow resilience to variable power demand [17] and participation to transactive energy markets [85], *ii*) continuity of service, via islanded operation in response to adverse localized events interrupting the mainstream electricity supply, and *iii*) optimal power quality, in terms of power factor and balanced power absorption [96].

The variegate requirements are commonly managed via hierarchical control systems, as shown in Fig. 4.2, of which the droop control constitutes the primary layer [39, 71]. Droop control with electronic power converters (EPCs) controlled as voltage sources is indeed widely used in ac microgrids [86, 82]. It sports the advantage of supporting the grid voltage and the capability of adapting the inverters voltage references so as to automatically share the power needs in islanded grids [82]. Actually, droop controlled EPCs are often referred to as playing a grid-forming functionality, in the sense that the grid voltage is determined by their aggregate contribution [54]. Fig. 4.2 also reports zero-level control, consisting of voltage and current controllers receiving reference signals from the primary controller [39, 71, 64].

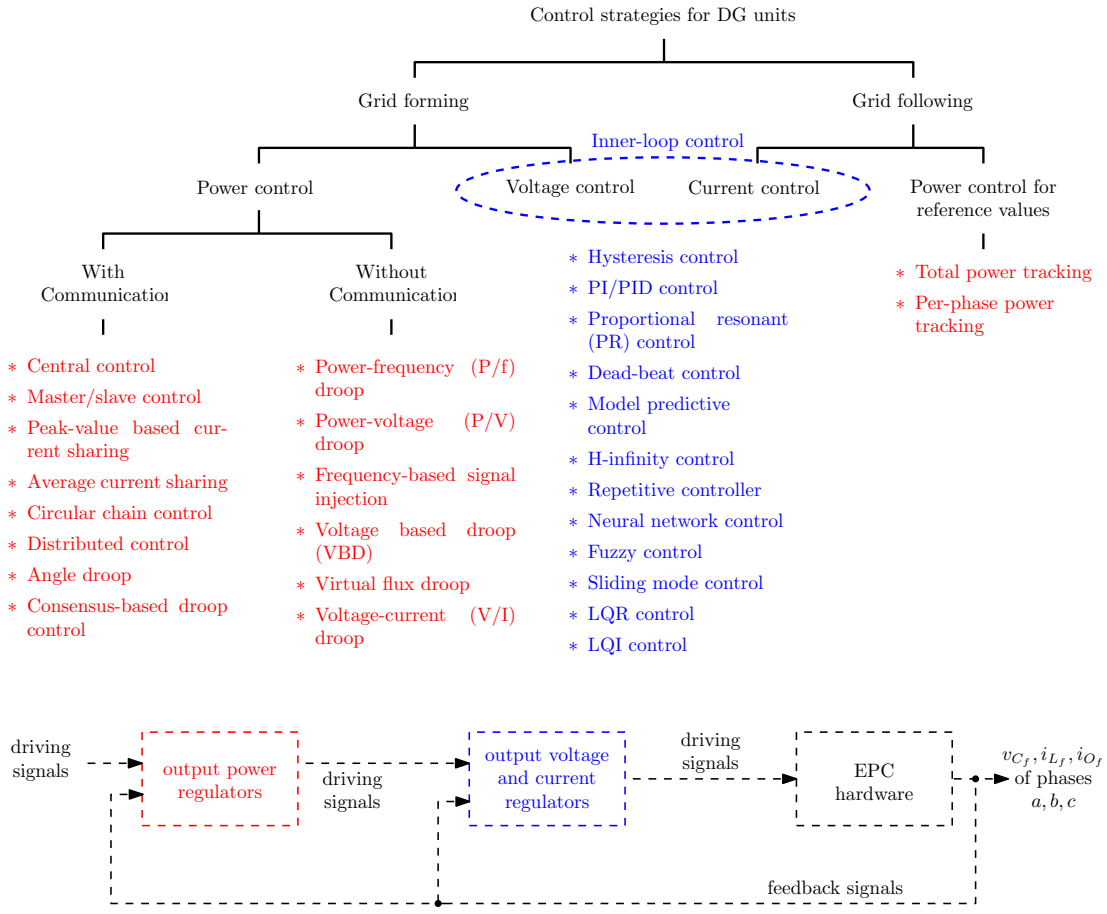


Fig. 4.1 Control techniques for inner-loop control and primary control.

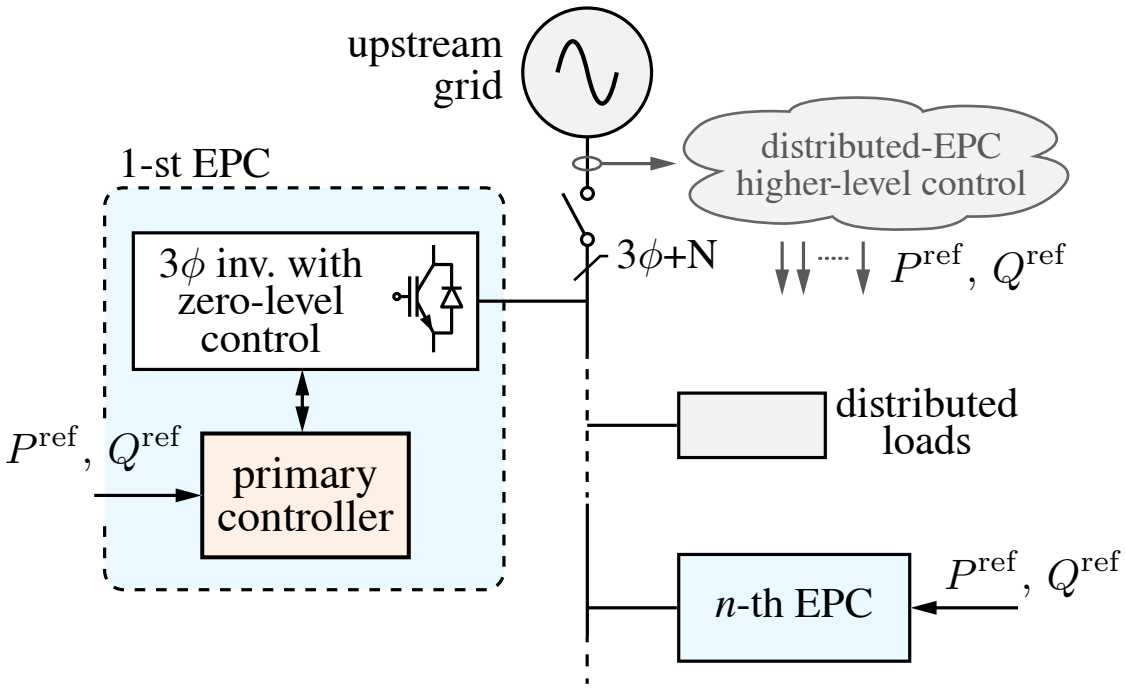


Fig. 4.2 Microgrid scenario with islanded capabilities and distributed electronic power converters (EPCs) accepting power references issued by higher-level control methods. The proposed solution relates to the primary controller block.

Various choices are possible for zero-level control implementation [90, 64, 84, 83], herein, natural reference frame *abc* with linear voltage and current regulators is considered.

On the other hand, output power control requires specific provisions. Two opposite needs are present, that is, *i*) supporting the grid voltage by adapting the inverter output power according to the droop laws, useful especially during islanded operation [41], *ii*) making the output power fixed and independent from grid voltages and loading conditions to allow power control, useful especially during grid-tied operation [84, 83]. These are requirements also considered in forthcoming relevant standards [52]. In [58] the two needs are accomplished considering the total power delivered by the inverter, but per-phase power control is not possible without losing the property of smooth transitions into islanded operation.

However, independent power control of each phase is necessary in several circumstances. In smart electricity grids, distributed EPCs can receive power references computed by optimization algorithms that pursue control goals like loss and current stress minimization. For example, [3] proposes a centralized controller that issues optimal per-phase power references to distributed three-phase EPCs, achieving power-flow controllability at the PCC of a microgrid with the upstream grid. Independent power control is shown in [97] to solve serious power quality issues due to unbalance and nonlinear loads in distribution networks,

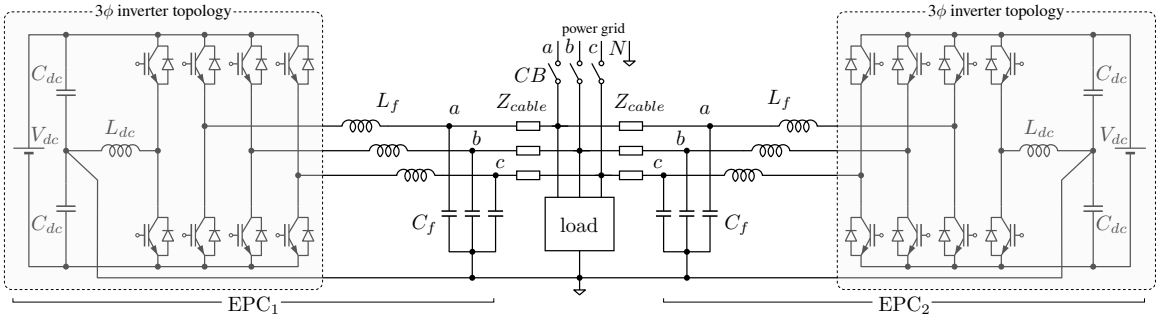


Fig. 4.3 EPCs connected to a three-phase four-wire low-voltage network.

Table 4.1 Functionalities of EPC primary controllers

Control kind	**islanded operation**	**grid-tied / islanded transitions**	**three-phase power-tracking**	**per-phase power tracking**	**ref.**
Grid-feeding	-	-	+	+	[90]
Traditional droop	+	+	-	-	[39]
Angle droop	+	-	-	-	[31]
Droop with 3ϕ power tracking	+	+	+	-	[58]
Proposed per-phase power tracking	+	+	+	+	herein

in which EPCs capable of flexibly regulating their injected per-phase power would induce greater loss reduction and remarkable power-quality improvements [79]. Similar results are reported in [96, 89, 12, 13]. Per-phase power control is useful in isolated master-slave microgrid architectures too, where centralized controllers with one or multiple master EPCs are present to improve microgrid operation [15, 41]. In such microgrids, per-phase control allows to support the master units in generating the power requests from the loads at the different phases, as shown in [72]. In general, flexible power control is crucial to achieve the control goals aimed for in the, continuously evolving, smart power systems scenario [7, 52].

Solutions have been presented in the literature to allow per-phase control of active-power sharing on four-wire microgrids under unbalanced loads [31, 59], but output power tracking is not considered. On the other hand, the literature reports per-phase output power controllers, like [32], but without considering or including islanded operation capabilities. In fact, the use of the traditional droop control scheme for per-phase power control would lead to unequal frequencies among the phase voltages at the transition to the islanded operation, that is, an unacceptable desynchronization among the phases. To the authors' knowledge, there is a lack of solutions considering per-phase power flow control while preserving the feature of seamlessly transition from the grid-connected into the islanded operation modes.

4.1.1 Outline

This chapter proposes a controller for grid-tied three-phase EPCs, displayed in Fig. 4.3, addressing the challenges discussed above. Specifically, the proposed solution features *i*) independent output power control for each phase of a three-phase four-wires grid-connected inverter, *ii*) smooth transitions into the islanded operation mode, *iii*) operation in islanded conditions, even when multiple parallel connected EPCs integrating the proposed controller are present. Tab. 4.1 shows the features supported by the proposed controller, also compared with other representative solutions described in the literature. The controller is also modeled analytically and analyzed, finally discussing a simple design procedure. The control scheme is presented in Sect. 4.2, its analysis and design is discussed in Sect. 4.3. Sect. 4.4 reports simulation and experimental results showing the obtained controller behavior. Sect. 4.5 concludes the chapter.

4.2 Per-Phase Control Principle

The control principle is to synchronize the inverter by considering the total three-phase active power delivered by the inverter itself and, while operating grid-connected, to achieve per-phase output active and reactive power regulation by adjusting the phase-shift and the voltage amplitude, respectively, of each phase independently. By extending the approach in [58], saturated controllers are employed to perform power control and achieve smooth transitions into the islanded operation.

Fig. 4.4 shows the block diagram of the proposed controller, where the generic x-th phase, $x \in \{a, b, c\}$, is represented. On top of the figure, a P-f droop relation processes the total three-phase power $P_{3\phi}$ exchanged at the inverter output and provides the angle $\varphi_{3\phi}$, which is the integral of the angular frequency given by the traditional droop characteristic:

$$\omega^* = \omega_0 + k_{p,3\phi}\left(P^*_{3\phi} - P_{3\phi}\right) \tag{4.1}$$

where ω_0 is the nominal frequency, $k_{p,3\phi}$ is the droop coefficient, and $P^*_{3\phi}$ is a reference three-phase power [82]. The phase angle $\varphi_{3\phi}$, rotating at frequency ω^*, is synchronized with the grid and used to derive the angle of each of the phases, as illustrated in Fig. 4.5. In this way, the synchronization capability of the droop control [104] is retained and exploited. The top branch in Fig. 4.4 is called synchronization branch hereinafter.

The angle φ_x of each phase is computed by adding to the synchronized angle $\varphi_{3\phi}$ the nominal phase angle φ_x^{nom} of the specific phase (i.e., 0, $-2/3\pi$ or $+2/3\pi$ for phases a, b, c, respectively) and by adjusting the result by the quantity $\Delta\varphi_x$ that aims at the desired active

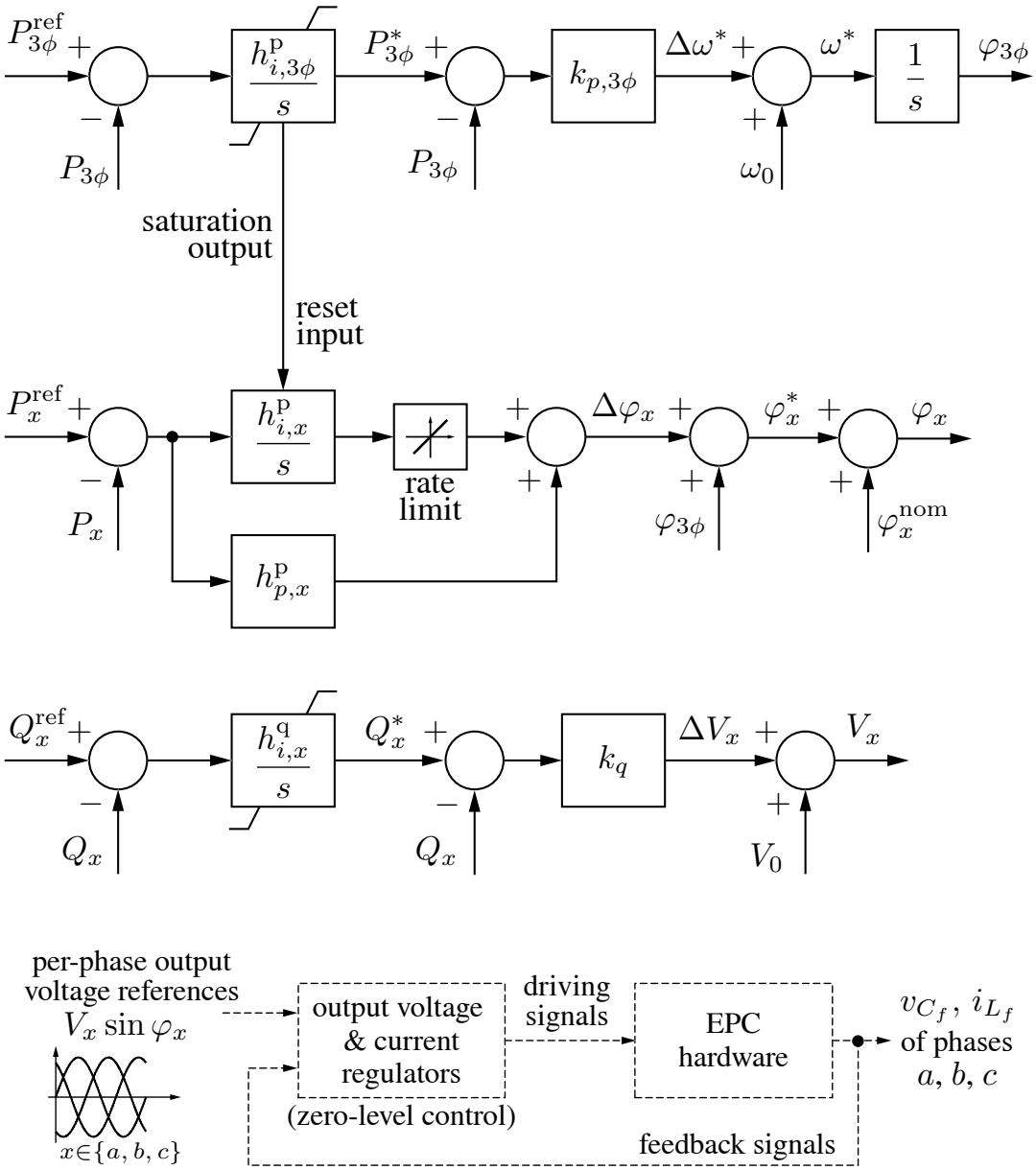


Fig. 4.4 Per-phase power controller. The top, synchronization branch provides a reference angle $\varphi_{3\phi}$ to the three phases, represented by the generic symbol x (i.e., a, b, c). The angle and amplitude of each phase are adjusted for per-phase power control. The resulting references $V_x \sin \varphi_x$ are given to EPC current and voltage regulators (zero-level control) for output voltage control.

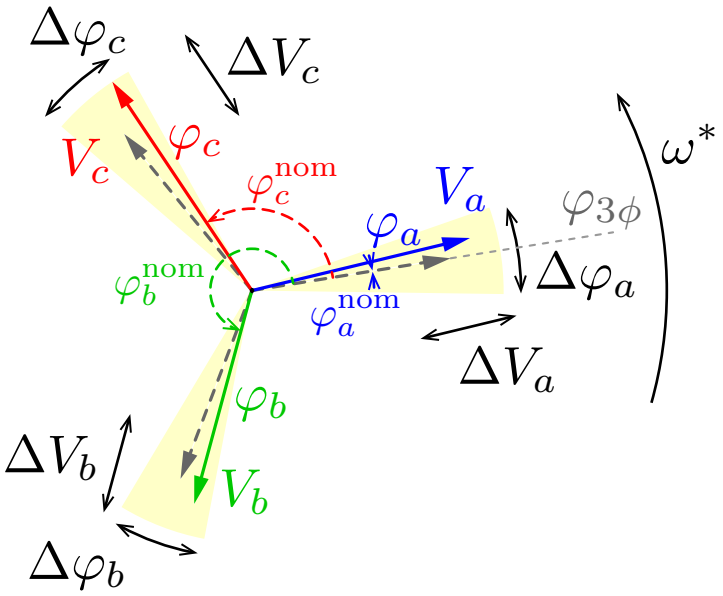


Fig. 4.5 Controlled quantities by the proposed per-phase control. Highlighted the possible phase variations $\Delta\varphi_x$ and amplitude variations ΔV_x for the desired active and reactive, respectively, per-phase power exchange.

power P_x at phase x. Nominal voltage amplitudes V_0 are similarly adjusted by the quantity ΔV_x for reactive power control. The instantaneous voltage reference value for the x-th phase results:

$$V_x \sin(\varphi_x) = (V_0 + \Delta V_x) \sin\left(\varphi_{3\phi} + \Delta\varphi_x + \varphi_x^{\text{nom}}\right) \tag{4.2}$$

where $\varphi_{3\phi}$ is the integral of the frequency ω^* in (4.1), while ΔV_x and $\Delta\varphi_x$ are constant terms in steady-state. Notably, variations $\Delta\varphi_x$ and ΔV_x are small and depend on the injected power and the interconnection impedances among sources. As commonly done with droop control, mainly inductive interconnection impedances are considered herein, which may be related to the characteristics of the grid or it may be imposed by proper converter control provisions [82, 39].

The controllers computing the introduced quantities, in Fig. 4.5, are discussed in the following.

4.2.1 Grid-connected operation

In order to achieve total three-phase output power tracking, which is possible during grid-tied operation [26], $P_{3\phi}^*$ is adjusted by a three-phase power regulator:

$$H_{3\phi}^{\text{p}}(s) = \frac{h_{i,3\phi}^{\text{p}}}{s} \tag{4.3}$$

Its control action modifies the total three-phase power $P_{3\phi}$ delivered by the inverter.

To achieve per-phase power tracking, the obtained $\varphi_{3\phi}$ is then adjusted phase-by-phase as displayed by the central blocks in Fig. 4.4, referring to the generic x-th phase. Here, a proportional-integral controller, denoted as:

$$H_x^{\mathrm{p}}(s) = h_{p,x}^{\mathrm{p}} + \frac{h_{i,x}^{\mathrm{p}}}{s} \tag{4.4}$$

produces the phase shift $\Delta\varphi_x$ that adds to the instantaneous three-phase angle $\varphi_{3\phi}$ and allows the phase power P_x to follow the respective reference power P_x^{ref} during grid-tied operation.

4.2.2 Islanded operation

Within an islanded subsystem, the generated and dissipated power must balance exactly, then, a transition into islanded operation makes output power control no more possible and automatically leads the power regulator $H_{3\phi}^{\mathrm{p}}$ in (4.3) into saturation. Consistently, the integral part of the per-phase regulator H_x^{p} is also disabled, as shown in Fig. 4.4. The saturation limits $P_{3\phi}^{*\max}$ or $P_{3\phi}^{*\min}$ can be designed considering the principles presented in [58], and reviewed in the next Sect. 4.3.2. Remarkably, during the islanded mode of operation, the controller behaves as a traditional droop controller, by which the converter frequency ω^* changes linearly with the total delivered three-phase power:

$$\omega^* = \omega_0 + k_{p,3\phi}\left(P_{3\phi}^{*\mathrm{sat}} - P_{3\phi}\right) \tag{4.5}$$

where $P_{3\phi}^{*\mathrm{sat}}$ is a constant saturation limit, namely, $P_{3\phi}^{*\max}$ or $P_{3\phi}^{*\min}$, further discussed in the following Sect. 4.3.2.

For what concerns reactive power control, per-phase reactive power control is more straightforward, because it acts on the amplitude of the generated voltages and does not affect the phases of the voltages, which are critical for synchronization. Then, a simple saturated controller can be directly applied to each phase, as described in [58].

Finally, it is worth to highlight the use of a rate limiter at the output of the integral part of H_x^{p}, which gradually brings to zero the corresponding phase adjustment when it is not required (i.e., during islanded operation). Instead, the proportional part can be optionally kept, in order to improve the dynamics and power sharing among multiple inverters operating in parallel [31, 70, 100, 41].

4.3 Stability Analysis and Control Design

The controller described in Sect. 4.2 presents two operation modes, namely, the grid-connected and the islanded operation mode. In the former operation mode, the controller $H^{\mathrm{p}}_{3\phi}$ in the synchronization branch and the per-phase power controllers H^{p}_{x} are active. Differently, during islanded operation, these regulators saturate, which reduces the control system dynamics to those of the traditional droop control, where the converter frequency ω^* changes linearly with the total delivered three-phase power, as in (4.5). This latter operation mode is analyzed in many relevant papers [103, 75], while the grid-connected behavior is peculiar to the proposed solution and it is analyzed next.

4.3.1 Small-signal analysis

Let us model the EPC by its Thevenin's representation, as a voltage source with series output impedance, operating connected to a voltage source representing the grid voltage [103]. Be $V_x\angle\varphi_x$ the EPC voltage, $V_g\angle 0$ the grid voltage, ω_g the system frequency and $Z\angle\theta_Z$ the EPC output impedance. The active and reactive power exchange among the two sources considering the generic x-th phase result [24, 103]:

$$P_x = \frac{V_g}{Z}\left[(V_x\cos\varphi_x - V_g)\cos\theta_Z + V_x\sin\theta_Z\sin\varphi_x\right] \tag{4.6}$$

$$Q_x = \frac{V_g}{Z}\left[(V_x\cos\varphi_x - V_g)\sin\theta_Z - V_x\cos\theta_Z\sin\varphi_x\right] \tag{4.7}$$

Assuming a mainly inductive impedance $Z = j\omega_g L_x$ and small phase-differences between the inverter output voltage and the grid voltage, the following simplified model can be derived:

$$P_x \simeq \frac{V_g V_x}{\omega_g L_x}\varphi_x \tag{4.8}$$

$$Q_x \simeq \frac{V_g\,(V_x - V_g)}{\omega_g L_x} \tag{4.9}$$

Based on (4.8) and (4.9), the small-signal model of the control system in Fig. 4.4 and the plant can be derived for stability analysis and regulators design.

The system phase at the output of the synchronization branch, on top of Fig. 4.4, is:

$$\varphi_{3\phi} = \frac{1}{s}\left[\omega_0 + k_{p,3\phi}\left[H^{\mathrm{p}}_{3\phi}\sum_x\left(P^{\mathrm{ref}}_x - P_x\right) - \sum_x P_x\right]\right] \tag{4.10}$$

where $H^{\mathrm{p}}_{3\phi}$ is defined in (4.3). The three per-phase output powers can be written by using (4.8) as:

$$P_x = \frac{V_x V_g}{\omega_g L_x}\left[H^{\mathrm{p}}_x\left(P^{\mathrm{ref}}_x - P_x\right) + \varphi_{3\phi} + \varphi^{\mathrm{nom}}_x\right] \tag{4.11}$$

where, to simplify the notation, the equal sign is used in the sense of small-signal linearized modelling. By collecting the per-phase quantities in column vectors, which are denoted hereafter by a bar [e.g., $\bar{P} = (P_a, \ldots, P_c)^T$ for the per-phase powers P_x, $x = a, b, c$], (4.10) and (4.11) can be written in matrix form for the three-phase system as:

$$\varphi_{3\phi} = \frac{1}{s}\left[\bar{\omega}_0 + k_{p,3\phi}\left[H^{\mathrm{p}}_{3\phi}\mathbb{1}_3^T\left(\bar{P}^{\mathrm{ref}} - \bar{P}\right) - \mathbb{1}_3^T\bar{P}\right]\right] \tag{4.12}$$

$$\bar{P} = \Gamma\left[H^{\mathrm{p}}_x\left(\bar{P}^{\mathrm{ref}} - \bar{P}\right) + \varphi_{3\phi}\mathbb{1}_3 + \bar{\varphi}^{\mathrm{nom}} - \bar{\varphi}_G\right] \tag{4.13}$$

where $\mathbb{1}_3$ is a 3×1 column vector of ones, Γ is a 3×3 diagonal matrix with elements $V_x V_g/\omega_g L_x$, and $\bar{\varphi}_G$ represents the instantaneous phase of the grid voltages.

For stability analysis, the exogenous inputs appearing in (4.12) and (4.13), namely, $\bar{\omega}_0$, $\bar{P}^{\mathrm{ref}}$, $\bar{\varphi}^{\mathrm{nom}}$, and $\bar{\varphi}_G$, can be neglected, yielding:

$$\varphi_{3\phi} = \frac{1}{s}k_{p,3\phi}\left(-H^{\mathrm{p}}_{3\phi}\mathbb{1}_3^T - \mathbb{1}_3^T\right)\cdot\bar{P} \tag{4.14}$$

$$\bar{P} = (I_3 + H^{\mathrm{p}}_x\Gamma)^{-1}\Gamma\cdot\left(\varphi_{3\phi}\mathbb{1}_3\right) \tag{4.15}$$

where I_3 represents the 3×3 identity matrix. Finally, (4.14) and (4.15) allow to write the loop gain of the control loop involving $\varphi_{3\phi}$:

$$T_{\varphi_{3\phi}} = -k_{p,3\phi}\left(H^{\mathrm{p}}_{3\phi} + 1\right)\mathbb{1}_3^T\left(I + H^{\mathrm{p}}_x\Gamma\right)^{-1}\Gamma\,\mathbb{1}_3 \tag{4.16}$$

and to analyze the poles of the closed-loop system, which correspond to the zeroes of $1 + T_{\varphi_{3\phi}}$. This is performed in the experimental Sect. 4.4, considering the used prototype parameters.

4.3.2 Controller design

The design of the controller $H^{\mathrm{p}}_{3\phi}$ in the synchronization branch and of the per-phase controllers H^{p}_x can be performed on the basis of the analysis presented above.

Time-scale separation is exploited in the following, allowing a practical design procedure for the two regulators. Specifically, the loop involving $H^{\mathrm{p}}_{3\phi}$ is designed faster than the per-phase power control loops involving H^{p}_x, which allows to neglect the effect of the per-phase controller (i.e., terms φ_x are assumed constant) while considering the design of $H^{\mathrm{p}}_{3\phi}$. Under

this assumption, and by noticing that the resulting regulation loop is in a unitary feedback configuration, the loop gain relevant to $H^{\mathrm{p}}_{3\phi}$ can be written as:

$$T_{P_{3\phi}} = \frac{k_{p3\phi}\frac{1}{s}\left(3\frac{V_x V_g}{\omega_g L_x}\right)}{1+k_{p3\phi}\frac{1}{s}\left(3\frac{V_x V_g}{\omega_g L_x}\right)} = \frac{1}{1+s/\omega_{p,3\phi}}, \qquad \omega_{p,3\phi} = k_{p3\phi}\left(3\frac{V_x V_g}{\omega_g L_x}\right) \tag{4.17}$$

Similarly, the loop-gain relevant to the per-phase controller H^{p}_{x} is:

$$T_{P_x} = \frac{V_g V_x}{\omega_g L_x} \tag{4.18}$$

which is a constant term. On this basis, the regulators coefficients $h^{\mathrm{p}}_{i,3\phi}$ with (4.17) and $h^{\mathrm{p}}_{p,x}$ and $h^{\mathrm{p}}_{i,x}$ with (4.18) can be easily found.

On the light of the considerations above, parameter settings of the controller in Fig. 4.4 can be performed as follows.

1. The droop coefficients are set, as commonly done, considering the maximum frequency and voltage variations, namely, $\Delta\omega_g^{\max}$ and $\Delta V^{\max}$, respectively, and the converter rated power S_N:
$$k_{p,3\phi} = \frac{\Delta\omega_g^{\max}}{2S_N} \quad k_q = \frac{\Delta V_g^{\max}}{2S_N} \tag{4.19}$$

2. The three-phase regulator integrative gain is set considering the loop-gain (4.17). For example, by basic regulators design, if a phase-margin of at least 60° is targeted, the chosen crossover frequency $\omega_{cross,3\phi}$ should not exceed about a half of the pole frequency $\omega_{p,3\phi}$ in (4.17). Under this assumption, the integrative gain can be set to:
$$h^{\mathrm{p}}_{i,3\phi} = \omega_{cross,3\phi} \tag{4.20}$$

3. The per-phase reactive power regulator can be set as done in [58], being it possible to set the voltage amplitude of each phase independently from the voltage amplitude of the other phases.

4. The per-phase power regulator H^{p}_{x} can be set considering the loop gain (4.18) and a crossover frequency significantly smaller than the one set for the synchronization control loop $\omega_{cross,3\phi}$.

5. The saturation limits are set to ensure power reference tracking within the whole allowed frequency and voltage range, as described in [58], that is:

$$P_{3\phi}^{*\max} = -P_{3\phi}^{*\min} = S_N + \frac{\Delta\omega_g^{\max}}{2k_{p,3\phi}} \tag{4.21}$$

$$Q_x^{*\max} = -Q_x^{*\min} = \frac{S_N}{3} + \frac{\Delta V_g^{\max}}{2k_q} \tag{4.22}$$

notably, these limits are fixed and depend on the nominal parameters of the EPC and the grid.

4.4 Experimental Results

The proposed controller was tested in simulation and by means of a laboratory-scale experimental prototype visible in Fig. 4.6 implementing the system in Fig. 4.3. The main hardware parameters are reported in Tab. 4.2. The converters were implemented using eight Imperix PEB8032 half-bridge modules, while the controller was deployed on an Imperix B-Box RCP embedding a Xilinx Zynq 7030 SoC. All the control blocks were executed once per switching period on the DSP module of the Xilinx SoC while the modulators and the protection blocks were executed on its FPGA module. As visible in Fig. 4.3, a split-link inverter with active balancing is used in the prototype to control the neutral-point voltage despite of the presence of neutral currents while supplying unbalanced powers, as done in [105]. Other solutions may be successfully adopted too [57, 94]. Besides, any other inverter topologies with related zero-level control, namely, current and voltage regulators, capable of imposing the line to neutral voltages, including, for example, multi-level converters and other more advanced topologies, may be used for the implementation of the circuit enclosed in the dashed box in Fig. 4.3.

The controller is designed by the procedure described in Sect. 4.3.2, resulting in the parameters listed in Tab. 4.3. The dynamics of the obtained closed-loop control can be studied by the analysis in Sect. 4.3.1, specifically, the loop-gain $T_{\varphi_{3\phi}}$ in (4.16). Fig. 4.7 displays the pole-zero plot of the transfer function $1/\left(1+T_{\varphi_{3\phi}}\right)$. Notably, the system presents stable and well damped poles, all lying on the right-half-plane.

The measured performance of the controller considering the described experimental setup are reported in the following. Six conditions are considered, namely, unbalance power reference step variation, balance power reference step variation, grid-tied to islanded transition, parallel operation while islanded, reactive power control, and islanded to grid-connected transition.

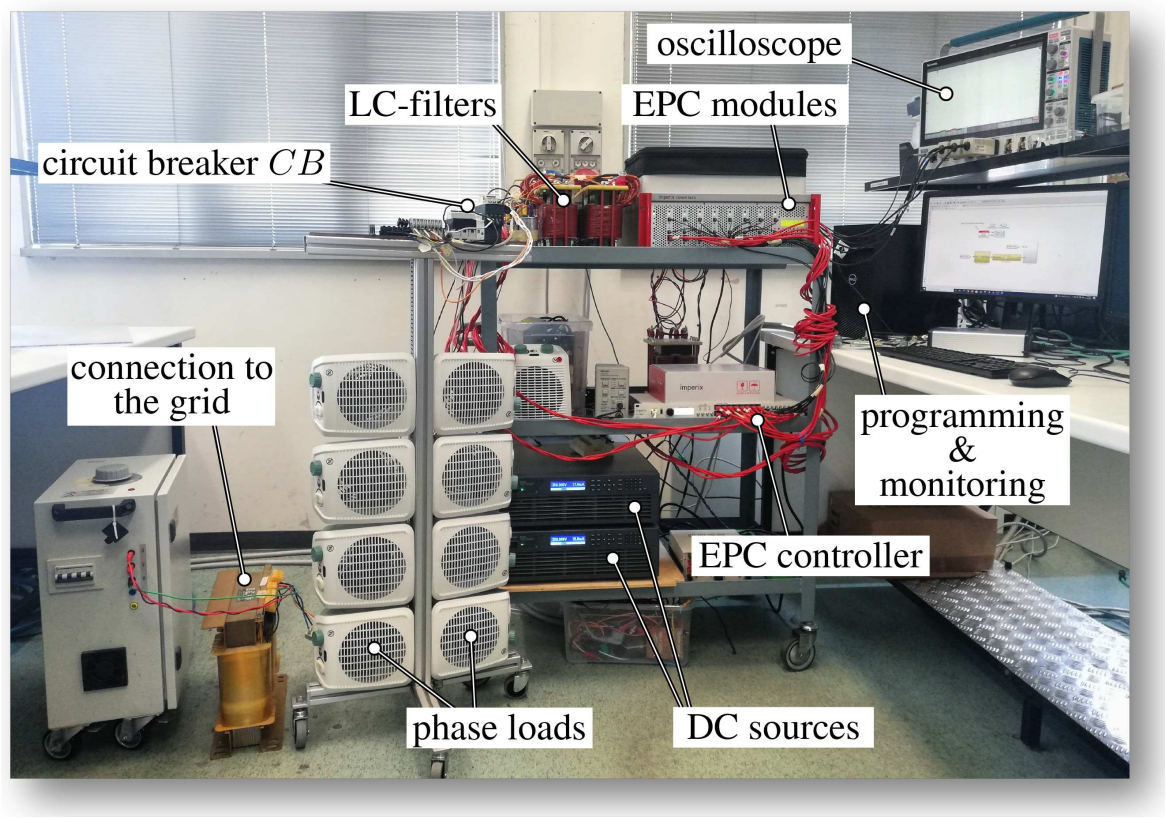


Fig. 4.6 Photo of the experimental setup implementing the system in Fig. 4.3.

Table 4.2 Inverters (EPCs) parameters

Parameter		**Value**	
dc-link voltage	V_{dc}	350	V
dc-link capacitor	C_{dc}	3.3	mF
dc-link inductor	L_{dc}	2.5	mH
output filter capacitor	C_f	50	µF
output filter inductor	L_f	1.5	mH
switching frequency	f_{sw}	20	kHz
nominal power rating	S_N	3	kVA
nominal grid voltage rms	V_g^{nom}	110	V
nominal grid frequency	ω_g^{nom}	$2\pi \cdot 50$	rad/s
grid frequency range	$\omega_g^{\text{min}}, \omega_g^{\text{max}}$	$2\pi \cdot [49, 51]$	rad/s

Table 4.3 Control parameters

Parameter		Value	
P-f droop coefficient	$k_{p,3\phi}$	0.28571	mHz/W
V-Q droop coefficient	k_q	1.6	mV/VAr
3-phase P contr. integ. gain	$h^{\mathrm{p}}_{i,3\phi}$	8	1/s
3-phase P saturation limit (4.21)	$P^{*\max}_{3\phi}$	± 7	kW
per-phase P contr. integ. gain	$h^{\mathrm{p}}_{i,x}$	0.875	mrad/Ws
per-phase P contr. prop. gain	$h^{\mathrm{p}}_{p,x}$	49.867	µrad/W
per-phase Q contr. integ. gain	$k^{\mathrm{q}}_{i,x}$	180	1/s
per-phase Q saturation limit (4.22)	$Q^{*\max}_{x}$	$\pm 7/3$	kVAr
nominal voltage amplitude	V_0	$\sqrt{2}\cdot 110$	V
nominal frequency	ω_0	$2\pi\cdot 50$	rad/s
maximum frequency variation	$\Delta\omega_g^{\max}$	4	% ω_0
maximum voltage variation	$\Delta V_g^{\max}$	10	% V_0

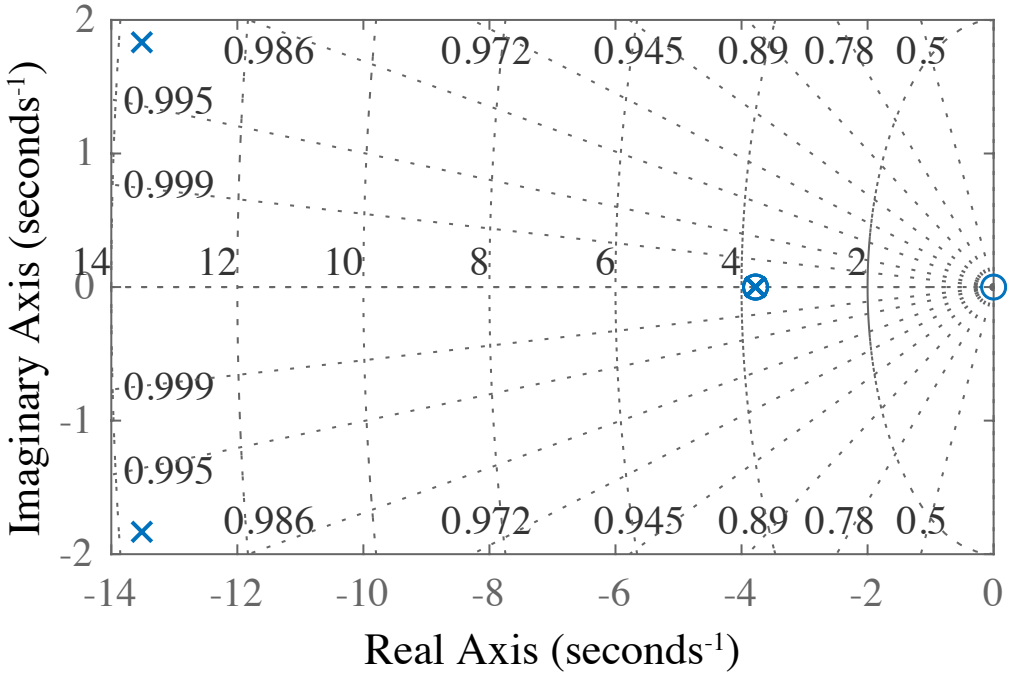


Fig. 4.7 Pole-zero plot of the controller in Fig. 4.4 coupled with the system in Fig. 4.3 and with parameters in Tab. 4.2 and Tab. 4.3.

Comparisons with simulation results are also reported. The models were developed in MatLab/Simulink® to implement the controller, in Fig. 4.4, coupled with the Thevenin's representation of the EPC and the grid, consistently with the assumptions made at the beginning of Sect. 4.3.1.

The followings figures, display the most significant experimental waveforms. Besides the instantaneous three-phase voltages that are always reported, the subfigures on the top display the measured output current for each phase and the phase displacement with respect to the first phase (i.e., $\varphi_b^* - \varphi_a^*$ and $\varphi_c^* - \varphi_a^*$), the subfigures on the bottom display the voltage amplitudes ΔV_a, ΔV_b, and ΔV_c and the frequency deviation $\Delta\omega^*$. The results are discussed in the following.

4.4.1 Unbalanced power reference step variation

Fig. 4.8 displays the response to a step change of the output power reference of a phase during grid-connected operation with EPC_1 connected to the main grid while EPC_2 is disabled. In this test, a reference step $P_c^{\text{ref}} : 0 \rightarrow 1\,\text{kW}$ is applied, while all the other active and reactive power references are kept to zero. The top figure in Fig. 4.8 shows that only phase-c increases the delivered current while the currents of the other phases—that are displayed with magnified scale—show just small, transient variations. A major phase displacement is observed in phase-c due to the increased power injection. The bottom figure in Fig. 4.8 displays the evolution of references V_1, V_2, and V_3, by means of the voltage variations ΔV_x, and the frequency variation $\Delta\omega^*$. Variations can be observed on phase-c due to not perfectly inductive interconnection impedances (measured X/R ratio of about 4.5), while ω^* does not change in steady-state, being it fixed by the main grid voltage.

Using the acquired waveforms, it is possible to compute the delivered per-phase active power and compare the results with the simulation models used to validate the analysis presented in Sect. 4.3.1. This is done in Fig. 4.10a, which shows good correspondence among simulation and experimental results.

4.4.2 Balanced power reference step variation

Fig. 4.9 displays the response to a step change of the power reference of all the three-phases during grid-connected operation with EPC_1 connected to the main grid while EPC_2 is disabled. In this test, a reference step $P_x^{\text{ref}} : 0 \rightarrow 1\,\text{kW}$ is applied, while reactive power references are kept to zero. The top figure in Fig. 4.9 show that the whole three-phase voltage frame angle $\varphi_{3\phi}$ is adjusted under the effect of $\Delta\omega^*$ in the upper block in Fig. 4.4, bringing to negligible variations of phase displacements $\varphi_b^* - \varphi_a^*$ and $\varphi_c^* - \varphi_a^*$. The bottom figure in

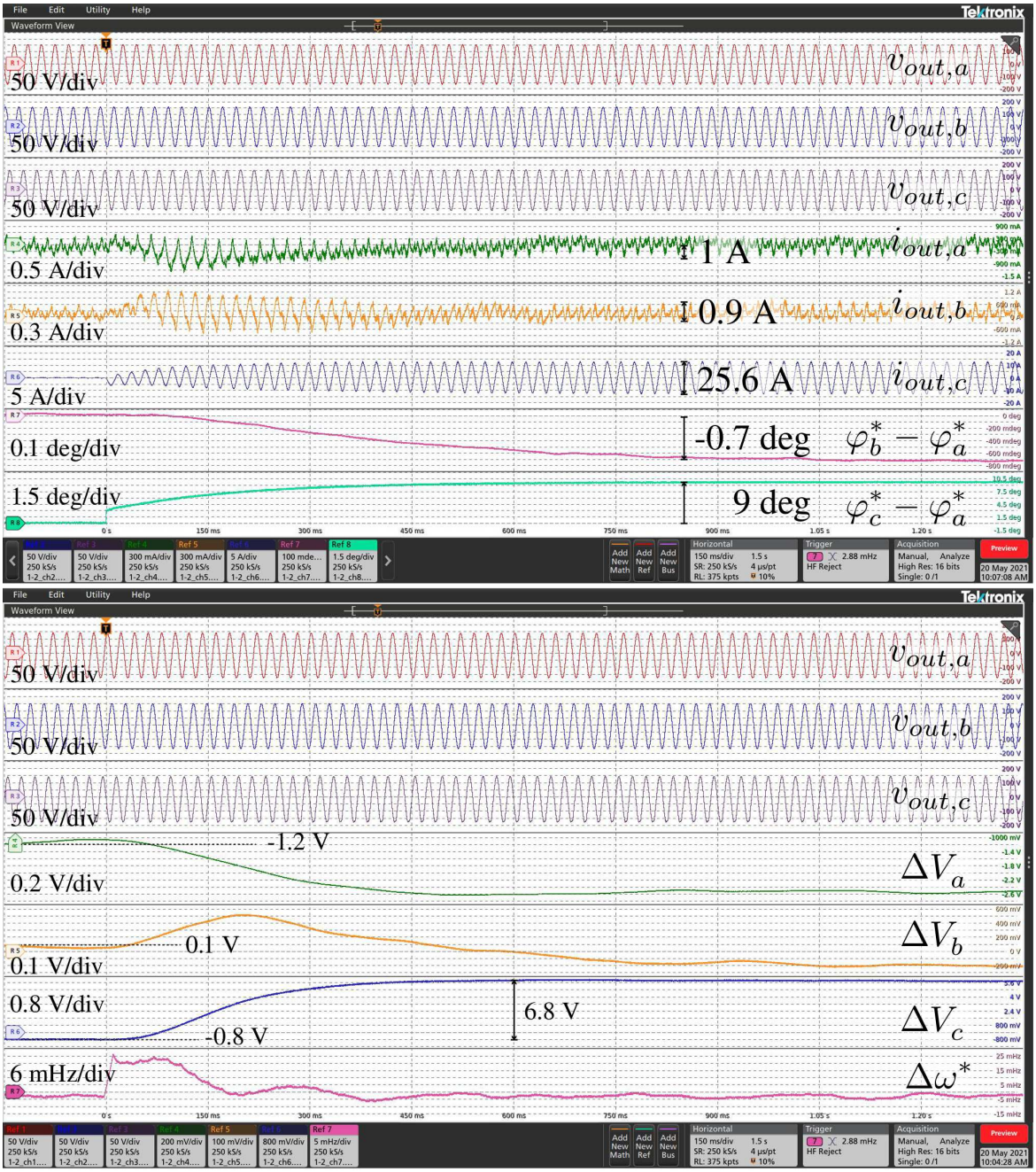


Fig. 4.8 Experimental results with EPC_1 in Fig. 4.6 implementing the proposed control scheme in Fig. 4.4. Reference step change $P_c^{\text{ref}} : 0 \rightarrow 1\,\text{kW}$ with balanced load of $13\,\Omega$.

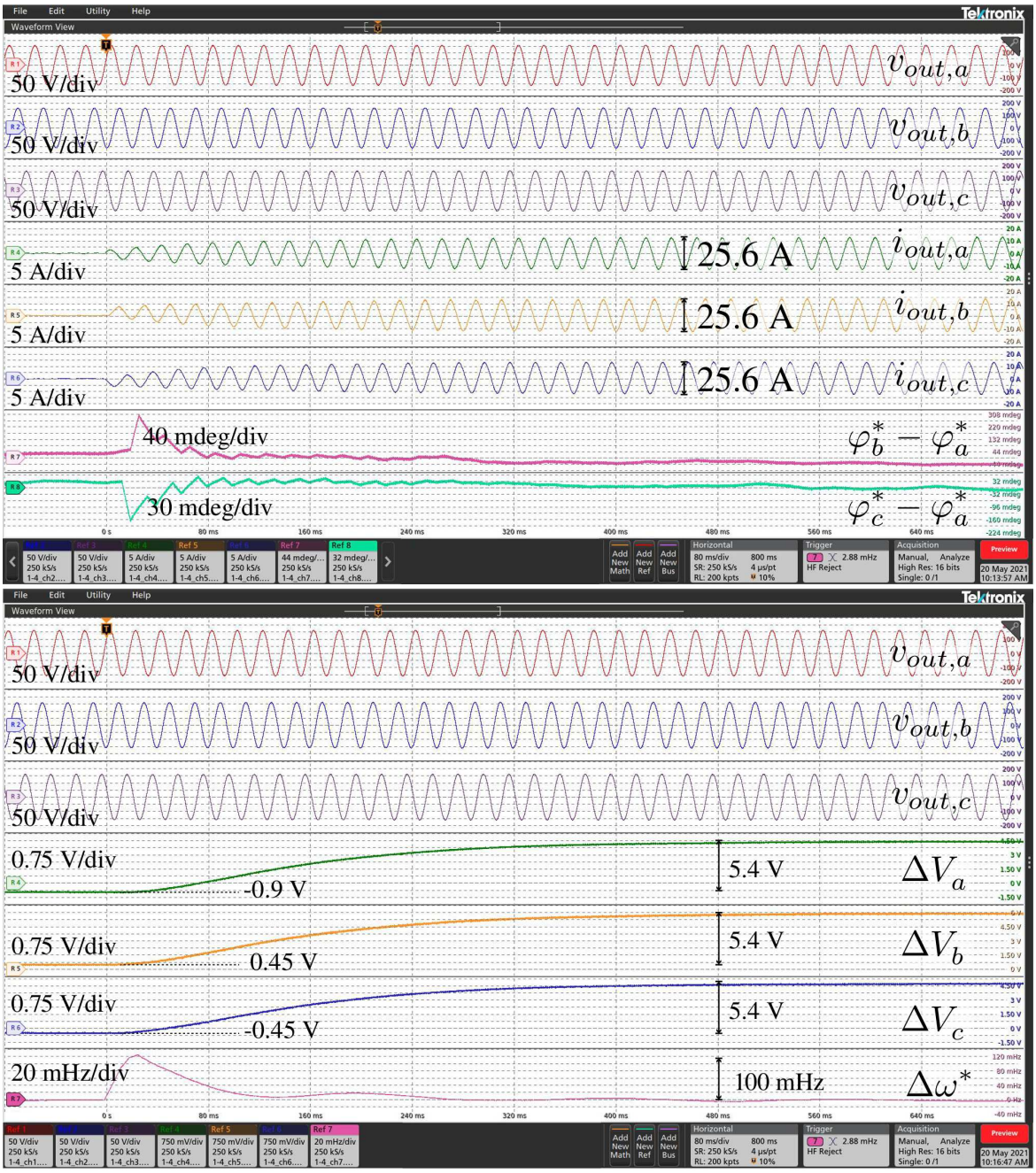


Fig. 4.9 Experimental results with EPC_1 in Fig. 4.6 implementing the proposed control scheme in Fig. 4.4. Reference step change of all the phases $P^{\text{ref}}_{a,b,c} : 0 \rightarrow 1\,\text{kW}$ with balanced load of $13\,\Omega$.

Fig. 4.9 displays analogous variations in voltage amplitude. Frequency ω^* is unchanged in steady-state due to the presence of the main grid.

As done considering the previous unbalanced test, for the aim of validation, Fig. 4.10b displays the obtained results from the simulation and the experimental test. A good correspondence among simulation and experimental results can be remarked.

4.4.3 Grid-tied to islanded transition

Fig. 4.11 displays the response to a transition from the grid-connected to the islanded operation modes with EPC_1 initially connected to a stiff voltage source emulating the main grid while EPC_2 is disabled. The initial condition is the final of the previous test [i.e., that of Fig. 4.9] and with a balanced three-phase load connected. The disconnection does not bring to visible effects on the instantaneous voltages, proving the capability of providing the required load current and of forming the local grid voltage while operating islanded. By a more precise inspection, the top figure in Fig. 4.11 shows a transient phase-displacement, especially involving phase-c, which brings back to zero after the transient. The bottom figure in Fig. 4.11 shows an increase of the voltage amplitude of all the phases due to the balanced reactive power absorption. The frequency ω^* decreases according to the chosen droop coefficient $k_{p,3\phi}$ and the total generated active power.

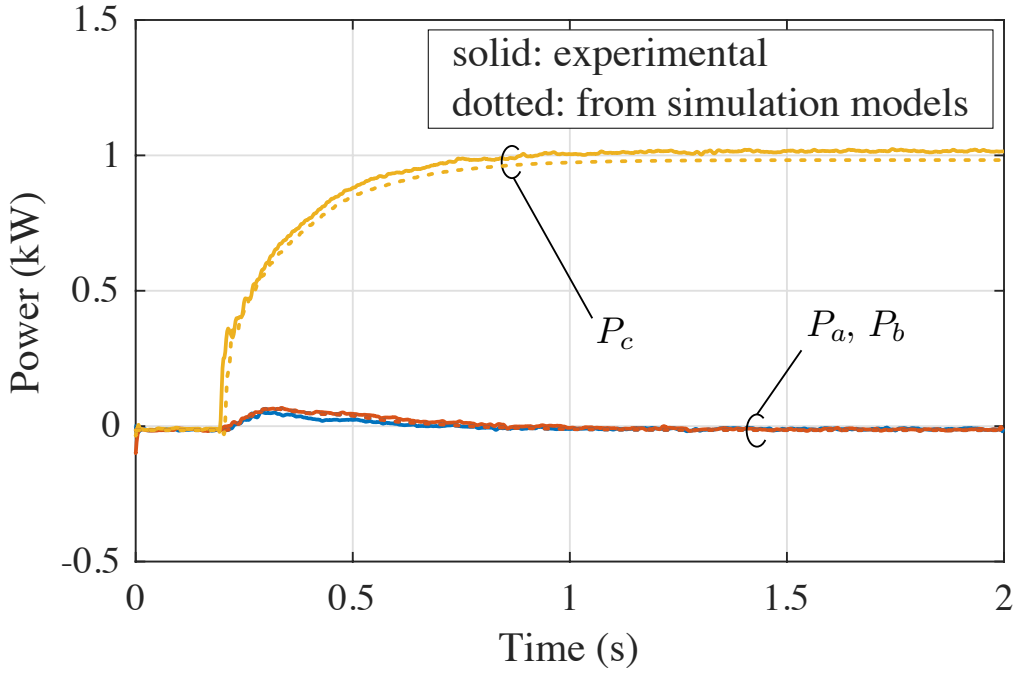
The same transition is also shown in Fig. 4.12 with both the EPCs initially connected to the grid operating at non-nominal conditions, with grid frequency of about 50.22 Hz. A smooth transition can be observed also in this case.

4.4.4 Parallel operation while islanded

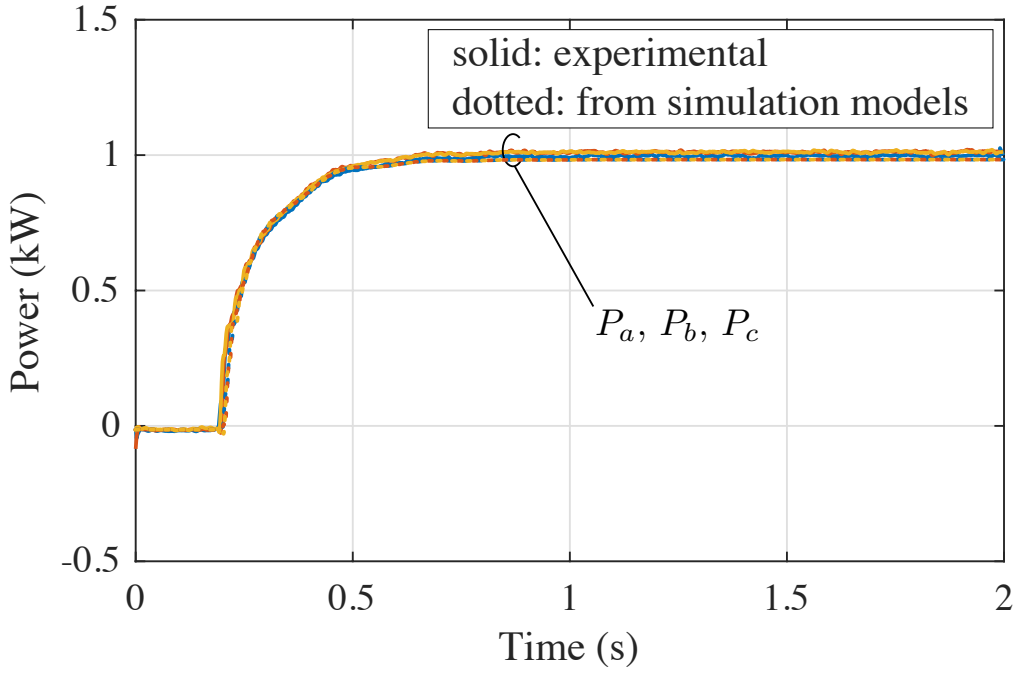
Fig. 4.13 displays the parallel operation of EPC_1 and EPC_2 while disconnected from the main grid and the response to a disconnection of EPC_2. The initial condition is the final one of the previous test in Fig. 4.11, but with an unbalanced load connected and the two EPCs active and equally sharing the load power. Then, EPC_2 is disconnected. This causes the operating frequency to transit from 47.73 Hz to 47.49 Hz, visible in Fig. 4.12, indicating a load increase of about 850 W for EPC_1. Notably, the converters are able to keep synchronized and nicely share the load among them.

4.4.5 Reactive power control

Fig. 4.14 shows the reactive power control capability of the solution. Firstly, a step change is applied to phase a, from 0 to 300 VAr, then, subsequently, the same step change is applied



(a)



(b)

Fig. 4.10 Output power response to step reference changes considering experimental and simulation models. (a) step change of phase-*c* power reference; (b) step change of the power references of all the three phases

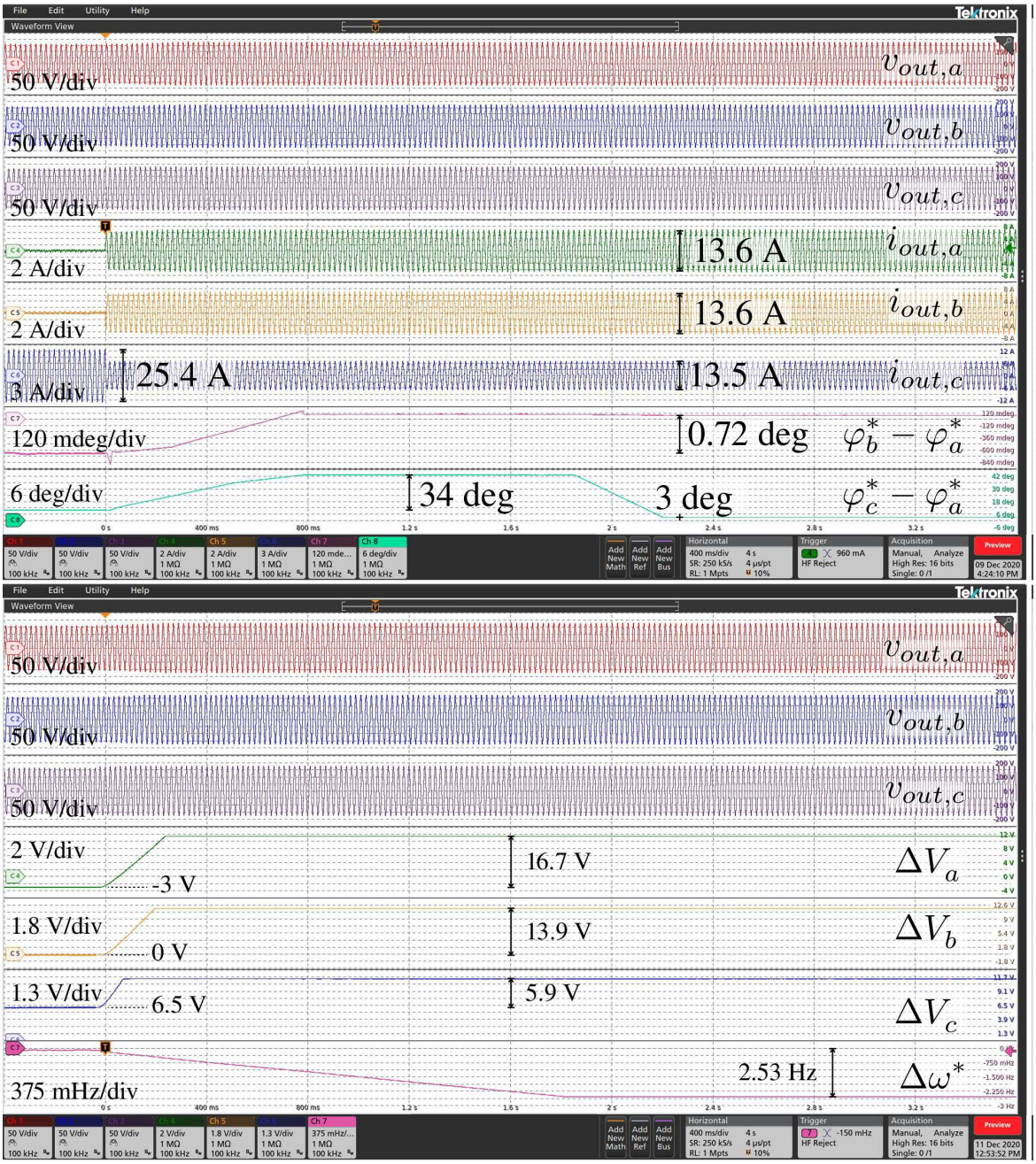


Fig. 4.11 Experimental results with EPC_1 in Fig. 4.6 implementing the proposed control scheme in Fig. 4.4. Transition into the islanded operation with balanced load of 25 Ω.

Fig. 4.12 Experimental results with EPC_1 in Fig. 4.6 implementing the proposed control scheme in Fig. 4.4. Transition into the islanded operation of EPC_1 and EPC_2 with balanced load of 12.5 Ω and grid frequency of 50.22 Hz.

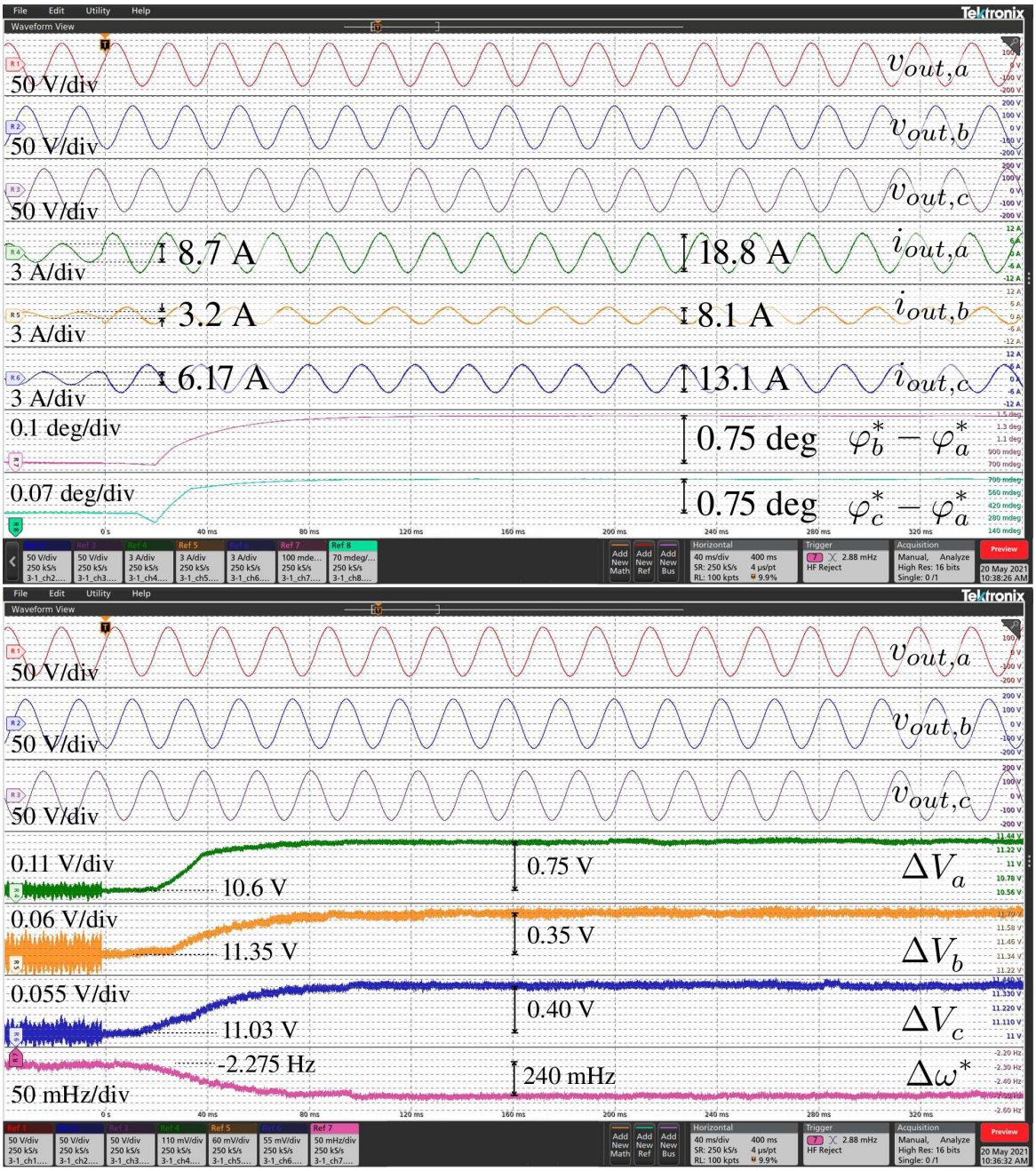


Fig. 4.13 Experimental results with EPCs in Fig. 4.6 implementing the proposed control scheme in Fig. 4.4. Islanded operation with two EPCs and unbalanced load a-N : 16.7 Ω, b-N : 50.0 Ω, c-N : 25.0 Ω.

to phases *b* and *c* as well. The main effect is an increase of ΔV_x, according to the linearized models (4.8)-(4.9). Remarkably, reactive power is less critical than active power control in terms of per-phase power control, because it consists in regulating the amplitude of the different phases, without significant effects on the other phases and the synchronization with the grid.

4.4.6 Islanded to grid-connected transition

The transition from the islanded to the grid-connected operation can be managed as commonly done in microgrids with distributed EPCs using the traditional droop control. Such a transition is briefly discussed in this subsection for completeness and demonstration purposes.

The synchronization of an islanded system to a grid voltage may be performed, for example, as discussed in [39], that is, by setting:

$$\omega_0 = \omega_g^{\text{nom}} + k_{i,\varphi}^{\text{synch}} \int \varphi_{MG} - \varphi_g \, \mathrm{d}t \tag{4.23}$$

$$V_0 = V_g^{\text{nom}} + k_{i,V}^{\text{synch}} \int V_{MG} - V_g \, \mathrm{d}t \tag{4.24}$$

where φ_g and V_g are the grid voltage phase angle and amplitude, respectively, while φ_{MG} and V_{MG} are the phase angle and amplitude of the islanded microgrid voltage, respectively. The phase angle $\varphi_{3\phi}$ and the mean voltage amplitude of the EPC that is closest to the circuit breaker *CB* constitute a good choice for φ_{MG} and V_{MG}, respectively. The integrative gains $k_{i,\varphi}^{\text{synch}}$, $k_{i,V}^{\text{synch}}$ should be set based on the desired speed of response (e.g., 1-10 s). PI regulators may be used as well to achieve faster dynamics.

The resulting transition is shown in Fig. 4.15, displaying the re-connection of the EPCs to the main grid. Four stages may be distinguished, marked at the top of the same figure: *i)* islanded operation, when the EPCs operate as droop-controlled converters as discussed in Sect. 4.2.2, *ii)* synchronization to the grid voltage by means of (4.23)-(4.24), which reduces to zero the signals $V_x - V_g$ and $\omega^* - \omega_g$, *iii)* connection to the grid by closing the circuit breaker *CB* in Fig. 4.3, *iv)* activation of the per-phase control. Remarkably, no overcurrents are present at the connection with the grid (i.e., across stage III and IV), demonstrating an accurate synchronization. At the beginning of stage IV the per-phase control is activated with zero power references for all the phases, demonstrating the possibility to restore the proposed per-phase power control smoothly during grid-tied operation.

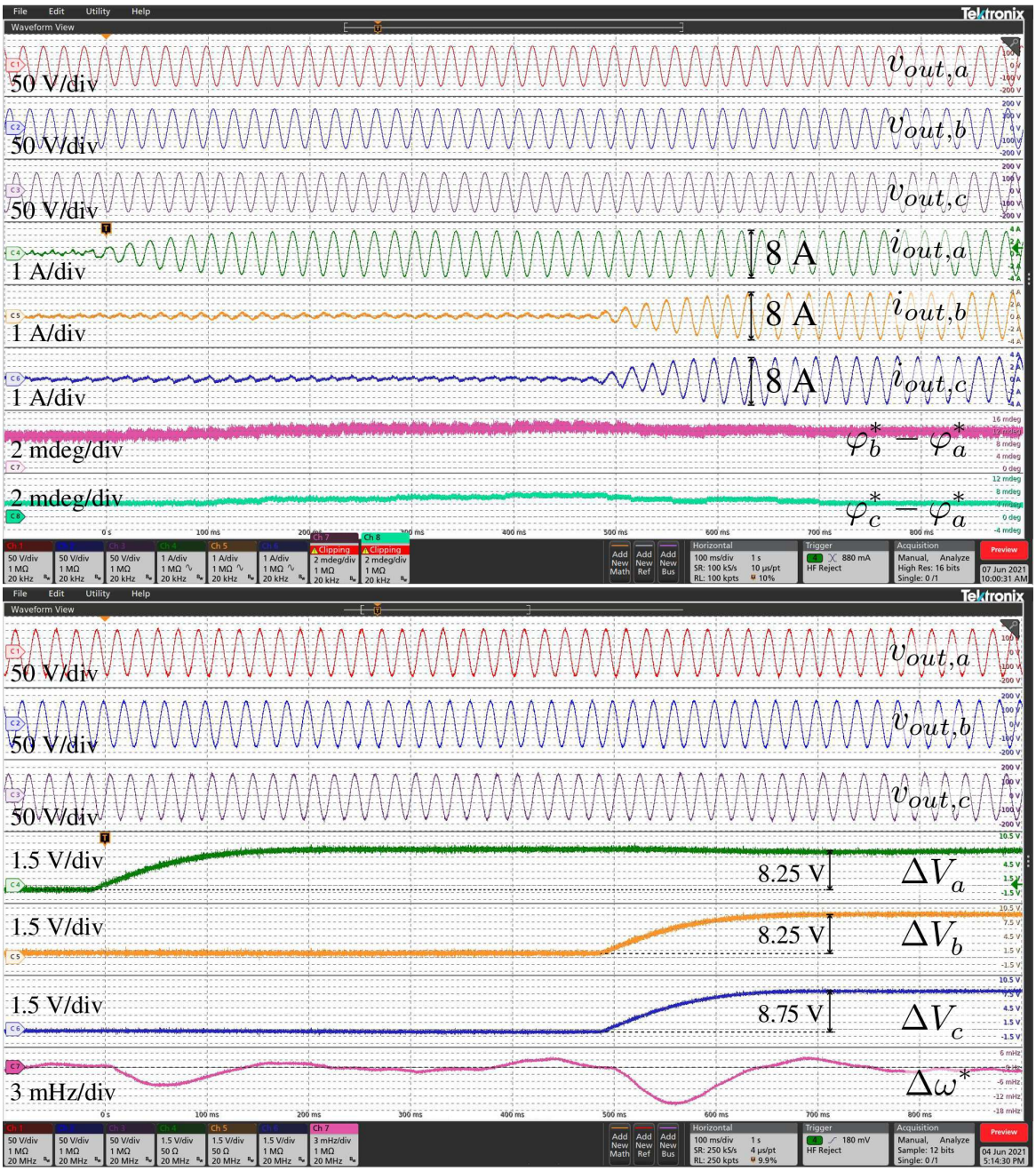


Fig. 4.14 Experimental results with EPCs in Fig. 4.6 implementing the proposed control scheme in Fig. 4.4. Reference step change of EPC$_1$, $Q_a^{\text{ref}} : 0 \rightarrow 300\,\text{VAr}$ and, subsequently, $Q_b^{\text{ref}}, Q_c^{\text{ref}} : 0 \rightarrow 300\,\text{VAr}$, with balanced load of $50\,\Omega$.

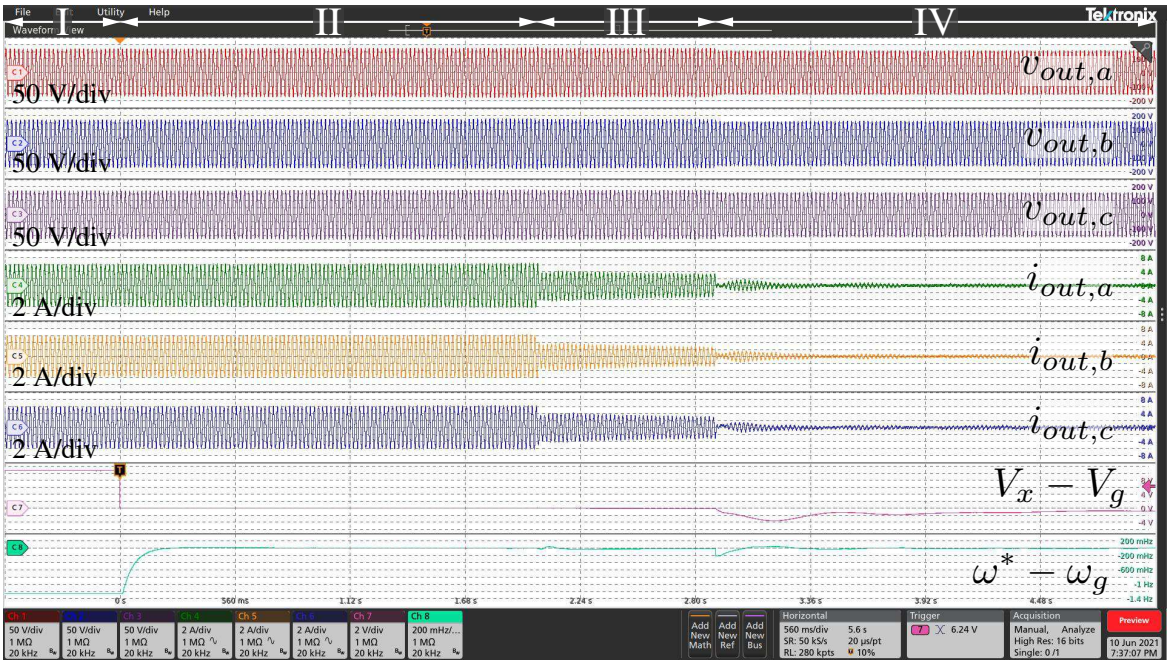


Fig. 4.15 Islanded into grid-connected transition of EPCs. Islanded operation is established in stage I, synchronization to the grid voltage is performed in stage II, connection to the grid takes place at the beginning of stage III, per-phase control is activated for both the converters at the beginning of stage IV.

4.5 Summary

In this chapter, a per-phase power controller is presented for three-phase four-wires grid-tied inverters that is capable of *i*) independent output power tracking for each phase while operating grid-connected, *ii*) smooth transitions into the islanded operation, *iii*) operation in islanded conditions even when multiple parallel connected converters integrating the proposed controller are present. The controller extends the functionalities of voltage-controlled inverters using traditional droop laws, allowing grid-connected operation and the independent control of the output power at each phase of the inverter. By the proposed structure, the capability of droop-like approaches of seamlessly transit into the islanded operation is preserved. The challenge in jointly providing per-phase output power control during grid-tied operation and seamless islanded transitions stems from the fact that output active-power control is done by adjusting the frequency of the phase voltage, according to the traditional droop laws. In practice, these adjustments are necessarily different among the different inverter phases, bringing to phase voltages with different frequencies in case of absence of a stiff grid voltage. For this reason the transition into islanded operation is particularly critical. The proposed solution is based on a three-phase synchronization loop, acting on all the three phases of the

inverter, with parallel power regulators to achieve per-phase power control. In the chapter, the controller is analyzed and a simple design procedure is devised. Experimental results are reported to show the operation of an inverter prototype driven by the proposed controller. The obtained results show that the controller fulfills the expected features with well damped dynamics, in accordance with the design. The controller can be employed in microgrids where output power tracking of distributed inverters is needed and smooth transitions into islanded operation due to unexpected events are possible.

Chapter 5

Conclusions and Future Works

This dissertation deals with the primary level control of distributed energy resource converters in DC and AC microgrids. The objective is to improve the performance of converters from three aspects by using advanced control methods.

A novel dual-edge (DE) PWM and its analytical analysis are presented, which is suitable for the DC/AC and AC/AC converters and allows higher bandwidth in the control loop, as a result to improve the stability and decrease the costs. This architecture shows improved dynamic performance for small and large signals compared to conventional modulation schemes in all modes. The proposed modulator results in lower delay and output impedance improvement. With the double update in this modulator, it is possible to achieve the peak performance with an actual modulation delay of 0 for each duty cycle value instead of Tw/4 modulation delay compared to the conventional triangular carrier DPWM. This DE modulator is a fixed frequency PWM, but without guaranteed synchronization and with a nonlinear behavior at large transients. Therefore, an additional synchronization control based on a PLL approach has been developed with satisfactory results. The overall structure of this modulator is quite simple. Only a few lines of VHDL code are required to implement the new scheme with the new synchronization control algorithm in a small FPGA. If the controller specification requires an FPGA implementation anyway, replacing the conventional PWM scheme with DE PWM would provide a noticeable performance improvement without increasing the development cost (or only slightly).

The next aspect is about reducing the output capacitor of the converter. The solutions studied herein include the improvement of the design principle for droop-controlled converters and the utilization of hysteresis control and driving its analytical model. In the second aspect, the analytical model of a high bandwidth pulse with modulation and its improvement on output impedance are discussed. This is achieved by less delay introduced in the transfer function of the modulator. As for the third aspect, the investigation focuses on the per-phase

power Controller with seamless disconnection of AC microgrids from upstream grids. A power-based droop controller is proposed to attain this goal.

A design approach for resource converters is proposed to achieve resistive output impedance so that the output capacitance can be reduced. Since the output capacitance should be selected as a function of the voltage loop bandwidth and the Droop coefficient, the main issue is the coordinated design of the Droop coefficient and high bandwidth voltage regulation such as hysteresis. The Droop coefficient should be designed as a frequency dependent term with respect to the system and other control parameters. This design guideline is applied to non-isolated boost DC-DC converters. The hysteresis control used to accelerate the dynamic response of the voltage loop is implemented in lower-cost digital signal processors with a sampling frequency of 200 kHz, which is 10 times the switching frequency. Although the implementation introduces a delay of one sampling period, the impact of this additional delay on the stability of the converter is acceptable.

To finish the dissertation, a power-based droop controller is proposed to provide a seamless transition from per per-phase power flow control to droop control. Based on this controller, the operation modes of a single inverter and an entire AC microgrid are described. The inverters connected to the grid operate with per-phase power flow control and the inverters disconnected from the grid operate as simple droop controlled inverters. The transition from power flow control to droop control is automatic, without the need for any communication or detection procedure required. The power sharing performance between two inverters is analyzed. The design policies of the proposed controller are reported. The above scenarios are all supported and validated by experimental results with lab-scale inverters (in the range of kilowatts). In addition, a AC microgrid prototype has been built using Imprix modules. This prototype includes two 3-phase inverters and a transformer for connection to the main grid.

Several aspects of this research can be further investigated in future. In particular:

- Output impedance shaping of the converters using DE-DPWM in different isolated and non-isolated topologies.
- DE-DPWM with different ramp slops to introduce more derivative behavior.
- Per-phase power control in 3 phase 3wire AC systems.

Appendix A

Prototype of DC microgrid

To experimentally verify the research proposals, a general-purpose laboratory-scale DC microgrid prototype, which includes three boost DC-DC converters is built. The prototype is built from scratch to have full access to every part of it, for testing various control techniques in the scenario of DC microgrids and apply any change in case of need. In the following, the structure of the single boost converter and that of the entire DC microgrid are introduced respectively. This arrangement is an evaluation of Guangyuan Liu, former PhD student's prototype.

A.1 Single converter unit

Fig fig A.1 is showing the simplified schematic and sensing circuit diagram of one boost converter. Besides, fig A.2 is displaying the boost converter boxed, including some other major elements, such as protection circuits and the digital controller that will be described in the following.

A.1.1 Power circuit

Two Insulated Gate Bipolar Transistors (IGBTs), one inductor, and input/output capacitors are the main components of the power circuit of the boost converter. The nominal power of this converter is 3 kW, with nominal input and output voltages equal to 200 V and 380 V. The nominal inductor current is 15 A with a switching frequency of 20 kHz. Considering the boost converter parameters, the power switches are IKW40N65ES5 from Infineon. The breakdown voltage of this IGBT is 650 V and the DC collector current can reach 40 A. To have a 30% switching ripple on the inductor current at nominal operating conditions, the inductance of the inductor is selected as 1 mH. The input and output capacitors use film

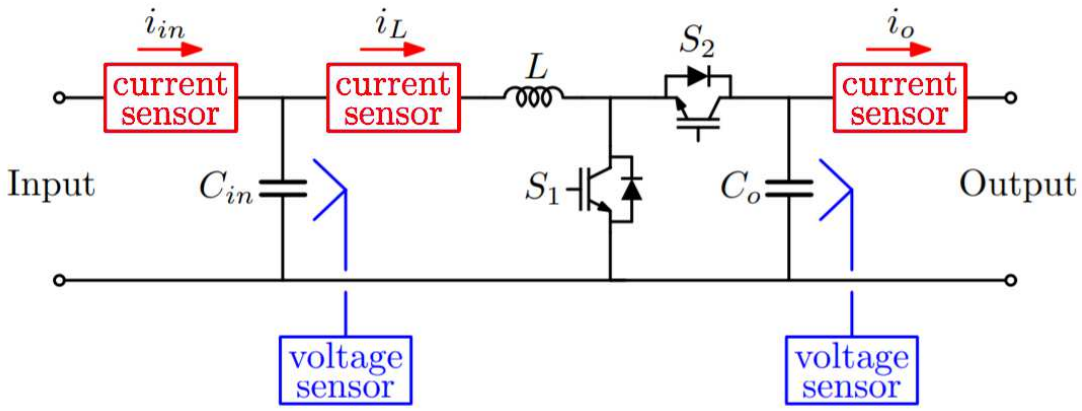


Fig. A.1 Simplified schematic of boost converter.

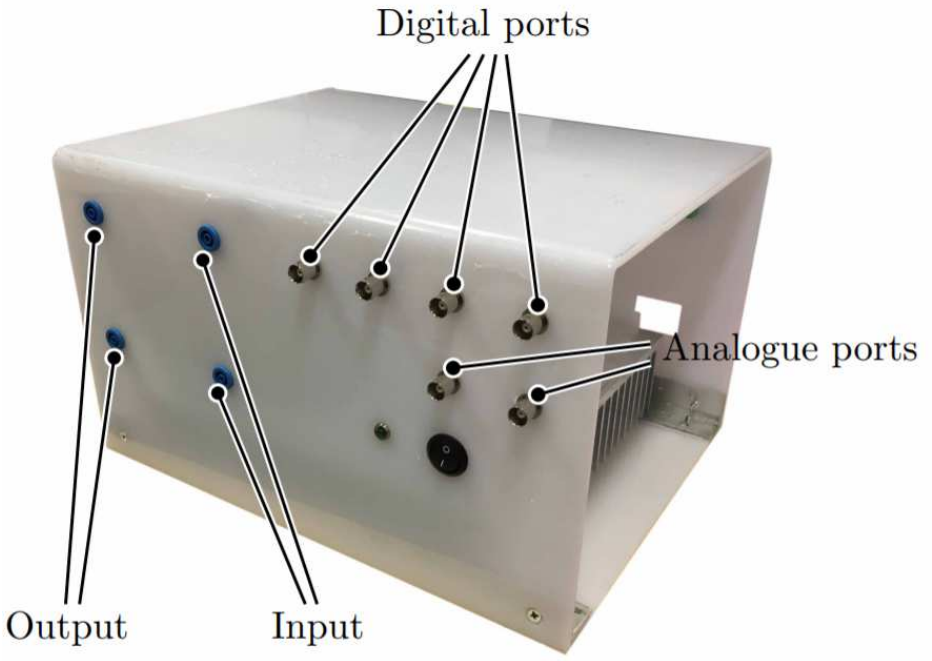


Fig. A.2 Single boost converter.

capacitors with values equal to 12 μF and 24 μF. It is possible to install more capacitors on the input and output sides. Another 470 nF snubber capacitor is placed close to the power switches to form a short commutation loop.

A.1.2 Sensing circuit

The current transducers used in this prototype and shown in fig A.1 are CAS-25NP from LEM, with maximum 25 A Root Mean Square (RMS) current and its measurement range is from -85 A to 85 A. To adjust the dc offset and the amplification gain, the output of current sensors are connected to a signal conditioning circuits. The outputs of conditioning circuits are sampled by Analog-to-Digital Converter (ADC) modules of the digital controller. Finally, the total linear measurement range of the current sensing circuits including current sensors and signal conditioning circuits is from -20 A to 20 A.

An isolated amplifier (TLP7820) is used to measure the voltage. The voltage signal is scaled down through resistors and a dc offset voltage is connected to the other input of the amplifier, in order to locate the measurement range in a band surrounding the nominal voltage. The output of this amplifier is directly connected to ADC modules. In this prototype, the measurement range of input voltage is from 170 V to 230 V, and the measurement range of output voltage is from 335 V to 425 V.

A.1.3 Protection circuit

This prototype also includes variable thereshhold hardware over-current protection circuits to set the maximum and minimum current limitation levels (shown in fig A.3). The protection circuits compare the current signals with upper/lower limits and if the current signals exceed the limitations, the over-current signal will disable the PWM signals.

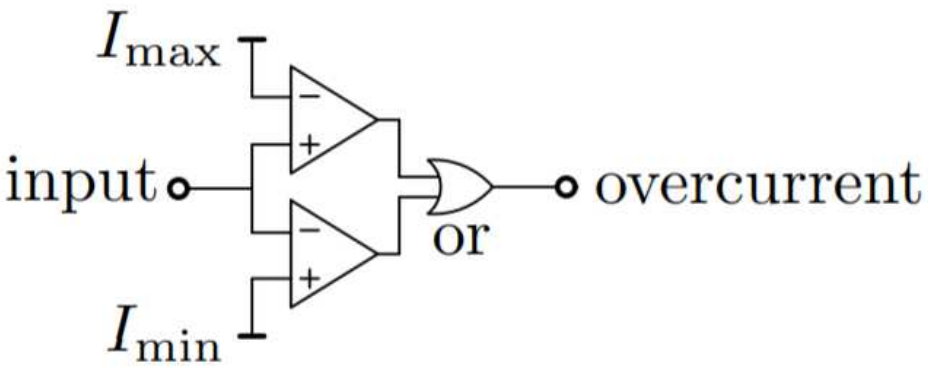


Fig. A.3 Diagram of current protection circuit of boost converter.

A.1.4 Digital controller

A dual core DSP TMS320F28379D from Texas Instruments is playing the role of the digital controller in this prototype. The CPU frequency of this DSP is 200 MHz. It also features a series of built-in peripherals, like ADC, DAC, PWM, CAN bus, etc.

A.2 Entire prototype structure

The entire DC microgrid prototype, as illustrated in fig A.4, is composed of three boost converters described above, and a controllable dc load. One of the converters is used as an injection circuit for output impedance measurement purposes. There is also a synchronization link between converters to eliminate circulating currents. Users could send commands to the central controller from the computer, and then, the commands are dispatched to converters.

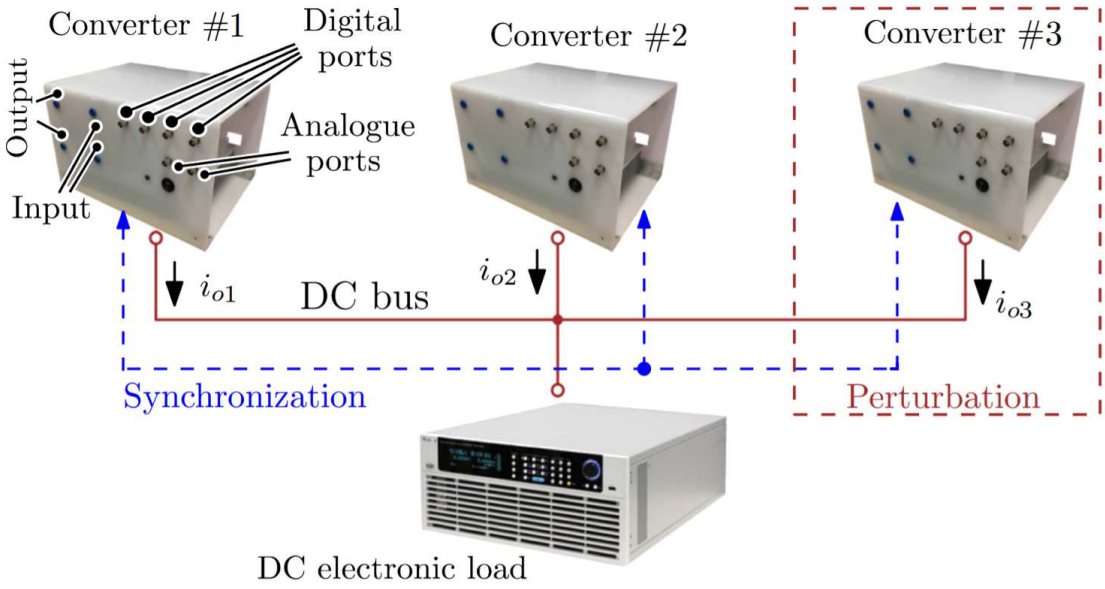


Fig. A.4 Diagram of entire DC microgrid prototype.

Appendix B

Rapid prototyping for power electronics (Imperix)

Imperix [47] develops plug-and-play hardware and prototyping equipment for power electronics and AC/DC smart microgrids to accelerate the implementation of laboratory-scale power converters. They support different aspects like software, controller, and power modules that will be discussed in the following.

B.1 Imperix controller and its software development kit

The B-Board PRO (fig B.1) and B-BoxRCP (fig B.2) are embedded controllers provided by Imperix, fully programmable using Simulink, PLECS, or C/C++. They have a Xilinx Zynq processor including both DSP and FPGA sections fully customized using the ACG SDK (Software development kit) blocks for Simulink and PLECS (Fig B.3). ACG SDK enables users to automatically generate code from Simulink or PLECS models. The FPGA section is responsible for the protections, PWMs and electrical communications. It is also freely editable so that challenging applications can leverage the power of unused FPGA resources for specific power converter control tasks. To this end, relying on all the Xilinx Vivado Design Suite tools and IPs for programming the Boards' FPGA part is as simple as programming any other Xilinx FPGA.

B.2 Imperix power module

Imperix half-bridge power modules (fig B.4) for the rapid implementation of power converter topologies. With the help of power modules and their associated chassis (fig B.5), power

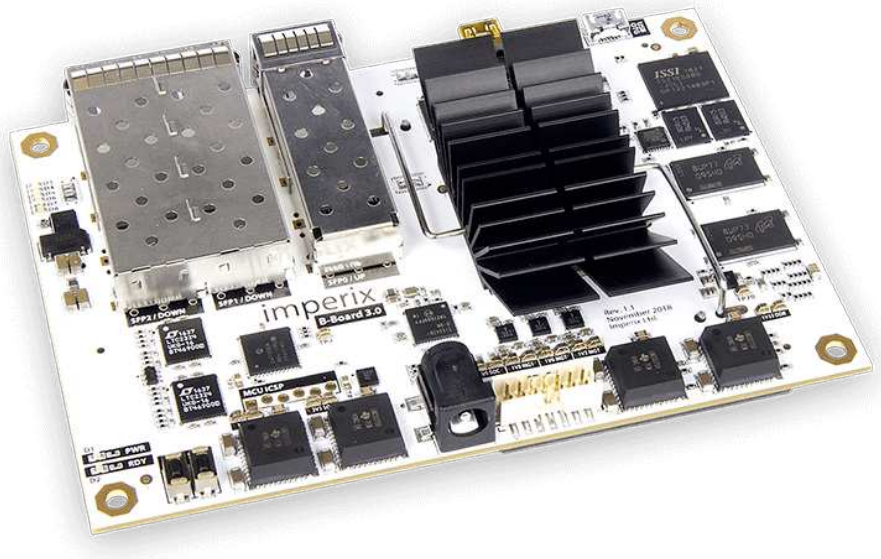


Fig. B.1 B-Board Pro by Imperix.

Fig. B.2 B-BoxRCP Pro by Imperix.

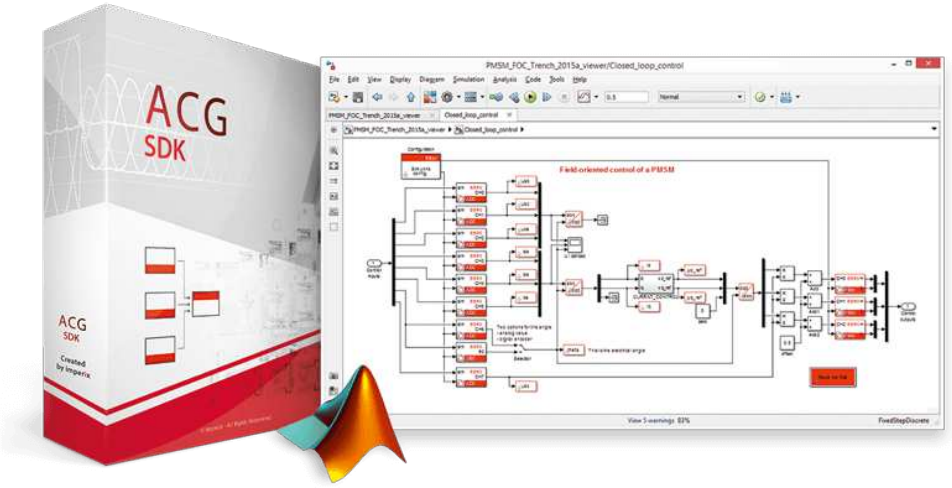


Fig. B.3 Imperix SDK supporting Simulink and PLECS.

converters of practically any topology can be built up within minutes. Topologies can of course always be used to form laboratory-scale ac or dc microgrid prototypes. These modules embed decoupling capacitors (DC bus), gate drivers, as well as onboard voltage and current measurements, protections, and optical connection to the control board for the PWM signals. Modules exist with various voltage and current ratings, hence offering multiple variants that can closely fit various applications.

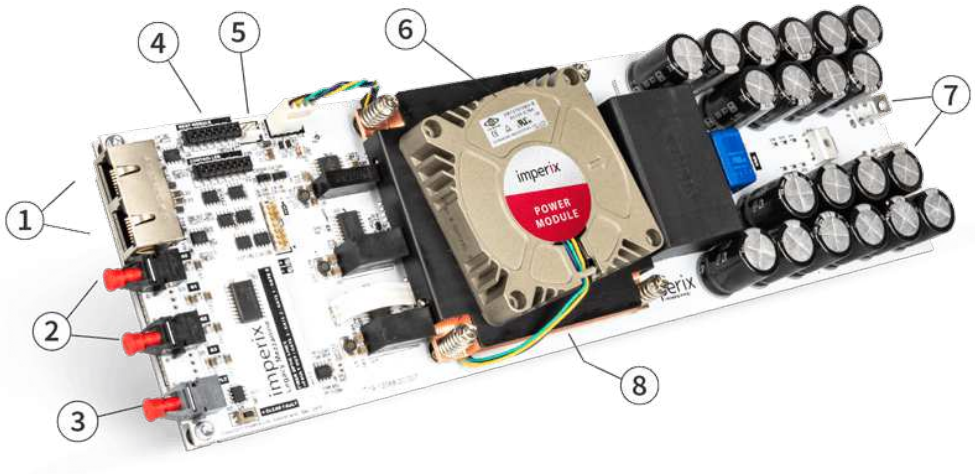


Fig. B.4 Imperix half-bridge power module.

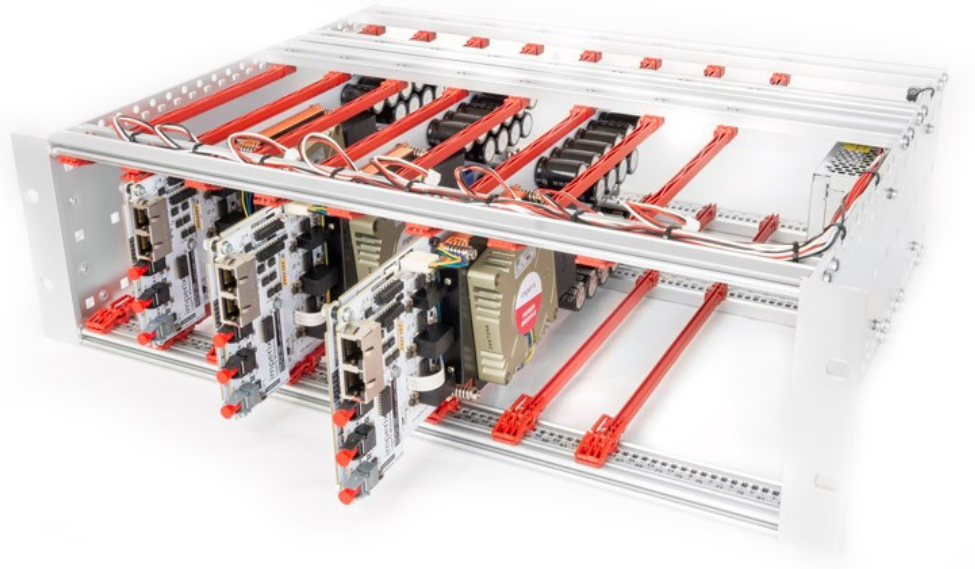
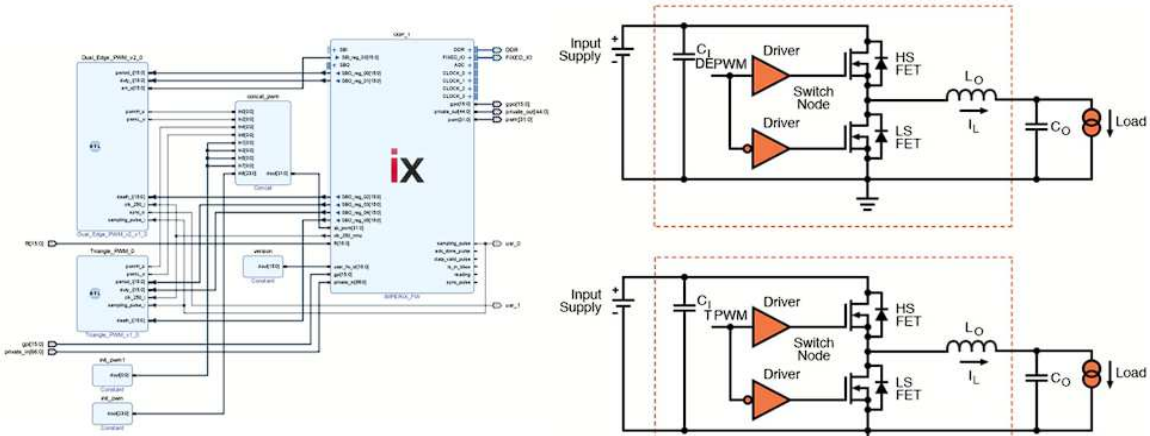


Fig. B.5 Imperix power rack.

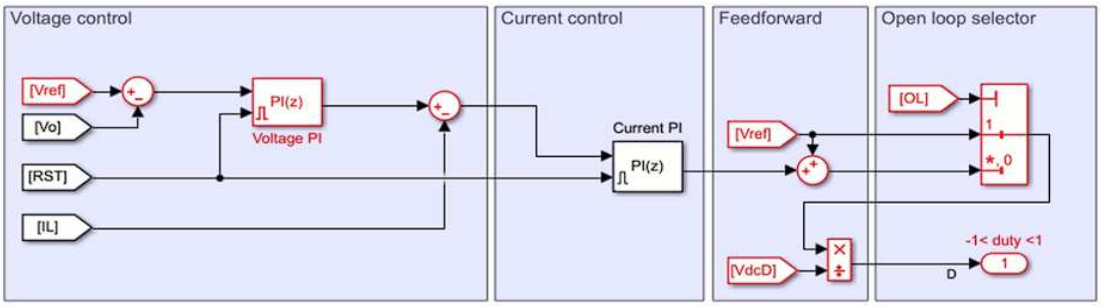
B.3 Imperix use-case

The DE-DPWM testing configuration for DC case study, as shown in fig B.6, is made up of two Imperix half-bridge power modules and the previously disclosed B-BoxRCP Pro.

The DE and TTE-based DPWMs are developed in VHDL to operate on the FPGA side of the Xilinx Zynq processor, and a cascade current and voltage PI regulator with the same properties is implemented in Matlab Simulink to generate the code to run the CPU part automatically.



VHDM model implimaed to run on Xilinx Kintex.



Matlab model used for auto code generation to run on ARM Cortex A9.

Fig. B.6 Structure of entire setup to test DE-DPWM by Imperix.

Same technique with diffident hardware configuration (three-phase four-wire low-voltage EPCs) is used to experimentally validate the *Per-Phase Power Controller*, discussed in Chapter 4.

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