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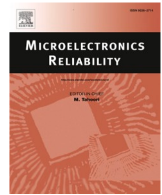

Trade-off between gate leakage current and threshold voltage stability in power HEMTs during ON-state and OFF-state stress

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ABSTRACT

We present a detailed investigation of the impact of electron gate leakage on the threshold voltage stability of normally-off GaN HEMTs with p-GaN gate. The analysis is based on combined DC, pulsed and transient measurements, carried out on two test wafers with different gate processes, resulting in different levels of gate leakage current. The key results demonstrate: (a) the existence of four different charge-trapping processes, whose interplay determines the sign and amplitude of the threshold voltage variation; (b) a reasonable increase in gate leakage is beneficial for eliminating the negative threshold voltage instability under positive gate bias, and for substantially reducing the positive threshold shift under off-state stress. Furthermore, (c) we present a proper characterization methodology for device understanding.

1. Introduction

Gallium nitride power devices are nowadays recognized as a competitive solution for high-efficiency power conversion, being able to displace silicon devices thanks to the possibility to deliver higher power densities [1]. The potential of GaN is exploited through the use of AlGaN/GaN High-Electron-Mobility-Transistors (HEMTs), that offer an extremely low ON-resistance due to the spontaneous presence of the 2-Dimensional-Electron-Gas (2DEG). However, HEMTs are intrinsically normally-ON devices, that are not suitable for fail-safe power applications, where normally-off power switches are required. Two effective solutions had been proposed to overcome the limitation of the normally-ON structures: i) the use of a cascode configuration [2], in which a fast silicon transistor is used to drive the normally-ON power HEMT; ii) the use of a p-GaN gate, where a p-doped GaN layer is placed between the gate contact and the AlGaN barrier [3]. The latter is nowadays more widely adopted, but the complexity of the structure complicates the analysis. Briefly, the p-GaN layer is used to lift-up the band diagram, obtaining the depletion of the 2DEG even when the gate voltage is zero. A gate Schottky contact is usually used to mitigate the gate current leakage, that otherwise would flow toward the p-i-n diode made of the p-GaN layer, the AlGaN barrier, and the channel [4]. However, this rises the problem of controlling the potential of the p-GaN region near the interface with AlGaN (mid-node), which directly controls the charge density in the 2DEG. Despite the recent developments, GaN power transistors are still far from the complete technology maturity, because different issues are affecting the performance of such devices. Among all, threshold voltage (V_{TH}) instabilities are a key factor limiting the performance of p-GaN gate power devices [5].

The aim of this paper is to report a detailed investigation of the factors limiting the threshold voltage stability of p-GaN gate power HEMTs test structures with different gate leakage current, submitted to ON-state and OFF-state. The role of the gate leakage current in the V_{TH} stability is assessed by means of combined DC, pulsed and transient measurements, thanks to which different mechanisms affecting the V_{TH} stability are identified. Results indicate that a higher gate leakage current increases the overall V_{TH} stability thanks to a better control of the floating p-GaN mid-node. Furthermore, this paper reports the description of a proper characterization methodology and consequence physical interpretation of the various behaviours/transients that are observed.

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2. Devices under test and stress procedure

The devices under test are p-GaN gate power HEMTs test structures (Fig. 1) used for gate module development and process understanding.

The analysis is carried out on two test wafers with different gate processes, resulting in one wafer with higher gate leakage current (Wafer H) and one wafer with lower gate leakage current (Wafer L). By variation in gate contact processing conditions, a different Schottky barrier height is obtained at the p-GaN/metal interface.

Significant DC characteristics are reported in Fig. 2.

Wafer H results in a gate leakage current two orders of magnitude higher with respect to wafer L. The V_{TH} extracted at 1 mA is $V_{TH-H} = 2.22\ V$ and $V_{TH-L} = 1.92\ V$ for wafer H and wafer L respectively.

It is then worth highlighting that only for wafer H, in the I_DV_G characteristics, there is an increase in drain current in two steps, with a small plateau for a gate voltage of about 1.2 V. This is attributed to electron trapping during the measurement phase, according to the threshold voltage transient results in Section 4, Fig. 5. Briefly, wafer H exhibits electron trapping in the AlGaN barrier (fast process) for low gate voltages, resulting in a positive threshold voltage shift. This electron trapping is faster if compared to the gate sweep during the DC measure (1 PLC per point – 20 ms), resulting in a shift of the I_DV_G characteristic. This highlights the necessity of performing faster measurements on both devices, to understand the different processes involved.

The analysis on the two test wafers is then carried out by means of a custom pulsed setup, to perform pulsed IV with measurement pulses down to 1 μs, and by means of a fast custom V_{TH} transient setup, to analyse the V_{TH} kinetics starting from the microseconds range.

3. Pulsed characterization

A widely adopted technique to analyse the dynamic performance of power devices is the so-called Pulsed-IV characterization, thanks to which it is possible to monitor the different electrical characteristics of the device (in general threshold voltage and on-resistance for a power device) when submitted to different operating quiescent biases. Within this paper, only the threshold voltage of the device will be analysed. The reported pulsed-IVs are performed with the following procedure: i) first, a 1 s pre-filling time at the given quiescent bias is applied, to fill all the traps involved in that particular operating condition; ii) second, the pulsed characterization is performed, with the device that is kept at the given quiescent bias and with 3 μs and 10 μs measurement pulses for ON-state stress (gate stress) and OFF-state stress (drain stress) respectively.

First, a comparison between DC and pulsed I_DV_{GS} measurements (with $V_G = 0$ V and $V_D = 0$ V as quiescent bias) is carried out. Significant results are summarized in Fig. 3.

Results show a noticeable difference between DC and pulsed I_DV_{GS} characterizations. The threshold voltages extracted at 1 mA are reported

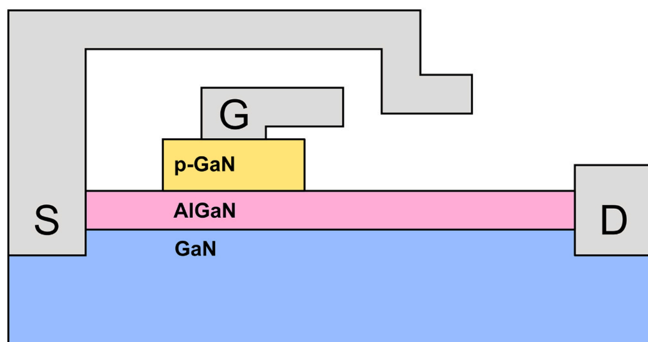

Fig. 1. Schematic cross-section of the p-GaN gate power HEMTs test structures under test.

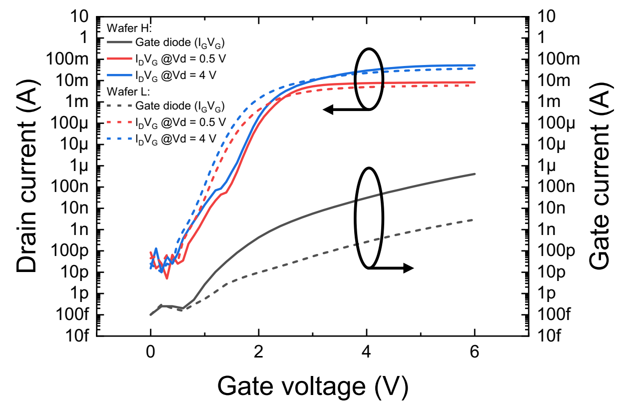

Fig. 2. Gate leakage current (black lines) and transfer characteristics (I_DV_{GS}) at a drain voltage of 0.5 V (red lines) and of 4 V (blue lines) for the two different wafers. Wafer H in solid lines, wafer L in dashed lines.

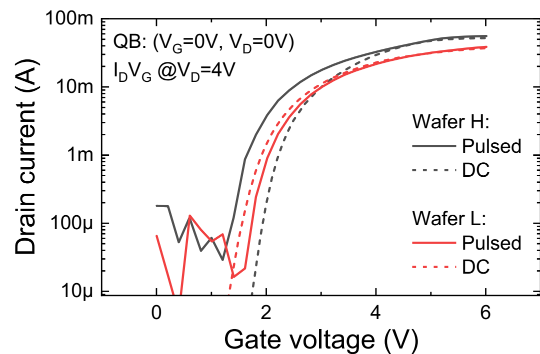

Fig. 3. I_DV_{GS} comparison between pulsed measurements, with $V_G = 0$ V and $V_D = 0$ V as quiescent bias (solid lines) and DC measurements (dashed lines) for the two wafers. Wafer H in black, wafer L in red.

in Table 1.

With a pulsed I_DV_{GS}, Wafer H shows a lower V_{TH} (0.57 V lower than the DC one) while Wafer L shows a higher V_{TH} (0.13 V higher than the DC one). This indicates the presence of charge trapping processes (both of positive and negative charge [5]) during the DC characterizations, that will be investigated in the following with the pulsed setup. It is important here to highlight the importance of pulsed characterizations on the understanding of the devices under test; without them it is impossible to have a full interpretation of the phenomena taking place in the device. To get further insight in the phenomena leading the threshold voltage instabilities, pulsed I_DV_{GS} with different quiescent biases were performed in both ON-state (increasing gate bias with drain fixed at 0 V) and OFF-state (increasing drain bias with gate fixed to 0 V) (Fig. 4). Different behaviours are highlighted in the two test wafers.

For ON-state stress (Fig. 4(a)): i) Wafer H shows a positive V_{TH} shift ($\Delta V_{TH} = 0.48$ V) for $V_{G\text{-}QB} = 2$ V and a zero shift for $V_{G\text{-}QB} = 6$ V; ii) Wafer L shows a zero V_{TH} shift for $V_{G\text{-}QB} = 2$ V and a negative shift ($\Delta V_{TH} = -0.83$ V) for $V_{G\text{-}QB} = 6$ V. As already observed in the comparison between DC and pulsed I_DV_{GS} measurements, both negative and positive charges are trapped in the gate stack.

For OFF-state stress (Fig. 4(b)), the two wafers show only positive V_{TH} shift (trapping of electrons), with Wafer H showing an overall lower

Table 1
Extracted threshold voltages for pulsed and DC characterizations.

	DC V_{TH}	Pulsed V_{TH}	ΔV_{TH}
Wafer H	2.22 V	1.65 V	0.57 V
Wafer L	1.92 V	2.05 V	−0.13 V

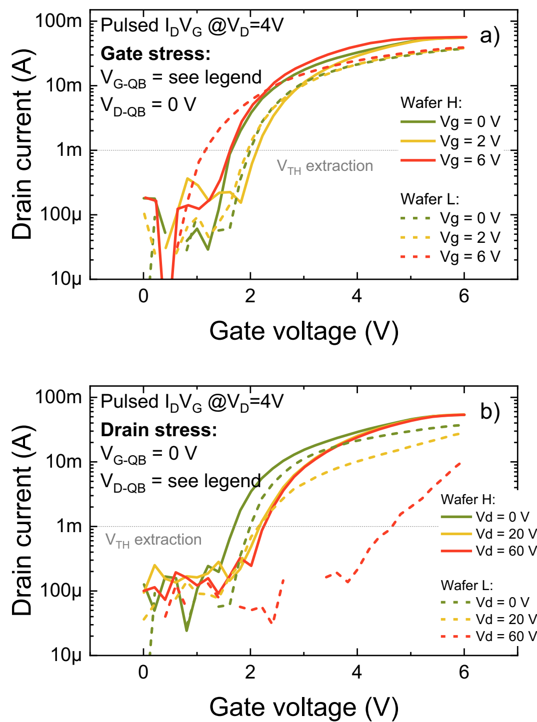

Fig. 4. Pulsed I_DV_{GS} at different quiescent biases for both a) ON-state stress (gate stress) and b) OFF-state stress (drain stress). Solid lines for Wafer H, dashed lines for Wafer L.

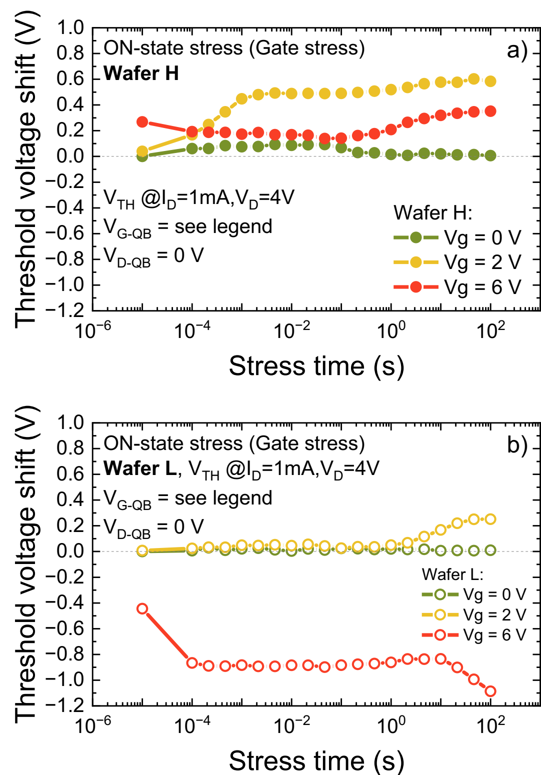

Fig. 5. Threshold voltage transient analysis during ON-state (gate) stress for: a) Wafer H; b) Wafer L.

ΔV_{TH} if compared to Wafer L (maximum V_{TH} shift of 0.55 V and 2.66 V respectively).

Results highlights that Wafer L suffers from negative V_{TH} shift under positive gate bias (that may lead to undesired turn-on), and to relevant positive V_{TH} shift in off-state bias, that may lead to a premature turn-off of the device and to an on-resistance increase. Such effects are mitigated in Wafer H.

The positive and negative shifts will be further investigated by means of transient measurements for both ON-state (gate) and OFF-state (drain) stress.

4. Transient analysis

Transient analysis was carried out on both test wafers for different conditions (ON-state and OFF-state) to extract the time evolution of the V_{TH} shift. Briefly, the test consists on applying, for 100 s, a constant voltage stress level at the device. The stress is briefly interrupted (exponentially spaced in time) to perform a fast (3 μs for ON-state, 10 μs for OFF-state) I_DV_{GS} characterization (at a fixed drain voltage of 4 V) for V_{TH} extraction (extracted at a current of 1 mA).

Significant V_{TH} transients for gate stress (ON-state) are reported in Fig. 5.

Results highlight the presence of different mechanisms involved in the threshold voltage instabilities (Fig. 6): i) With no stress applied (V_G = 0 V, green curves) it is possible to observe a tiny (<0.1 V) V_{TH} shift in Wafer H, that is only due to the charge trapping induced by the measurement itself. ii) With a gate stress voltage of 2 V, a fast increase in threshold voltage is observed in Wafer H. Through a literature comparison, this is ascribed to the trapping of electrons in pre-existing traps in the AlGaN/GaN interface and/or in the AlGaN barrier [6–9] (mechanism "b" in Fig. 6).

This mechanism does not occur in wafer L, because, due to the lower gate leakage, less holes are accumulated in the p-GaN/AlGaN interface resulting in a higher electric field across the AlGaN that prevents electrons injection from the 2DEG.

The fast electron trapping is responsible for the small V_{TH} shift observed during the measurements in Wafer H. Then, in both wafers, a slow (t > 100 ms) increase in V_{TH} is present. This is due to the emission of holes from the 2DHG across the AlGaN barrier (mechanism "a" in Fig. 6), that leave a net negative charge in the p-GaN region, leading to the positive V_{TH} shift [9,10]; iii) With a gate stress voltage of 6 V, the accumulation of holes in the 2DHG and the subsequent trapping in AlGaN traps (mechanisms "c" in Fig. 6) take place [5,9]. Its impact is moderate in Wafer H (due to the interplay with electron trapping and due to the electron-hole recombination that takes place between electrons, mechanism "b1" in Fig. 6, and trapped holes in the AlGaN); iv) Finally, only in Wafer L, an additional decreasing trend is observed for long stress time. This is attributed to hole trapping in the GaN buffer and/or in the Strain Relief Layers (SRL) interface [5,10] (mechanism "d" in Fig. 6).

Results show the better stability of the devices with higher gate leakage current, that exhibit also faster detrapping processes (not shown).

Finally, the V_{TH} shift due to drain stress (off-state) is analysed. Remarkably, Wafer H shows a lower overall V_{TH} shift (Fig. 7(a)), that is only positive, while wafer L exhibits a signal V_{TH} shift with both positive and negative transients (Fig. 7(b)). It is worth to highlight that the transients are consistent with previous studies in p-GaN gate HEMTs [11–13] and are interestingly different from the ones observed in GaN MOS channel HEMTs [14].

The positive shift is ascribed to hole deficiency [13]. When a positive drain bias is applied, holes are pushed toward the gate contact, where they can be emitted, leaving a net negative charge in the p-GaN and thus leading to the positive V_{TH} shift. The negative transient is possibly ascribed to the generation of positive charges during the drain stress, as previously shown in [15], that are then accumulated under the gate stack because of the band bending [16] In wafer H, this phenomenon is suppressed by the higher leakage of electrons injected from the gate stack during the OFF-state stress (not shown).

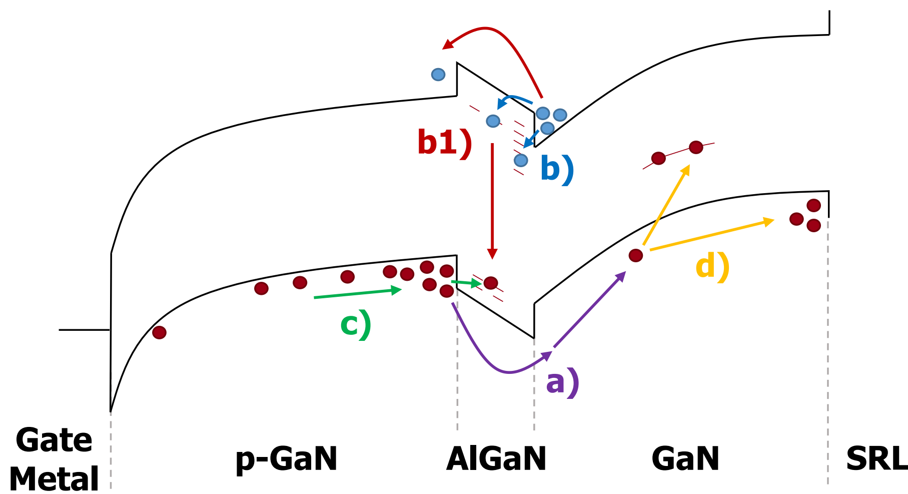

Fig. 6. Mechanisms involved in the threshold voltage instabilities in the devices under test: a) hole depletion from the p-GaN (positive V_{TH} shift); b) trapping of electrons in the AlGaN/GaN interface and/or in AlGaN traps (positive V_{TH} shift); c) hole accumulation in the 2DHG and consequent hole trapping in the AlGaN (negative V_{TH} shift); d) hole trapping in the GaN buffer and/or in the SRL interface (negative V_{TH} shift); b1) mechanisms occurring in Wafer L, that makes the V_{TH} more stable.

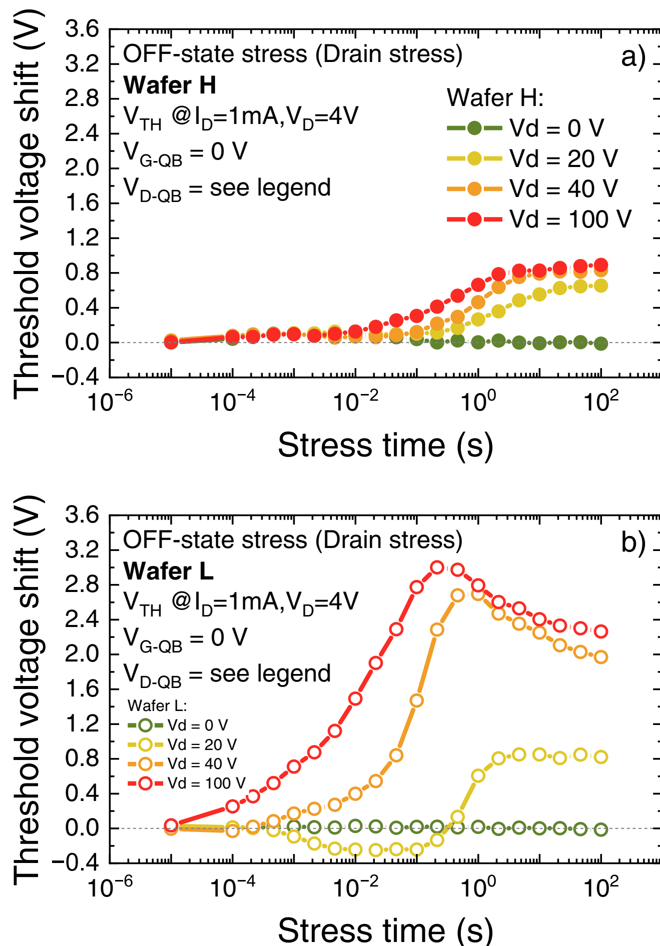

Fig. 7. Threshold voltage shift induce by OFF-state (drain) stress for: a) Wafer H; b) Wafer L.

Remarkably, as during ON-state stress, test structures with higher gate leakage current show better V_{TH} stability and faster detrapping processes (not shown).

5. Conclusions

We reported a detailed investigation of the impact of electron gate leakage on the V_{TH} stability of normally-off p-GaN gate power HEMTs test structures. Based on DC, pulsed and transient measurements we demonstrated: a) the existence of 4 different charge-trapping processes, whose interplay determines the sign and amplitude of the threshold voltage variation during ON-state stress; b) a reasonable increase in gate leakage is beneficial for eliminating the negative V_{TH} shift under positive gate bias, and for minimizing the positive V_{TH} shift under off-state stress. The results are of relevance for the development and optimization of normally-off GaN HEMTs with p-GaN gate.

CRediT authorship contribution statement

All authors contributed equally to the paper.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

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