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A Two-Stage DC-DC Isolated Converter for Battery-Charging Applications

NICOLA ZANATTA [1] (Student Member, IEEE), TOMMASO CALDOGNETTO [1] (Senior Member, IEEE), DAVIDE BIADENE [1] (Member, IEEE), GIORGIO SPIAZZI [2] (Member, IEEE), AND PAOLO MATTAVELLI [1] (Fellow, IEEE)

[1]Department of Management and Engineering, University of Padova, 35122 Vicenza, Italy
[2]Department of Information Engineering, University of Padova, 35122 Padova, Italy

CORRESPONDING AUTHOR: NICOLA ZANATTA (e-mail: nicola.zanatta.2@phd.unipd.it)

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ABSTRACT This paper proposes and analyzes a two-stage dc-dc isolated converter for electric vehicle charging applications, where high efficiency over a wide range of battery voltages is required. The proposed conversion circuit comprises a first two-output isolation stage with CLLC resonant structure and a second two-input buck regulator. The transformer of the first stage is designed such that its two output voltages correspond, ideally, to the minimum and maximum expected voltage to be supplied to the battery. Then, the second stage combines the voltages provided by the previous isolation stage to regulate the output voltage of the whole converter. The first stage is always operated at resonance, with the only function of providing isolation and fixed conversion ratios with minimum losses, whereas the second stage allows output voltage regulation over a wide range of battery voltages. Overall, it is shown that the solution features high conversion efficiency over a wide range of output voltages. This paper comprehensively describes the solution, including modeling, analyses, design considerations for the main circuit components (e.g., magnetics, switches), and modulation choices. Experimental results are reported considering a converter module prototype rated 10 kW, input voltage 800 V, and output range 250 V to 500 V, employing silicon-carbide and gallium-nitride semiconductors.

INDEX TERMS Battery charger, CLLC, dc-dc converter, dc-transformer (DCX), fast-charging, gallium-nitride, resonant LLC, post-regulator, silicon-carbide, soft-switching, two-input buck converter.

I. INTRODUCTION

Electric transportation is gaining ground in many countries due to growing concerns about global greenhouse gas emissions and fossil fuel supply and depletion. These concerns have lately propelled the exponential growth of the demand for electric vehicles (EVs) [1], [2]. Such a high demand combined with the strive for longer ranges and reduced charging time is pushing newer generations of EVs that implement higher battery capacities and charging rates. Consequently, new EV charging stations are needed to supply more power, more quickly than ever before [3], [4], [5].

Moreover, new wide-bandgap (WBG) semiconductors are setting unprecedented performance levels in terms of power density and efficiency. Current WBG devices based on silicon carbide (SiC) or gallium nitride (GaN) power switches easily outperform those based on silicon (Si) in numerous applications, thanks to their higher voltage breakdown, higher switching speed and lower on-resistance. The design of EV power electronics converters in an example of a modern relevant application [4].

A. CHALLENGES

DC-DC converters with galvanic isolation are the beating heart of an effective EV battery charging system [6], [7], [8], [9]. Several topologies are highlighted in the literature for their merits in terms of efficiency and power density, such as the dual-active-bridge (DAB) and the resonant converter [5], [7], [10], [11], [12], [13], [14]. The resonant LLC and CLLC converters are commonly adopted in many applications for their simple structure and efficient power conversion.

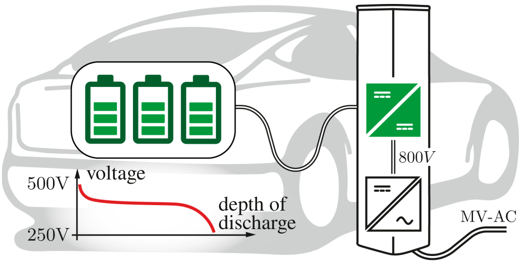

FIGURE 1. EV-charging application.

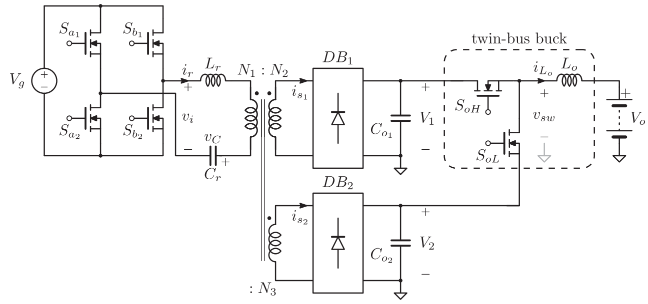

FIGURE 2. Proposed two-stage topology: two-output dc-transformer & post-regulator.

These converters present the merit of an inherent zero-voltage switching (ZVS) and zero-current switching (ZCS) operation for primary-side and secondary-side switches, respectively [12], [15], [16]. In these topologies, output voltage regulation is normally obtained through frequency modulation. However, performance significantly degrades at input or output voltages that do not allow near-resonance operation [7], [12], [17], [18]. Conditions that impede near-resonance operation for classical LLC and CLLC converters are often encountered in the considered application in Fig. 1, where battery state of charge variations due to typical mission profiles may bring to wide ranges of operating voltages [2], [5], [7], [19], [20].

B. LITERATURE OVERVIEW

Numerous approaches and methods to overcome the limitations of these frequency-modulated resonant converters are reported in the literature [12], [18], [21]. Herein are summarized the main relevant methods. Solutions include variants in the conversion circuits related to the primary-side [22], [23], [24] or the secondary-side [25], [26], [27], [28], [29], the resonant tank [30], [30], [31], [32], the application of strategies like the partial-power processing [8], [12], [33], [34], [35], [36], [37], [38], [39], [40], [41], and the design of structures using multiple stages of conversion [21], [42], [43], [44]. Converters that adopt reconfigurable structures as described, for example, in [20], [22], [26], [28], can obtain wide voltage gain, but achieving smooth transitions between the different configurations may be difficult to cope with. Solutions implementing partial-power processing strategies show potential advantages to accommodate wide operating voltage ranges and high efficiency, at the cost of a high components number and complex design and modulation [33], [40].

An effective method to overcome the limitations of the frequency-modulated LLC converter is to keep working the LLC stage at its optimal operating point (i.e., DCX operation) [15], [16] and employ an additional conversion stage to regulate the output voltage, which results in multi-stage structures [42], [43], [44], [45], [46]. In these structures, the isolated DCX-LLC resonant converter, widely used in applications including power supply, energy storage, data centers, and solid-state transformers, is often employed because it can interface with galvanic isolation two dc buses involving very limited power losses [15], [16]. These multi-stage topologies are favorable to accommodate wide operating voltage ranges with very high efficiencies; however, more components are required, which might reduce the overall power density.

The integration of power switches in multi-stage structures are studied in several paper to address these disadvantages [21], [47], [48], [49]. The half-bridge LLC converter could be integrated with a boost structure by sharing the switches and regulating the voltage via the duty cycle. Compared with two-stage topologies, these can reduce the number of switching devices. However, using the boost stage for voltage regulation and the related high conduction losses can affect efficiency.

Table 1 summarizes some relevant converter structures for EV fast-charging applications. For each approach, the table includes the core topology and the related class (Cl.): Cl. 0 represents classic topologies; Cl. 1 represents topologies with modifications in the primary or secondary-side structures; Cl. 2 represents modifications in the resonant tank; Cl. 3 represents topologies that adopt additional partial-power processing stages, and Cl. 4 represents multi-stage topologies. The table also reports, for each topology: the presence of an ac front-end (ac-FE) stage, the input voltage of the dc stage v_{IN} and its output voltage v_{OUT}, the rated power P_{OUT}, the peak efficiency $\eta^{\max}$, and the number of active switches, diodes, transformers, and inductors used in the dc/dc stage, indicated by the symbols S, D, T, and L, respectively. Noticeably, the relevant research on the topic focuses on developing high-efficient dc-dc conversion solutions.

C. PROPOSED SOLUTION

Based on the brief literature overview reported above, to improve the performance of the LLC resonant dc-dc converter in a wide output-voltage range, a two-stage conversion structure in which the second stage performs the post-regulation of the output voltage is considered, analyzed, and experimentally evaluated in this paper. The proposed structure is displayed in Fig. 2. The post-regulation stage is directly connected to intermediate dc-links (i.e., V_1 and V_2), supplied by an isolation stage based on a resonant LLC-like structure with two outputs. The principle of the proposed solution is to operate

TABLE 1 Representative Approaches for High-Efficiency Converters for EV-Charging Applications

Cl.	Ref.	Topology	ac-FE	v_{IN}	v_{OUT}	P_{rated}	$\eta_{\max}$	S/D/T/I*	Peculiarities
0	[10]	HB-CLLC	no	500 V	200 - 420 V	1 kW	96.5% (0.6 kW, 300 V-out)	4/0/1/2	Bidirectional operation, limited controllability under wide v_{OUT}.
0	[17]	LLC	no	380 - 420 V	400 V	6.6 kW	98% (3 kW, 390 V-in)	4/4/1/0	High η, wide variation of f_{sw}, narrow v_{IN}, fixed v_{OUT}, η drops far from resonance.
1	[26]	FB/HB-LLC + VD	no	400 V	100 - 400 V	2 kW	96.36% (0.5 kW, 200 V-out)	6/4/1/0	Wide controllable v_{OUT}, high η over a wide load range.
3	[51]	switched tank	no	200 - 400 V	1200 V	4 kW	97.71% (4 kW, 350 V-in)	22/0/0/6	Low volume, no galvanic isolation.
0	[52]	phase-shift FB	no	700 - 800 V	350 - 700 V	20 kW	98.9% (13 kW, 700 V-in, 686 V-out)	4/4/1/1	High η, hard switching operated.
0	[53]	LLC	yes	7 kV	400 V	350 kW	98.6% (350 kW, 400 V-out)	6/0/1/1	10 kV SiC devices, 4.16 kV ac grid input, limited controllability under the wide v_{OUT}.
3	[38]	CLLC + buck	no	750 V	314 - 450 V	18 kW	98.8% (18 kW, 375 V-out)	20/0/2/3	High η and power density.
1	[20]	interleaved LLC	no	390 V	230 - 440 V	1.3 kW	97.31% (1.3 kW, 440 V-out)	6/6/2/0	Limited v_{OUT} range.
4	[42]	ISOP boost + LLC	no	1 - 2 kV	700 V	12 kW	93.7% (12 kW, 1.2 kV-in)	5/5/1/1	Modularity, high pre-regulator losses.
1	[24]	LLC	no	160 - 320 V	400 V	1 kW	95.2% (1 kW, 160 V-in)	4/4/2/1	Wide v_{IN}, simple control, fixed v_{OUT}.
0	[54]	CLLC	no	400 V	250 - 450 V	1 kW	97.9% (1 kW, 325 V-out)	4/0/1/2	Wide v_{OUT}, low η far from resonance.
1	[23]	interleaved LLC	no	390 V	10 - 420 V	1 kW	98.1% (0.82 kW, 420 V-out)	4/4/2/0	Very wide v_{OUT}.
1	[27]	LLC + VQ	no	390 V	250 - 420 V	1.3 kW	93.94% (0.95 kW, 420 V-out)	5/6/1/1	Wide v_{OUT}.
0	[55]	LLC	yes	380 - 660 V	200 - 500 V	6.6 kW	98% (6.6 kW, 440 V-out)	8/0/1/1	Bidirectional, low voltage-gain of the dc/dc stage, 220 V ac input.
2	[30]	LLC with adj. transf.	no	390 V	126 - 420 V	1 kW	97.18% (0.7 kW, 420 V-out)	8/6/1/1	Smooth transitions without transients.
0	[4]	CLLLC	yes	650 - 900 V	214 - 413 V	11 kW	98.75% (11 kW, 792 V-in, 330 V-out)	8/0/2/2	Bidir., 380 V input PFC for voltage regulation.
1	[56]	active NPC DAB	no	10 kV	700 V	30 kW	99.1% (10 kW, 700 V-out)	10/0/1/1	High η and power density, fixed conversion ratio, careful layout and integrated modules required.
4	[44]	3-phase CLLC + buck	no	850 V	200 - 800 V	12.5 kW	97.72% (12.5 kW, 800 V-out)	20/0/3/4	Ultra wide v_{OUT} for 400 and 800 Vbattery systems, low η over the wide range, high component count.
0	[3]	interleaved buck	yes	900 V	200 - 650 V	22 kW	99.51% (22 kW, 200 V-out)	6/0/0/6	Very high η, no galvanic isolation, 480 V ac input.
3	[12]	3-port CLLC + PPP	no	388 - 412 V	250 - 450 V	2.3 kW	98% (2.3 kW, 450 V-out)	8/0/1/1	PPP, with low-voltage devices, and limited overall conduction losses, high component count and complexity.
3	[40]	2-level LLC + PPP	no	1500 V	630 - 900 V	50 kW	NA	14/8/2/4	Modularity, utilization of low voltage semiconductors.
0	[57]	buck-boost	yes	150 V	48 - 450 V	1.5 kW	95.6% (1.5 kW, 110 V-in ac, 250 V-out)	6/0/0/2	Bidir., non-isolated, limited η, 85-265 V ac input.
0	[58]	phase-shift FB	yes	400 V	330 V	3.3 kW	97.2% (3.3 kW, 330 V-out)	4/4/1/1	On-board charger, 230 V ac input.
0	[29]	resonant LCL-T	no	800 V	150 - 500 V, 500 - 950 V	6.6 kW	98.2% (6.6 kW, 580 V-out)	8/0/1/2	Wide v_{OUT}, reconfigurable rectifier, phase shift modulation, resonant network for η optimization during CC charging phase.
4	[21]	Buck-Boost + LLC	no	800 V	250 - 500 V	5 kW	98% (3 kW, 400 V-out)	4/4/1/1	Very wide voltage gain (potential), high losses at light-load.
4	herein	CLLC + twin-bus buck	no	800 V	250 - 500 V	10 kW	98.63% (7 kW, 500 V-out)	8/8/1/2	Wide v_{OUT}, simple control, high component count.

* S/D/T/I: number of active switches, diodes, transformers, and inductors, respectively.

the first isolation stage at maximum efficiency, namely, at resonance, and use the post-regulation stage to perform output voltage regulation, with minimum voltage stresses. The parallel structure of the second stage and its operation with limited voltage stresses allow low conversion losses over the wide range of output voltages of the considered battery charging application. The high overall conversion efficiency over the wide range of operating voltages is achieved at the cost of a higher number of components. The solution is demonstrated with reference to a dc-dc conversion module rated 10 kW with a nominal input voltage of 800 V and output voltage ranging from 250 V to 500 V [5]. The input voltage is assumed to be provided by a front-end three-phase power-factor-correction stage. Noteworthy, the scaling of the conversion module and/or the use of multiple modules connected in parallel may be required for field use, as typically done in actual implementations.

This paper extends the preliminary results presented in [50]. In addition to the extended literature review discussed in this Sections I and II includes details on the operating principle of the converter, with the main relations governing the design of the proposed solution now highlighted and discussed; Section III is dedicated to the design of the DCX stage, and it reports further details on the designed transformer; Section IV presents a comparison with other representative topologies, which are herein also compared in terms of losses, including now a loss breakdown analysis for each of the solution; extended experimental results are reported in Section V considering a converter module prototype rated 10 kW. Finally, Section VI concludes the paper.

II. STRUCTURE AND OPERATING PRINCIPLE

A. TWO-STAGE CONVERTER CONFIGURATION

Several configurations of two-stage dc-dc converters exploiting a voltage post-regulator are described in the literature [39], [59], [60]. As shown in Fig. 2, the proposed two-stage converter consists of a first isolation stage based on an LLC resonant converter, and a second post-regulator stage based on a buck converter. Such a post-regulator is responsible of the output voltage regulation and it is supplied by means of a high-efficiency two-output DCX converter, with secondary voltages V_1 and V_2. From Fig. 2, it is clear that the voltage stress of the post-regulator, namely, $V_1 - V_2$, is lower that the output voltage V_o, which consequently allows switching devices with smaller on-resistance as well as lower switching losses.

It is worth remarking that the topology where the two DCX-LLC outputs are connected in series can also be considered. This variant will be considered in future investigations. Preliminary studies, shown as potential advantage in the transformer design but as disadvantage the additional losses due to the output current passing trough both the two diodes-rectifier bridges.

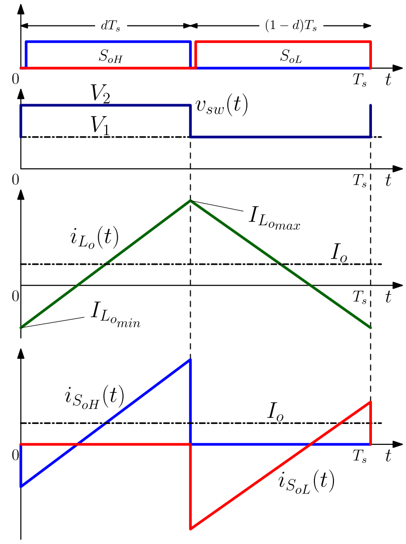

FIGURE 3. Main waveforms of TBB stage shown in Fig. 2. In order: gate driver signals including dead times, switching node voltage of TBB, L_o inductor current and S_{oH}, S_{oL} switch currents.

B. OPERATING PRINCIPLE

The two-output LLC resonant converter is designed for a constant voltage conversion ratio, independent from the actual load. In such an operating condition the LLC behaves as two-output DCX converter and its voltage gains can be defined as follows:

$$G_1 = \frac{V_1}{V_g} = \frac{N_2}{N_1} = n_1$$
$$G_2 = \frac{V_2}{V_g} = \frac{N_3}{N_1} = n_2 \tag{1}$$

where N_1, N_2, and N_3 are the number of turns of the three windings of the transformer, as indicated in Fig. 2.

The two-input post-regulator, herein referred to as twin-bus buck (TBB) converter, is highlighted in Fig. 2 while its main waveforms are displayed in Fig. 3. It is based on a two-input buck topology [61], [62], designed to operate in quasi-square wave, that is, with a peak-to-peak inductor current ripple higher than twice the average load current. This allows zero-voltage turn-on of both the switches S_{oH} and S_{oL}. The TBB is responsible of the output voltage regulation of the whole converter. The output voltage V_o is a function of the TBB input voltages V_1 and V_2, with $V_1 > V_2$, and the duty cycle d of the upper switch S_{oH}:

$$V_o = d\,V_1 + (1-d)\,V_2 \tag{2}$$

Therefore, the voltage gain of the converter in Fig. 2 results:

$$G = \frac{V_o}{V_g} = d\,n_1 + (1-d)\,n_2 \tag{3}$$

TABLE 2 Converter Parameters

Parameter	Symbol	Value	
Input voltage	V_g	800	V
Output voltage	V_o	250 - 500	V
Nominal output voltage	V_o^{nom}	400	V
Maximum output current	I_o^{max}	25	A
Nominal power	P_o^{nom}	10	kW
Switching freq. of CLLC	f_s	200	kHz
Switching freq. of TBB	f_{s_o}	50 - 400	kHz
Turns ratio N_2/N_1	n_1	0.625	-
Turns ratio N_3/N_1	n_2	0.292	-
Intermediate bus V_1	V_1	500	V
Intermediate bus V_2	V_2	234	V
Magnetizing inductance	L_m	215	µH
	L_{r_1}	795	nH
Leakage inductances	L_{r_2}	445	nH
	L_{r_3}	271	nH
TBB inductor	L_o	30	µH
Transformer	Core: PQ65/60, Material: N87		
Inductor	Core: PQ40/40, Material: N97		
	C_{r_1}	796	nF
Resonant capacitances	C_{r_2}	1.42	µF
	C_{r_3}	2.34	µF
S_{a_1}, S_{a_2}, S_{b_1}, S_{b_2}	G3R30MT12K, 1.2 kV SiC MOSFETs		
S_{oH}, S_{oL}	LMG3422R030, 600 V GaN FET		
Output Rectifier DB_1	UJ3D06560KSD, 650 V SiC diodes		
Output Rectifier DB_2	STTH100W04CW, 400 V Si diodes		

For fixed input voltages V_1 and V_2, the minimum and maximum output voltages can be defined as:

$$V_o^{\min} = d^{\min} V_1 + (1 - d^{\min}) V_2$$
$$V_o^{\max} = d^{\max} V_1 + (1 - d^{\max}) V_2 \tag{4}$$

with $d^{\min}$ and $d^{\max}$ the minimum and maximum duty cycles of S_{oH}, corresponding to $V_o^{\min}$ and $V_o^{\max}$ in Table 2, respectively. Their value must guarantee the zero-voltage switching operation of S_{oH} and S_{oL} at the respective output voltage levels. Thus the needed input voltages V_1 and V_2 provided by the DCX stage, can be calculated from (4) as:

$$V_1 = \frac{V_o^{\max}(1 - d^{\min}) - V_o^{\min}(1 - d^{\max})}{d^{\max} - d^{\min}}$$
$$V_2 = \frac{V_o^{\min} d^{\max} - V_o^{\max} d^{\min}}{d^{\max} - d^{\min}} \tag{5}$$

and the voltage gains (1) of the DCX-LLC can be derived.

By using (5), the maximum voltage stress of the switches can be computed as:

$$V_1 - V_2 = \frac{V_o^{\max} - V_o^{\min}}{d^{\max} - d^{\min}} \tag{6}$$

which is always lower than the voltage stress of the switches of a full-power converter that requires a supply voltage higher than the maximum output voltage. In order to minimize such voltage stress, and the related switching loss, the duty-cycle excursion $d^{\max} - d^{\min}$ should be maximized; then, for example, by imposing $d^{\min} = (1 - d^{\max}) = 5\%$. Consequently, the converter in Fig. 2 with voltage ratings $V_o^{\max} = 2\,V_o^{\min} = 500\,\mathrm{V}$ presents a voltage stress on the switching devices of $V_1 - V_2 = 278\,\mathrm{V}$, allowing the use of devices of low rated-voltages, which typically implies lower losses [37], [38].

Once the duty-cycle range of the TBB stage is defined, zero-voltage switching (ZVS) can be achieved with a proper selection of the output inductor value and the switching frequency, for the whole output voltage range. As shown in Fig. 3, the TBB is operated in continuous conduction mode (CCM) and the inductor current at switching instants can be computed as:

$$I_{L_{o max}} = I_o + \frac{V_1 - V_2}{2 f_s L_o} d\,(1 - d)$$
$$I_{L_{o min}} = I_o - \frac{V_1 - V_2}{2 f_s L_o} d\,(1 - d) \tag{7}$$

In order to achieve zero-voltage switching, these current values should satisfy the minimum switched current conditions for ZVS (refer, e.g., to [13], [16], [21], [63], [64], [65]). The inductor current value and the switching frequency of the TBB stage are key parameters for the converter design and operation over the whole range of output voltages and powers.

III. DESIGN OF LLC STAGE OPERATED AS DCX

The converter structure is shown in Fig. 2. When the LLC resonant tank is operated at the resonance frequency, the voltage conversion ratio becomes ideally independent from the actual load. In other words, the LLC converter maintains a constant voltage conversion ratio and adjusts its current automatically, according to the load conditions, behaving as a DCX. In this operating condition, the LLC shows its maximum efficiency, with a minimum flow of reactive power and zero-voltage switching (ZVS) and zero-current switching (ZCS) conditions always satisfied [37]. Notably, the DCX operation of the LLC does not require an external resonant inductor, because the conversion gain is fixed. An equivalent solution based on a resonant FB-LLC designed to operate over the same wide range of output voltages is expected to show higher losses than the LLC in permanent DCX conditions, as demonstrated in Section IV-B.

From (1) and (5) and considering $d^{\min} = (1 - d^{\max}) = 5\%$, the transformer turns ratio can be calculated as $n_1 = N_2/N_1 = 0.642$ and $n_2 = N_3/N_1 = 0.295$ to make the LLC converter operate at the resonant frequency f_s at input voltage $V_g = 800\,\mathrm{V}$ and output bus voltages V_1 and V_2 as in (5).

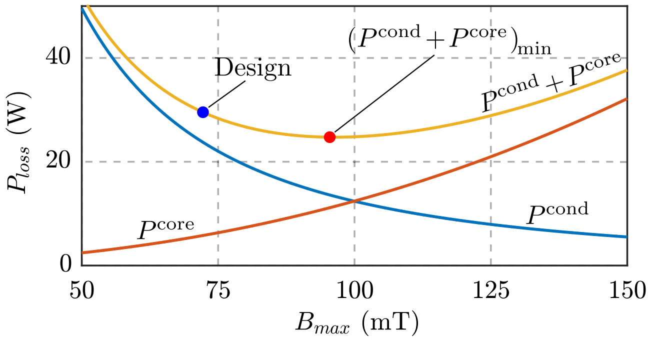

FIGURE 4. P-B plot for transformer design at $V_o = 400\,\text{V}$ and $P_o = 10\,\text{kW}$.

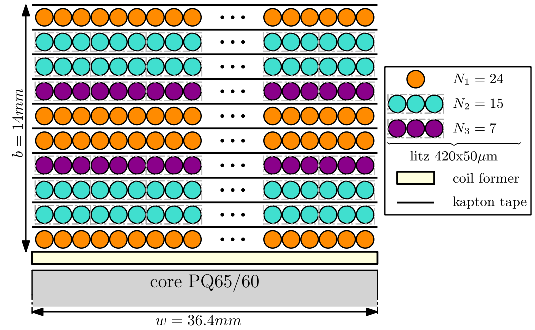

FIGURE 5. Winding arrangement at the design point in Fig. 4.

A. TRANSFORMER DESIGN

In the design of the main magnetic element, both winding and core losses must be considered. The transformer design procedure adopted herein is based on [21], [47], [66].

Once the magnetic core is selected, with given magnetic volume V_c, window winding area W_a, core cross-sectional area A_c, Steinmetz parameters K_c, α and β, and maximum window filling factor k_u (typ., assume $k_u \leq 40\%$), it is possible to calculate the winding losses as:

$$P^{\text{cond}} = RF(f_s)\rho_w V_w k_u J_0^2 \tag{8}$$

where ρ_w is the copper resistivity, V_w is the total windings volume, $RF(f_s) = R^{\text{ac}}/R^{\text{dc}}$ is the resistivity factor for the selected litz wire at fundamental frequency f_s [66] and J_0 is the current density. The last parameter is calculated as:

$$J_0 = \frac{\sum VA}{K_v f_s k_f B_{\max} k_u A_p} \tag{9}$$

where $\sum VA$ is the power rating of the transformer, K_v is the waveform factor, $B_{\max}$ is the peak flux density, k_f is core stacking factor, and $A_p = A_c W_a$ is the area product of the core.

The core losses can be estimated using the Steinmetz equation:

$$P^{\text{core}} = V_c K_c f_s^{\alpha} B_{\max}^{\beta} \tag{10}$$

where K_c, α and β are the Steinmetz parameters for the considered material, while V_c is the core volume. The total transformer dissipated power is then computed as the sum of (8) and (10) and it must be lower than the thermal dissipation capability of the component at the desired operating temperature, which can be estimated during the design phase. Fig. 4 reports the results of the calculated transformer losses, showing a total loss of 24 W at nominal conditions, namely, $V_1 = 514\,\text{V}$ and $V_2 = 236\,\text{V}$, and $P_o = 10\,\text{kW}$. According with Fig. 4, the selected design point is more conservative in terms of core losses with respect to the optimal point, this is due to a trade-off between the desired magnetizing inductance and the conductor sections.

Fig. 5 depicts the winding layout of the designed transformer of Fig. 6(a). The designed transformer presents turns ratio $n_1 = 0.625$ and $n_2 = 0.292$, current density $J_0 =$ $5\,\text{A/mm}^2$, number of turns per winding $N_1 = 24$, $N_2 = 15$, $N_3 = 7$.

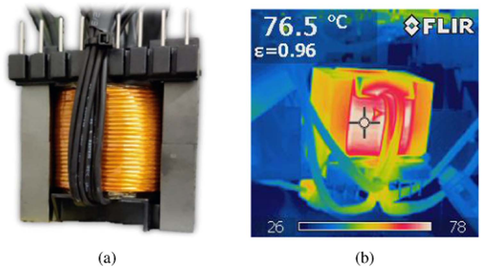

FIGURE 6. (a) Transformer prototype, and (b) thermography at the design point in Fig. 4, namely, $V_o = 400\,\text{V}$, $P_o = 10\,\text{kW}$, natural convection conditions.

B. RESONANT TANK DESIGN

For what concerns the design of the resonant L_rC_r tank, the transformer leakage inductance can be exploited for the implementation of the inductive part. Given the DCX operation mode of the LLC, low values of L_m can be used, which is beneficial in terms of transformer design, losses, and resonant capacitor voltage stress. With the aimed DCX operation, the value of the magnetizing inductance L_m is typically chosen to ensure a sufficiently high magnetizing current to allow ZVS for all the switches of the main converter. A classical design for a DCX-LLC with voltage ratings of Table 2 requires a magnetizing inductance of about $200\,\mu\text{H}$ (see, for example, [16], [21], [37]). The designed transformer in Fig. 6(a) achieves the design target, with a magnetizing inductance of about $215\,\mu\text{H}$.

The capacitive part of the resonant tank can be selected on the basis of the desired resonant frequency (i.e., converter switching frequency at DCX-LLC operation). The winding arrangement of the designed transformer in Fig. 4 is shown in Fig. 5. The interleaving of the primary and secondary-side windings is an effective solution to limit the leakage inductance and winding losses [67]. The experimental prototype in Fig. 6(a), which results from the design in Fig. 4 and winding arrangement in Fig. 5, presents values of leakage inductances

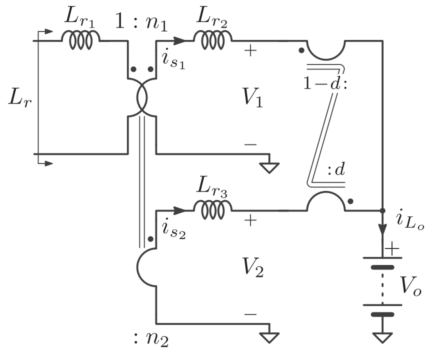

FIGURE 7. Equivalent circuit model for the estimation of resonant inductance at the primary side of the transformer, namely L_r in Fig. 2.

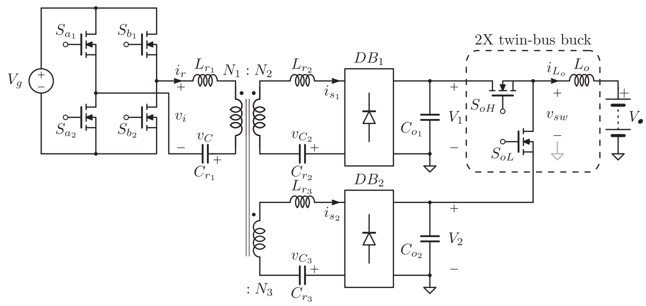

FIGURE 8. Overall circuit schematic of the solution described herein, composed of a DCX-CLLC stage plus two interleaved twin-bus buck stages.

$L_{r_1} = 795\,\text{nH}$, $L_{r_2} = 445\,\text{nH}$, and $L_{r_3} = 271\,\text{nH}$ for the input, high-voltage, and low-voltage windings, respectively. The secondary windings leakage inductances L_{r_2} and L_{r_3} affect the overall resonance frequency proportionally to the normalized conduction interval of the respective diode bridge rectifier. In fact, these inductances come into play only when the corresponding rectifying diodes are conducting, and these intervals are related to the duty-cycle of the TBB stage, as well as to the load current. The TBB stage imposes a strict relationship between the average charge transferred through each output ports of DCX-LLC stage with respect to the output voltage V_o and current I_o. Then, the stage can be modelled as shown in Fig. 7. The series-equivalent inductance L_r of the resonant tank referred to the primary side of Fig. 7 can be calculated as:

$$L_r = L_{r_1} + \frac{d^2 L_{r_2} + (1-d)^2 L_{r_3}}{[n_1 \tilde{} d + n_2(1-d)]^2} \tag{11}$$

which is a function of the converter operating point, according to (2). The validity of (11) is shown in Section IV referring to a specific operating point. In order to remove the dependence of the resonance frequency from the load, two additional resonant capacitors are connected in series with the two output ports of the transformer, as shown in Fig. 8. At resonance, the capacitive part of each of the series-resonant impedances $L_{r_i}C_{r_i}$ cancels out with the corresponding inductive part. $C_{r_1} = 796\,\text{nF}$, $C_{r_2} = 1.42\,\mu\text{F}$ and $C_{r_3} = 2.34\,\mu\text{F}$ are then calculated as proper values for the resonant capacitances in order to achieve a continuous resonant current operation, where the resonant frequency of the CLLC stage becomes independent from the duty-cycle and the output current of the TBB stage, as otherwise shown in (11). The proposed post-regulated converter is then shown in Fig. 8.

IV. SIMULATION RESULTS

A. DCX RESONANT CURRENT OPERATION

A converter topology with parameters reported in Table 2 is considered for validation. Based on the considerations reported in Section III, herein are reported the simulation results focused on demonstrating the continuous resonant current operation of the DCX stage. First, the operation of the converter in Fig. 2 is considered with a single resonant capacitor C_r and, then, the operation of the proposed converter in Fig. 8 is considered. Converters in Figs. 2 and 8 are simulated and the resonant currents are shown in Fig. 9. Let us consider different operating points at the maximum output current $I_o = 25\,\text{A}$ and minimum, nominal, and maximum output voltage V_o (i.e., 250, 400, 500 V). Fig. 9(a)–(c) shows the resonant currents i_r, i_{s_1}, and i_{s_2}, and the magnetizing current i_m of the circuit in Fig. 2 with resonant capacitance $C_r = 174\,\text{nF}$. Such a value is designed to have the desired resonance frequency f_s, with $L_r = 3.64\,\mu\text{H}$ given by (11) at $V_o = 250\,\text{V}$. Indeed, the current i_{s_2} is resonant only in such an operating point. While, Fig. 9(d)–(f) shows the resonant currents considering the circuit in Fig. 8 with resonant capacitances C_{r_i} in Table 2. Simulation results show that the resonance conditions are satisfied, for the whole wide output voltage range, only in this later case. Furthermore, conduction losses are minimized only if the resonance conditions are satisfied. Based on the obtained results, the CLLC solution is considered for the investigations in the following.

B. PERFORMANCE COMPARISON

This section compares three different topologies, namely, the classical full-bridge LLC (FB-LLC), the buck-boost LLC presented in [21] (reported in Fig. 10 for reference), and the solution proposed herein. As discussed in Section I, these last two multi-stage topologies present higher efficiency than the classical frequency-modulated LLC converter. The considered topologies are rated 10 kW and have been carefully designed in order to optimize their performances. The FB-LLC is designed to allow the required output voltage range, while the FB-LLC of the proposed two-stage solution is designed for DCX operation. In principle, the FB-LLC for DCX operation allows lower loss because it does not require an inductor for accommodating a wide voltage gain range.

Fig. 11 reports and compares the efficiency curves of the three topologies for $V_o = 250\,\text{V}$, 400 V, and 500 V. The

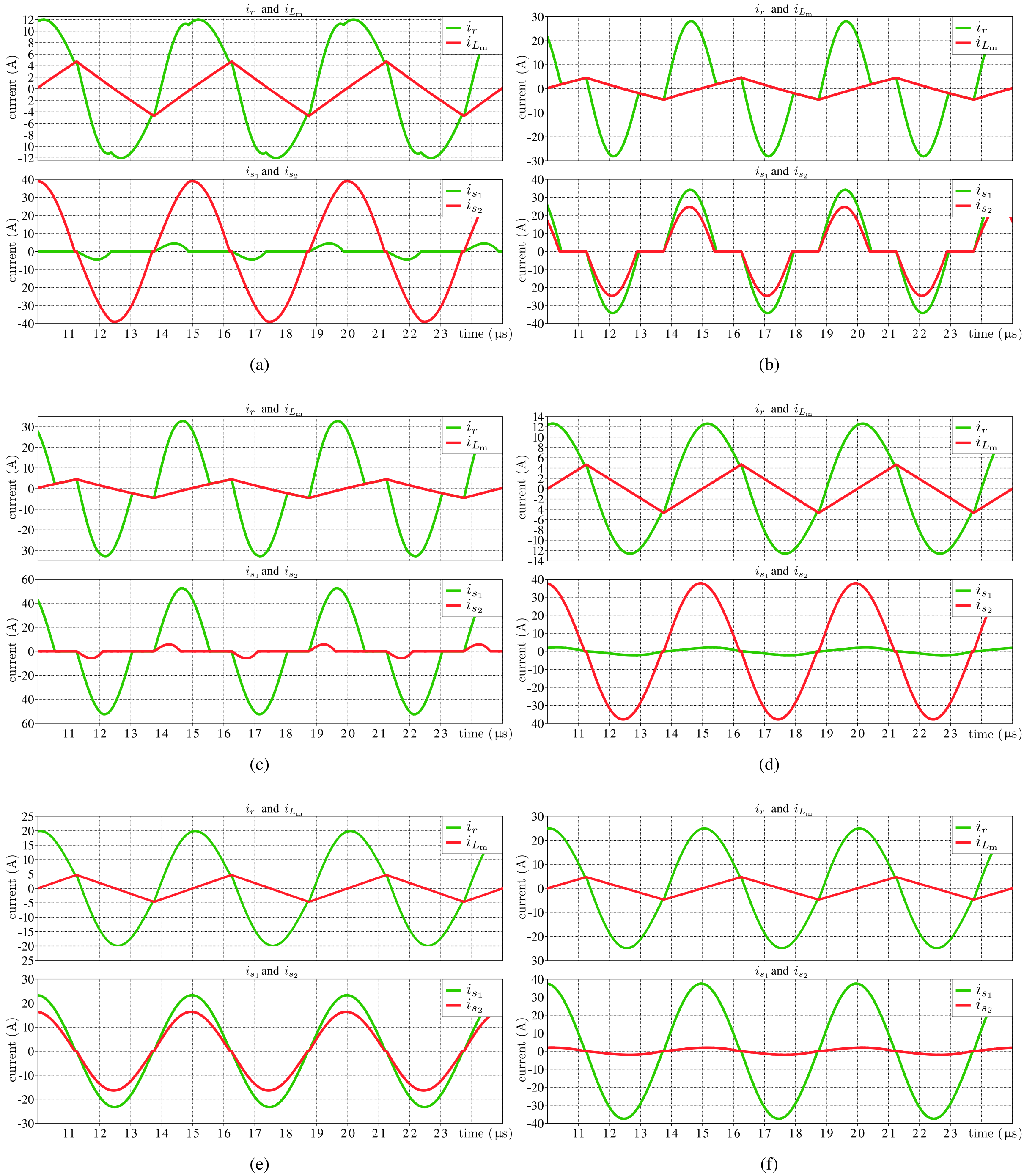

FIGURE 9. Simulation results for LLC with different resonant tank designs, (a)–(c) refer to Fig. 2 and (d)–(f) refer to Fig. 8. (a), (d) $V_o = 250$ V; (b), (e) $V_o = 400$ V; (c), (f) $V_o = 500$ V. $I_o = 25$ A. Converter parameters are reported in Table 2.

results are obtained by PLECS models tuned for accurately accounting for switching, magnetic, and conduction losses [21]. Such models were validated experimentally by means of thermal measurements in [21]. The efficiency performances of the topology in [21] is limited due to the high conduction and switching losses in the pre-regulation stage. The frequency-modulated FB-LLC converter has low-efficiency performances in the minimum output voltage range due to the limited voltage gain and the higher switching frequencies. Furthermore, the low Q-factor in the light-load region and minimum output voltage pose a lower limit in the transferred power due to the upper limit in the switching frequency. This would require the adoption of dedicated modulation provisions in the low-voltage region. An interleaved version of the proposed topology in [21] has also been considered for evaluation, providing negligible benefits. Fig. 12 shows the

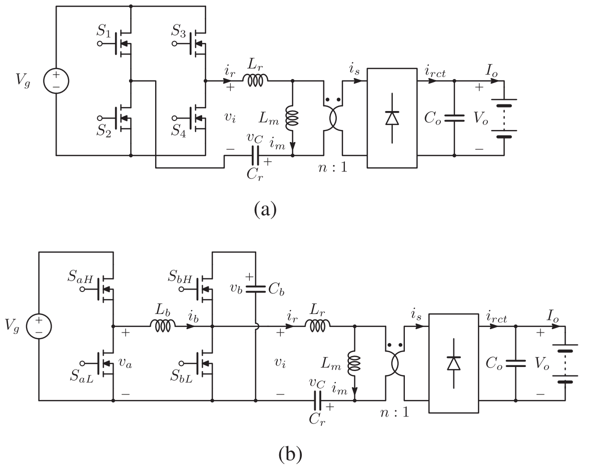

FIGURE 10. Additional topologies considered for efficiency and loss comparisions in Section IV. (a) FB-LLC, (b) solution in [21].

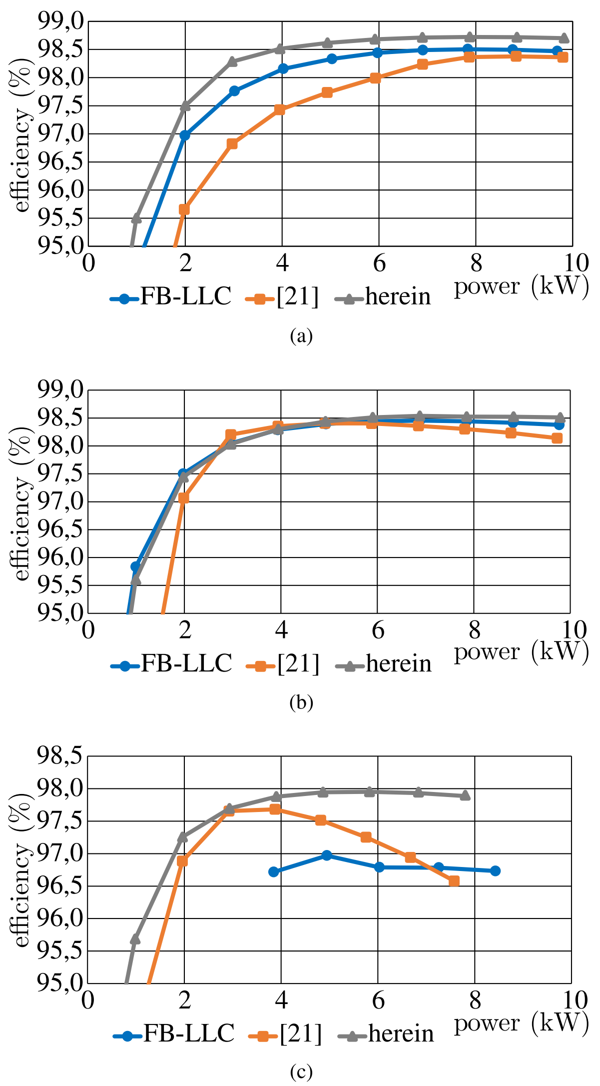

FIGURE 11. Efficiency comparison: full-bridge LLC, topology in [21], and solution herein. (a) $V_o = 500$ V, (b) $V_o = 400$ V and (c) $V_o = 250$ V.

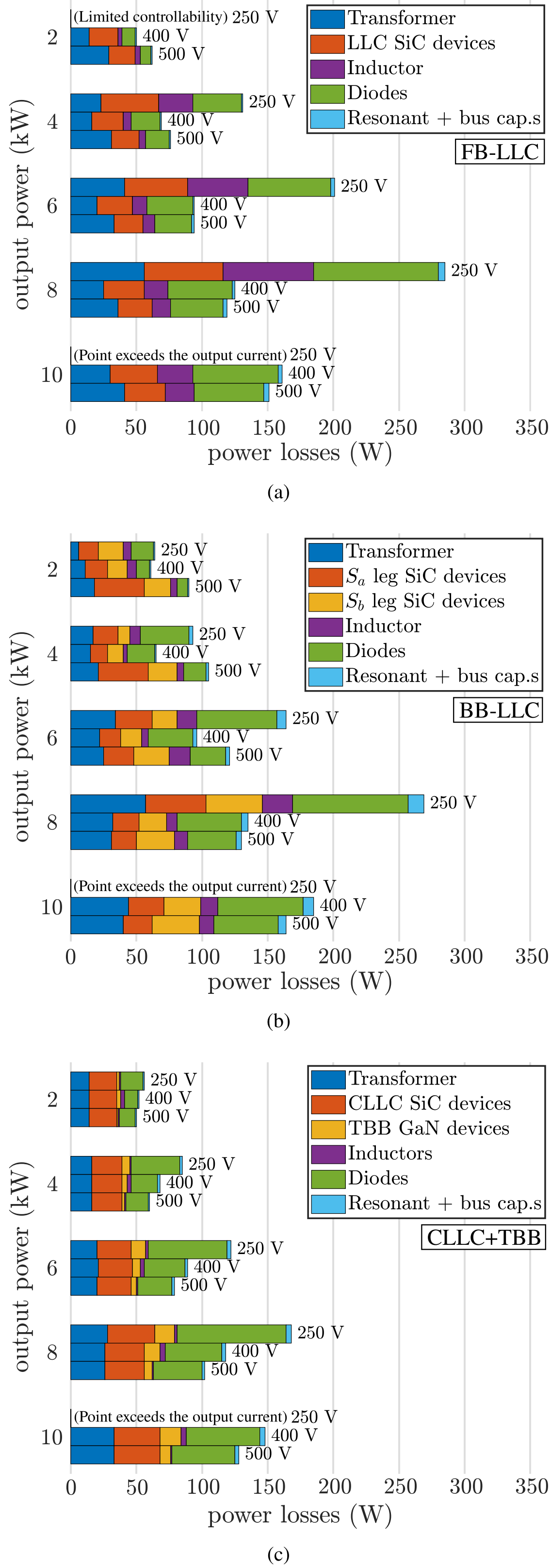

FIGURE 12. Loss breakdown at different output power and minimum, nominal, and maximum output voltages. Topologies in Fig. 10 with efficiency profiles in Fig. 11. (a) FB-LLC, (b) [21], (c) herein.

TABLE 3 **Compared Topologies Considerations**

Topology	Peak efficiency	# Switches / Diodes / Transformers / Inductors	Pros vs Cons
FB-LLC (Fig. 10a)	98.5% (8 kW, 500 V-out)	4 (4x 1.2 kV SiC MOSFET) / 4 (4x 650 V SiC Diode) / 1 (150 µH, PQ65/60-N87) / 2 (2x 16 µH, PQ40/40-N97).	Pros: Low component count; Cons: frequency modulation, limited controllability over the wide range, high magnetic losses.
BB-LLC (Fig. 10b)	98.4% (5 kW, 400 V-out)	4 (4x 1.2 kV SiC MOSFET) / 4 (4x 650 V SiC Diode) / 1 (150 µH, PQ65/60-N87) / 2 (2x 8 µH, PQ40/40-N97).	Pros: very wide voltage gain (potential); Cons: high circulating reactive currents in light-load, higher losses.
CLLC+TBB (Fig. 8)	98.72% (8 kW, 500 V-out)	8 (4x 1.2 kV SiC MOSFET + 4x 600 V GaN FET) / 8 (4x 650 V SiC Diode + 4x 400 V Si Diode) / 1 (200 µH, PQ65/60-N87) / 2 (2x 30 µH, PQ40/40-N97).	Pros: high efficiency in a wide range, simple control; Cons: high component count.

loss breakdown of the considered topologies for the efficiency comparison in Fig. 11, using the same methodology. In general, the major loss contribution comes from the rectification stages; if active rectification is implemented, the performances of all the considered topologies will improve consequently, at the cost of higher circuit complexity. Substantial magnetic losses are present in the frequency-modulated FB-LLC converter that affect the efficiency performances.

In summary, the proposed solution in Fig. 8 offers valuable efficiency improvements, at the cost of a small component increment. The number of semiconductors is doubled and additional bus capacitances are needed for the proposed structure in Fig. 8, as compared to the classical FB-LLC. Nevertheless, excellent efficiency performances for the whole wide range of operation are achieved. The main features of the compared topologies in Figs. 8 and 10 are summarized in Table 3.

V. EXPERIMENTAL RESULTS

Fig. 14 displays the experimental prototype implementation of a module rated 10 kW, with parameters in Table 2, used to validate the reported analysis, design choices, and feasibility of the proposed converter, in Fig. 8. Fig. 15 shows the measurement and control setup built around the proposed converter in order to collect the experimental results reported herein.

Fig. 13 shows the experimental validation of the considerations discussed in Section IV. In particular, Fig. 13(a), (c), and (e) show the measured resonant currents at the same operating points of the simulated waveforms in Fig. 9(d), (e), and (f), respectively. It is possible to appreciate that the current waveforms are very close to the continuous resonant current operation of the DCX-CLLC. The measured waveform amplitudes correspond to the expected values. The switching frequency is set to $f_s = 200$ kHz and dead-time to $t_d = 260$ ns. If needed, additional refinements to match the true resonance frequency may be performed by adjusting the values of the resonant capacitors or the used operating frequency in the controller [16], [68], [69].

Fig. 13(a) and (b) show the converter waveforms at minimum output voltage $V_o = 250$ V and output current $I_o = 25$ A. The duty-cycle of the TBB is set to 7%, and the switching frequency to the lower limit of $f_{s_o} = 50$ kHz. Such a lower limit comes from a trade-off between the dc-link capacitances and the output voltage ripple. The conversion efficiency in such an operating point is about 97.6%. For $V_o = 250$ V ZVS conditions are not satisfied for average output currents higher than about 10 A. Remarkably, the typical charging profile of a battery requires a constant current mode charging when the battery is discharged (i.e., at low battery voltages). In this condition, the charging current is maximum and equals to the output current $I_o^{\max}$ at the nominal output power (see, e.g., [70]), namely, 25 A at 10 kW in the considered case.

Fig. 13(c) and (d) show the converter waveforms at nominal output voltage $V_o = 400$ V and output current $I_o = 25$ A. The duty cycle of TBB is set to 65% and the switching frequency of the TBB is $f_{s_o} = 73$ kHz in order to achieve ZVS. The conversion efficiency in such a point is about 98.4%.

Fig. 13(e) and (f) show the converter waveforms at maximum output voltage $V_o = 500$ V and output current $I_o = 25$ A. The duty cycle of the TBB is set to 95%, the switching frequency to the lower limit of $f_{s_o} = 50$ kHz. The conversion efficiency in such a point is about 98.5%. For $V_o = 500$ V, ZVS conditions are not satisfied for output currents higher than about 10 A. Remarkably, the loss of ZVS in heavy load conditions and extreme duty-cycle is the direct consequence of the selected inductance L_o. Indeed, the selected value allows to achieve ZVS in light-load conditions and with a switching frequency of the TBB limited to $f_{s_o} = 400$ kHz.

Some ringing at the commutations of the input full-bridge current is visible in Fig. 13(a), (c), and (e). The ringing appears during the dead-times and is generated by resonances between the transformer leakage inductances and the devices output capacitances. These resonances may bring partial ZVS and ZCS conditions and eventually cause increased switching losses. This aspect is investigated in [16], which also proposes a method to reduce the related switching loss based on switching frequency and dead-time perturbations.

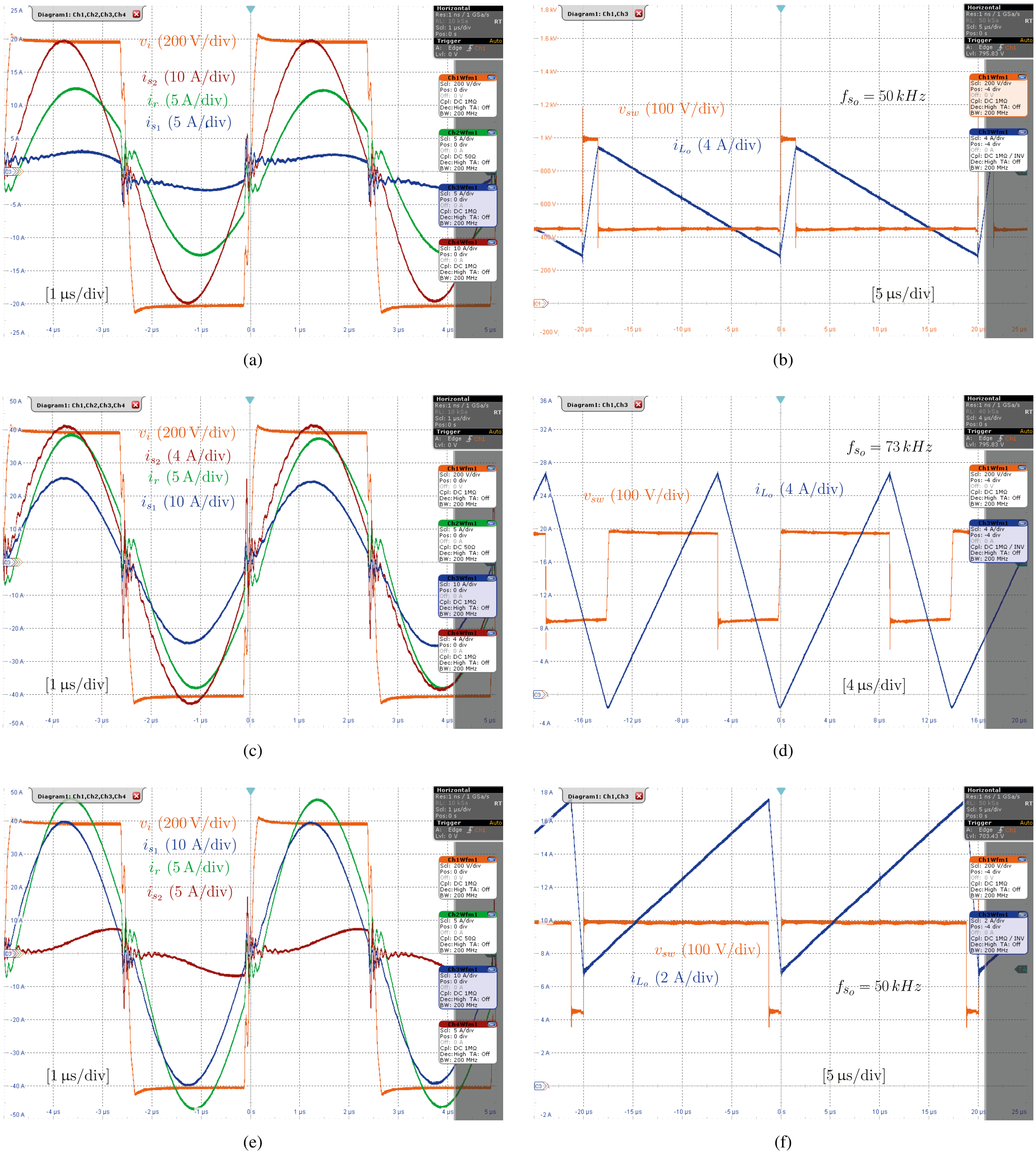

FIGURE 13. Experimental results of the proposed converter in Fig. 8 at $I_o = 25$ A. (a),(b) $V_o = 250$ V; (c),(d) $V_o = 400$ V; (e),(f) $V_o = 500$ V. (a), (c), (e) are the experimental validations of the simulations in Fig. 9(d), (e), and (f), respectively.

Finally, Fig. 16 shows the converter efficiency measured at the minimum, nominal, and maximum output voltage. Efficiency measurements were performed by means of a Keysight PA2203 A power analyzer. The measured peak efficiency at minimum output voltage is 97.8%, while at nominal output voltage is 98.51%, which is very close to the absolute maximum efficiency of 98.63% measured at maximum output voltage conditions. Such values are very close to the estimations performed by the tuned simulation shown in Fig. 11 and previously presented in [50].

VI. CONCLUSION

A two-stage converter, not previously documented for EV battery charging applications, has been proposed, designed, and demonstrated in this paper. The conversion structure is composed of a DCX-CLLC and a post-regulator and features high efficiency, a wide range of output voltage, and a simple principle of operation. The DCX-CLLC converter always operates at its optimal operating point and the additional post-regulator based on a two-input buck converter is used to regulate the output voltage. In such a post-regulator,

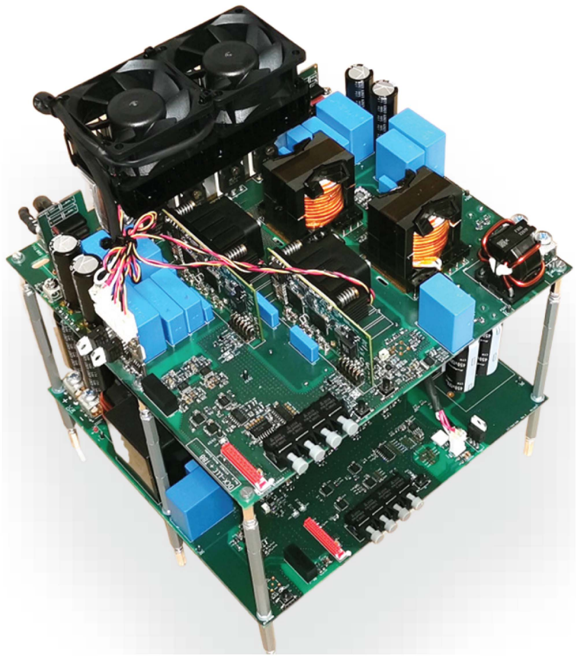

FIGURE 14. DCX-CLLC + twin-bus buck converter prototype.

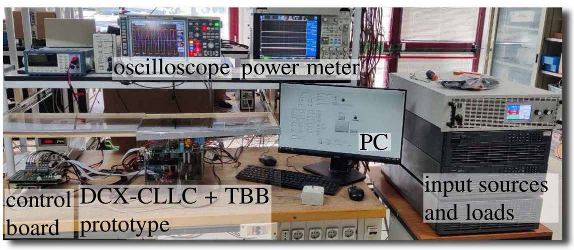

FIGURE 15. Experimental setup for validation.

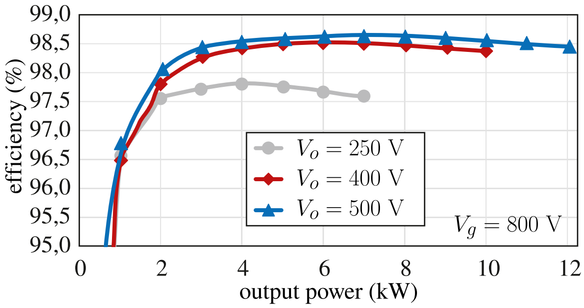

FIGURE 16. Measured efficiency at minimum, nominal and maximum output voltage.

the stress of the switches is a fraction of the rated voltages. Hence, the efficiency of the proposed configuration, compared with standard dc/dc converters processing full power, can be improved. The considered topology is presented, simulation results of a resonant two-output CLLC are reported and an efficiency performance comparison is included. The reported analysis and the experimental characterizations and tests were performed on a 10 kW prototype module based on silicon-carbide (SiC) devices and gallium-nitride (GaN) devices. Conversion performances covering the whole power and voltage ranges have been reported experimentally, showing high efficiency over a wide range of operating conditions, recording a peak efficiency of 98.63% at 500 V output voltage and 7 kW transferred power. In final applications, series or parallel connections of multiple modules can be considered for scaling the voltage or current ratings of the final implementation, thanks to the isolated output. Future studies may include on-line controllers for optimal converter modulation and procedures for the optimal design of the components of the converter, like the output TBB inductors.

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NICOLA ZANATTA (Student Member, IEEE) received the M.S. degree in electronic engineering from the University of Padova, Padua, Italy, in 2020. He is currently working toward the Ph.D. degree in mechatronics and product innovation engineering with the Department of Management and Engineering, University of Padova, Vicenza, Italy. His main research interests include the analysis, design, and optimization of dc-dc converters for ultra-fast charging applications.

TOMMASO CALDOGNETTO (Senior Member, IEEE) received the M.S. (Hons.) degree in electronic engineering and the Ph.D. degree in information engineering from the University of Padova, Padova, Italy, in 2012 and 2016, respectively. He is currently an Assistant Professor with the Department of Management and Engineering, University of Padova, Vicenza, Italy. His research interests include the control of grid-tied converters, microgrid architectures, converters for dc nanogrids, and real-time simulation for power electronics applications.

DAVIDE BIADENE (Member, IEEE) received the M.S. degree in electronic engineering and the Ph.D. degree in information engineering from the University of Padova, Padova, Italy, in 2014 and 2017, respectively. He is currently a Research Fellow with the Department of Management and Engineering, University of Padova, Vicenza, Italy. From 2017 to 2021 he was with Infineon Technologies Italia, employed as an R&D Test Engineer with the Automotive Business Line Team. His research interests include dc-dc converters for renewables and energy storage devices, and artificial intelligence techniques applied to modeling and controlling of power electronic converters.

GIORGIO SPIAZZI (Member, IEEE) received the graduation (*cum laude*) degree in electronic engineering and the Ph.D. degree in industrial electronics and informatics from the University of Padova, Padua, Italy, in 1988 and 1993, respectively. He is currently a Full Professor with the Department of Information Engineering (DEI), University of Padova. His main research interests include dc-dc converters for renewable energy sources, highpower-factor rectifiers, soft-switching techniques, solid-state lamp ballasts, and electromagnetic compatibility in power electronics.

PAOLO MATTAVELLI (Fellow, IEEE) received the M.S. (Hons.) and Ph.D. degrees in electrical engineering from the University of Padova, Padova, Italy, in 1992 and 1995, respectively. From 1995 to 2001, he was a Researcher with the University of Padova. From 2001 to 2005, he was an Associate Professor with the University of Udine, Udine, Italy, where he led the Power Electronics Laboratory. In 2005, he joined the University of Padova, Vicenza, Italy, with the same duties. From 2010 to 2012, he was with the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA. He is currently a Professor with the University of Padova, Vicenza. His current Google Scholar H-index is 82. He has been leading several industrial and government projects in his research fields. His research interests include analysis, modeling, and analog and digital control of power converters, grid-connected converters for renewable energy systems and microgrids, and high-temperature and high-power-density power electronics. Dr. Mattavelli was an Associate Editor for IEEE TRANSACTIONS ON POWER ELECTRONICS, from 2003 to 2012. From 2005 to 2010, he was the Industrial Power Converter Committee Technical Review Chair of IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. For terms 2003–2006, 2006–2009, and 2013–2015, he was a Member-at-Large of the IEEE Power Electronics Society's Administrative Committee. He was the recipient of the Prize Paper Award in IEEE Transactions on Power Electronics in 2005, 2006, 2011, and 2012 and the second Prize Paper Award at the IEEE Industry Application Annual Meeting in 2007. He is the Co-Editor-in-Chief for IEEE TRANSACTIONS ON POWER ELECTRONICS.

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