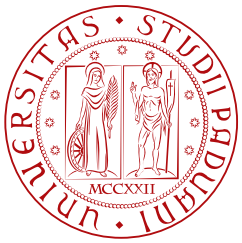


Università degli Studi di Padova
Department of Information Engineering

Ph.D. School of Information Engineering
Curriculum: Information and Communication Technologies
Cycle: 34°

Multi-Level Flying Capacitor Buck Converters With Digital-Predictive Current-Mode Control

Supervisor:
Luca Corradini

Ph.D. Candidate:
Giovanni Bonanno

Academic Year 2020-2021

to Anita and Clara

Abstract

This thesis investigates the use of digital predictive current-mode control (DPCMC) in dc-dc multi-level flying-capacitor (MLFC) Buck converters. In particular, stability and flying-capacitors (FCs) voltages balancing properties of predictive *peak*, *average* and *valley* current-mode controllers are studied when operated in single-sampled and multi-sampled mode. Although the DPCMC technique has been extensively studied for traditional dc-dc converters, its application to MLFC converters is not documented in the current literature. This thesis proposes a unified analysis methodology that can be used for predicting FCs voltages stability properties in such converters. The developed analysis can be used for the generic MLFC Buck converter with a generic number of levels and all operating modes.

In addition to stability analysis tools, this thesis provides a new implementation methodology for DPCMC control that takes full advantage of the multi-level topology. In fact, when MLFC converters operate with stable and balanced FC voltages, the output LC filter is excited by signals whose frequency is integer multiple of the switching frequency. Precisely, by indicating with N-LFC Buck the MLFC step-down converter which has N voltage levels available at the switching node, it is possible to show that during the steady-state operation the output LC filter is excited by a signal with a frequency equal to N-1 times the switching rate. This equivalent frequency multiplication effect allows the N-LFC Buck converter to gain advantages deriving from the increasing of the switching frequency without actually increasing it. In addition to the advantages in terms of inductance and out-

put capacitance reduction, it is possible to exploit this property to increase dynamic performances. The proposed control indicated as *multi-sampled* DPCMC (MS-DPCMC) exploits exactly this opportunity and allows to obtain a faster inner-current loop, thus increasing the available bandwidth for the outer-voltage loop. Additionally, a variant of the MS-DPCMC obtained through a *fast-update* of the duty cycle command is disclosed and analysed. When the available hardware makes it possible, the *fast-update* implementation increase the speed of the corrective action on the inductor current error, further increasing the available bandwidth for the outer-voltage control loop.

For the 3-LFC Buck converter, simulating and experimental results indicate that single-sampled *peak*, *valley* and *average* DPCMC are always stable and that fast-update approaches can strongly improve the converter dynamic response. Multi-sampled controllers are also shown to be inherently more robust than single-sampled ones against timing mismatches in the control signals, resulting in a smaller flying-capacitor voltage imbalance. All developed stability results regarding the 3-LFC Buck converter are validated in simulation and experimentally on a custom prototype.

Contents

Chapter 1

Introduction

The current historical period is marked by major events on a global scale. There is a need to achieve greater awareness and control of the environmental impact of the current system of production and consumption of goods and services. Many aspects of daily lives are linked to the use of technologies and/or resources that together produce non-negligible effects on the environment. Some of these effects are not well understood and the contours of potential consequences are not always clearly delineated. The most common aspects of which awareness and social sensitivity are slowly increasing are those related to CO_2 emissions and global warming. Nevertheless, the set of environmental problems is much broader and more complex. Other lesser-known issues of environmental concerns include: large presence of plastics in seas and oceans, air pollution by particulate matter of various kinds in the atmosphere, the disappearance of several animal and plant species, the increase in energy demand, the growing world population and the consequent consumption of food and water resources, the reduction of water supplies and/or the worsening of the quality of drinking water, the dramatic reduction in the number of bees, etc.. In short, the set of environmental problems is rather broad and these are linked together in a tricky way. What is of interest here is the role that power electronics has played and plays with respect to the issues mentioned above.

Power electronics plays a leading role in the production, storage, and routing of energy from renewable sources (e.g., solar, wind, water) but also in the construction of efficient power systems for electric vehicles (EVs), or in the realization of fast and low-loss battery chargers. These examples are directly related to the need to reduce CO_2 emissions or more generally to environmental issues. Power electronics is nowadays a mature scientific field, interconnected with several aspects of our daily lives and to whom more and more responsibility and competence in the field of high efficiency and low emissions is delegated. This thesis focuses on the application of *digital predictive current-mode controls* to *multi-level flying-capacitor converters*. This topology currently represents a solution capable of bridging the gap between the needs of increasingly scaled converters and converters with similar performance to traditional discrete component-based converters. Moreover, the digital-predictive control allows to further increase the dynamic performance bringing to the final solution suitable for the new modern power electronic applications.

This opening chapter provides the basic motivation that clarifies the importance of the chosen topic highlighting what the current technological context is and what the new demands are. The first part of this introduction begins with a snapshot of the political and socioeconomic situation related to climate change and the role played by power electronics. This provides one of the basic motivations that has been driving technological development in recent years and is leading to the emergence of this family of topologies in the automotive field but also in the mobile telecommunications industry. The central part of this chapter provides an overview of the most common solutions for the integration of dc-dc converters. A description of the thesis structure closes this introduction.

1.1 Climate change and the European situation

The latest European report about air quality can be found in [1]. This document is written by the *European Environment Agency* (EEA) and its European Topic Centre on Air Pollution, Noise, Transport and Industrial Pollution (ETC/ATNI), and presents data collected through June 2020. A summary look at the current situation is depicted in Fig. 1.1. The figure presents the percentage of the EU-28[1] urban population exposed to concentrations above certain European Union (EU) limit or target values and World Health Organization (WHO) air quality guidelines (AQGs) levels in 2018. Some significant facts can be extracted from this data. In 2018, 15% of the EU-28 urban population was exposed to PM10 (particulate matter with a diameter of 10 µm or less) above the EU daily limit value, decreasing again after the increase in 2017. The extent of exposure above this EU daily limit value fluctuated between 13% and 42% during the period 2000-2018, with 2003 identified as the year with the highest extent of exposure. Furthermore, 48% of the same urban population was exposed to concentrations exceeding the stricter WHO AQG value for PM10 in 2018. The percentage of the urban population exposed to levels above the WHO annual AQG (20 µg/1 m) ranged between 43% and 91% (maximum also reached in 2003) during the period 2000-2018. About 4% of the EU-28 urban population was exposed to PM2.5 (particulate matter with a diameter of 2.5 µm or less) above the EU limit value in 2018. The urban population's exposure to levels above the more stringent WHO AQG for PM2.5 was 74% in 2018, also reaching a new minimum from the initial maximum of 97% in 2006. The presence of these impurities in the atmosphere, added to CO_2 emissions, is producing several negative effects on health as well as a marked global warming effect. Immediate and decisive action on climate change is essential.

[1]The EU-28 is an abbreviation for the group of European states which consists of a group of 28 countries that *operates as an economic and political block*.

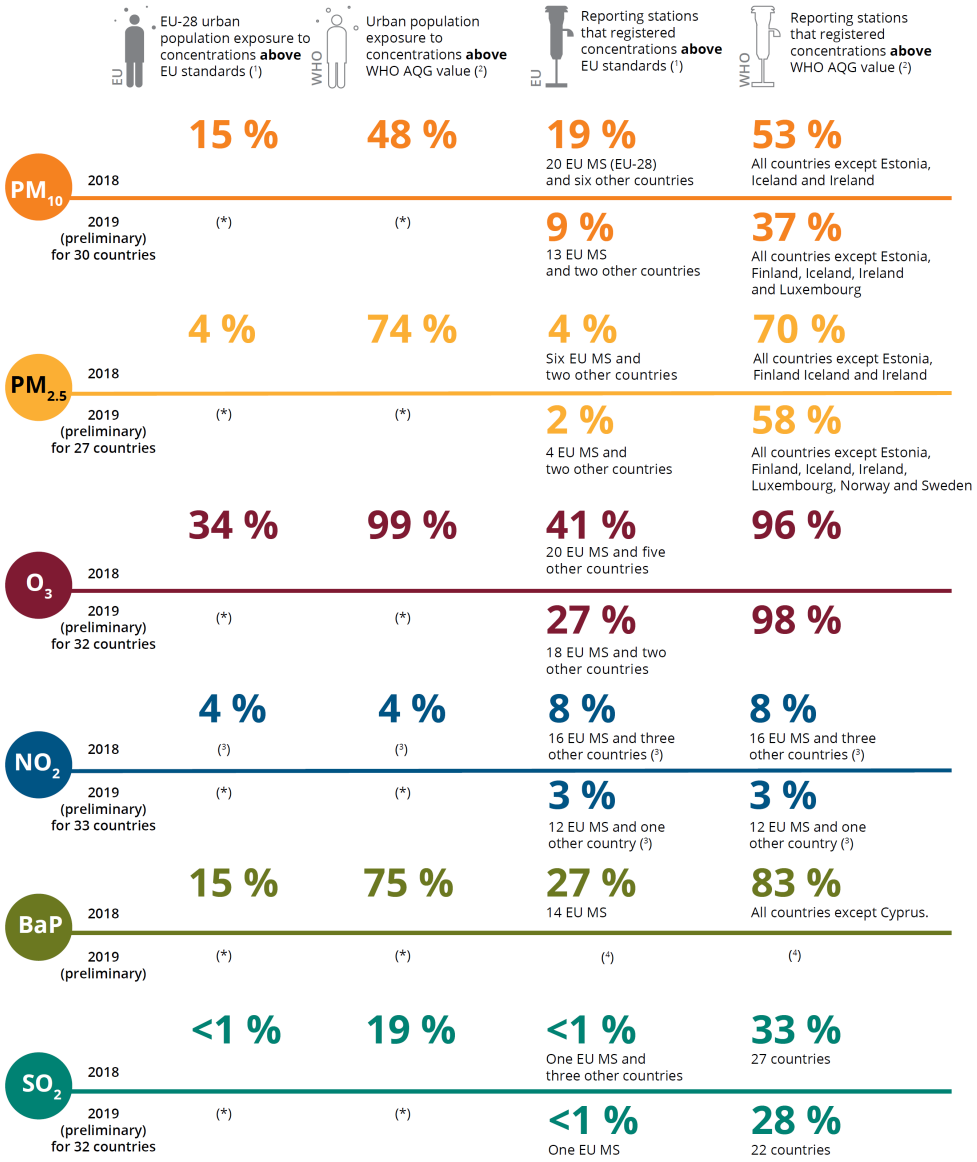


Figure 1.1: *Percentage of the EU-28 urban population exposed to concentrations above certain EU limit or target values and WHO AQG levels in 2018. (1) PM10 daily limit value, PM2.5 annual limit value, O_3 target value, NO_2 annual limit value, BaP target value and SO_2 daily limit value. (2) For BaP, reference level. (3) For NO_2, both the EU annual limit value and the WHO AQG are set at the same. (4) BaP is not included in the UTD data exchange.*
(*) Estimates of urban population exposure are not available for 2019.

Climate changes are redesigning the world and amplifying risks of environmental instability. The last two decades have been 18 of the hottest years in human history. Our environment is negatively changing and the average temperature is undoubtedly rising. During summer 2019, temperatures above the Arctic Circle were +5 °C higher than the average of the last 100 years. Last summer (August 2021) the U.S. National Science Foundation research station near the highest point of the Greenland ice sheet spotted rain for the *first* time since tracking began in 1950. The amount of ice lost is seven times the daily average for that time of year. Another direct result of climate change is the increasing frequency and intensity of extreme weather events. New areas in Europe are suffering from severe droughts. At the same time, flood events are increasingly dangerous and frequent, see the recent floods in Germany and Belgium in mid-July this summer (i.e., summer 2021). Other extreme events related to climate change, such as forest fires, flash floods, typhoons, and hurricanes, are also causing massive devastation and loss of life, as demonstrated by Hurricanes Irma and Maria, in 2017, or Hurricanes Ophelia and Leslie, respectively on September 2017 and 2018.

The *Intergovernmental Panel on Climate Change* (IPCC) published its Special Report on the Impacts of Global Warming in 2019 [2] according to what was formally approved by the world's governments in 2018. During its three decades of existence, the IPCC has shed light on climate change, contributing to the understanding of its causes and consequences and options for managing risk through adaptation and mitigation. On December 12, 2015, the IPCC's Fifth Assessment Report provided the scientific input for the Paris Agreement, which aims to strengthen the global response to the threat of climate change by keeping the global average temperature increase well below 2 °C above pre-industrial levels and to continue efforts to limit the temperature increase to 1.5 °C above pre-industrial levels. The strategies proposed by IPCC regards political, social and economic areas. These profoundly influence the investment and production of innovative technologies and also scientific research. For this reason, it has been necessary to develop

models capable to capture the trend of acquired data as well as to predict future behaviour and how this response can be enhanced by economically and socially sustainable policies.

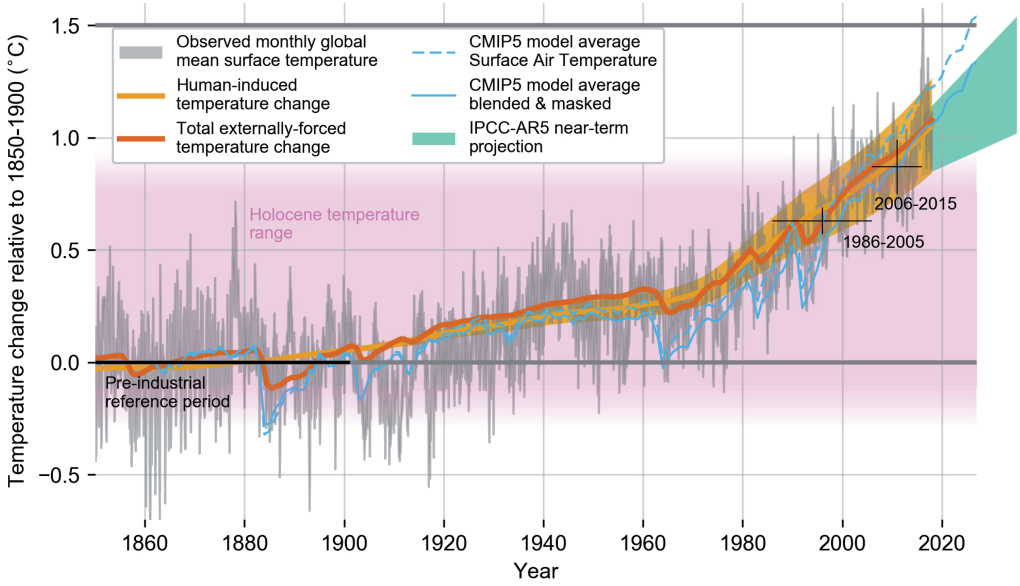
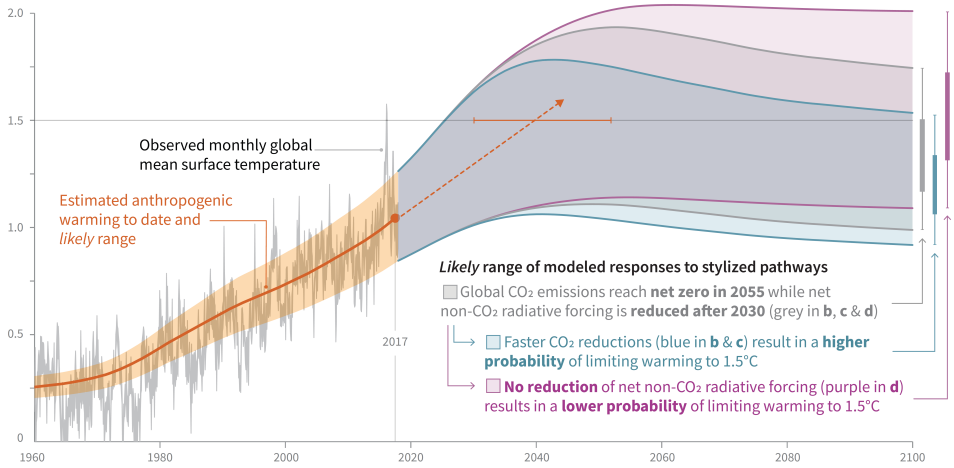


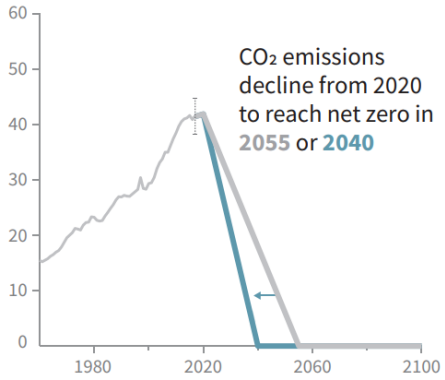
Figure 1.2: *Evolution of global mean surface temperature (GMST) over the period of instrumental observations. Grey shaded line shows monthly mean GMST in the HadCRUT4, NOAAGlobalTemp, GISTEMP and Cowtan-Way datasets, expressed as departures from 1850–1900. Human induced (yellow) and total human-naturally-forced (orange) contributions to these GMST, from Otto et al. (2015) and Haustein et al. (2017). Thin blue lines show the modelled global mean surface air temperature (dashed) and surface air and sea surface temperature accounting for observational coverage (solid) from the CMIP5 historical ensemble average extended with RCP8.5 forcing (Cowtan et al., 2015; Richardson et al., 2018).*

The model used for forecasting encompasses a rather large amount of data. The available measurements, although with varying levels of detail, date back to 1850. Fig. 1.2 shows all the data that it has been possible to use in the study of the IPCC forecasting model. Based on this model, political and socioeconomic strategies that should induce the desired changes and keep the temperature increase limited to +1.5 °C have been proposed. The collection of data presented in Fig. 1.2 and the associated model developed

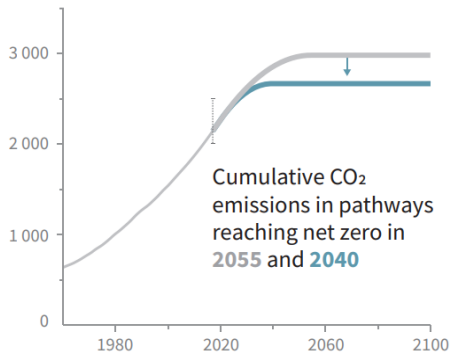
allowed to obtain predictions for what will be the future trends in Earth's temperature increase with or without the implementation of control, mitigation, and trend reversal strategies. Fig. 1.3a shows forecasts and achievable results according to 2015 Paris Agreement strategies. Fig. 1.3b and Fig. 1.3c show trends and forecasts decline and emission of CO_2. Both figures show two different curves obtained according to different implementation of intervention strategies.



(a)



(b)



(c)

Figure 1.3: *(a) Observed monthly global average surface temperature change and estimated anthropogenic global warming. The central estimate (orange line) and likely range (orange area) of the time at which 1.5 ℃ is reached if the current rate of warming continues. (b) Data and forecasts of CO_2 emission decline to reach net zero by 2055. (c) Data and forecasts of the cumulative CO_2 emissions.*

An increasingly widespread use of electronics

From a technological perspective, environmental change and related policies are leading to new industrial scenarios. One of these involves the development of Plug-in hybrid electric vehicles (PHEVs) and full electric vehicles (HEV). Fig. 1.4 shows the trend of global electric car stock by country from 2013-2017 [2]. The graph shows a doubling of the overall stock every two years. Growth forecasts for subsequent years appear to be even more pronounced.

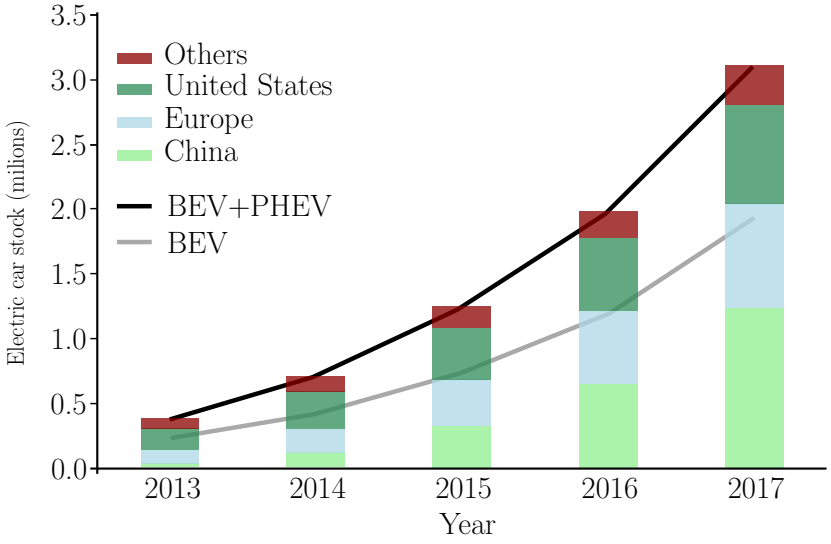


Figure 1.4: *Increase of the global electric car stock by country (2013– 2017). The grey line is battery electric vehicles (BEV) only while the black line includes both BEV and plug-in hybrid vehicles (PHEV). Source: (IEA, 2018). Based on IEA data from Global EV Outlook 2018 © OECD/IEA 2018, IEA Publishing.*

The structures of EVHs or PHEVs are permeated by electronic systems such as microcontrollers, microprocessors and sensors. These systems must be properly powered and often economic demands and reliability standards lead to the need to reduce the size of these power supply systems while trying to maintain high-performance and efficiency. But these demands are not limited only to the automotive sector.

There are several fields of technological research that are inherent to the

transformation that the automotive world is experiencing in recent years also because of the policies mentioned above. Even in the telecommunications sector, the energy issue is beginning to take a key role. The efficiency per bit, as well as the absolute power consumption of each radio station and/or radio-mobile devices are increasingly being studied and are among the branches of interest of power electronics. In general, also for other technology areas related to power electronics, the demand for smaller, cheaper, higher-performance and more efficient power supply systems is polarizing the efforts of manufacturers and research. This new generation of power supply systems must therefore be cost-effective both in terms of area/volume occupied and in absolute economic terms. They must be able to offer excellent static and dynamic performance and must also be as efficient as possible to increase the reliability of the equipment itself. This thesis analyses the application of a digital-predictive control to one of the promising topology for the new generation of scaled power supply systems: the multi-level flying-capacitor Buck converter.

The next section contains a series of numbers about the power electronics market and presents the growing need for new dc-dc conversion solutions that can be scaled or directly integrated, without compromising performance, efficiency and reliability.

1.2 The demand for smaller and more efficient converters

Multiple economic, political and social impulses have led to the need for cheaper, more reliable and smaller switched converters. Power electronics is a large market and continues to be a great economic opportunity given continued global growth. Fig. 1.5 shows the current market value and projected growth evaluated in United States dollar (USD). Fig. 1.6 shows how the power electronics market is spread out and which are the current leading sectors and their projections. These numbers suggest important facts:

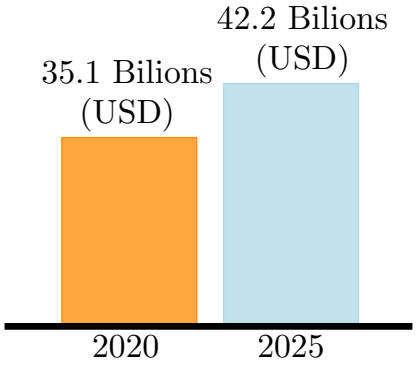


Figure 1.5: *Valued power electronics market value at the end of 2020 and estimated growth. Military and civilian segments are excluded from these figures.*
Source: Markets And Markets.

power electronics is an economically growing field from the manufacturer and industry point of view, the automotive field is experiencing an important technological revolution. Other numbers and forecasts with respect to monetary value, growth, and market breakdown are given in [3–5].

The central topic of this thesis is mainly addressed to applications in the automotive field. This area has already faced an initial technological revolution with regard to onboard electronics. In fact, as regards the dc-dc conversion, linear converters have slowly given way to switching converters. These power supplies are more efficient, more reliable and generally more flexible than linear converters. Nowadays, linear regulators in automotive applications are usually used for small voltage step-down regulations. In practice, linear converters are currently used almost exclusively as LDOs. To have direct feedback on the rarity of using linear regulators in applications where they cannot be considered LDOs, refer to the internal organization of modern automotive power supply distribution systems [6] and/or power supply systems for automotive microcontrollers [7, 8].

The ongoing technological revolution involves now the miniaturization of these switched converters. For the new generation of electronic systems for automotive and telecommunication applications, it is in fact necessary

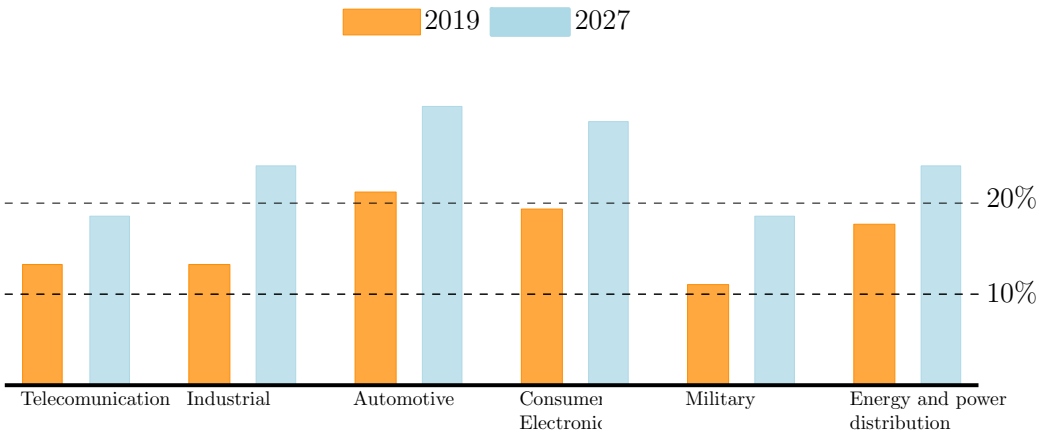


Figure 1.6: *Current market share of various power electronics sectors and their growth forecasts.*
Source: Allied Market Research.

to reduce the overall size of the converters so that they can be integrated on the same silicon die or within the same package of the systems to be powered. This integration would bring numerous benefits not only from an economic perspective. The next two sections detail the two main alternatives for integrating dc-dc converters within more complex electronic systems that require power.

1.2.1 Main approach to dc-dc converter integration

Some of the most common solutions used in the realization of integrated or partially integrated dc-dc converters are the following: switched-capacitor converters, dc-dc converters with integrated magnetic elements, dc-dc converters with reduced magnetic elements and cascaded low-dropout voltage (LDO), dc-dc converters with inductors integrated into the chip package [9–14]. The first two converter families fully embrace integrated circuit design and enable true integrated dc-dc converters. The last two categories in the previous list are actually the result of some compromises. In particular, when an LDO is used in cascade with a dc-dc converter, it is done in order to lighten the specifications of the switching converter so that more

compromises can be made with respect to the typically integrated magnetic element.

The proposed structure in Fig. 1.7 represents a common solution for implementing dc-dc voltage converters [13,14]. The presence of the LDO allows lightening the specifications on the magnetic element and on the output capacitance of the Buck converter by significantly reducing the footprint of the switched converter. However, with this architecture, it is generally not possible to integrate the entire converter and the magnetic element must remain outside the die or package. In order to achieve the full converter integration, LDOs are used cascaded to switched capacitor converters. In both cases, the final converter is the result of the superposition of a dc-dc converter and a linear regulator, with the problems of efficiency and heat dissipation that are well known.

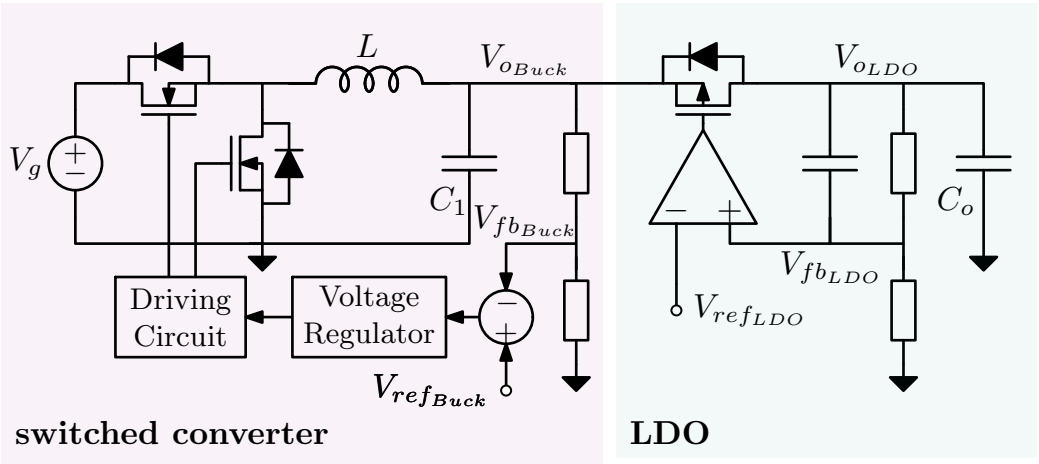


Figure 1.7: *Example of implementation of dc-dc voltage converter with switched converter and LDO.*

1.2.2 Integration of magnetic element for power converter applications

Various studies have been and are still being conducted in the field of magnetic element integration for power electronics applications. A few ex-

amples can be found in [15–20]. Common difficulties are those related to the small obtainable inductance value, on the inductance over equivalent series resistance ratio (L/R), on the total area occupancy and overall cost of the fabrication process. Despite many efforts, the values of integrated inductances are typically on the order of a few tens of nH. Higher values may be achievable at the expense of other parasitic parameters (e.g. increased equivalent-series resistance and/or non-negligible capacitive effects). These full integration solutions are not currently of interest to the application domain to which this thesis refers.

1.2.3 The embedded solution

Currently, the embedded integration strategies, also referred to as on-pack solutions, seem to be the best alternatives to the discrete component realization, at least from a performance point of view. The main reason lies in the quality of inductors that can be implemented with the different strategies developed in recent years [21–26].

From the switched converter point of view, the resulting structures are often called hybrid because they consist of an integrated part often similar to that of the switched-capacitor circuits realized also through the use of an external inductor, incorporated in the same package containing the integrated circuit. Hybrid switched converters also include structures obtained with switched-capacitor circuits and inductors. These solutions allow improving performances and flexibility. A rather simple example is the *voltage tripler* presented in [27]. This topology is used as fixed voltage conversion ratio dc-dc converter (i.e., step-up voltage conversion ratio equal to 3, or step-down voltage conversion ratio equal to 1/3 used in the opposite direction). Adding an inductor between the low-voltage load and the switching node, this dc-dc converter can operate similarly at the traditional Boost converter or as the traditional Buck converter in the opposite direction. With the addition of the inductor, the converter gains some advantages. For example, it can adjust the power flow in the two directions, improve the harmonic content

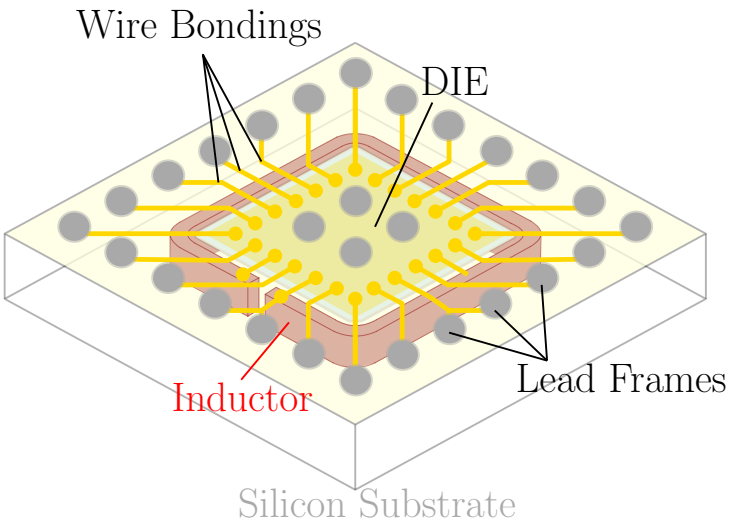


Figure 1.8: *Schematic 3-D view of the fan-out-package-embedded inductor [21].*

of the output voltage and allow for lighter bus capacitors specifications. The obtained topology belongs to a wider family called multi-level flying-capacitor (MLFC) converter. Due to its unique characteristics, this topology is suitable for working with embedded inductor solutions.

An embedded inductor solution is exemplified in Fig. 1.8. With this solution, it is possible to obtain inductances of some nH, but with higher L/R ratios than planar *on-die* integration solutions. In [21] this strategy is used to build a $L = 2.4\,\text{nH}$ / $R_{\text{ESR}} = 5\,\text{m}\Omega$ inductor, with quality factor $Q = 43 - 67$ in the range $100 - 500\text{MHz}$. Although with a rather low inductance value, this type of inductor is already suitable for power electronics applications, mainly due to the low R_{ESR} value.

By operating on a slightly different scale and increasing the number of turns, higher inductance values can be obtained. In [22] is proposed a new power inductor integration technology using a silicon interposer. These inductors are suitable for DC-DC power converter applications. In this case, coreless spiral inductors can be embedded from the back of a silicon interposer and connected with the front-side metal routing through-silicon vias. The experimental results obtained in [22] show higher achievable inductance val-

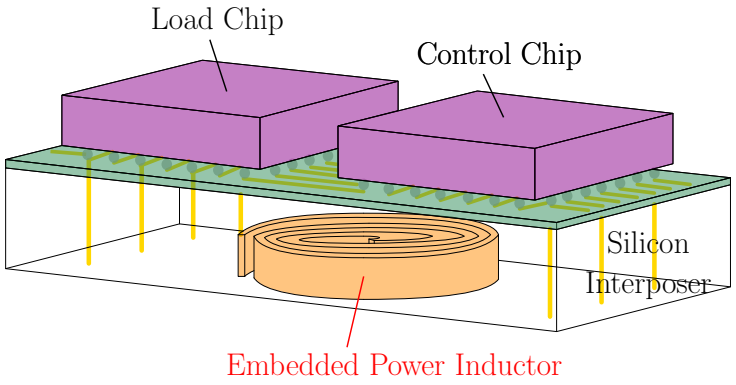


Figure 1.9: *Example of integration of an embedded power inductor with other chips using a silicon interposer [22].*

ues with respect to the *fan-out-package-embedded* techniques shown in [21]. Precisely, the measured inductance and ESR are respectively $L \approx 4.2\,\mu\text{H}$ and $R_{\text{ESR}} \approx 1.86\,\Omega$. By further increasing the working volume and working on the integration of small inductors resting on an insulating layer directly on the die slightly higher inductance values and/or lower ESR can be realized, as shown in [23].

1.2.4 Multi-level flying-capacitor converters: a promising compromise.

The techniques to embed small inductors mentioned in the previous section allow to obtain inductors with characteristics in line with those required by power electronic applications (e.g., low ESR, reduced capacitive effects). However, the achievable inductance values are still quite small compared to those of discrete components. In order to operate effectively with such small inductors, it is necessary to use topologies capable of maintaining high performance even with small inductance values. One promising solution comes from *multi-level flying-capacitor converters*. Fig. 1.10 shows the traditional Buck converter and the three-level flying-capacitor (3-LFC) Buck converter side by side. The 3-LFC Buck sketched in Fig. 1.10b is the simplest MLFC Buck converter. The flying-capacitor C_f is used in order to provide an in-

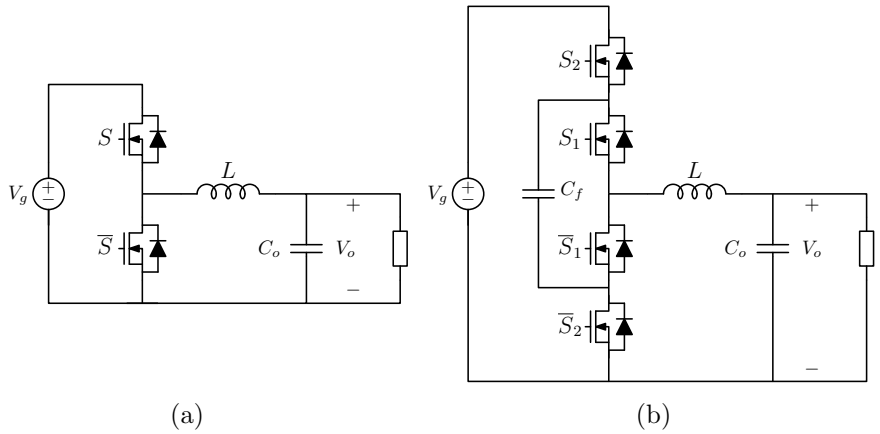


Figure 1.10: *Traditional Buck converter (a) and three-level flying-capacitor Buck converter.*

termediate voltage. When the converter operates stably and with balanced flying-capacitor voltage, this topology provides several advantages.

The following example clarifies the achievable advantages given by this solution. The traditional synchronous Buck converter, sketched in Fig. 1.10a, is taken as a reference example since it represents the most common solution for the application target. In a 500 kHz, 12 V-to-1.5 V dc-dc conversion application with 500 mA output current, a design of the traditional Buck converter, with the following given specification of the inductor current ripple over average output current ratio $\Delta I_L/I_o = 10\%$, results in an inductance value of $L_{\text{Buck}} = 52.5\,\mu\text{H}$. As detailed in Chapter 3, multi-level converters allow the overall inductance value to be significantly reduced. For instance, assuming to operate in the same application, with the same given specifications, using a 3-levels flying-capacitor Buck converter instead of the traditional one, the inductance value can be reduced down to $L_{\text{3-L}} = 22.5\,\mu\text{H}$ while using the 4-levels flying-capacitor Buck converter one has $L_{\text{4-L}} = 12.5\,\mu\text{H}$. Even with significantly lower inductance values, the multi-level flying-capacitor Buck converters are able to maintain the given specification for the inductor current ripple over the average output current ratio $\Delta I_L/I_o$. In addition, multi-level converters also allow for significantly reduced output capacitance and

other benefits in terms of harmonic contents and dynamic performances. For these reasons, multi-level converters are currently of considerable importance in the development of scaled dc-dc converters.

Modern power supply systems require not only scaled solutions but also high dynamic performances. In order to achieve such dynamic performances, it is necessary to use suitable control systems. In this thesis, the application of digital-predictive current-mode controls (DPCMC) to multi-level converters is discussed. These digital-controls are known for their high-speed in correcting errors on the current. The corrective action is in fact a dead-beat type. By combining the advantages offered by this controller with the unique properties of multi-level flying-capacitor converters is possible to obtain even higher dynamic performances. Unfortunately, the application of any control strategy, even the best known, to MLFC converters needs to be carefully studied. Indeed, such topology suffers from the problem of balancing and/or stability of FCs voltages. During the last years, numerous FC voltage stability analyses have been proposed, but the application of digital-predictive current-mode controls is not documented in the current literature. For this reason, this thesis addresses these issues by providing a unified analysis strategy and proposing a series of simulation and experimental tests to verify the obtained results.

1.3 Thesis Outline

This thesis discusses the application of digital predictive current-mode controls (DPCMC) to multi-level flying-capacitor (MLFC) Buck converters. Throughout the thesis, these converters are often referred to as N-level flying-capacitor (N-LFC) Buck converters, where the emphasis is on the number N of possible levels that the switching node can reach during stable operation. In detail, the rest of the thesis is organized according to the following outline.

- **Chapter 2: Digital Control of Switching Converters**
  This chapter takes a sweeping look at digital controls and the differ-

ent types of applications that have emerged over the years in power electronics. After a brief and general introduction to digital controls in power electronics, attention is shifted to a particular family of digital controllers: digital predictive controls. At this point, the origin and evolution of this family of controls is discussed, clarifying where the current literature on the subject has gone to date. Stability issues and how they are significantly dependent on the digital pulse-width modulator implementation are discussed in relation to the synchronous Buck converter. The chapter closes with a table summarizing the stability properties of this controller regarding the considered application.

- **Chapter 3: Multi-Level Flying-Capacitor Buck Converters**
  This chapter introduces multi-level converters. The topology is introduced through an example involving one of the first important applications of this family of converters: the 7-level flying-capacitor full-bridge voltage-source inverter. Next, multi-level step-down converters are introduced, namely: N-LFC Buck converters. Normal steady-state operation is described using the 4-LFC Buck converter. Next, the main issue arising from the use of this converter family is discussed, namely the problem of balancing and stability of the flying-capacitors voltages. The chapter closes with a review of the advantages of applying these converters over the more common solution based on the synchronous Buck converters. This chapter concludes the first part of this thesis.

- **Chapter 4: Peak DPCMC For 3-LFC Buck Converters**
  This chapter opens the second part of the thesis, in which the fundamental results of the PhD project are presented and discussed. The chapter discusses the application of DPCMC to 3-LFC Buck converters. The application of this type of control to this converter brings up new issues but also new possibilities for increasing dynamic performances. In fact, by combining the advantages offered by predictive digital controls with the operation of multi-level converters two new control techniques

are disclosed in this chapter. The chapter also presents analysis techniques for FC voltage stability. Two approaches were developed during this doctoral project. The first and simplest stability analysis approach is based on small-ripple approximations. Thanks to this hypothesis the inductor current can be approximated by a piecewise linear waveform that greatly simplifies the overall analysis. The second approach, more complex and more accurate, adds the effect of the output voltage ripple on the inductor current waveform allowing for a more accurate and precise analysis. The chapter continues with a series of simulation and experimental tests made to validate what is obtained with the proposed FC voltage stability approach. The dependence and the sensitivity of system performances with respect to the converter parameters and with respect to mismatches in the control signals are analysed, tested and discussed. The chapter is closed with two tables that summarize some stability properties regarding both the implementation of the digital pulse-width modulator and the flying-capacitor voltage.

- **Chapter 5: Average and Valley DPCMC For 3-LFC Buck Converters**

  This chapter follows the approach of the previous one. What has been developed about *peak* DPCMC is extended to *average* and *valley* current controls. Again, both simulation and experimental tests are presented to validate the developed theory. The chapter is closed by reporting the stability properties of all three digital predictive control techniques for both operating modes with respect to FC voltage stability.

- **Chapter 6: General Approach For The Stability Analysis Of N-LFC Buck Converters with DPCMC**

  In this chapter, the analysis techniques developed in the previous two are extended to the general case of N-LFC Buck converter with any N. The general analysis strategy for these converters operating with digital

predictive controls is therefore formalized. At the end of this chapter, some results about the stability of FC voltages and some simulations to validate these predictions are presented.

- **Conclusion**
  A summary of the most significant results and some comments close this thesis.

Chapter 2

Digital control of switching converters

Power electronics nowadays is a mature discipline that embeds technology and engineering of discrete component-based switch mode power supplies, notions of automatic controls, device physics, network analysis or more generally graph analysis and several branches of mathematical methods for engineering. Some of the research aspects of greatest interest in this area include topological studies, control/modulation models and design, efficiency optimization techniques, applications for stable and reliable interconnections of different devices/energy sources, research for more robust and reliable solutions, electromagnetic interference issues, development of new power devices, etc. The ultimate goal is very often the same: to provide results, products, ideas that can lead to new and/or more efficient applications in any field where electrical energy is required.

In this regard, digital controls for switching converters have always been considered for their intrinsic versatility, but also for their natural robustness to environmental variations as well as the higher tolerance to signal noise. These advantages are even more pronounced when we compare them to their analog counterparts. Moreover, digital controls also allow the implementation of control techniques that are difficult or impossible to synthesize

analogically.

In recent years, interest in this approach has increased due to the development of smaller, more powerful, and accessible embeddable devices at a significantly lower cost. Thanks to this, the development of technologies and design tools allowing the integration of control circuits and power devices on the same semiconductor chip has been possible. From this standpoint, the application of digital control techniques to switching converters can play a very significant role. Indeed, the integration of complex control functions, such as those that are likely to be required by the next-generation power supplies, is a problem that can realistically be tackled only with the powerful tools of digital control design [28, 29].

The research to which this thesis relates focuses on the study of predictive digital control techniques for multilevel step-down converters. To this end, digital control will be briefly introduced and discussed in some cases of theoretical and practical relevance. After an introduction on general issues related to digital control, the focus of this chapter is shifted to a particular family of digital controls that are the predictive digital controls, often referred to as digital dead-beat controls.

2.1 General description

Describe with a unified approach the numerous applications of digital control for switched converters is very difficult and this is certainly beyond the scope of this thesis. For this reason, in this section, the general concepts of digital controls are introduced near remarkable examples. The control of the single-phase voltage source inverter is certainly one of the first applications of digital control. Other relevant examples could certainly be found in adjustable speed drives (ASDs) and uninterruptible power supplies (UPSs) that are nowadays fully controlled with digital controllers [28].

2.1.1 Digital current-mode of single-phase voltage source inverter

Fig. 2.1 shows the half-bridge voltage source inverter and a typical microcontroller based current control. Fig. 2.1 highlights the current sensing section represented by the H_i block, the analog-to-digital converter (ADC) formed by an ideal sampler and an ideal quantizer, the control-algorithm block and a digital pulse-width modulator. In this example, the structure has the dual purpose of providing appropriate control signals for the correct operation of the inverter while controlling the average current on the load. Precisely, the structure allows to impose the average load voltage and at the same time to control the average current flowing through it. The expression *average value* refers to the average over a time interval equal to the switching period T_s. Therefore, given a generic signal $u(t)$, its average value on a moving window of duration T_s is defined as follows

$$\langle u \rangle_{T_s} = \frac{1}{T_s} \int_{t_o - \frac{T_S}{2}}^{t_o + \frac{T_S}{2}} u(\tau) d\tau. \tag{2.1}$$

The principle of operation of the half-bridge in 2.1 is the following. Closing the high-side switch S_1 (i.e, $S_1 = 1$ and $S_2 = 0$) imposes the voltage $V_x = V_{DC}$ across the load. On the contrary, closing the low-side switch S_2 (i.e, $S_2 = 1$ and $S_1 = 0$), the load voltage is $V_x = -V_{DC}$. If the digital control exemplified in Fig. 2.1 is able to properly regulate the average voltage across the load, it is clearly possible to make the state variable i_{L_s} follow the desired trajectory. For detailed analysis on the operation of the single-phase voltage source inverter, please refer to [30, 31]. In the example here considered, the control signals for S_1 and S_2 are thus chosen by a specific digital algorithm in order to regulate the current through the load branch and at the same time ensure the correct operation of the VSI. It must be considered that in addition to the duration of the on and off state for the switches S_1 and S_2, the control must also impose the dead-time between those. This last addi-

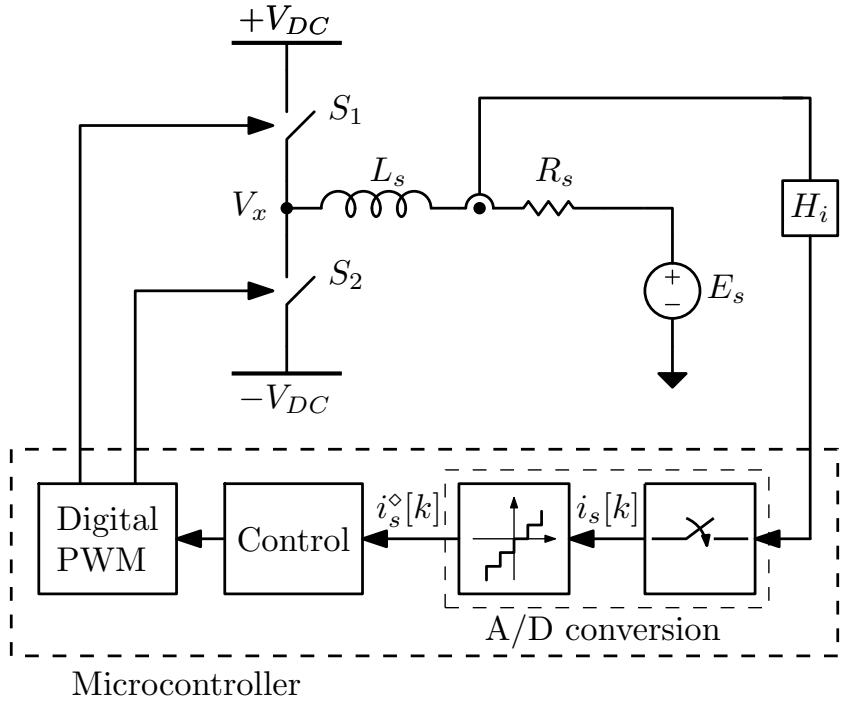


Figure 2.1: *Half-bridge voltage source inverter with digital control.*

tional variable may play a key role in the operation of the VSI but is not considered at this time.

Although this is only one of many possible examples of digital control applications, it is possible to recognize and generalize the strengths and weaknesses of digital controls. While some common advantages have already been described at the beginning of this section and will be further presented concerning specific digital control techniques, the critical points of digital control are now be briefly exposed. Precisely the following critical aspect are now introduced:

- filtering and sampling frequency
- depth and error of quantization
- sampling and synchronization with the digital pulse-width modulator
- quantizations and non-linear effects

- total loop delay

2.1.2 Filtering and sampling frequency

When passing from the continuous to a discrete (and quantized) domain or more precisely, when trying to reconstruct a signal-information from its sampled and quantized version, there are some precautions to which pay particular attention. The first problem concerns the aliasing issue.

The representation in the frequency domain of an ideal sampled signal $u(t)$ is the periodic repetition [32]:

$$\text{(ideal) sampling of } u(t) \overset{\mathscr{F}}{\Longrightarrow} \sum_{\nu=-\infty}^{+\infty} U(f - \nu f_{smpl}) \tag{2.2}$$

where $U(f)$ is the Fourier transform of $u(t)$ and f_{smpl} the sampling frequency. It is immediately noticeable by taking into account two consecutive repetitions, that if the signal is not band limited or if the signal band exceeds half of the sampling frequency f_{smpl}, the original information on $u(t)$ is lost due to overlapping of repetitions in the frequency domain. The situation is exemplified in Fig. 2.2. The top part in the figure represents the Fourier transform of the input signal. The middle part represents a situation where the chosen sampling rate is not large enough and aliasing occurs between periodic repetitions. The bottom part represents a situation where a suitable sampling rate is chosen to ensure the absence of the aliasing phenomenon.

Therefore, the first problem encountered is that of the appropriate conditions for sampling the signals: if the input signal of the analog-to-digital converter (ADC) is not band-limited, designing an appropriate filter that limits the bandwidth of the input signal is mandatory in order to satisfy the Nyquist-Shannon theorem [32] conditions for correct sampling and reconstruction. At the same time, the input filter must ensure that the information to be acquired remains after the filtering operation.

In Fig. 2.1 H_i represent the part designated to the sensing and appropri-

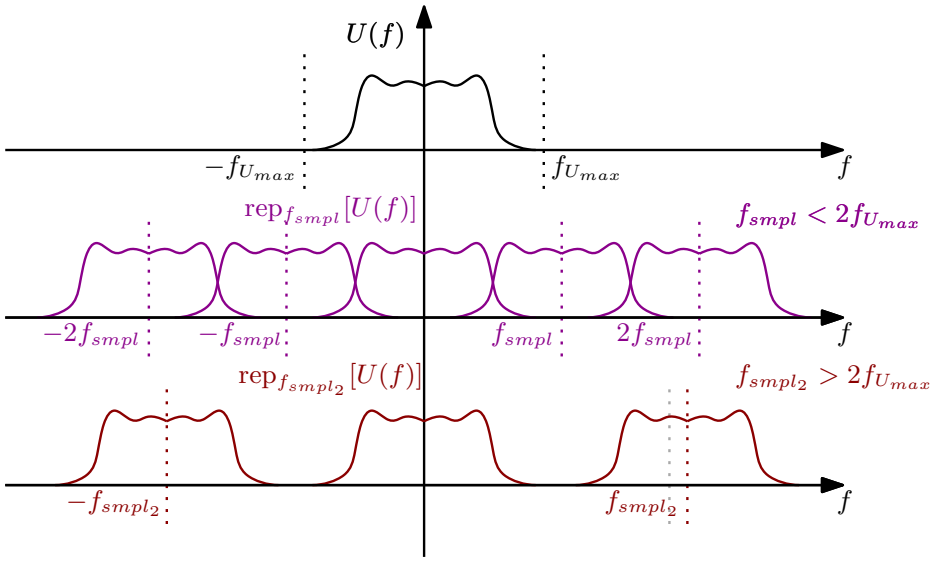


Figure 2.2: *Aliasing phenomenon exemplification.*

ate filtering section. Apparently in contrast to the above discussion, a rather common choice is to set the sampling frequency equal to the switching frequency f_s

$$\boxed{f_{smpl} = f_s}\,. \tag{2.3}$$

Although (2.3) violates the proper sampling conditions, this choice is motivated by synchronization requirements. Therefore, a small error in the sampled average current can be accepted in order to keep the acquisition process synchronized with the switching frequency. This will be clearer later in section 2.1.4 that is devoted to the digital pulse-width modulator synchronization concerns.

2.1.3 Depth and error of quantization

Once the sampling frequency has been set, the resolution of the ADC is the next key point. Resolution is generally expressed in number of bits, $n_{A/D}$, and thus in terms of possible levels into which the scale of variation of the input signal can be divided. Assuming in fact that the input signal to the quantizer can vary in a known range, indicated as $[-I_{FS}, I_{FS}]$, fixed

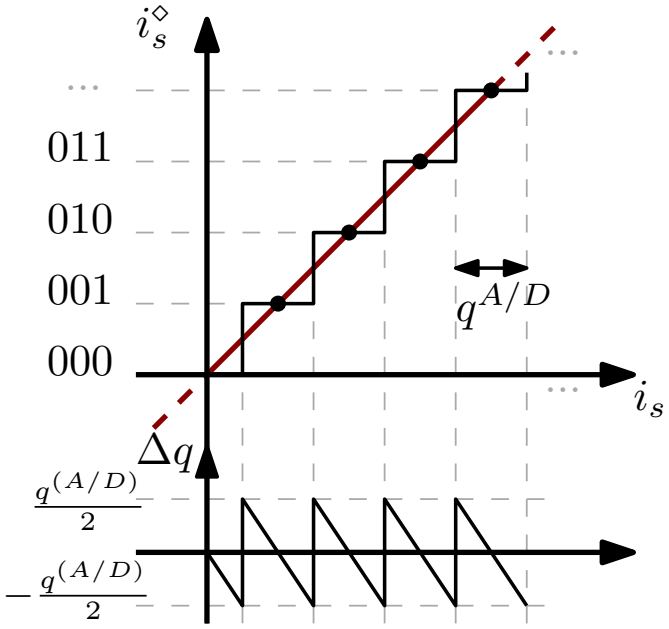


Figure 2.3: *Quantizer transcharacteristic and quantization error.*

the number of bits $n_{A/D}$ the number of levels is equal to $N_L = 2^{n_{A/D}}$ and the quantization step can be expressed as

$$q^{(A/D)} \triangleq \frac{2I_{FS}}{2^{n_{A/D}}} \tag{2.4}$$

The number of bits of the quantizer depends on the maximum regulation error that can be accept. For an ideal linear quantizer, the quantization error is defined as

$$\Delta q[k] \triangleq i_s^{\diamond}[k] - i_s[k] \tag{2.5}$$

where k denotes the k-th acquired sample. Fig. 2.3 shows the linear quantization transcharacteristic and the quantization error. The regulation and the quantization errors depend on $n^{(A/D)}$: the higher the number of bits, the smaller the quantization error and the regulation error are.

The quantized signal, processed with the ideal sampler and quantizer is always affected by the quantization error. A non-ideal linear quantizer can have two other remarkable sources of error, with respect to how non-linear the

behaviour is. These parameters are called integral non-linearity (INL) and differential non-linearity (DNL). Both parameters are related to the goodness of fit of the quantizer's transcharacteristic. INL and DNL will not be taken into account in this thesis and the quantization transcharacteristic is supposed to be always ideal.

2.1.4 Sampling and synchronization with the digital pulse-width modulator

In Sec. 2.1.2 the sampling concerns are briefly introduced. (2.3) closes the section. As mentioned above, this sampling condition violates the Shannon-Nyquist theorem. The apparent inconsistency is now analysed and justified. Moreover, it will be shown how the final implementation allows to keep intact the information about the average value of the acquired inductor current.

Fig. 2.4a shows the pulse-width modulator (PWM) and the sampling operations. For the purposes of this discussion, it is not important to dwell on the quantization of the amplitudes and the discretization of the time of the signals $u(t)$ and $c(t)$ in the figure, thus a generic discretization and quantization of the two quantities sufficiently large that they cannot be appreciated in the figure is subtended. Directly, from the graphical analysis one can immediately see that if the sampling instant is at the beginning of the switching period (i.e., when the carrier grows from zero value) for the nature of the trailing-triangle carrier, the sampled value of the current i_{L_s} is equal to its average value. To be strictly true two fundamental assumptions must be verified: the first is that the current waveform is triangular, the second is that the frequency of the modulating signal is much lower than the carrier frequency.

Therefore, if the sampling and switching processes are suitably synchronized, the resulting aliasing effect is the automatic reconstruction of the average value of the sampled signal, which is, in this case, exactly what has to be controlled. This means that the violation of the Shannon-Nyquist sampling theorem conditions does not actually limit the controller performance, but

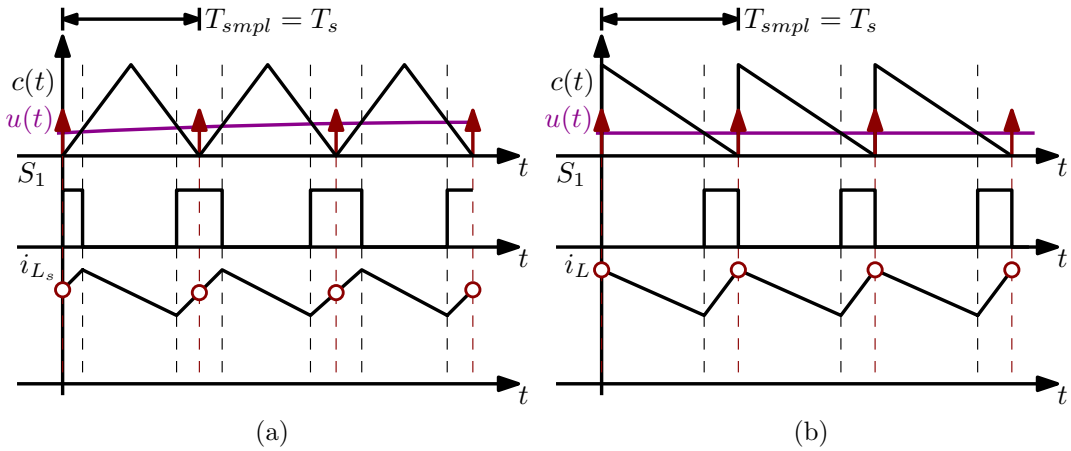


Figure 2.4: *Pulse-width modulator with TTE (a) and LE (b) carriers and sampling operations.*

it even helps to reduce the overall cost and complexity of the digital control system. Moreover, the low pass filter, necessary to limit the bandwidth of i_{L_s} in order to avoid the aliasing phenomenon can be eliminated. Therefore, the chosen sampling strategy also allows to relax the specifications of the H_i block.

In other applications, peak current information may be required (e.g., peak current-mode control for dc-dc converter). Therefore, the information to be acquired is no longer the average value of the current over a period. In order to acquire the peak current information, the structure of the PWM block must be modified. A simple approach, in line with the choice of sampling rate $f_{smpl} = f_s$ is shown in Fig. 2.4b. It is therefore sufficient to use a leading-edge (LE) carrier, instead of a TTE carrier, to properly acquire the peak current value with a single sample per switching period. Similarly, to acquire the valley current value, a trailing edge (TE) carrier can be used in the PWM block.

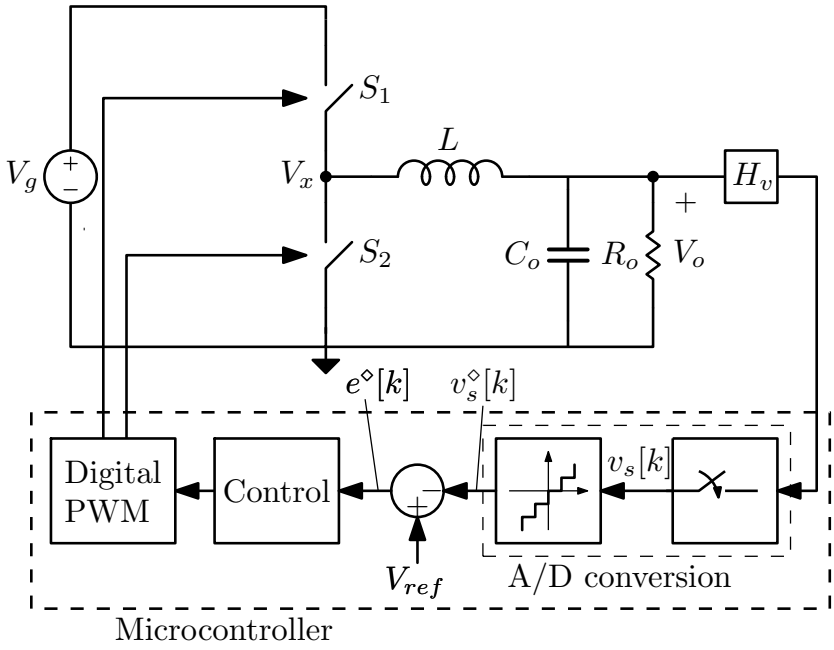


Figure 2.5: *Synchronous Buck convert and digital output voltage mode control.*

2.1.5 Quantizations and non-linear effects

Whenever a quantizer is used in a feedback control loop, it can run into a series of problems that can lead to small oscillations of the controlled signal up to large stability problems. The topic is very complex and its in-depth study is certainly beyond the scope of this thesis. For introductory purposes only, the limit cycle issue in a dc-dc Buck converter with digital output voltage-mode control is now discussed. In this example is analysed the limit cycle issue caused due to the presence of a quantizer in the ADC section and the quantization in the digital pulse-width modulator (DPWM). Fig. 2.5 shows a synchronous Buck converter and a simplified block diagram of the digital output voltage control. In 2.1.4, for the purpose of discussing the sampling rate and synchronization with the DPWM block, the quantization of the carrier/modulator was not considered. However, the carrier of the DPWM block is usually generated from a counter and is therefore discrete in timing and quantized in amplitudes. Indeed, fixed the switching period

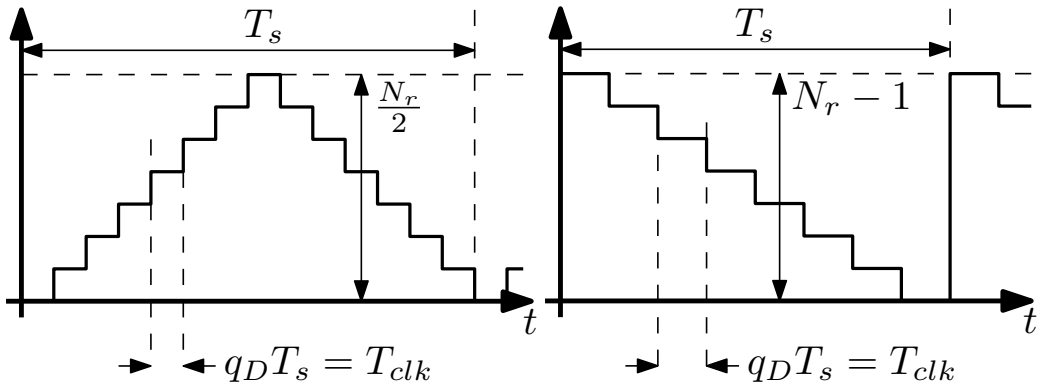


Figure 2.6: *Trailing-Triangle edge (a) and leading edge (b) carriers implemented by a counter.*

T_s, and known the minimum available clock period T_{clk} the resolution of the DPWM q_D can be found as follows

$$q_D \triangleq \frac{1}{N_r} = \frac{T_{clk}}{T_s} \tag{2.6}$$

Since the time interval between one count and the next one is constrained to be equal to T_{clk}, 2.6 is easily proved. Fig. 2.6 shows two examples of DPWM based on trailing-triangle edge (TTE) carrier and leading-edge (LE) carrier. Please note that the effective resolution of the DPWM block is lower in the case of TTE carrier than in the case with TE carrier. This is immediate if one observes that the modulating can be compared with $\frac{N_r}{2}$ (assuming, without loss of generality that N_r is even) carrier values, in case a TTE carrier is used, while the possible comparison values in case of LE carrier, but would still be true even with leading edge (TE) carrier, are exactly N_r. These issues are related to the implementation point-of-view; for more on this topic, see [citation needed]. The finite resolution problem is introduced only for the purpose of completeness and to be able to explain the limit cycle phenomenon in a less vague way.

Fig. 2.7 illustrates a set of possible output voltages due to DPWM quan-

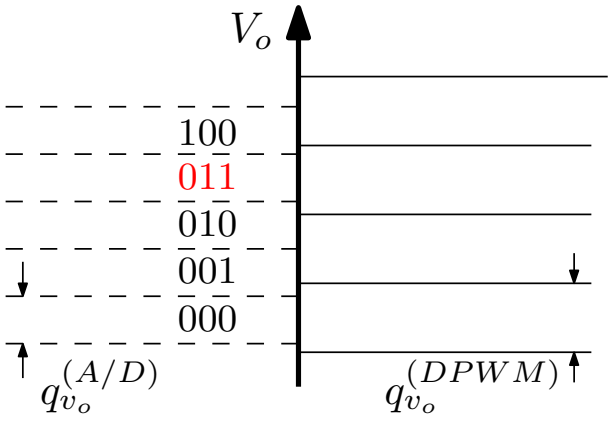


Figure 2.7: *DPWM and ADC resolutions.*

tization, and the output voltage bins due to ADC. Suppose the value to be regulated is the one corresponding to the binary sequence 011. precisely, the control error $e^{\diamond}[k]$ (see Fig. 2.5) is exactly 011. By looking Fig. 2.7, one can immediately notice that no DPWM quantization level of V_o falls into ADC bin 011. As the zero-error condition cannot be attained, the controller must continuously adjust the output voltage in a vain attempt to null the regulation error. As result, a limit cycle arises. Detailed analysis and discussion of this issue can be found in [33]. The necessary condition to avoid this phenomenon can therefore be easily summarized as

$$q_{v_o}^{(DPWM)} < q_{v_o}^{(A/D)} \tag{2.7}$$

The treatment here made of the phenomenon of the limit cycles is purely illustrative. It is a widely studied and complex phenomenon, here it has been discussed only as a typical problem of digital controls without any claim of completeness. Further discussion can be found in [34–36].

2.1.6 Total loop delay

The last issue that is here introduced concerns the total loop delay t_d. The various parts of a digital control system introduce time-delays. These delays

must be taken into account as they could further degrade the phase margin, in closed-loop system, leading to further static and/or dynamic problems. Thus, differently from the analog world, a digital control system must be modelled as a system that introduces additional delays. Indeed, in a purely analog system, the signal acquisition is instantaneous and the only delays introduced by the control system are those attributable to the controller unit. Typically, the total loop delay of a digital control system is divided into two fundamental components: the control delay and the modulation delay

$$t_d = t_{cntrl} + t_{mod}. \tag{2.8}$$

The first component incorporates everything that is before the modulator: the delay due to the ADC and the actual controller delay. The second part is instead inherent to the strategy and implementation of the modulation itself. The latter is typical of digital controls and almost always absent in their analog counterparts. Further insights can be found in [28, 29, 33].

Fig. 2.8 shows the operation of DPWM implemented with different carriers. Using the approach in *Appendix C* of [33], the small-signal frequency response can be developed for these DPWM implementations. The small-signal expression in the frequency-domain, are written in Fig. 2.8 near to the respective sketch. In contrast with the analog counterpart, the DPWM exhibits a non-null time delay. This is the delay countered in the second term in (2.8). Despite the additional delay introduced by DPWMs and the other issues discussed earlier, digital control techniques retain unique advantages that have allowed them to greatly take the place of purely analogue control techniques, especially for the applications mentioned at the beginning of this chapter. Moreover, the trend of switching to digital control techniques is still ongoing and in the next future, these applications will certainly be even more numerous.

This section concludes the introduction to digital controls. The purpose of this part is to fix the notation and language used in the rest of the text before delving into more nuanced and specific discussions.

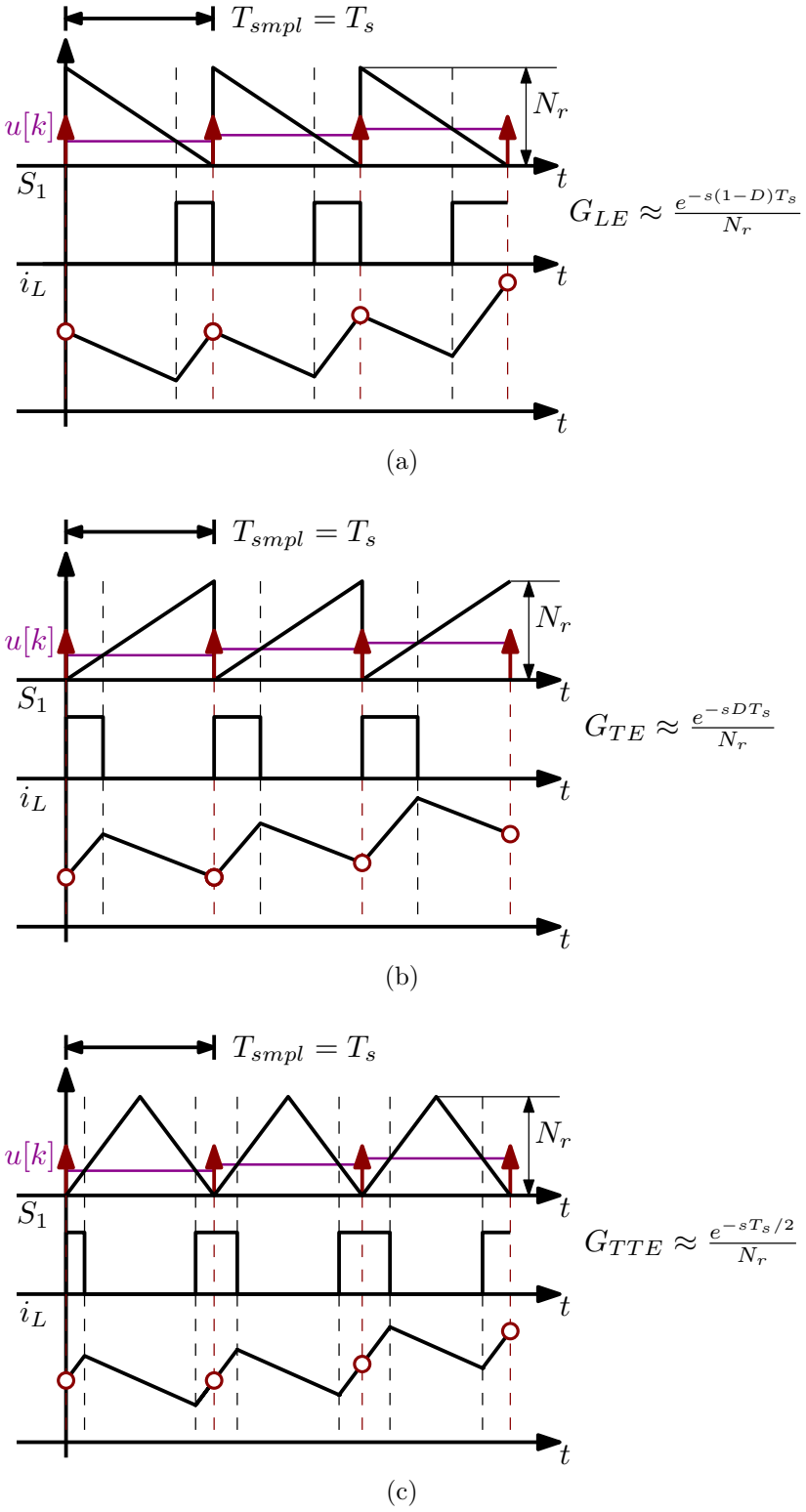


Figure 2.8: *DWPM operation and small-signal frequency response: (a) LE carrier, (b) TE carrier and (c) TTE carrier.*

2.2 Digital predictive current-mode control

Digital predictive controls are a rather unique family of digital control systems. They are usually realized through the acquisition of more informations than only variables under control and allow to obtain extremely fast corrections: ideally, a perturbation in the controlled signal is exhausted in a single switching cycle. One of its first practical applications involves average current control of a VSI [28, 29] while the application for basic dc-dc converter topologies is detailed [37]. Since this is a central theme of the research activity to which this thesis refers, the operation of the digital predictive current-mode control (DPCMC) for Buck converter is now detailed.

The block diagram of the digital predictive control proposed in [37] can be summarized as in Fig. 2.9. The figure illustrates a synchronous Buck converter with a digital predictive current-mode control. The reference current I_{ref} is maintained constant for the purposes of this chapter. Generally, this reference can be generated from the control error on the output voltage V_o, this case is detailed in later chapters.

In order to derive the equations underlying the block diagram in Fig. 2.9, the case of *peak* inductor current-mode control with LE carrier based DPWM, is now considered. Fig. 2.10 illustrates the operation of the DPWM block, the control signal and the inductor current waveform for a synchronous Buck converter. The figure highlights how the initial error $\Delta i_L[n-1]$ on the steady-state inductor current i_L is eliminated in one switching cycle. The circle indicates the sampling instant, the square is the updating instant of the signal $d[k]$ while the filled circle represents the controlling point. The three red arrows highlight the corrective action on the duration of the control signal S in the $(n+1)$-th switching cycle.

By synchronizing the sampling and the updating instants at the beginning of the switching period, the peak inductor current value is acquired from the controller. The value of i_L at the end of the next cycle can generically be

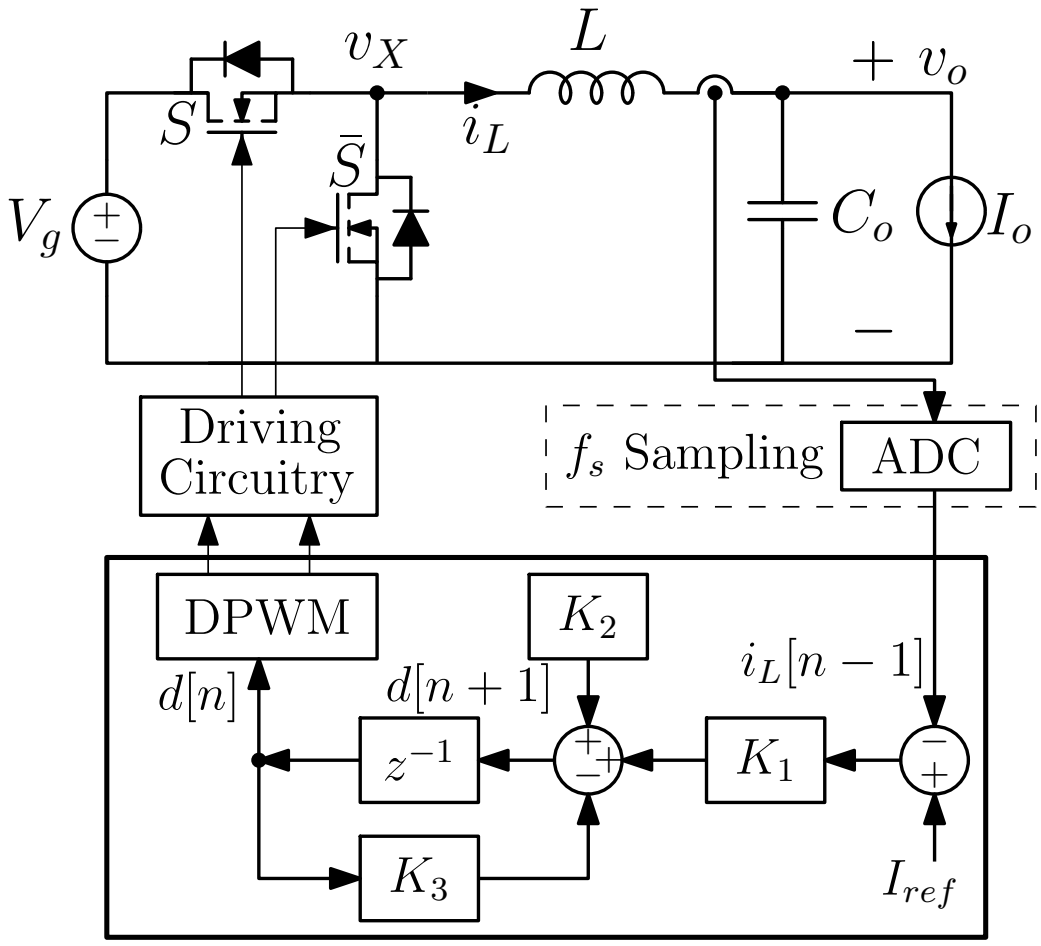


Figure 2.9: *Synchornous Buck converter and digital-predictive current-mode control block diagram.*

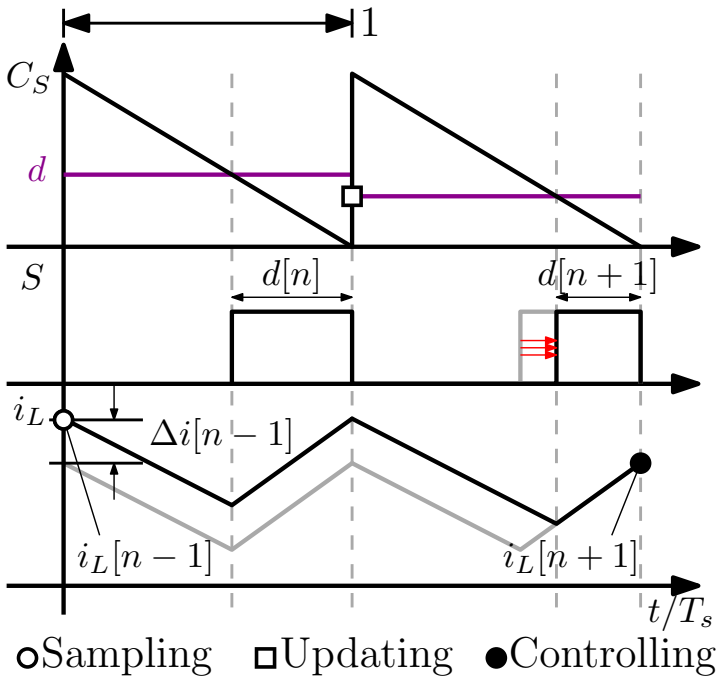


Figure 2.10: *Leading edge DPWM operation and inductor current of the synchronous Buck converter.*

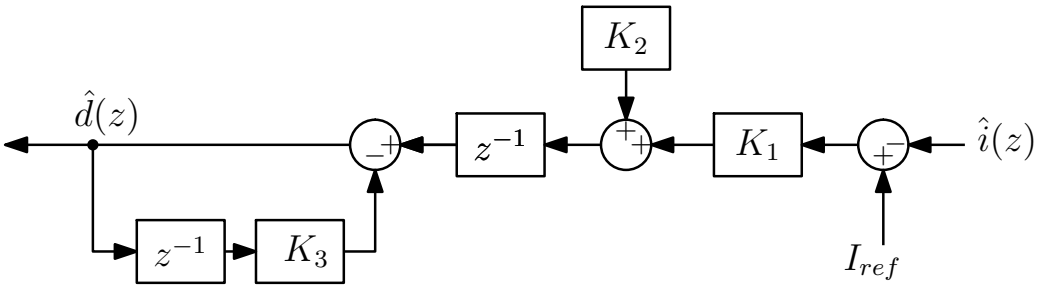


Figure 2.11: *Block diagram implementation of* (2.14).

rewritten as

$$i_L[n+1] = i_L[n-1] - \frac{V_{off}}{Lf_s}(1 - d[n]) + \frac{V_{on}}{Lf_s}d[n] - \frac{V_{off}}{Lf_s}(1-d[n+1]) + \frac{V_{on}}{Lf_s}d[n+1], \tag{2.9}$$

where $i_L[n-1]$ denotes the sampled value of i_L at the end of $(n-1)$-th switching cycle, while V_{on} and V_{off} are the voltage across the inductor during on and off phase respectively. By supposing true the small-ripple approximation on V_o and V_g, it is therefore immediate to notice that $i_L[n+1]$ is a function of new duty-cyle $d[n+1]$, the sampled inductor-current $i_L[n-1]$ and the previous duty-cycle $d[n]$

$$i_L[n+1] = f\left(d[n+1], d[n], i_L[n-1]\right). \tag{2.10}$$

The last two terms of (2.10) are known, while $d[n+1]$ has to be chosen in order to reach $i_L[n+1] = I_{ref}$. Using this in (2.9) and solving with respect to $d[n+1]$ the control equation [37] can be finally derived

$$\boxed{d[n+1] = \left(I_{ref} - i_L[n-1]\right)\frac{Lf_s}{V_g} + 2M - d[n]}, \tag{2.11}$$

where

$$\begin{aligned} V_{on} = V_g - V_o &= (1-M)V_g \\ V_{off} = V_o &= MV_g. \end{aligned} \tag{2.12}$$

The control equation (2.11) allows to determine which is the duty cycle value necessary to eliminate the sampled (i.e., measured) current error at the controlling point. This equation can be written in a more general form as follows

$$d[n+1] = K_1\left(I_{ref} - i_L[n-1]\right) + K_2 - K_3 d[n]. \tag{2.13}$$

Where K_1, K_2 and K_3 are suitable constants that depend on the operating point and the converter parameters. Applying the *Zeta-transform* operator

to both sides, (2.13) becomes

$$\hat{d}(z)z = K_1 \left(I_{ref} - \hat{i}_L(z) \right) + K_2 - K_3 \hat{d}(z). \tag{2.14}$$

Fig. 2.11 illustrates the straightforward block-diagram implementation of (2.14). Now, moving the input delay block z^{-1} to the innermost loop, since K_2 and I_{ref} are constant, immediately results in the block diagram shown in Fig. 2.9.

Please note that, in applying the zeta transform to the term $i_L[n-1]$, the expression $\hat{i}_L(z)z^{-1}$ was not used because the sample to be processed is exactly $i_L[n-1]$ and not $i_L[n]$. In other words, the input information to the predictive control, when $d[n+1]$ is being computed, is $i_L[n-1]$ and not $i_L[n]$, therefore the block diagram has in input the term $i_L[n-1]$.

Digital predictive control is similar to proportional control. The proportional constant that multiplies the current regulation error is defined as K_1 (see Fig. 2.9). The part involving K_2, K_3, the delay block, and the summing node is used to generate a constant modulating signal with zero regulation error. The modulating signal $u[k]$ is therefore compared with an appropriate carrier, inside the DPWM block. Thus, the DPWM block generates the control signals for the MOSFET S and $\bar{S}$. Clearly, this is not strictly a proportional control since the part involving K_3, z^{-1} and the *algebraic sum node* has a frequency-dependent transfer function.

2.2.1 On the estimation of the control equation coefficients

As mentioned at the beginning of this section, predictive controls need to collect more information than only variables under control. For instance, in 2.11 the parameters f_s and L need to be known but also the actual values of V_g and V_o (or V_g and M) has to be acquired and/or calculated.

This is a common aspect of all digital predictive controls. The first observation in this regard is that, in the integrated applications targeted by

this study, a package pin is usually reserved for input voltage sensing. This sensing is necessary for several reasons depending on the specific function. For example, it can be useful to know the value of the input voltage for the converter start-up, or in order to realize a proportional-integral-derivative feed-forward (PIDF) control or to properly handle the standby operation. This trend is evidenced in several commercial integrated circuits datasheets as in [38–40].

Therefore, assuming that the information on V_g is available to the controller is consistent with the state-of-the-art for several commercial products. Furthermore, for converters considered in this work one has $M = D$, (i.e., the voltage conversion ratio is equal to the duty cycle), this is a signal always available inside the digital controller. Also notice that an estimate of V_g can also be numerically obtained as V_o/M, eliminating the need for input voltage sensing altogether at the expense of a slight increase in hardware complexity. Overall, the presence of V_g and M in the predictive control laws do not pose significant technical challenges to the application of DPCMC since all equations can be digitally implemented using measured or online-estimated coefficients. For the values of f_s and L the problem is more elaborate. While the switching frequency is constant, there can be significant variations from the nominal inductance values. For this reason, in chapter 4 when the practical implementation of the controller is considered, its robustness with respect to such variations is detailed and validated through simulations.

2.2.2 Current stability and dead-beat behaviour

Once the equation governing the steady-state has been found, its stability character has to be clarified. The methodology for studying the static stability of the inductor current is proposed in [37]. The inductor peak current error is defined as

$$\Delta i_L[n] \triangleq i_L[n] - i_{L_{ss}} \tag{2.15}$$

where $i_{L_{ss}}$ is the steady-state inductor current calculated for the given operating point at the sampling instant. As a reference to 2.10, the inductor peak current error can be generally written as

$$\Delta i_L[n+1] = \Delta i_L[n-1] + \frac{V_g}{Lf_s}\left(d[n] + d[n+1]\right) - \frac{2MV_g}{Lf_s} \tag{2.16}$$

Assuming, without loss of generality, that the situation depicted by (2.16) is related to the perturbation of a steady-state operation, one can substitute $d[n]$ with the steady-state duty-cycle $D = M$ and $d[n+1]$ with (2.9), obtaining

$$\frac{\Delta i_L[n+1]}{\Delta i_L[n-1]} = 0. \tag{2.17}$$

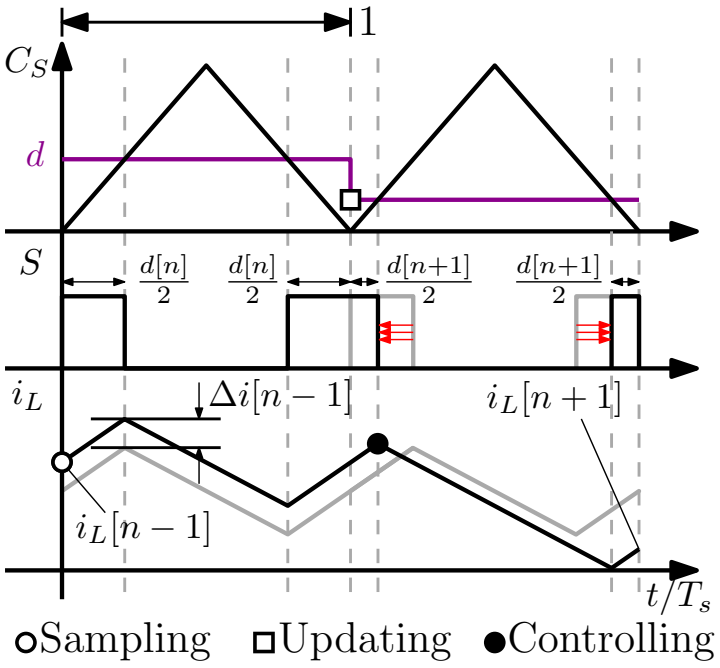
Therefore inductor peak current error $\Delta i_L[n+1]$ is zero whatever the value of $\Delta i_L[n-1]$. The controller act in a dead-beat fashion since *the initial error is recovered in one switching cycle* after the acquisition instant.

2.2.3 Other controller-carrier pairings

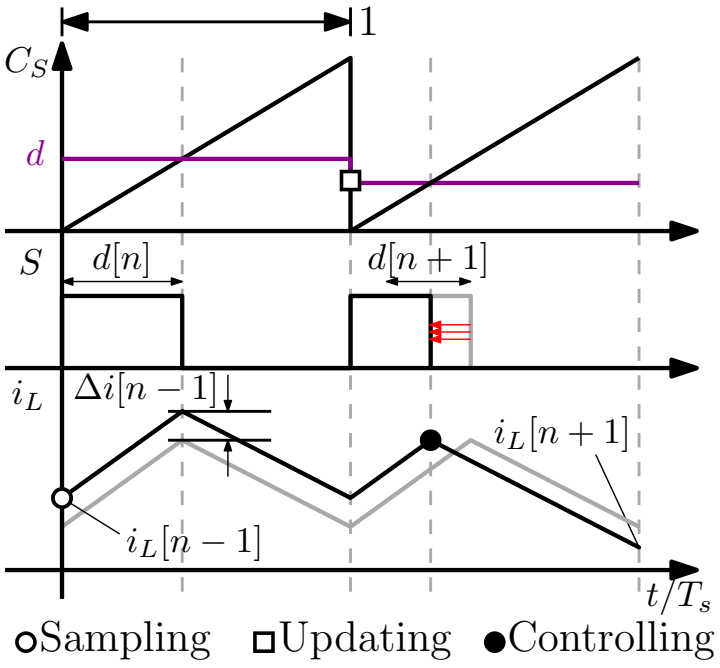
For the control strategy described in the previous section, the time distance between the sampled instant and the controlling point is constant and always equal to two whole switching cycles. This is obtained since a LE carrier is used and also because the controlling point coincides with the sampling point at the next cycle. However, it is possible to extend the described approach making other pairings between carriers and variables under control. To better clarify this aspect, the two peak current-mode controllers that can be implemented with TTE and TE carriers are now presented.

Fig. 2.12 shows the operation of the *peak* DPCMC where the DPWM is realized with a TTE and TE carrier respectively. With the same methodology used in 2.2, the following control equations can be founded for *peak* DPCMC implemented with a TTE and TE carrier respectively

$$d[n+1] = \frac{2Lf_s}{V_g(1-M)}(I_{ref} - i_L[n-1]) + \frac{2M}{1-M} - \frac{2}{1-M}d[n] \tag{2.18}$$



(a)



(b)

Figure 2.12: *Peak DPCMC with trailing triangle edge (a) and trailing edge (b) carrier based DPWM operation.*

$$d[n+1] = \frac{Lf_s}{V_g(1-M)}(I_{ref} - i_L[n-1]) + \frac{M}{1-M} - \frac{1}{1-M}d[n]. \qquad (2.19)$$

By inspecting (2.11) and (2.18) (2.19), a first difference can be grasped: all coefficients are functions of the operating point (i.e., V_g, M or V_g and V_o). Furthermore, observing the qualitative operation of the controls, exemplified in 2.12, one immediately observes that the error on the sampled value differs from the error at the control point. Thus, *while the error at the control point is recovered, the error at the sampled instant continues to change.* This causes a significant change in the static stability properties of the inductor current.

In fact, the ratio between two consecutive current errors, for the two considered cases, can be written as follows

$$\frac{\Delta i[n+1]}{\Delta i[n-1]} = -\frac{1+M}{1-M} \qquad (2.20)$$

$$\frac{\Delta i[n+1]}{\Delta i[n-1]} = -\frac{M}{1-M}. \qquad (2.21)$$

(2.20) and (2.21) are obtained by substituting the predictive equation relative to the implementation with TTE and TE carrier respectively, in equation (2.16).

The ratio used in (2.17) can be interpreted as the pole position of the closed-loop transfer function of the inductor current control system. This requires its absolute value to be less than one throughout the operating range. In other words, the stability criterion for inductor current can be summarized as follows

$$\left|\frac{\Delta i[n+1]}{\Delta i[n-1]}\right| < 1. \qquad (2.22)$$

This stability condition is necessary to avoid sub-harmonic oscillation and can be represented graphically as in Fig. 2.13. Thus, the closed-loop system guarantees a stable operation of the inductor current if the absolute value

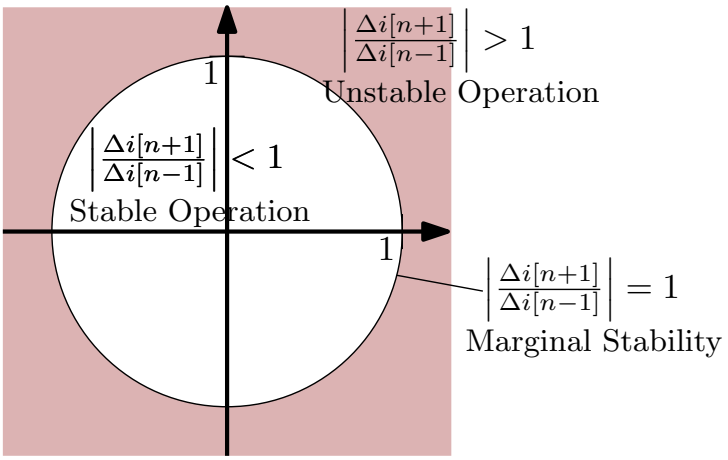


Figure 2.13: *Graphical representation of stability condition* (2.22)

of the ratio defined in (2.22) belongs to the unitary radius circle. For the two cases introduced in this paragraph, the ratios (2.22) allow to derive the following stability conditions

$$\begin{aligned} M \leq 0 \quad \text{or} \quad M > 1 \quad &\text{for peak DPCMC implemeted with TTE carrier} \\ M \leq \frac{1}{2} \quad \text{or} \quad M > 1 \quad &\text{for peak DPCMC implemeted with TE carrier} \end{aligned} \tag{2.23}$$

Therefore, in the first case, the system is always unstable, whereas, in the case of *peak* DPCMC implemented with a TE carrier, the system operates stably for half the range of the conversion ratio M. The latter control can therefore be implemented as long as $M < \frac{1}{2}$ but its behaviour is not dead-beat since the current error at the sampling point is recovered in several successive cycles.

2.2.4 Average and valley DPCMC

The technique described in the previous sections can be extended to the *average* and *valley* DPCMC as well. In order to obtain a bead-beat behaviour for the first one the DPWM has to be realized with a TTE carrier. Indeed, by synchronizing the sampling instant at the beginning of the switching pe-

riod, thanks to the shape of the TTE carrier, the average value is acquired. Average is here used intended as the middle point of the triangular inductor current waveform. In [37] the average DPCMC is implemented using the definition 2.1, this leads to a different control equation and therefore different inductor current stability properties. This aspect is clarified later in chapter 5.

Fig. 2.14a exemplifies the *average* DPCMC operation. The main difference with respect to the *peak* DPCMC regards the corrective action: since a TTE carrier is used, both edges of S (and therefore $\bar{S}$) can be adjusted. In *peak* DPCMC, as well as in the *valley* DPCMC, only one edge can be moved. This property doesn't lead to significant differences in the dynamic behaviour of the controlled Buck converter but will cause remarkable differences when applied to the flying-capacitor multi-level converters.

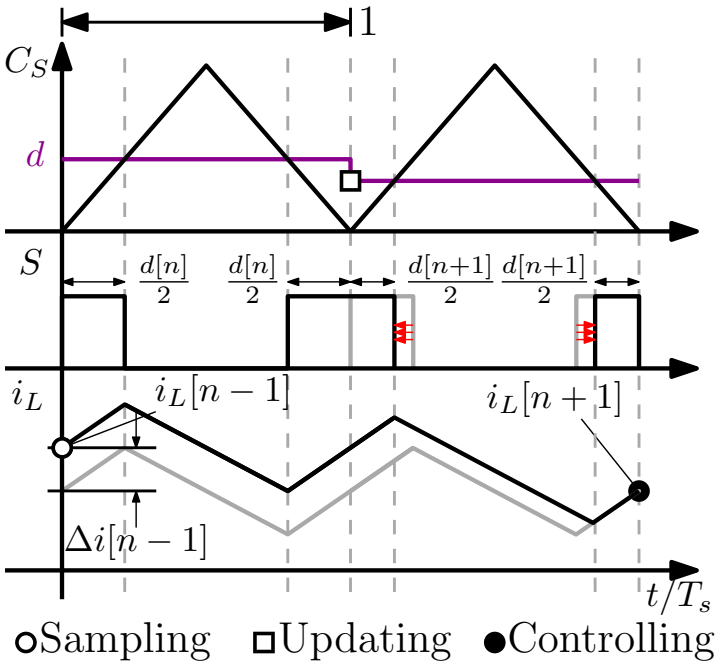
Fig. 2.14b exemplifies the operation of the *valley* DPCMC with a TE carrier based DPWM. In this case, the controller is able to only change the trailing edge of the controlling signal S.

Both predictive controllers presented in this section share the same control equation and same stability properties of inductor current as the peak current-mode control. Therefore, for *average* and *valley* DPCMC implemented with a TTE carrier and TE carrier respectively, (2.11) and the property (2.17) apply.

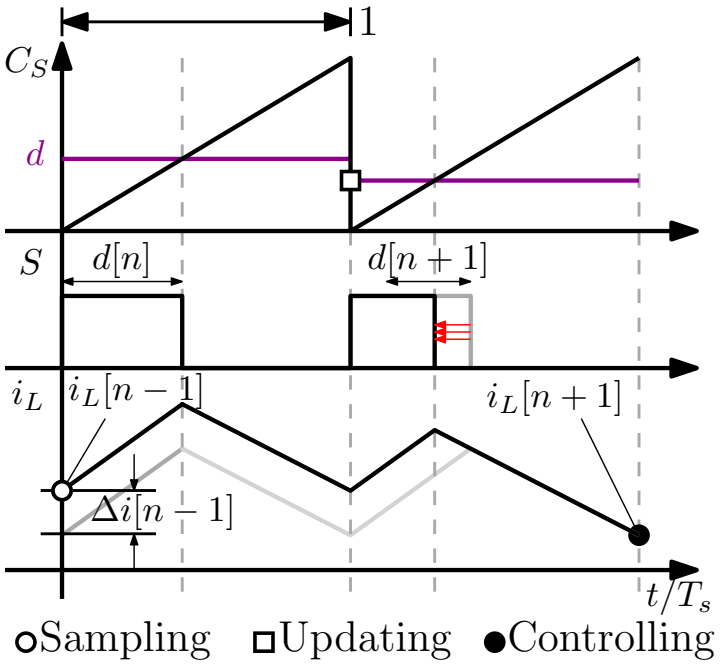
2.2.5 Stability summary

Following the approach described in the previous paragraphs, a total of nine digital-predictive controls can be made by pairing the controlling points and the carrier types: *peak*, *valley* and *average*, with the different DPWM implemented with the three carries: LE, TE and TTE. The described methodology for the nine cases can be easily extended to other cases, such as DPWM realized with a leading-triangle edge (LTE) carrier. A stability inductor-current summary is reported in Tab. 2.1.

Hence, in order to achieve stable current operation and dead-beat be-



(a)



(b)

Figure 2.14: Average *DPCMC based on trailing-triangle edge DPWM (a)* and valley *DPCMC based on trailing edge DPWM operation and inductor current waveform.*

Table 2.1: *Summary of the stability properties for* peak, average *and* valley *DPCMC implemented with LE, TTE and TE carrier.*
(*) Dead-Beat behaviour.

Carrier	*Peak* DPCMC	*Average* DPCMC	*Valley* DPCMC
LE	Stable*	Stable	Stable for $\frac{1}{2} < M < 1$
TTE	Unstable	Stable*	Unstable
TE	Stable for $0 < M < \frac{1}{2}$	Stable	Stable *

haviour, it is necessary to choose the appropriate carrier depending on the value to be controlled. The pairings on the main diagonal of Tab. 2.1 identify this type of control. For these, the inductor current error is recovered in one switching cycle after the sampling instant and there are no static stability issues. The other pairings between carriers and control points lead to different inductor current dynamics. Precisely, with TTE carrier based DPWM, only the average current-mode control can be correctly implemented. With LE carrier, valley current-mode control can be effectively implemented provided the conversion ratio is limited: $\frac{1}{2} < M < 1$. Finally, with TE carrier, a peak current-mode control can be implemented only if $0 < M < \frac{1}{2}$.

The dead-beat controllers achievable with DPCMC are the main focus of this thesis and will be extensively studied throughout next chapters with reference to their application to multi-level flying-capacitor Buck converters.

Chapter 3

Multi-Level Flying-Capacitor Buck Converter

In this chapter, the multi-level converter topologies are introduced. After a brief description of the most relevant topologies, the focus is moved to the multi-level flying-capacitor Buck converter. This is a dc-dc step-down converter topology family. Firstly, the open-loop operation is analysed. Next, the issues regarding the FC voltages are detailed. This is a critical topic since the straightforward extension of the most common controls techniques used for the traditional Buck solution, cannot be done without proper considerations and/or specific modifications in the control strategy regarding the flying-capacitor voltages balance and stability. This chapter is closed with a comparison between MLFC Buck converters and the traditional *two-level* Buck converter (2-LBC).

3.1 Multi-Level topologies

Multi-level denotes a group of dc-ac and dc-dc converters. Some of the most relevant topologies are: the multi-level diode-clamped (ML-DC) converter, multi-level cascaded (ML-C) converter and multi-level flying-capacitor (MLFC) converter. These topologies share modular properties that gener-

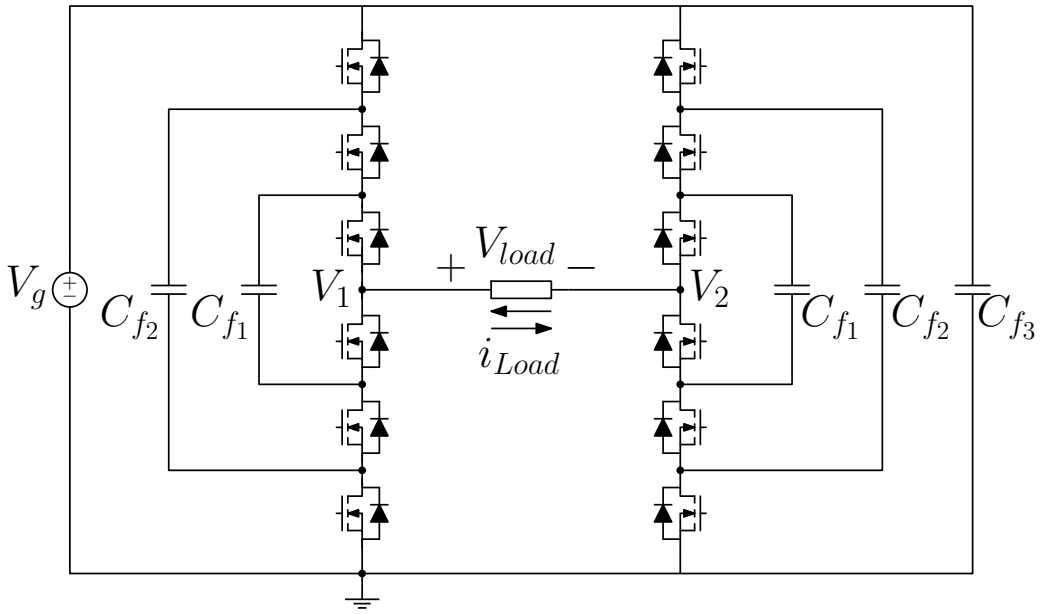


Figure 3.1: *7-level flying-capacitor full-bridge voltage-source inverter scheme.*

ally allow them to subdivide a specific voltagelevel into sub-levels in order to ensure lower voltage stresses, better accuracy in reconstructing a given waveform and/or higher flexibility [41, 42]. Some multi-level topologies also allow an equivalent frequency multiplication effect on the current through the magnetic elements. This makes it possible to reduce the overall converter footprint leading to a cost reduction [43, 44].

Multi-level converters were initially used in dc-ac applications. Subsequently, their unique properties have attracted attention for dc-dc application as well. This thesis focuses on the implementation of digital predictive controls for multi-level flying-capacitor converters. For this reason, the following introduces this converter type with reference to one of the first practical applications. Several multi-level dc-ac and dc-dc converters with flying-capacitors can be deduced from the circuit in Fig. 3.1. This is a 7-level flying-capacitor full-bridge voltage-source inverter (7LFCFB-VSI) [43]. The operating principle of the 7LFCFB-VSI is explained as follows. Assuming that all FCs are balanced (i.e., $V_{f_i} = i\frac{V_g}{n},\ n = 3,\ i = 1, 2, 3$), through an appropriate control law it is possible to make the voltages V_1 and V_2 follow a specific trend. For

instance, in order for V_1 to be brought to the voltage value $\frac{V_g}{3}$ three different topological states can be used: V_g in series to the capacitance C_{f_2} as shown on Fig. 3.2a, the topological state whit the series interconnection of C_{f_2} and C_{f_1} as shown on Fig. 3.2b or the one that interconnects C_{f_1} directly to the switching node as in Fig. 3.2c. For the three cases exemplified in Fig. 3.2, $V_2 = V_g$, therefore $V_{load} = \frac{V_g}{3} - V_g = -\frac{2}{3}V_g$.

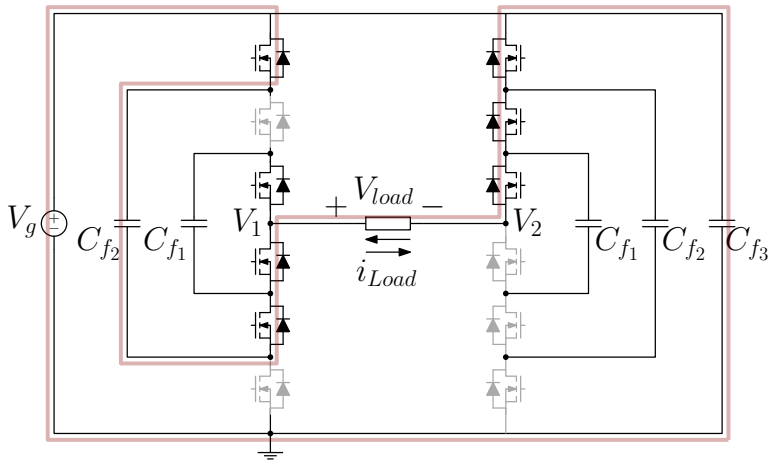
Since both V_1 and V_2 can reach four voltage levels (including $V_1 = V_2 = 0$) the load voltage V_{load} moves over seven distinct voltage levels:

$$\frac{V_{load}}{V_g} \in \left\{-\frac{3}{3}, -\frac{2}{3}, -\frac{1}{3}, 0, +\frac{1}{3}, +\frac{2}{3}, +\frac{3}{3}\right\}. \tag{3.1}$$

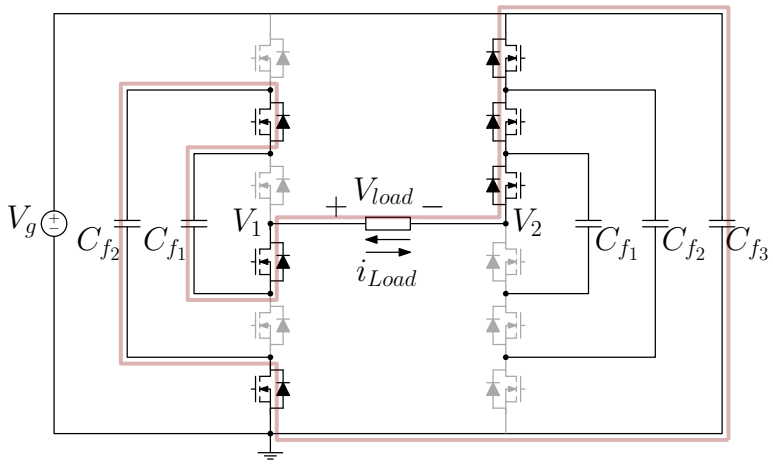
An example of waveforms for the open-loop operation of the 7-LFCFB-VSI is shown in Fig. 3.3. As explained before, voltages V_1 and V_2 can move across four voltage levels. By operating an appropriate phase shift in the control signals for the two legs of the full-bridge, it is possible to obtain that $V_{load} = V_1 - V_2$ moves over seven voltage levels. In Fig. 3.3, the time axis is normalized with respect to the inverse of the network frequency (i.e., $T_{50} = 1/f_{50}$). The current i_{load} is obtained assuming that an inductive load is used. This solution clearly offers superior performance in terms of reduced harmonic distortion and reduced voltage stresses compared to a classical *two-level* full-bridge VSI topology [45]. Similar advantages apply to ML-DC and ML-C topologies.

3.2 Multi-level flying-capacitor Buck converter

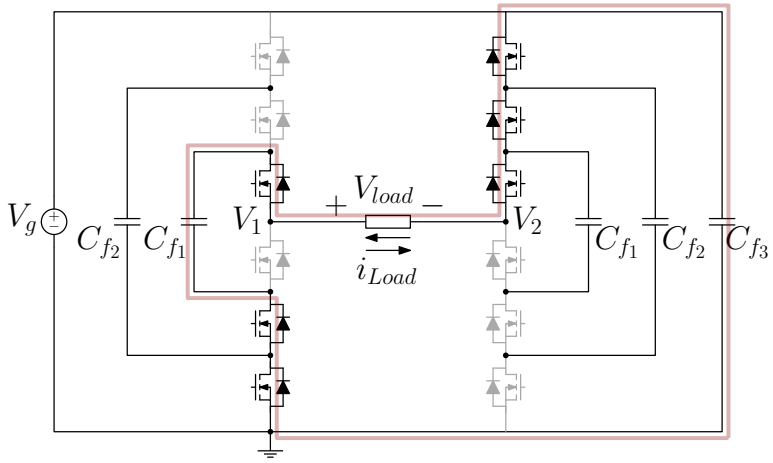
This section is intended to provide to the reader: a comprehensive overview of the operation of multi-level flying-capacitor Buck converters and the most important issues associated with their use. The MLFC Buck converter can be derived from the circuit on Fig. 3.1. By supposing that the load is purely inductive, by removing the V_g connection between the two legs a bi-directional multi-level flying-capacitor Buck-Boost converter is obtained. From this, the



(a)



(b)



(c)

Figure 3.2: *7LFCFB-VSI operation for* $V_{load} = \frac{V_g}{3} - V_g = -\frac{2}{3}V_g$*: (a) topological-state with* V_g *in series to the capacitance* C_{f_2}*, (b) topological-state with* C_{f_2} *in series to the capacitance* C_{f_1} *and (c) topological state with* C_{f_1} *directly connected to the switching node 1. The red line highlights the* i_{load} *path.*

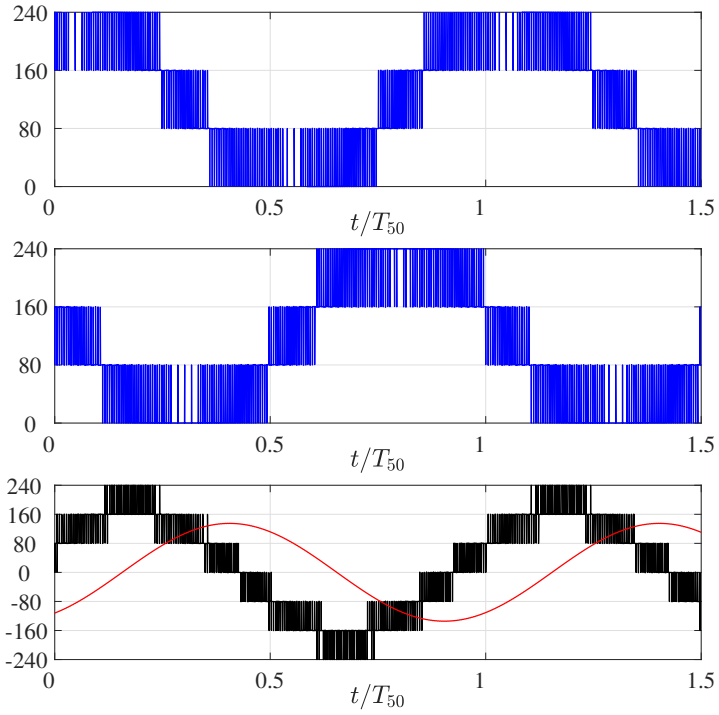


Figure 3.3: *7-LFCFB-VSI operation: (from top to the bottom) switching node voltages V_1 and V_2, load voltage V_{load} (black) and current i_{load} (red).*

multi-level flying-capacitor Buck converter scheme can be obtained by substituting the second leg with a single capacitance. This Buck topology is sketched in Fig. 3.4. This multi-level step-down topology is also referred to as a N-level flying-capacitor (N-LFC) Buck converter where N represent the number of possible voltage levels for the switching node v_X. In order to obtain the N voltage levels, $2(N-1)$ power switches and $N-2$ flying-capacitors (FCs) are required. For the correct operation, average FCs voltages must remain *stable* and *balanced* at precise values. Precisely, by indicating with V_{f_i} the average voltage of C_{f_i}, the balanced average FC voltages can be generally written as follows

$$\boxed{V_{f_i} = \frac{i\,V_g}{N-1} \quad \text{for} \quad i = 1, 2...N-2} \tag{3.2}$$

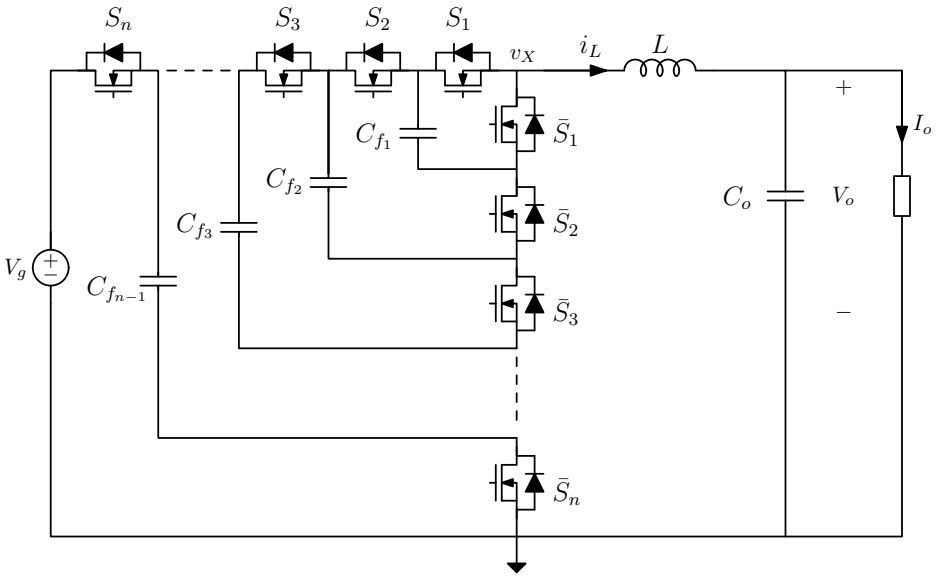


Figure 3.4: *Multi-level flying-capacitor Buck converter scheme.*

In order to simply and concisely explain the open-loop operation, in the following section, (3.2) is supposed to be always verified unless expressly stated.

3.2.1 Open-loop operation with multi-carrier pulse-width modulator

The control signals for the switches S_1, S_2, ... S_{N-1} can be generated by extending the pulse-width modulator technique using as many carriers as there are switch pairs to control. The used driving strategy is summarized in Fig. 3.5a, this structure is called phase-shifted multi-carrier pulse-width modulator (PSMC-PWM). The PSMC-PWM uses $N-1$ carriers each one delayed by $T_s/(N-1)$ with respect to the previous one. In Fig. 3.5a the time axis is normalized with respect to the switching period (i.e., $x = \frac{t}{T_s}$). Therefore, the normalized time-shift between two consecutive carriers is $\frac{1}{N-1}$. In this example, LE carriers are used to implement the modulator. For this example, the modulating signal $u(x)$ is the same for all carriers. Fig. 3.5b exemplify how the control signal S_i is generated from the comparison of $u(x)$

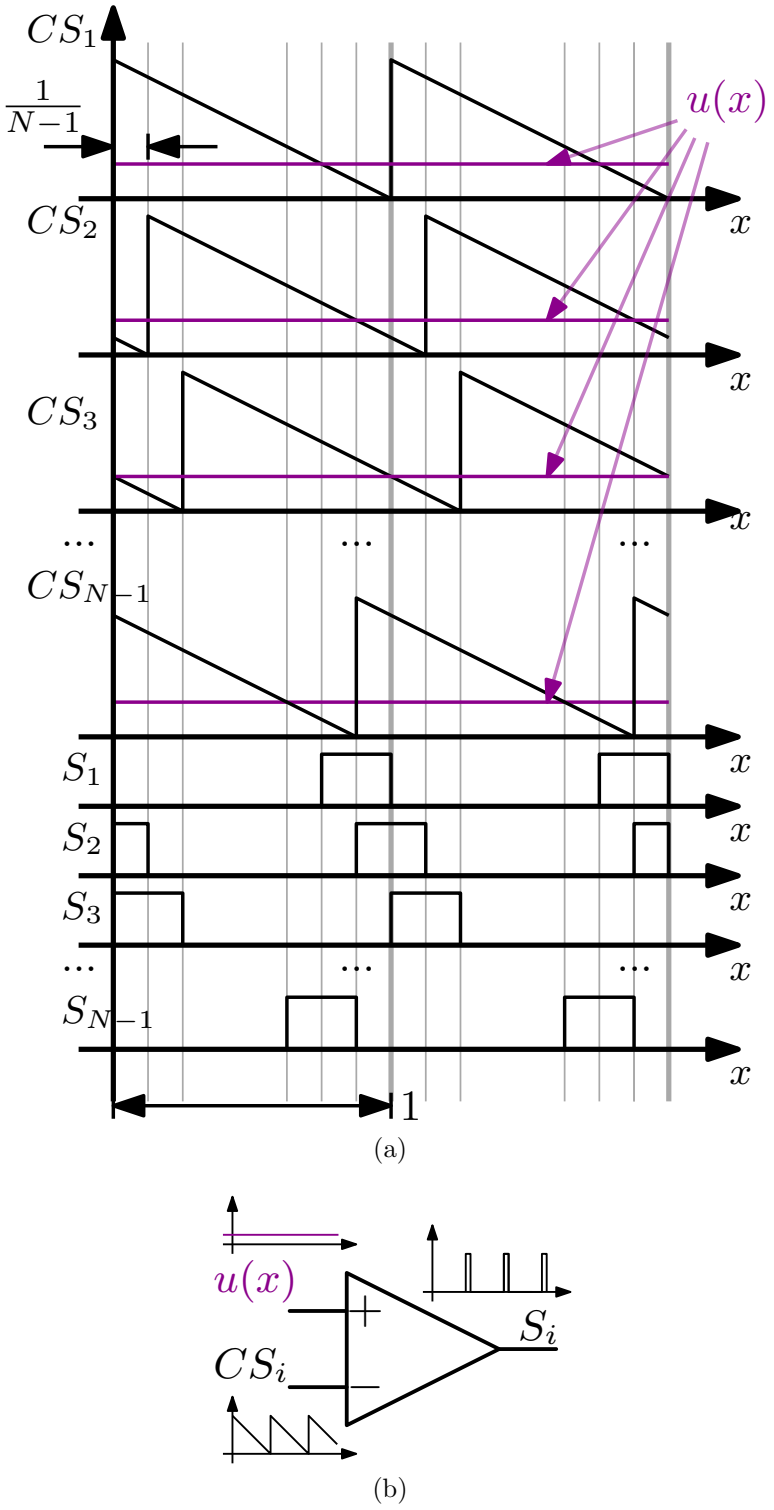


Figure 3.5: *(a) Multi-carrier pulse-width modulator for open-loop operation of a N-LFC Buck converter and (b) comparator operation and control signal generation.*

and the i-th LE carrier CS_i.

Assuming to use the above-mentioned PSMC-PWM a generic N-LFC Buck admits $N-1$ operating modes depending on the value of the voltage conversion ratio $M = \frac{V_o}{V_g}$. Indeed, as M varies, the different operating modes can be deduced from the following inequalities:

$$\boxed{\frac{mode_i - 1}{N-1} < M < \frac{mode_i}{N-1}} \tag{3.3}$$

For instance, using (3.3) with $N = 4$, one can immediately find that the 4-LFC Buck converter admits three (i.e., $N-1 = 4-1 = 3$) operating modes:

$$\text{operating mode} = \begin{cases} mode_1 & \text{IF} \quad \frac{0}{3} < M < \frac{1}{3} \\ mode_2 & \text{IF} \quad \frac{1}{3} < M < \frac{2}{3} \\ mode_3 & \text{IF} \quad \frac{2}{3} < M < \frac{3}{3} \end{cases} \tag{3.4}$$

Continuing to use the 4-LFC Buck converter as example, the $mode_1$ operation is now detailed.

4-LFC Buck converter operating in $mode_1$

The control signals S_1, S_2, S_3 can be directly deduced from Fig. 3.5a: since there are exactly three pairs of switches in the four levels, the first three carriers and the first three related control signals can be considered for this example. The control signals $\bar{S}_1$, $\bar{S}_2$, $\bar{S}_3$ are the negated logic version of the first three control signals, therefore no dead-times are here considered. Fig. 3.6a shows the 4-LFC Buck converter. Please note that when this will not cause ambiguity and with abuse of language S_i indicates the switch and the control signal that drives it as well. In this section *small ripple approximation* (SRA) hypothesis is used for both, the input and output voltages and for the

FC voltages:

$$\begin{aligned} v_g(x) &= V_g + \hat{v}_g(x) \quad \text{SRA:} \quad V_g \gg \hat{v}_g(x) \implies v_g(x) \approx V_g \\ v_o(x) &= V_o + \hat{v}_o(x) \quad \text{SRA:} \quad V_o \gg \hat{v}_o(x) \implies v_o(x) \approx V_o \\ v_{f_i}(x) &= V_{f_i} + \hat{v}_{f_i}(x) \quad \text{SRA:} \quad V_{f_i} \gg \hat{v}_{f_i}(x) \implies v_{f_i}(x) \approx V_{f_i} \quad i = 1, 2 \end{aligned} \tag{3.5}$$

Under hypotheses (3.5), $mode_1$ operation (i.e., $0 < M < \frac{1}{3}$) of the 4-LFC Buck converter is now detailed. Inductor and FC currents are sketched in Fig. 3.7 for a generic 4-L case. In the following analysis the converter is supposed to operates with ideal timing-conditions (i.e., $d_1 = d_2 = d_3 = D = M$) and with balanced FC voltages (i.e., $V_{f_1} = \frac{V_g}{3}$ and $V_{f_2} = \frac{2}{3}V_g$).

1. $0 < x < D$

   Fig. 3.6b shows the corresponding sub-topological state, obtained for $S_1 = 1$ and $S_2 = S_3 = 0$. The voltage at the switching node can be written as

   $$v_x = V_g - V_{f_2} = V_g - \frac{2}{3}V_g = \frac{V_g}{3}. \tag{3.6}$$

   During this time-interval the current through C_{f_2} coincides with the inductor current, while the current through C_{f_2} is zero

   $$i_{f_2} = i_L \quad \text{and} \quad i_{f_1} = 0. \tag{3.7}$$

2. $D < x < \frac{1}{3}$

   The next topological-state, obtained for $S_1 = S_2 = S_3 = 0$, is sketched in Fig. 3.6c. In this case the switching node is connected directly to the ground and both FC are floating, therefore

   $$\begin{aligned} v_x &= 0 \\ i_{f_1} &= i_{f_2} = 0. \end{aligned} \tag{3.8}$$

3. $\frac{1}{3} < x < \frac{1}{3} + D$

   The subsequent topological state, obtained for $S_2 = 1$ and $S_3 = S_1 = 0$,

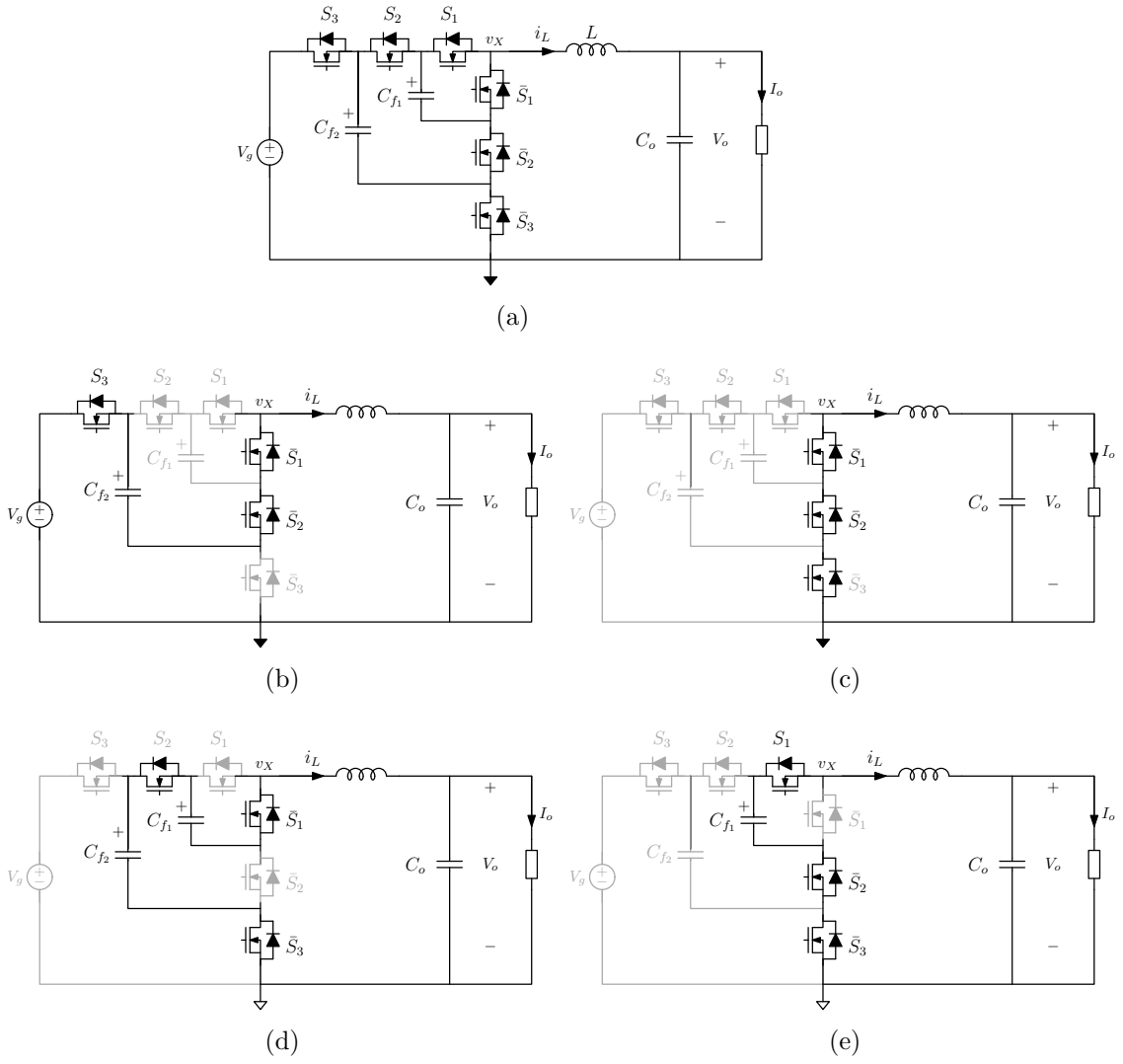


Figure 3.6

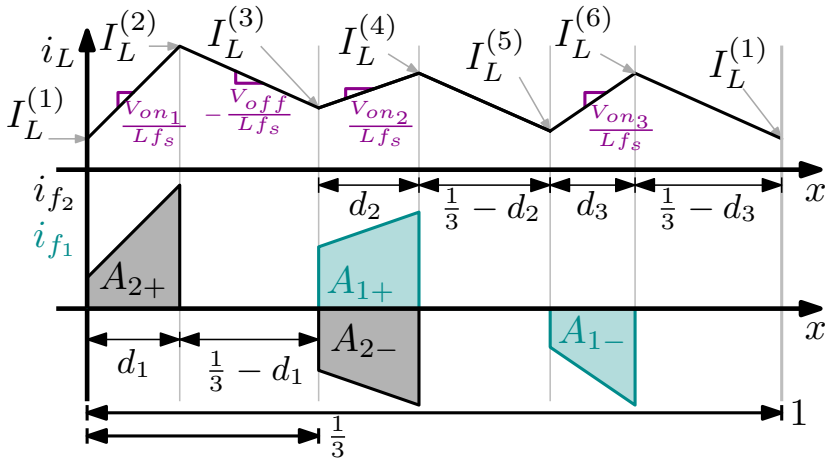


Figure 3.7: *Inductor and FC currents of the 4-LFC Buck converter.*

is sketched in Fig. 3.6d. In this case one can deduce

$$\begin{aligned} v_x &= V_{f_2} - V_{f_1} = 2\frac{V_g}{3} - \frac{V_g}{3} = \frac{V_g}{3} \\ i_{f_1} &= -i_{f_2} = i_L. \end{aligned} \tag{3.9}$$

4. $\frac{1}{3} + D < x < \frac{2}{3}$
   Moving forward in the time sequence, the topological state identified by $S_1 = S_2 = S_3 = 0$ is again encountered, therefore (3.8) applies again.

5. $\frac{2}{3} < x < \frac{2}{3} + D$
   Fig. 3.6d shows the topological state obtained for $S_1 = 1$ and $S_3 = S_2 = 0$. The switching node voltage and the FC currents can be written as follows

$$\begin{aligned} v_x &= V_{f_1} = \frac{V_g}{3} \\ i_{f_1} &= -i_L \quad \text{and} \quad i_{f_2} = 0. \end{aligned} \tag{3.10}$$

6. $\frac{2}{3} + D < x < \frac{3}{3}$
   The last topological state is, once again, the one identified by $S_1 = S_2 = S_3 = 0$.

By putting together (3.6), (3.8), (3.9) and (3.10) the following equation for the inductor voltage can be derived

$$v_L = \begin{cases} \frac{V_g}{3} - V_o & \text{when } 0 < x < D \\ -V_o & \text{when } D < x < \frac{1}{3} \\ \frac{V_g}{3} - V_o & \text{when } \frac{1}{3} < x < \frac{1}{3} + D \\ -V_o & \text{when } \frac{1}{3} + D < x < \frac{2}{3} \\ \frac{V_g}{3} - V_o & \text{when } \frac{2}{3} < x < \frac{2}{3} + D \\ -V_o & \text{when } \frac{2}{3} + D < x < \frac{3}{3}. \end{cases} \tag{3.11}$$

The voltage conversion ratio expression is therefore obtained by imposing the *volt-second balance* condition for the steady-state operation

$$V_L \triangleq \langle v_L \rangle_{T_s} = \frac{1}{T_s} \int_{t_o}^{t_o+T_S} v_L(\tau) d\tau = \int_{x_o}^{x_o+1} v_L(x) dx = 0. \tag{3.12}$$

From equation (3.12) the voltage conversion ratio expression is immediately obtained

$$3 \left(\frac{V_g}{3} - V_o \right) D = 3V_o \left(\frac{1}{3} - D \right) \implies M \triangleq \frac{V_o}{V_g} = D. \tag{3.13}$$

The open-loop operation, in presence of FC voltage unbalances is now analysed. To achieve a more elegant and concise treatment, the average FC voltages can be re-written highlighting the imbalance with respect to the ideal steady-state balanced value as follows

$$\begin{aligned} V_{f_1} =& \frac{V_g}{3} + \hat{v}_{f_1} = \frac{V_g}{3} \left(1 + \hat{v}_{N_1}\right) \\ V_{f_2} =& \frac{2}{3} V_g + \hat{v}_{f_2} = \frac{V_g}{3} \left(2 + \hat{v}_{N_2}\right), \end{aligned} \tag{3.14}$$

where $\hat{v}_{f_i}$ is the i-th absolute voltage imbalance, while the $\hat{v}_{N_i}$ is the i-th

normalized voltage imbalance defined as follows

$$\hat{v}_{N_i} \triangleq \frac{\hat{v}_{f_i}}{\frac{V_g}{3}}. \tag{3.15}$$

For this unbalanced operation, the inductor voltages during the on-phases are given by

$$\begin{aligned} V_{on_1} =& \frac{V_g}{3}(1 - v_{N_2}) - V_o \\ V_{on_2} =& \frac{V_g}{3}(1 - v_{N_1} + v_{N_2}) - V_o \\ V_{on_3} =& \frac{V_g}{3}(1 + v_{N_1}) - V_o, \end{aligned} \tag{3.16}$$

while the inductor voltages during the off-phases are all equals to $-V_{off} = -V_o$. For the open-loop operation with ideal timing condition (i.e., $d_1 = d_2 = d_3 = D$) but with unbalanced FC voltages, using (3.16), (3.11) becomes

$$v_L = \begin{cases} \frac{V_g}{3}(1 - \hat{v}_{N_2}) - V_o & \text{when } 0 < x < D \\ -V_o & \text{when } D < x < \frac{1}{3} \\ \frac{V_g}{3}(1 + \hat{v}_{N_2} - \hat{v}_{N_1}) - V_o & \text{when } \frac{1}{3} < x < \frac{1}{3} + D \\ -V_o & \text{when } \frac{1}{3} + D < x < \frac{2}{3} \\ \frac{V_g}{3}(1 + \hat{v}_{N_1}) - V_o & \text{when } \frac{2}{3} < x < \frac{2}{3} + D \\ -V_o & \text{when } \frac{2}{3} + D < x < \frac{3}{3}. \end{cases} \tag{3.17}$$

Applying the *volt-second balance*, as in (3.12), one can immediately observe that the voltage conversion ratio equation (3.13) holds also for this unbalanced case. This is true under the given hypotheses and with equal duration of FC charging/discharging phases (i.e., $d_1 = d_2 = d_3$). Regarding the steady-state average FC currents, with reference to Fig. 3.7, one can immediately notice that for open-loop operation the following expression applies

$$I_{f_2} \triangleq \langle i_{f_2} \rangle_{T_s} = \int_{x_o}^{x_o+1} i_{f_2}(x)dx = A_{2+} - A_{2-} = \frac{M^2}{2} \frac{V_g}{3Lf_s} \hat{v}_{N_1}. \tag{3.18}$$

Similarly, for the average C_{f_1} current, one has

$$I_{f_1} \triangleq \langle i_{f_1} \rangle_{T_s} = \int_{x_o}^{x_o+1} i_{f_1}(x)dx = A_{1+} - A_{1-} = -\frac{M^2}{2}\frac{V_g}{3Lf_s}\hat{v}_{N_2}. \tag{3.19}$$

In steady-state operation, the two average FCs currents must be zero. Therefore, by imposing the steady-state condition in (3.18) and (3.19), from (3.14), one immediately obtains

$$\hat{v}_{N_1} = \hat{v}_{N_2} = 0 \implies V_{f_1} = \frac{V_g}{3} \text{ and } V_{f_2} = \frac{2}{3}V_g. \tag{3.20}$$

Thus, for the ideal open-loop operation for $d_1 = d_2 = d_3 = D = M$, the steady-state condition for the average FCs currents (i.e., $I_{f_i} = 0$) allows to uniquely obtain the average FC voltages.

In order to remark an important difference between some MLFC Buck converters, the open-loop operation of the 3-LFC Buck converter is now analysed and compared with the results obtained for the open-loop operation of the 4-LFC Buck converter.

3-LFC Buck converter operating in $mode_1$

The open-loop voltage conversion ratio under ideal timing condition (i.e., $d_1 = d_2 = D$) is [46]

$$M \triangleq \frac{V_o}{V_g} = D. \tag{3.21}$$

The expression (3.21) holds also in presence of FC voltage imbalance. Although this expression is identical to that obtained for the 4-L case, there are some rather important differences that need to be analysed between the 3-L and 4-L cases. The most important aspect concerns the average FC voltage.

The steady-state operation for the 3-L case for unbalanced FC voltage is exemplified in Fig. 3.8. By supposing to operate in open-loop with $d_1 = d_2$, the following statement is always true [47]

$$d_1 = d_2 \implies I_f = 0 \; \forall \; v_N \tag{3.22}$$

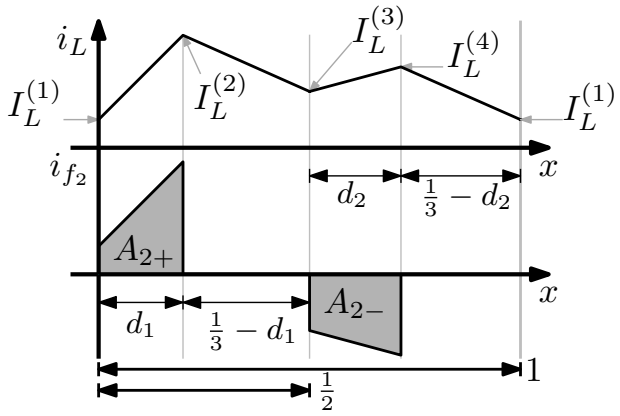


Figure 3.8: *Inductor and FC currents for the 3-LFC Buck converter.*

Therefore, under hypotheses (3.5), while in the 4-L case it is always possible to solve the steady-state, for the 3-L case this is indeterminate. In other words, whether or not the average FC voltages can be unambiguously determined with the simplified analysis obtained under hypotheses (3.5) is not guaranteed for all N-LFC Buck converters. In general, there are remarkable differences between N-LFC Buck converters with even and odd N. An in-depth discussion in this regard can be found in [48]. The next section details this issue.

3.3 Flying-capacitor Voltage Imbalance issues in N-LFC Buck converter

As anticipated at the end of the previous section, some general properties of N-LFC Buck converters are analysed in [48]. In particular, this paper highlights some remarkable differences between even and odd levels in multi-level converters. The study starts showing the *failure of the standard averaged model approach* when all control signals are ideal (i.e., no dead-times nor mismatches). Precisely, in this condition, the averaged model approach can

be summarized by following system

$$A_{avg} \cdot \begin{bmatrix} V_{f_{N-2}} \\ V_{f_{N-3}} \\ \dots \\ V_{f_1} \\ I_L \\ V_o \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \dots \\ 0 \\ \left\langle S_{N-1}^{(i)} \right\rangle_{T_s} \\ 0 \end{bmatrix} V_g \ , \tag{3.23}$$

Where the vector with N elements at the first part represents the average steady-state value of the N state-variables. For the proper definition of the matrix A_{avg} and the averaged value $\left\langle S_{N-1}^{(i)} \right\rangle_{T_s}$, please refer to [48]. The paper shows that for the *ideal timing condition*, the rank of A_{avg} is 2, so the system of equations (3.23) is underdetermined for the general N-level case with $N > 2$. Precisely, due to the structure of the matrix A_{avg}, it is possible to derive expressions in closed form for I_L and V_o, but not for V_{f_i} with $i = 1, 2, ...N - 2$. Thus, the methodology is reliably applicable to the *two-level* Buck converter case but not to the other cases where $N > 2$, since the average FC voltages remain indeterminate. In other words, the complete steady-state solution cannot be obtained with this simplified methodology.

Next, the paper verifies the effectiveness of the *augmented state-space approach* method [49] and then moves to the simplified analysis based on the assumptions of *piecewise linear inductor current* (PWLIC) approximation (i.e., hypotheses (3.5)). The methodology proposed in [49] is general and always allows to obtain the steady-state solution and this solution is verified to be unique. Unfortunately, this methodology is very complex, especially in the case of a generic number of levels. Instead, the analysis based on PWLIC

approximation is very simple and provide good insights about the converter behaviour. Under this assumption, the charge-balance equations are written as a function of peak and valley currents. For example, in the case of 3-L and 4-L the following expressions can be easily obtained [48]

$$\begin{aligned} \frac{I_L^{(1)}+I_L^{(2)}}{2} &= \frac{I_L^{(3)}+I_L^{(4)}}{2} \quad \text{for the 3-L case} \\ \frac{I_L^{(1)}+I_L^{(2)}}{2} = \frac{I_L^{(3)}+I_L^{(4)}}{2} &= \frac{I_L^{(5)}+I_L^{(4)}}{6} \quad \text{for the 4-L case ,} \end{aligned} \tag{3.24}$$

where $I_L^{(i)}$ represent the valley and peak inductor current values as defined in Fig. 3.8 and Fig. 3.7. It is pointed out that while for the 4-L case, (3.24) leads to a unique solution for the average FC voltages, that coincides with the balanced one (i.e., 3.2), for the 3-L case (3.24) leads to infinite solutions. Under the assumption of PWLIC approximation, it is therefore not possible to unambiguously solve the steady-state of the converter in case the number of levels is odd.

Starting from these two considerations a possible explanation about the reason why multi-level converters with an odd number of levels are inherently more sensitive to mismatches with respect to the multi-level converter with even number of levels can be formulated. In fact, these prove that for odd number of levels, the DC solution for FC voltages depends directly on second-order effects e.g., the impact of the output voltage ripple on the inductor current waveform, mismatches in control signals, parasitic elements in the path of I_{f_i}, etc. Instead, the steady-state solution for even multi-levels is straightforwardly held by the simple analysis in PWLIC approximation. Thus, it is logical to expect that the intrinsic sensitivity of multi-level converters with even N is lower with respect to the second-order phenomena mentioned earlier.

3.4 Advantages with respect to the traditional *two-level* Buck converter

The advantages offered by multi-level flying-capacitor Buck converter can be easily summarized by comparing it with the *two-level* Buck converter. The following comparison between the 3-LFC Buck and the traditional *two-level* (2L) Buck converters is made supposing to maintain the same input and output voltages and for the same output current and switching frequency. Both output LC filters have supposed to be equal as well. Fig. 3.9a and Fig. 3.9b show the 3-LFC Buck and the 2L Buck respectively. Fig. 3.9c shows the qualitative trend of $v_L(x)$ and $i_L(x)$. For the 3-LFC Buck, the flying-capacitor is supposed to be balanced with $V_f = \frac{V_g}{2}$. In Fig. 3.9c, for the 3-LFC Buck the inductor voltage is reduced as well as the peak-to-peak inductor current ripple with respect to the traditional Buck topology. Indeed, the switching voltages can be written as follows

$$\begin{aligned} v_{X-2L}(x) &= d_{2L}(x)V_g \\ v_X(x) &= d(x)\frac{V_g}{2}, \end{aligned} \tag{3.25}$$

whit

$$\begin{aligned} d_{2L}(x) &= \begin{cases} 1 & \text{for} \quad k < x < D + k \\ 0 & \text{elsewhere} \end{cases} \\ d(x) &= \begin{cases} 1 & \text{for} \quad \frac{h}{2} < x < D + \frac{h}{2} \\ 0 & \text{elsewhere,} \end{cases} \end{aligned} \tag{3.26}$$

where k and h are non-negative integers. Using (3.25), the inductor voltages can be written as follows

$$\begin{aligned} v_{L-2L}(x) =& v_{X-2L}(x) - V_o \\ v_L(x) =& v_X(x) - V_o. \end{aligned} \tag{3.27}$$

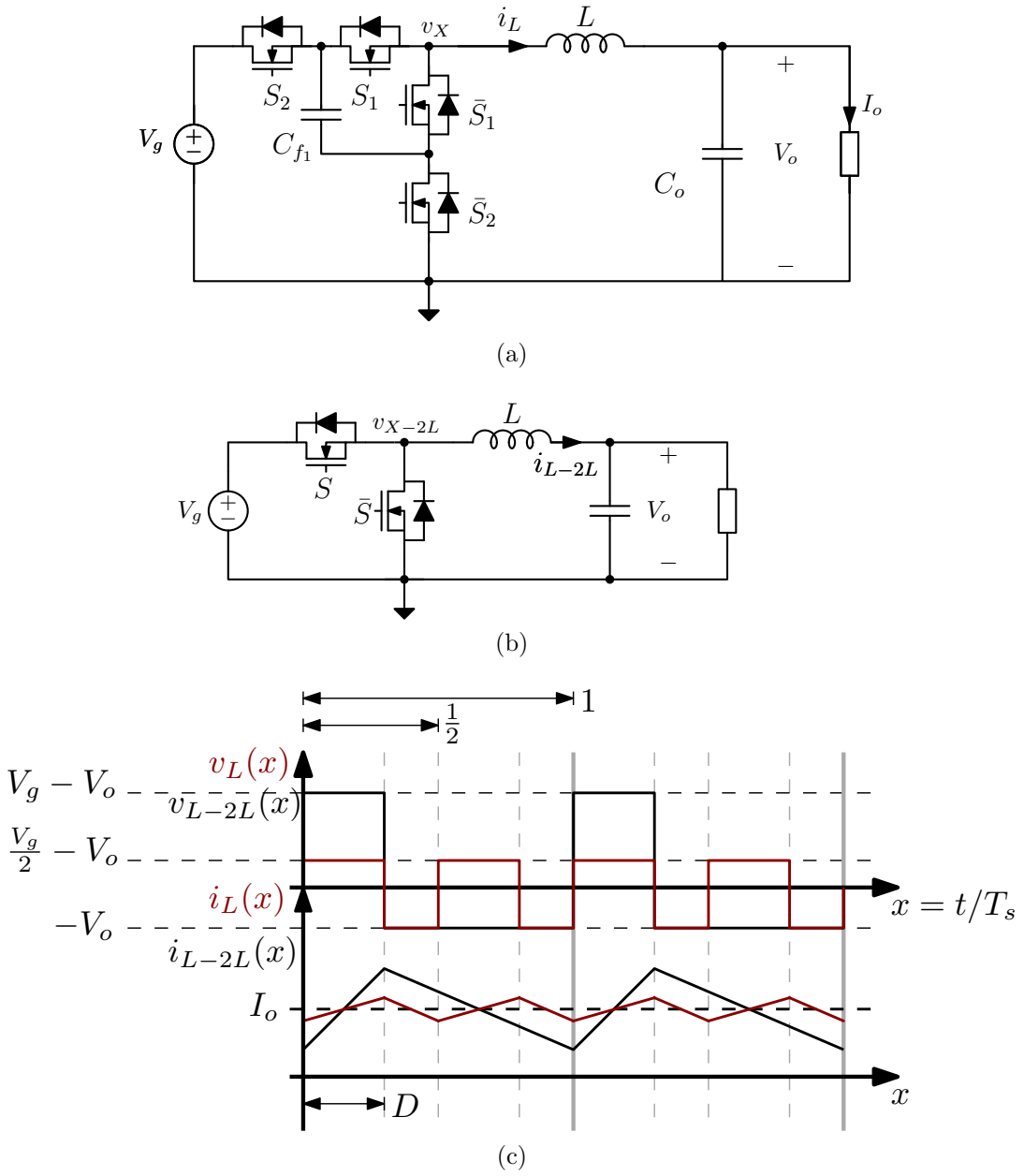


Figure 3.9: *(a) 3-LFC Buck and (b)* two-level *Buck schemes. (c) Switching node voltages and inductor currents waveforms.*

The reduced peak-to-peak inductor current ripple in the multi-level solution is due to two main factors: the first one is the reduced excursion of the voltage v_X with respect to v_{X-2L}, the second factor is the doubling of the effective switching frequency. Indeed, in (3.25) the voltage level of the switching node is halved in the 3-LFC Buck topology while the frequency of $d(x)$ in (3.26) is doubled with respect to $d_{2L}(x)$.

Assuming now that a step-down converter has to be designed, with given specifications for input and output power and for the inductor current and output voltage ripples, it is possible to replace a conventional Buck converter with a 3-LFC Buck in which both the inductor and the output capacitance are significantly reduced. To prove the above, it is necessary to first analyse the inductor current ripple Δi_L and later the output voltage ripple Δv_o as the conversion ratio M varies.

By supposing V_g constant, 3-LFC Buck inductor current ripple can be written as follows

$$\Delta i_{L-mode_1} = \frac{V_g}{2Lf_s}(1-2M)\,M \qquad \text{for} \quad 0 < M < \frac{1}{2} \tag{3.28}$$

$$\Delta i_{L-mode_2} = \frac{V_g}{2Lf_s}(2-2M)\left(M-\frac{1}{2}\right) \quad \text{for} \quad \frac{1}{2} < M < 1 \tag{3.29}$$

$$\tag{3.30}$$

The peak-to-peak inductor current ripple in (3.30) exhibits maximum values for $M = \frac{1}{4}$ and for $M = \frac{3}{4}$:

$$\begin{aligned} \Delta i_{L-mode_1}\Big|_{M=\frac{1}{4}} &= \frac{V_g}{16Lf_s} \\ \Delta i_{L-mode_2}\Big|_{M=\frac{3}{4}} &= \frac{V_g}{16Lf_s} \end{aligned} \tag{3.31}$$

Fig. 3.10 shows a comparison between the normalized inductor current ripple for the 3-LFC Buck and the traditional *two-level* Buck. $k_g = \frac{V_g}{Lf_s}$ is used as normalization constant.

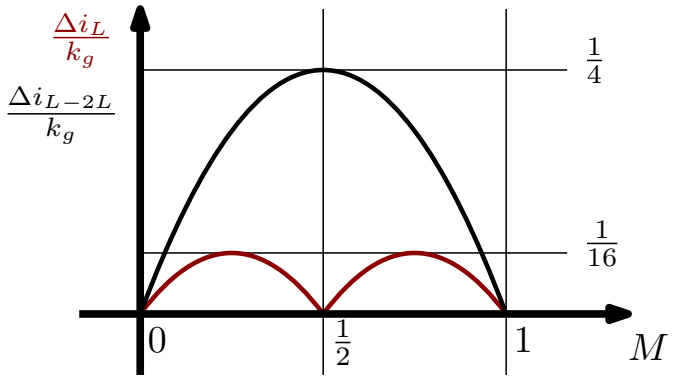


Figure 3.10: *Peak-to-peak inductor current ripple trends VS voltage conversion ratio M for* two-level *Buck (black line) and for 3-LFC Buck (dark red line).*

If the given specification for the current ripple is on the form $\frac{\Delta i_L}{I_o} < y\%$ the inductor size reduction can be easily deduced. By supposing that $0 < M < \frac{1}{2}$, the values of L_{min} for the two step-down topologies can be written as follows

$$\begin{aligned} L_{2L} > L_{min-2L} &= \frac{V_g}{f_s I_o y\%} (1 - M) M \\ L > L_{min} &= \frac{V_g}{2 f_s I_o y\%} (1 - 2M) M \end{aligned} \tag{3.32}$$

The resulting ratio between the two minimum-size inductors is a function of M. Indeed, for both operating modes of the 3-LFC Buck converter one has

$$\frac{L_{min}}{L_{min-2L}} = \begin{cases} \dfrac{1-2M}{2-2M} & \text{for} \quad 0 < M < \dfrac{1}{2} \\ \dfrac{2M-1}{2M} & \text{for} \quad \dfrac{1}{2} < M < 1 \, . \end{cases} \tag{3.33}$$

As shown on Fig. 3.11, both expressions in (3.33) are less than 0.5. In this example, where V_g is supposed constant, it is shown how the multilevel solution is able to guarantee the same specifications on the $\Delta i_L / I_o$ with an inductor at least two times smaller with respect to the traditional *two-level* solution. If the conversion ratio is limited from a minimum to a maximum

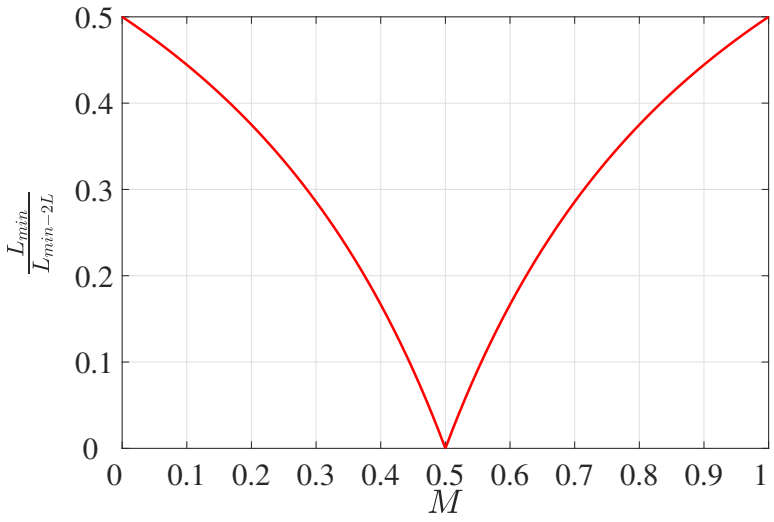


Figure 3.11: $\frac{L_{min}}{L_{min-2L}}$ *VS the voltage conversion ratio* M.

value, due to requirements for a given application, the possibilities of inductor reduction would increase. For example, if the voltage conversion ratio is limited in the range $(0.25, 0.75)$ one could use an inductor three times smaller in the 3L case, with respect to the 2L case, while maintaining the required specifications on Δi_L. Since the inductor is the bulkiest element, being able to operate with one that is significantly smaller for the same given specifications allows a significant reduction in the overall converter footprint.

The output capacitance can also be significantly reduced maintaining unchanged the output voltage ripple specification. Fig. 3.12 shows the output capacitance current and the output voltage for the two topologies. The calculation of the output voltage ripple can be done by evaluating areas of triangles A and A_{2L} in Fig. 3.12

$$\begin{aligned}\Delta v_{o-2L} =& \frac{1}{2C_o}\frac{(t_{on-2L}+t_{off-2L})}{2}\frac{\Delta i_{L-2L}}{2} = \frac{\Delta i_{L-2L}}{8f_sC_o} = \frac{V_g}{8C_oLf_s^2}(1-M)M \\ \Delta v_o =& \frac{1}{2C_o}\frac{(t_{on}+t_{off})}{2}\frac{\Delta i_L}{2} = \frac{\Delta i_L}{16f_sC_o} = \frac{V_g}{32C_oLf_s^2}(1-2M)M\end{aligned} \tag{3.34}$$

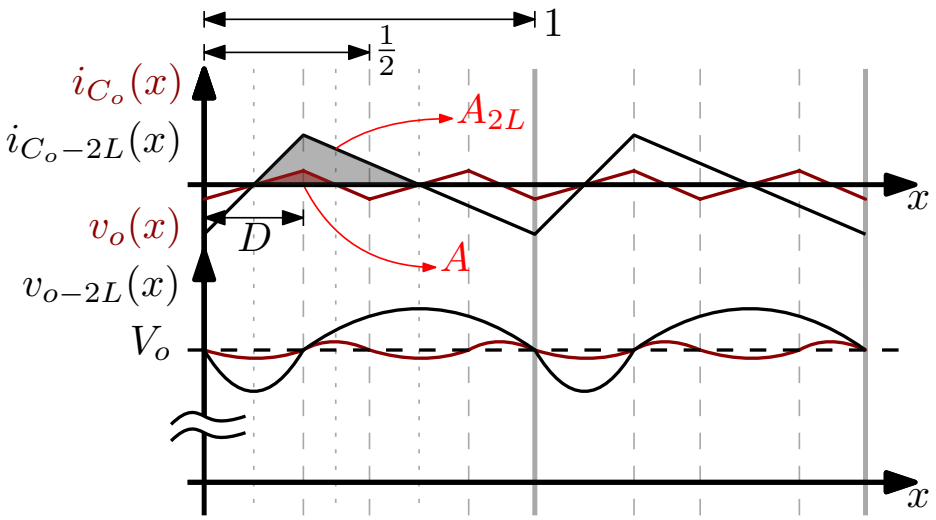


Figure 3.12: *Inductor currents and output voltages waveforms for the 3-LFC Buck (dark red lines) and* two-level *Buck (black lines).*

In (3.34) expression for operating $mode_1$ is used for the calculation of Δv_o however, the final results are also valid for operating $mode_2$. Expressions (3.34) show that maintaining unchanged the given specification for the output voltage ripple, the output capacitance C_o can be reduced at least by a factor four with respect to the traditional *two-level* Buck topology.

Another remarkable advantage given by the 3-LFC Buck converter is the reduced voltage stress for the power switches. With reference to Fig. 3.9a is easy to show that the voltage across the power switches during their off-time is $\frac{V_g}{2}$ for the multi-level solution, while is V_g for the classic solution. Therefore, the voltage stresses for the power switches are halved in the multi-level solution.

In the example aforementioned, a 3-LFC Buck converter is used in the comparison with the traditional *two-level* solution. However, the advantages offered by multilevel topologies can be easily extended to the general case of Buck N-LFC converter operating in $mode_i$, $i = 1, 2, ..N-1$. Precisely, for the generic N-LFC Buck converter operating in $mode_i$, the inductor current

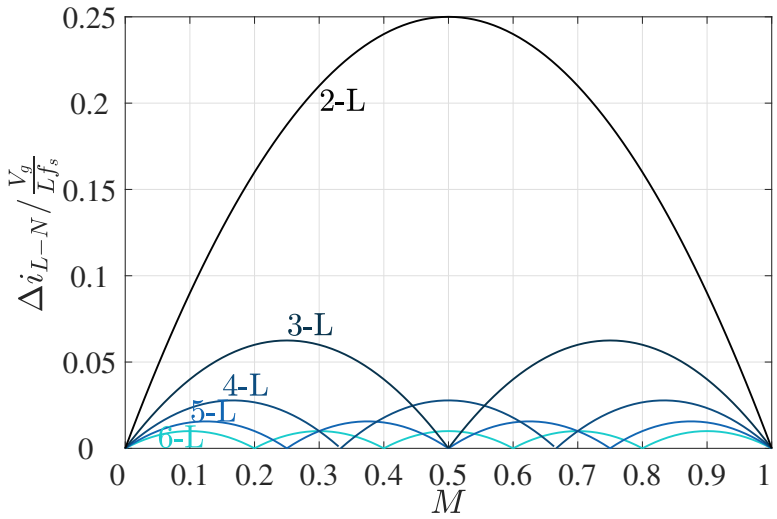


Figure 3.13: $\Delta i_{L-N}/\frac{V_g}{f_s L}$ *VS voltage conversion ratio* M*, for* $N = 2, 3, 4, 5, 6$.

can be generalized as follows

$$\boxed{\Delta i_{L-N} = \frac{V_g}{Lf_s}\left(\frac{i}{N-1} - M\right)\left(M - \frac{i-1}{N-1}\right), \quad i = 1...N-1}. \tag{3.35}$$

Fig. 3.13 shows plots of the function (3.35), normalized with respect to the quantity $\frac{V_g}{Lf_s}$, versus the voltage conversion ratio M for $N = 2, 3, 4, 5, 6$. This figure clearly shows how as the number of levels increases the inductor current ripple decreases. It is also immediate to observe how the number of the points in which the current ripple is zero increase as the number of levels increase. Proper functioning for these operation points requires special consideration and modification of control and/or modulation strategies. This thesis does not address operation at these particular operating points.

Using (3.35), the corresponding ratio of (3.33) can be easily deduced. For the generic N-LFC Buck converter this ratio is always greater than $(N-1)$. Therefore, using the approach followed in this section, and starting from (3.35), the advantages given by the generic N-LFC Buck converter with respect to the traditional *two-level* solution can be summarized as in the following list

- The inductor value can be reduced (at least) by a factor $N-1$
- The output capacitor can be reduced by a factor $(N-1)^2$
- The effective frequency for the output LC filter is $N-1$ the switching frequency
- The voltage stresses for the power switches are reduced by a factor $N-1$
- The reduction in the converter footprint allows a significant cost reduction
- The reduction in the values of both element of the output LC filter plus the equivalent frequency multiplication effect allow a faster dynamic response to a load step changes.

The above advantages are guaranteed as long as the multi-level converter operates with stable and balanced FCs and as long as the voltage conversion ratio is not an integer multiple of the quantity $\frac{1}{N-1}$. Furthermore, in multi-level converters, a start-up must be foreseen in order to bring the FCs voltage values close to the equilibrium avoiding voltage over-stresses on the active components. Unlike the other issues mentioned above, it is extremely difficult to generalize the extension of the control techniques used for *two-level* Buck to the general N-level case. Indeed, the least trivial issue to address and generalize concerns the FC voltages balance and stability and their interaction with the control strategies. In the next chapter, the *peak* DPCMC is applied to the 3-LFC Buck converter, highlighting which problems can arise in the interaction between the inductor current control and the FC voltage.

Chapter 4

Peak DPCMC for 3-LFC Buck converter

In this chapter is discussed the application of the digital predictive current-mode control to the 3-LFC Buck converter. The digital-predictive technique was initially used for average load current control in dc-ac application, [28]. [37] discusses its extension to the most common dc-dc converter topologies. As discussed in the previous chapter, the interaction between control technique and FC voltages can generally leads to unbalancing and/or stability issues. For this reason, the application of the DPCMC has to be analysed, with particular attention to the FC voltages dynamics. In this chapter, a 3-LFC Buck with a single-sampled *peak* DPCMC with a LE carrier based DPWM is firstly analysed. Next, two techniques for FC stability are proposed and discussed. The first methodology is rather simple but not always exhaustive, while the second approach allows for more accurate FC voltage stability analysis and always provides comprehensive results. After the proposed FC voltage stability analysis techniques, other two digital predictive controllers are presented. For both, the speed of corrective action on the inductor current error is increased with respect to the single-sampled approach, allowing a design of a faster outer control-loop. All three techniques will be validated in simulation and experimentally on a custom prototype.

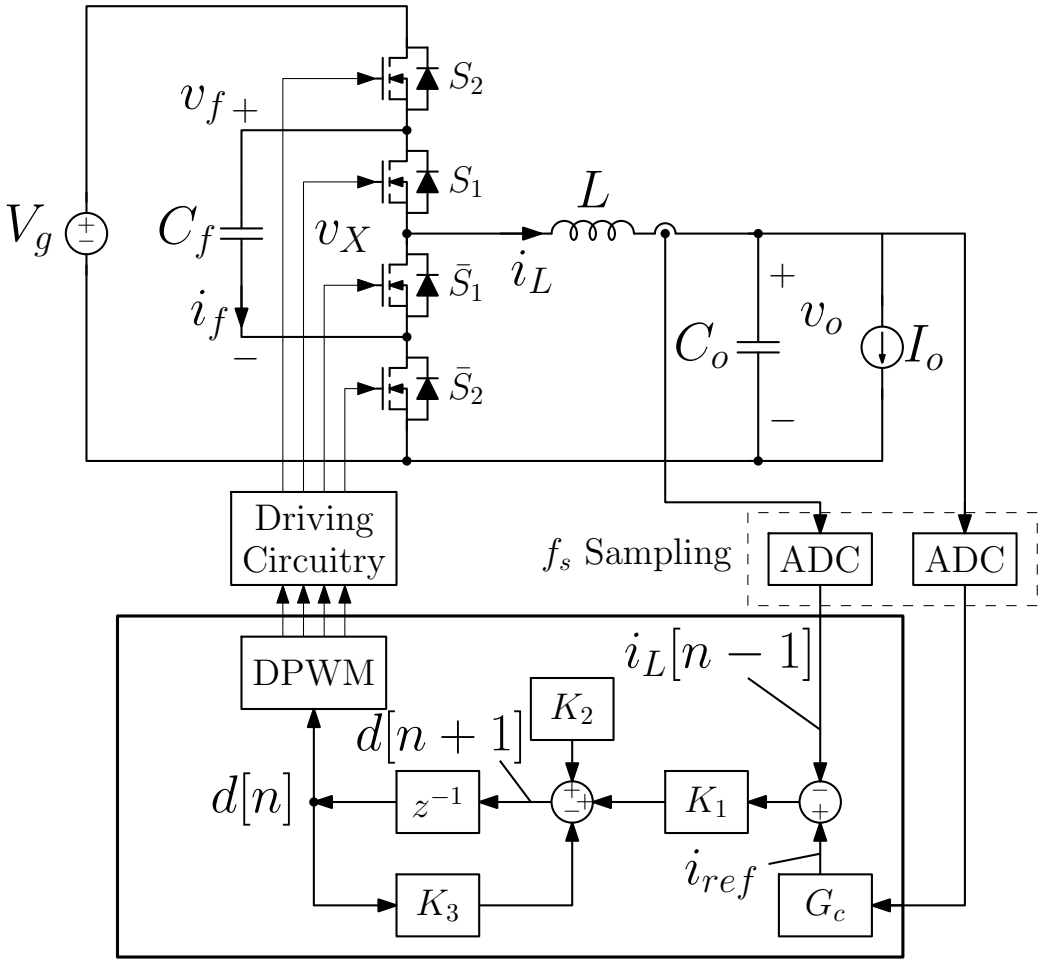


Figure 4.1: *Generic block diagram of a 3-LFC Buck converter with a single-sampled digital predictive current-mode controller.*

The content of this chapter is featured for the most part in [47, 50].

4.1 Single-Sampled DPCMC

The 3-LFC Buck converter circuit with single-sampled DPCMC block diagram is illustrated in Fig. 4.1. Expressions of coefficients K_1, K_2 and K_3 depend on the specific type of DPCMC (i.e., whether *peak*, *valley* or *average* current control is considered). For this single-sampled implementation, the sampling frequency is equal to the switching rate f_s.

Operation of single-sampled *peak* DPCMC with LE carrier based DPWM is illustrated in Fig. 4.2. The DPWM operation could be deduced from the general case of PSMC-DWPM discussed in subsection 3.2.1 for $N = 3$. However, in order to simplify the treatment, an equivalent simpler structure with a single carrier with frequency $2f_s$ and amplitude $1/2$ is used in this example. This DPWM implementation, for $M < 1/2$ is completely equivalent to the most general case discussed above. For $M > 1/2$ the same structure can be used in order to derive the signal $\overline{S}_1$ and $\overline{S}_2$. The equivalence is exemplified in Fig. 4.3. Please note that for $M < 1/2$ signal S_1 and S_2 are obtained from the comparison with the carrier signal CS while $\overline{S}_1$ and $\overline{S}_2$ are their logic negated version. Instead, for $M > 1/2$, signal $\overline{S}_1$ and $\overline{S}_2$ are obtained from the comparison with the carrier signal $\overline{CS}$ while S_1 and S_2 are their logic negated version.

From the top to the bottom, Fig. 4.2 sketches the modulating signal along with the LE carriers, the DPWM commands for switches S_1 and S_2, the switching node voltage v_X, the inductor current i_L and the flying-capacitor current i_f. Since no dead-times are here considered, $\overline{S}_1$ and $\overline{S}_2$ are the negated logic version of S_1 and S_2. The time-axis is normalized with respect to the switching period T_s. The figure exemplifies how an initial perturbation of the inductor current peak value, $\Delta i_L[n-1] \triangleq i_L[n-1] - I_{ref}$, is corrected according to the predictive control equation. Continuous gray lines indicate steady-state operation, continues black lines indicate the operation during the inductor current error correction, while red arrows indicate the time-position adjustment of S_1 and S_2 leading edges. In Fig. 4.2 one can see that there is only one sampling/update per switching cycle. For this reason and to distinguish it from the other implementations discussed later, this control strategy is called *single-sampled* DPCMC.

The stability analysis regarding the FC is discussed later, here its average voltage is supposed to be stable and balanced (i.e., (3.2) holds), while its voltage ripple is small enough to be neglected. Therefore, assuming $V_f = V_g/2$, the general expression of $i_L[n+1]$ of the inductor current at the controlling

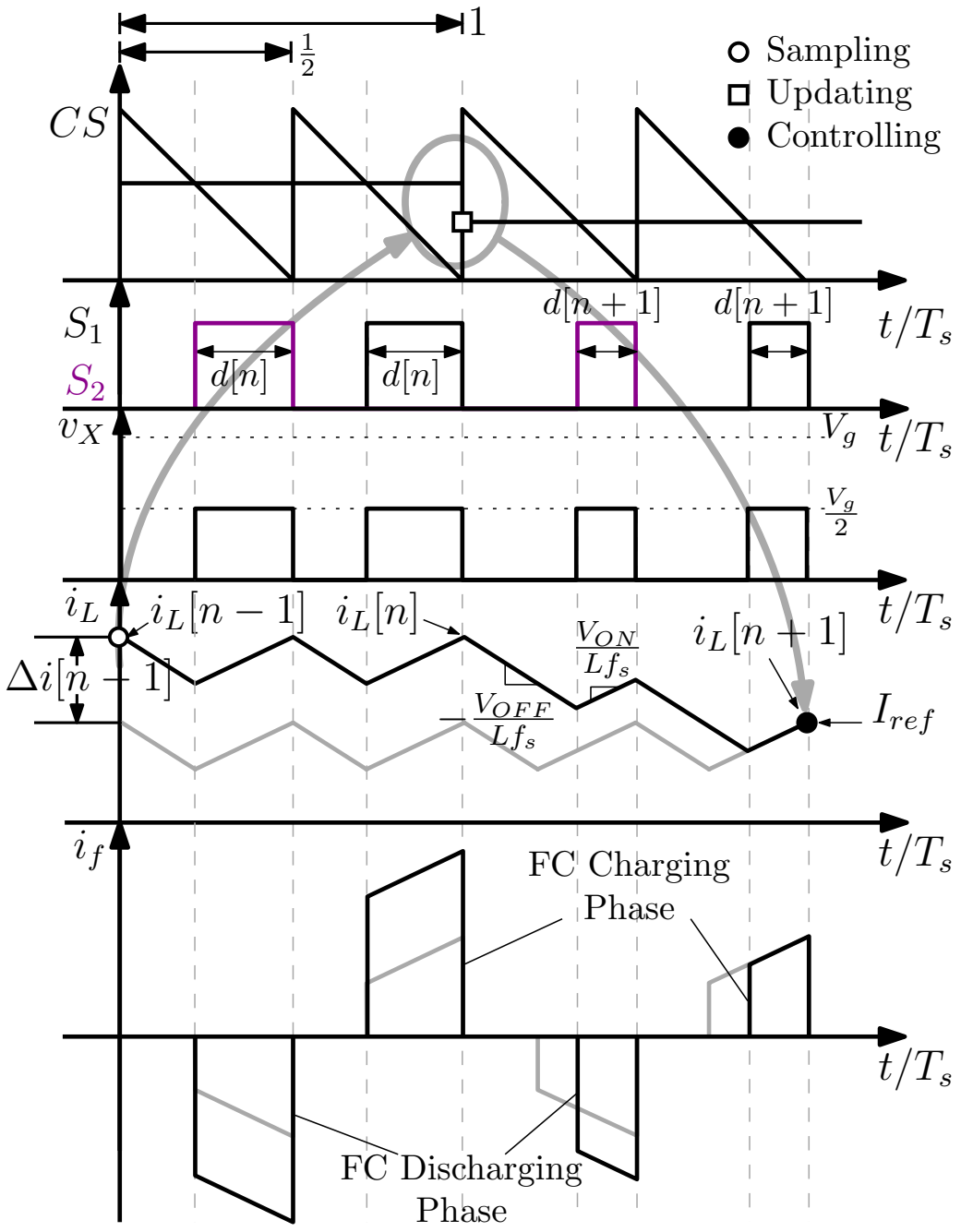


Figure 4.2: *Operation of the single-sampled* peak *DPCMC controller with a LE carrier for* $M < 0.5$.

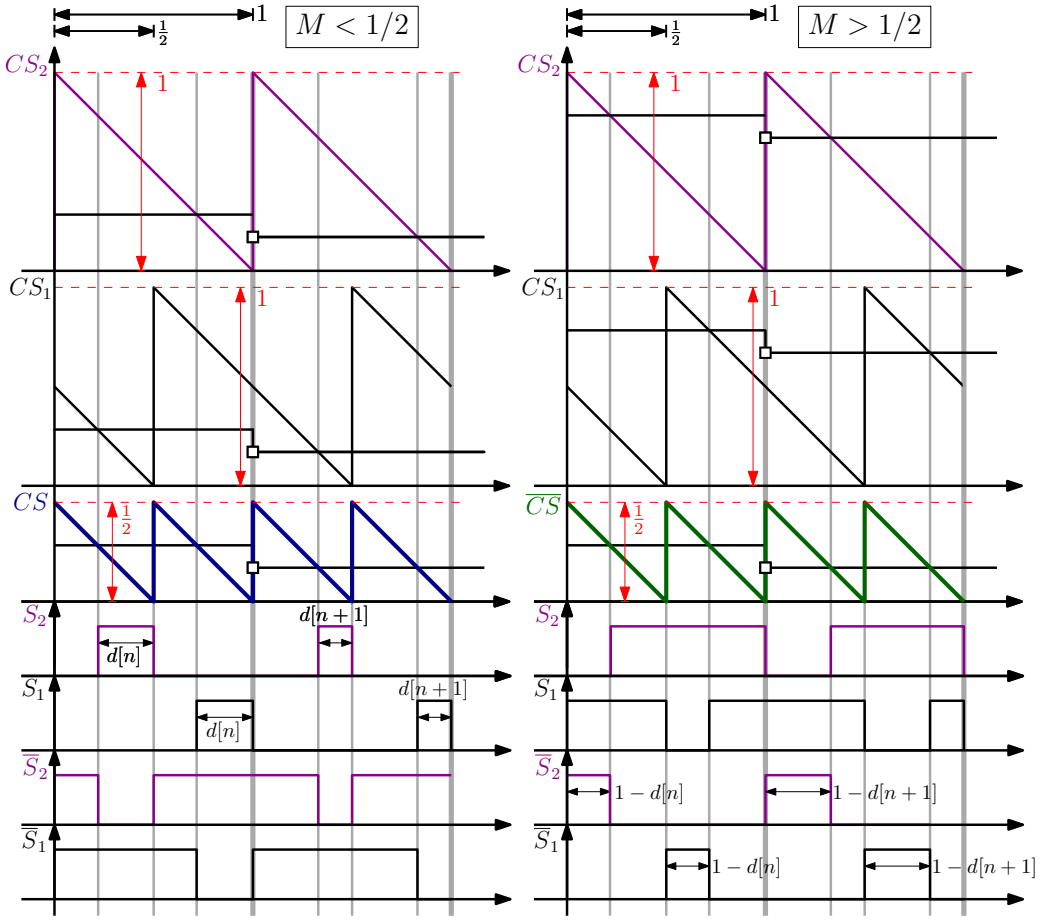


Figure 4.3: *Equivalent operation behaviour of the two considered implementation of the LE carrier based DPWM for the single-sampled* peak *DPCMC controller for* $M < 1/2$ *(on left) and* $M > 1/2$ *(on right).*

point can be written in terms of the sampled current $i_L[n-1]$, the inductor current slopes and the two duty cycles $d[n]$ and $d[n+1]$,

$$\begin{aligned} i_L[n+1] =& i_L[n-1] - \frac{V_{OFF}}{f_s L}\left(1-2d[n]\right) + 2\frac{V_{ON}}{f_s L}d[n] + \\ &- \frac{V_{OFF}}{f_s L}(1-2d[n+1]) + 2\frac{V_{ON}}{f_s L}d[n+1], \end{aligned} \tag{4.1}$$

where V_{ON} and V_{OFF} are the voltages across the inductor during the on and the off-phases respectively.

Assuming, for the time being, that the voltage conversion ratio M is less

than 0.5 (i.e., the 3-LFC Buck converter operates in $mode_1$), one has

$$\begin{aligned} V_{ON} &= \frac{V_g}{2} - V_o = \frac{V_g}{2}\left(1 - 2M\right), \\ V_{OFF} &= V_o = MV_g \end{aligned} \tag{4.2}$$

From (4.1), by imposing that the new duty cycle $d[n+1]$ makes the peak current $i_L[n+1]$ equal to I_{ref}, one solves for $d[n+1]$ and obtains the control equation

$$d[n+1] = \frac{f_s L}{V_g}\left(I_{ref} - i_L[n-1]\right) + 2M - d[n]. \tag{4.3}$$

For $M > 0.5$ (i.e., the 3-LFC Buck converter operates in $mode_2$), one has

$$\begin{aligned} i_L[n+1] =& i_L[n-1] - \frac{V_{OFF}}{f_s L}\left(2 - 2d[n]\right) + \left(2d[n] - 1\right)\frac{V_{ON}}{f_s L} + \\ &- \frac{V_{OFF}}{f_s L}\left(2 - 2d[n+1]\right) + \left(2d[n+1] - 1\right)\frac{V_{ON}}{f_s L}, \end{aligned} \tag{4.4}$$

with

$$\begin{aligned} V_{ON} &= V_g - V_o = \frac{V_g}{2}\left(2 - 2M\right), \\ V_{OFF} &= \frac{V_g}{2} - V_o = \frac{V_g}{2}(1 - 2M). \end{aligned} \tag{4.5}$$

Now, from (4.4), by imposing that the new duty cycle $d[n+1]$ makes the peak current $i_L[n+1]$ equal to I_{ref}, one solves for $d[n+1]$ and obtains the same control equation as 4.3. The coefficient in Fig. 4.1 can be now deduced from 4.3, precisely for *peak* DPCMC one has $K_1 = f_s L/V_g$, $K_2 = 2M$ and $K_3 = 1$.

4.2 Carrier selection and bead-beat behaviour

As discussed in Chapter 2, in order to assess the static stability of the inductor current, it is necessary to evaluate the time-domain evolution of the discrete sequence $\Delta i[k]$ with respect to a perturbation on the steady-state operation. This time-evolution behaviour changes as the implementation of

the DPWM modulator changes. In order to better illustrate this concept, one must first distinguish between the inductor current error *at the sampling point* and *at the control point*. As discussed in 2.2.3, only some combinations between carriers, and therefore sampling point, and controllers, lead to stable and/or dead-beat operation. In fact, while the error at the controlling point can be *always* recovered with a suitable control equation, the error at the sampling point depends on the evolution of the current throughout the remaining period. Therefore, if these two errors coincide the cancellation of the error at the control point also implies cancellation at the sampling point, otherwise, the error at the sampling point is always non-zero and the resulting control strategy may have static stability problems.

Fig. 4.4 shows three examples of *peak* single-sampled DPCMC obtained for three different implementations of the modulator. In the first example, which is shown in Fig. 4.4a, the DPWM is implemented with a LE carrier, as in Fig. 4.2. The time-distance between the sampling and the controlling point is constant and equal to $2T_s$. The error at the controlling point coincides with the error at the sampling point. In this case, the application of an appropriate control equation (i.e., (4.3)) leads to a total recovery of the two errors in two consecutive switching cycles after the sampling instant. In Fig. 4.4a, the current perturbation at the end of the $n+1$ cycle can be generally written as

$$\Delta i[n+1] = \Delta i[n-1] + \frac{2d[n+1]}{f_s L}(V_{OFF} + V_{ON}) - \frac{V_{OFF}}{f_s L}. \tag{4.6}$$

By replacing $d[n+1]$ with (4.3) one obtains

$$\frac{\Delta i[n+1]}{\Delta i[n-1]} = 0. \tag{4.7}$$

The current error $\Delta i[n+1]$ is zero independently of the value $\Delta i[n-1]$ and of the operating point. Such result, which holds also for $M > 1/2$, confirms the static stability of the inductor current and that, as expected, the peak value of the inductor current is regulated in a dead-beat fashion. As mentioned in Chapter 2 and as is now illustrated, this property is only guaranteed for

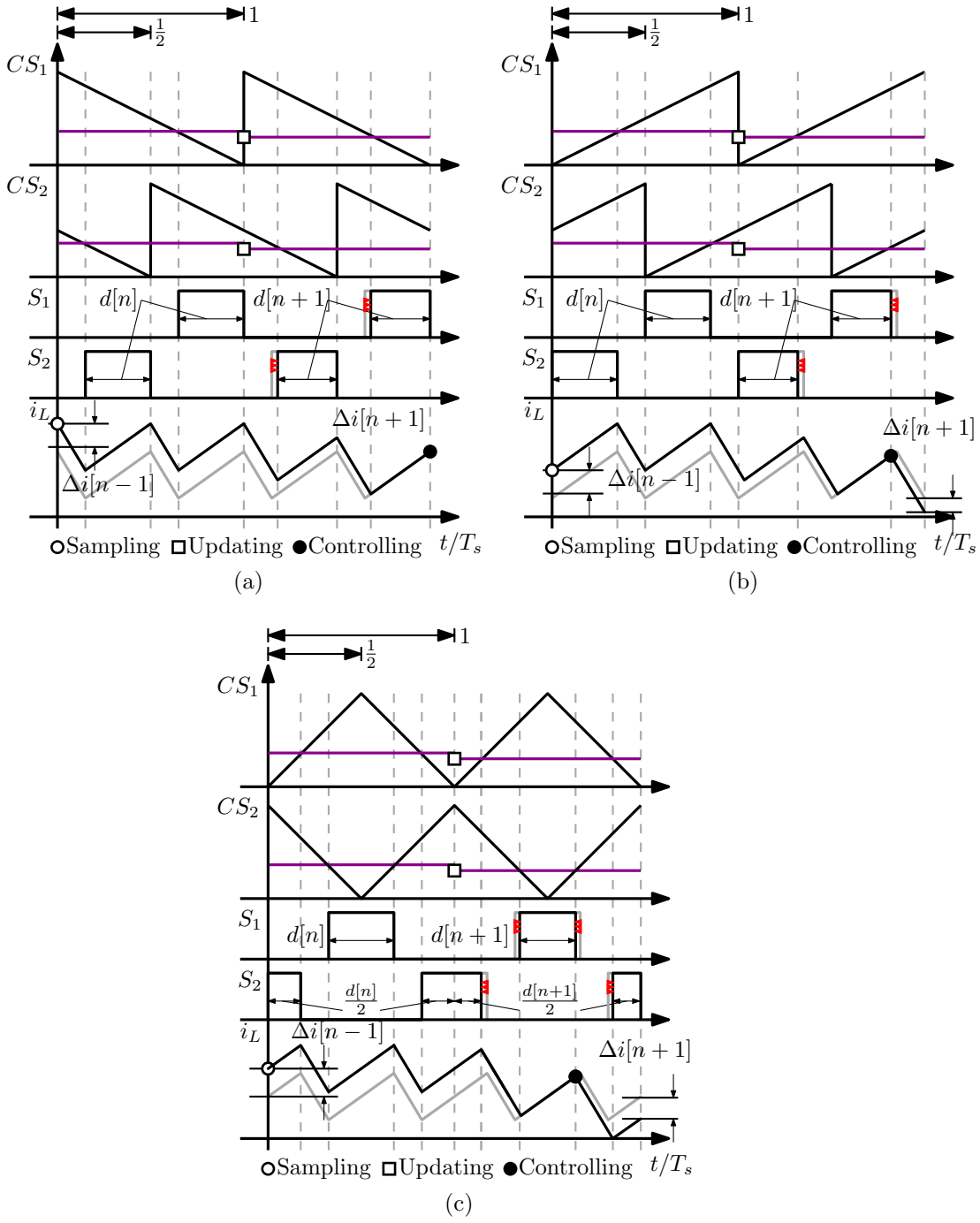


Figure 4.4: *Corrective actions of the sampled inductor current error at the controlling point in 3-LFC Buck converter with* peak *single-sampled DPCMC for: (a) LE carrier based DPWM, TE carrier based DPWM, TTE carrier based DPWM.*

certain pairings of DPWM carriers and control strategies. The following two examples clarify what has just been stated.

Fig. 4.4b shows an implementation of the *peak* single-sampled DPCMC with a TE carrier based DPWM. In this case the control equation (4.3) has to be changed with the following ones

$$d[n+1] = \begin{cases} \dfrac{Lf_s}{V_g}\dfrac{I_{ref} - i_L[n-1]}{1-M} + \dfrac{3/2M}{1-M} - \dfrac{d[n]}{1-M} & \text{for } \; 0 < M < \dfrac{1}{2} \\ \dfrac{Lf_s}{V_g}\dfrac{I_{ref} - i_L[n-1]}{\frac{3}{2}-M} + \dfrac{\frac{1}{2}+M}{\frac{3}{2}-M} - \dfrac{d[n]}{\frac{3}{2}-M} & \text{for } \; \dfrac{1}{2} < M < 1 \; . \end{cases} \tag{4.8}$$

Unlike dead-beat DPCMC cases where the control point coincides with the sampling point, all other pairings of carriers and controls lead to control equations that change depending on the operating mode. For instance, the control equation (4.8) changes from $mode_1$ (i.e., $0 < M < 1/2$) and $mode_2$ (i.e., $1/2 < M < 1$). Therefore, the current stability properties can be expected to depend on the operating mode. In fact, following the discussed methodology for the inductor current static stability analysis, for the single sampling *peak* DPCMC with TE carrier based DPWM, one has

$$\frac{\Delta i[n+1]}{\Delta i[n-1]} = \begin{cases} \dfrac{M}{1-M} & \text{for } \; 0 < M < \dfrac{1}{2} \\ \dfrac{M-1}{\frac{3}{2}-M} & \text{for } \; \dfrac{1}{2} < M < 1 \; . \end{cases} \tag{4.9}$$

Thus, this control strategy needs two different control equations for the two operating modes. For both, the controller is not dead-beat. In fact, although the error at the controlling point is exhausted at the next cycle after the sampling one, the error at the sampling point is not immediately recovered. More switching cycles are required so that the error at the sampling point is also recovered. Moreover, the current-error correction is asymptotic and depends on the operating point. The situation is represented in Fig. 4.4b, where the current error at the control point is zero while the current error at the sampling point is not. The time evolution at the sampling point follows

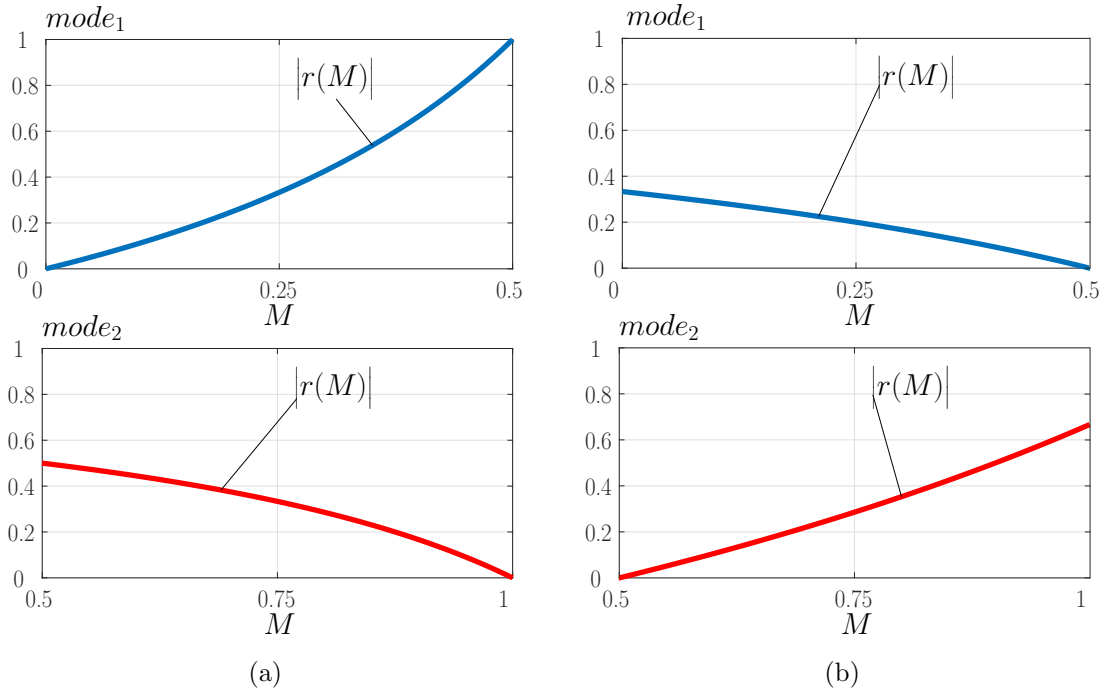


Figure 4.5: *Absolute value of the inductor current errors ratio* $|r(M)| = \left|\frac{\Delta i[n+1]}{\Delta i[n-1]}\right|$ *for the* peak *DPCMC with TE based DPWM (a) and with TTE based DPWM (b) VS voltage conversion ratio* M *for operating* $mode_1$ *(on top) and operating* $mode_2$ *(on bottom).*

(4.9). In both operating modes, the control does not lead to static instabilities in the current since the two ratios, in modulus, are always less than one, as sketched in Fig. 4.5a.

Fig. 4.4c shows an implementation of the *peak* single-sampled DPCMC with a TTE carrier based DPWM. For this control strategy the control equation is

$$d[n+1] = \begin{cases} \dfrac{2Lf_s}{V_g}\dfrac{I_{ref} - i_L[n-1]}{\frac{3}{2} - M} + \dfrac{3M}{\frac{3}{2} - M} - \dfrac{2d[n]}{\frac{3}{2} - M} & \text{for } \; 0 < M < \dfrac{1}{2} \\ \dfrac{2Lf_s}{V_g}\dfrac{I_{ref} - i_L[n-1]}{\frac{5}{2} - M} + \dfrac{\frac{1}{2} + 3M}{\frac{5}{2} - M} - \dfrac{d[n]}{\frac{5}{2} - M} & \text{for } \; \dfrac{1}{2} < M < 1 \, . \end{cases} \tag{4.10}$$

The time evolution of the inductor current errors at the sampling point can

be described by the following equations

$$\frac{\Delta i[n+1]}{\Delta i[n-1]} = \begin{cases} -\dfrac{1-2M}{3-2M} & \text{for } \ 0 < M < \dfrac{1}{2} \\ -\dfrac{2M-1}{5-2M} & \text{for } \ \dfrac{1}{2} < M < 1 \ . \end{cases} \tag{4.11}$$

Differently from the *two-level* Buck converter with *peak* DPCMC implemented with a TTE based DPWM, this control strategy applied to the 3-LFC Buck converter does not lead to static instability issues on the inductor current. Plots of the absolute values of (4.11) are sketched in Fig. 4.5b.

4.3 Flying-capacitor voltage stability analysis

The stability of the FC voltage is crucial for the correct operation of the 3LFC Buck converter and must be verified by means of an *ad-hoc* analysis [46–48, 50–53]. The first approach proposed in this section, based on the small-ripple approximation (SRA) for both the flying-capacitor and output voltages, predicts *marginal* stability for the FC voltage of all single-sampled predictive controllers. The SRA assumption does not therefore allow to assess the actual stability character of this single-sampled based digital-predictive controller. Failure of such simplified approach justifies the use of a CAD-assisted analysis, which predicts asymptotic stability of the FC voltage. In addition, this proposed simplified analysis will prove to be comprehensive for many case studies encountered later. Before delving into a detailed explanation of the two proposed methodologies, the next section clarifies some key aspects of the chosen approach and justifies its use.

4.3.1 Proposed methodology for FC voltage stability analysis

Both FC voltage stability-study approaches proposed in this thesis i.e., the SRA based analysis or the more accurate one that includes the output voltage ripple, are based on a *quasi-stationary approximation* of the FC current.

The instantaneous and the average FC currents[1] [31] can be generally written as

$$i_f(t) = C_f \frac{dv_f(t)}{dt} \quad \rightarrow \quad \langle i_f(t) \rangle_{T_\mathrm{s}} = C_f \frac{d \langle v_f(t) \rangle_{T_\mathrm{s}}}{dt}. \tag{4.12}$$

The average FC current can be rewritten using the normalized time-notation introduced in the previous sections

$$\langle i_f(xT_\mathrm{s}) \rangle_{T_\mathrm{s}} = C_f \frac{d\left(\frac{V_g}{2} + \hat{v}_f(xT_\mathrm{s})\right)}{dxT_\mathrm{s}} \implies \langle i_f(x) \rangle_1 = C_f f_s \frac{V_g}{2} \frac{d\hat{v}_N(x)}{dx}, \tag{4.13}$$

where $\hat{v}_N(x)$ is the normalized average FC voltage imbalance defined as

$$\hat{v}_N(x) \triangleq \frac{v_f(x)}{\frac{V_g}{2}}. \tag{4.14}$$

In order to obtain a simpler analysis strategy, the stability study approach, proposed in this thesis, uses the simplifying assumption summarized as follows. The flying-capacitor C_f is substituted by an ideal voltage source, with value $V_f = \frac{V_g}{2}(1 + \hat{v}_N)$. The steady-state of the converter obtained with this ideal voltage source is analysed and the average FC current I_f is calculated as a function of the normalized average voltage perturbation $\hat{v}_N$. The

[1] For the generic signal $u(t)$ the moving average operator $\langle \cdot \rangle_T$ is defined as

$$\langle u(t) \rangle_T \triangleq \frac{1}{T} \int_{t-\frac{T}{2}}^{t+\frac{T}{2}} u(\tau) d\tau \, .$$

simplification is made when I_f is used in (4.13) instead of $\langle i_f(x)\rangle_1$.

This assumption is legitimate under SRA hypothesis and in the case where the inductor current dynamics is much faster than the FC voltage one. Therefore, it is assumed that the cycle-by-cycle current integration effect due to the FC and the consequent change in its average voltage is slow enough to be considered *practically* negligible for many switching cycles. This *snapshot* is considered *close* to the steady-state operation obtained with the 3-LFC Buck converter where the FC is replaced by an ideal voltage source with value equal to the average FC voltage of the original circuit. This is clearly a simplified scenario. However, this approach finds its ultimate justification in the veracity of the results obtained both in simulation and experimentally.

In the considered scenario, one therefore has

$$\langle i_f\rangle_1 = C_f f_s \frac{V_g}{2}\frac{d\hat{v}_N}{dx} \approx I_f \tag{4.15}$$

Now the analysis is continued around the operating point whose stability is to be verified (i.e., $\hat{v}_N \to 0$). Therefore, for small values of the normalized average FC voltage perturbation, the average FC current can be approximate around using the Taylor-series formula, arrested at the first term

$$I_f \approx I_f\Big|_{\hat{v}_N=0} + \hat{v}_N \frac{dI_f}{d\hat{v}_N}\Big|_{\hat{v}_N=0}. \tag{4.16}$$

The term $I_f\big|_{\hat{v}_N=0}$ is always zero and therefore (4.16) can be written in the following, more general, form

$$\frac{d\hat{v}_N}{dx} \approx \omega\ \hat{v}_N, \tag{4.17}$$

where $\omega \in \mathbb{R}$ is the system's eigenvalue that depends on the converter parameters and the operating point. This is a homogeneous first order differential equation. Its general integral can be written as follows

$$\hat{v}_N(x) = e^{\,\omega\, x}. \tag{4.18}$$

Thus, if the constant ω is positive the function $e^{\omega x}$ diverges for x increasing. Instead, if ω is negative $\hat{v}_N$ will asymptotically converge to zero for x increasing.

4.3.2 Failure of the small-ripple approximation method

Assume that the FC voltage is initially unbalanced, i.e., $V_f = \frac{V_g}{2} + \hat{v}_f = \frac{V_g}{2}(1 + \hat{v}_N)$. The switching node, the FC current and the inductor current in such hypothetical unbalanced steady-state condition are shown in Fig. 4.6. Notice that the switching node no longer swings between 0 and $V_g/2$, and that the inductor current waveform has a period equal to T_s.

Using the assumptions (3.5), stability of the FC voltage is determined by the sign of the average FC current I_f being *discordant* with respect to the sign of the FC voltage perturbation $\hat{v}_N$, i.e., a positive $\hat{v}_N$ should induce a *discharge* of the flying capacitor, and vice-versa. Small-signal wise, this means that FC voltage stability is characterized by a *negative* value of the (normalized) quantity[2]

$$\lambda \triangleq \left.\frac{\partial \tilde{I}_f}{\partial \hat{v}_N}\right|_{\hat{v}_N=0}, \tag{4.19}$$

with

$$\tilde{I}_f \triangleq \frac{2R_o}{V_g} I_f \qquad \left(R_o \triangleq \frac{V_o}{I_o}\right). \tag{4.20}$$

For the 3LFC Buck, the voltage conversion ratio can be written, in general, as

$$M \triangleq \frac{V_o}{V_g} = \frac{D_1 + D_2}{2} + \frac{\hat{v}_N}{2}(D_2 - D_1), \tag{4.21}$$

where D_1 and D_2 are the duty cycles associated with the charging and discharging phases respectively, as illustrated in Fig. 4.6. Since the single-

[2]In this section and in general for the study of FC voltage stability properties for 3-LFC Buck converter, the parameter λ defined by (4.19) is used instead of the eigenvalue ω in (4.17). The two parameters are related by the following proportionality relation $\lambda = \omega\, C_f f_s R_o$ and therefore their signs are always concordant. The reason why a new parameter is introduced is clarified by Sec. 4.3.3. Indeed, the notation that uses λ parameter instead of ω allows to write simpler equation for the more accurate study of FC voltage stability and also allows a more effective presentation of the final results.

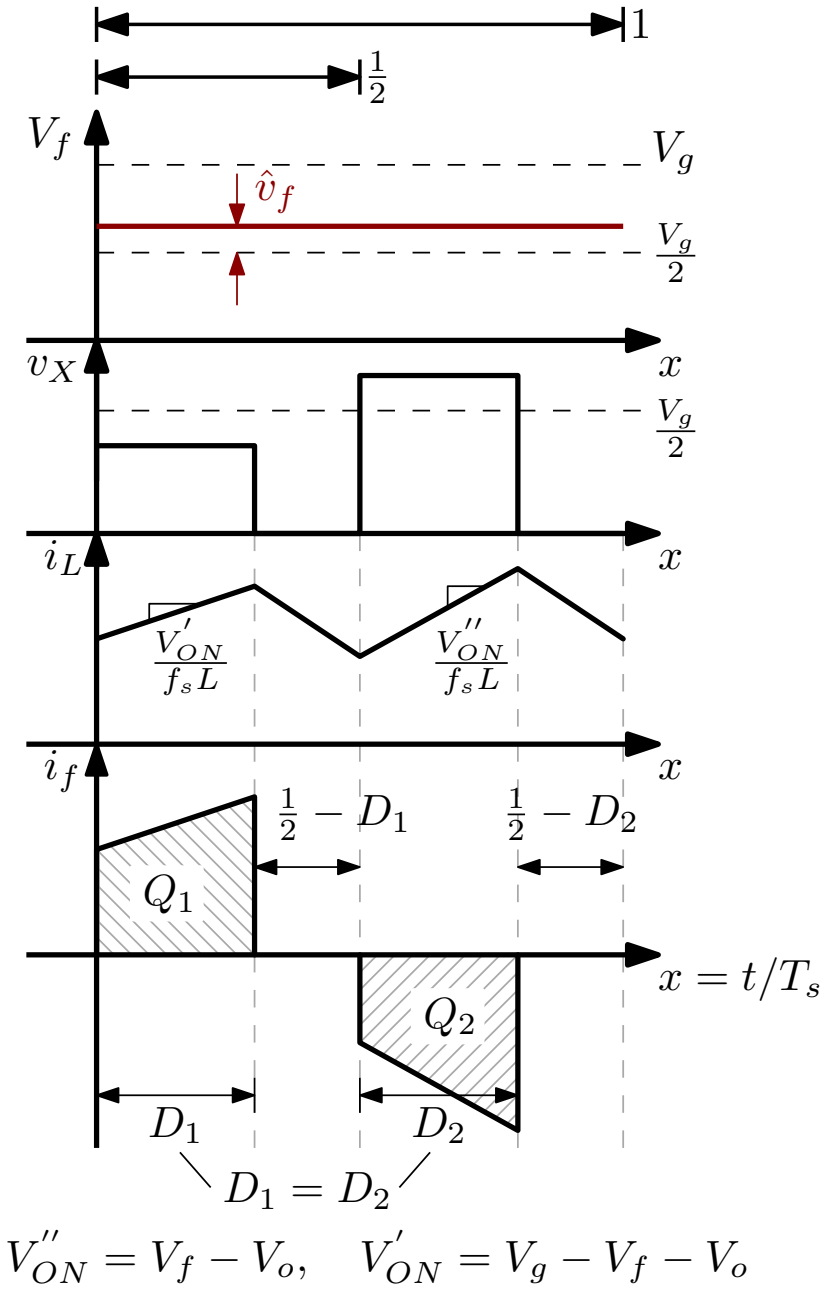


Figure 4.6: *Single-sampled* peak *DPCMC: main waveforms in presence of FC voltage imbalance.*

sampled DPCMC forces D_1 and D_2 to be equal, the voltage conversion ratio does not depend on the value of $\hat{v}_N$, i.e., $M = D_1 = D_2 = D$ as proved in Sec. 3.2.1

In reference to Fig. 4.6, under the traditional small-ripple appoximation for both v_f and v_o, the average FC current can be written as difference between charges Q_1 and Q_2,

$$I_f \triangleq \int_x^{x+1} i_f(\tau) d\tau = Q_1 - |Q_2| \,. \tag{4.22}$$

Both Q_1 and $|Q_2|$ can be written as a function of the average FC voltage perturbation $\hat{v}_N$:

$$Q_1 = \frac{D}{2}\left[2I_{pk} - \frac{2MV_g}{f_s L}(1-D) + \frac{V_g}{2f_s L}\left(1 - 2M - \hat{v}_N\right)\right], \tag{4.23}$$

$$|Q_2| = \frac{D}{2}\left[2I_{pk} - \frac{V_g}{2f_s L}\left(1 - 2M + \hat{v}_N\right)\right], \tag{4.24}$$

where $I_{pk} = I_o + \frac{V_g}{4f_s L}\left(1 - 2M\right) D$.

By substituting (4.23) and (4.24) into (4.22), the terms $\hat{v}_N$ simplify and the average FC current is

$$I_f = \frac{V_g}{2f_s L} D\left(M - D\right). \tag{4.25}$$

Since, as anticipated, $D_1 = D_2 = D = M \; \forall \hat{v}_N$, the above result implies that

$$I_f = 0 \quad \Rightarrow \quad \lambda = 0, \tag{4.26}$$

i.e., the FC voltage is marginally stable. A similar result is found for $M > 0.5$.

This result, derived under the small-ripple approximation for both v_f and v_o, does not predict the fact – documented in sections 4.5 and 4.6 – that the flying-capacitor voltage is, indeed, stable.

Failure of the SRA-based approach in capturing the actual stability character of the FC voltage is consistent with what is reported in Sec. 3.3 and

in [48] in regard to odd-level converters. It must be observed, however, that the scenario here considered includes the closed-loop effects of the *peak* DPCMC controller.

4.3.3 A more accurate FC voltage stability analysis

In this section the SRA hypothesis on v_o is removed and the average FC current is calculated for a lossless 3-LFC Buck by including the effect of the output voltage ripple on $i_f(t)$. The following analysis is based on a state-space model approach and is developed upon the basic simplifying assumption that the switching instants, as well as the state vector at $t = 0$ are the same as the ones obtained with the SRA-based analysis. As before, the FC is replaced with an ideal, unbalanced dc voltage source $V_f = \frac{V_g}{2}(1 + \hat{v}_N)$.

To keep the problem in a normalized form, define the state vector as

$$\begin{aligned} \tilde{v}_o(x) &\triangleq \frac{2v_o(xT_s)}{V_g}, \\ \tilde{i}_L(x) &\triangleq \frac{2R_o i_L(xT_s)}{V_g}, \end{aligned} \tag{4.27}$$

with $x \triangleq t/T_s$ and $R_o = V_o/I_o$. The steady-state solution is obtained by solving the four linear systems corresponding to the four sub-topological states whose waveforms are sketched in Fig. 4.6,

$$\begin{cases} \dot{\boldsymbol{x}}_i = \boldsymbol{A} \cdot \boldsymbol{x}_i + \boldsymbol{B}_i \cdot u_i \\ \boldsymbol{x}_{o_i} = \boldsymbol{C}_i \end{cases} \tag{4.28}$$

where index $i = 1 \ldots 4$ indicates the topological state. Vector $\boldsymbol{x}_{o_i}$ represents the initial condition for topological state i. Values of the constants $\boldsymbol{C}_i$ are calculated by imposing the continuity of the state vector at the switching instants, and the overall periodicity of the sought solution.

State matrix $\boldsymbol{A}$ is the same for all four sub-topological states and can be

put in the normalized form

$$\boldsymbol{A} = 2\pi f_N \begin{pmatrix} -\dfrac{1}{Q} & \dfrac{1}{Q} \\ -Q & 0 \end{pmatrix}, \tag{4.29}$$

where f_N and Q are normalized constants defined by

$$f_N \triangleq \frac{f_o}{f_s}, \qquad Q \triangleq R_o\sqrt{\frac{C_o}{L}}. \tag{4.30}$$

Expressions of u_i and $\boldsymbol{B}_i$ are

$$u_1 = 1 - \hat{v}_N;\ u_2 = u_4 = 0;\ u_3 = 1 + \hat{v}_N, \tag{4.31}$$

$$\boldsymbol{B_1} = \boldsymbol{B_3} = \begin{pmatrix} 0 \\ \\ 2\pi f_N Q \end{pmatrix};\ \boldsymbol{B_2} = \boldsymbol{B_4} = \begin{pmatrix} 0 \\ \\ 0 \end{pmatrix}. \tag{4.32}$$

Solution of the above equations has been obtained in closed-form with the aid of Wolfram Mathematica®. Once the time-domain evolution of the state vector is obtained, the average value $\tilde{I}_f(M, \hat{v}_N, f_N, Q)$ of the FC current is evaluated. Lastly, the expression of $\lambda(M, f_N, Q)$ is calculated following the definition (4.19).

A closed-form expression of λ is unfortunately too complex to be reported here. Behaviour of λ is therefore studied graphically. Fig. 4.7a shows λ versus f_N for various values of M. To generate the plot, a fixed value $Q \approx 8$ is used, which corresponds to the full-load quality factor of the case study converter later considered for simulation and experimental verification. As seen in the plot, λ is always negative regardless of f_N or M, confirming the asymptotic

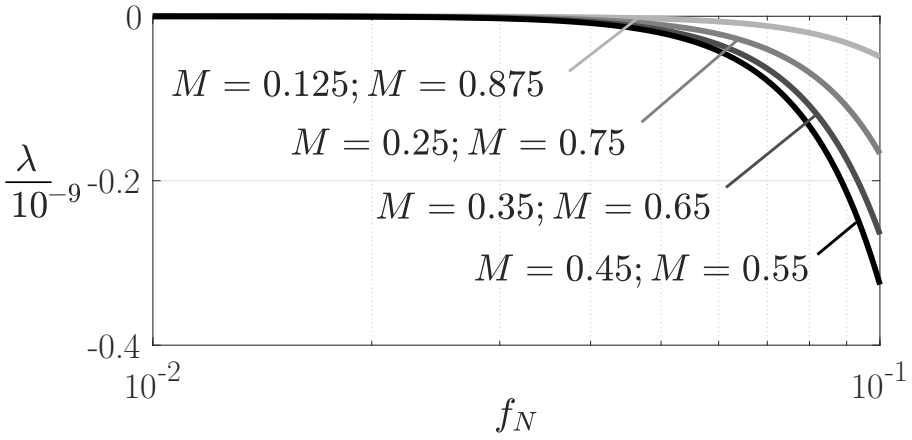
stability of the FC voltage. Furthermore, one has

$$\lim_{f_N \to 0} \lambda = 0. \tag{4.33}$$

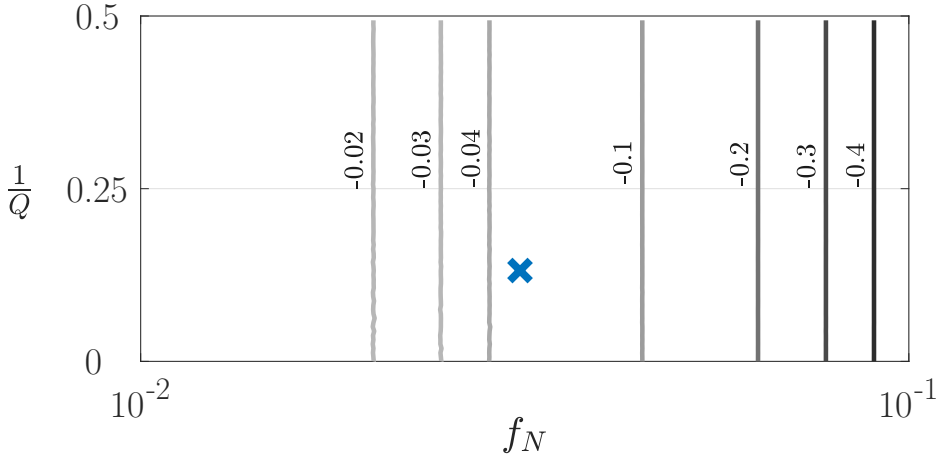
This result is compatible with the simplified SRA-based analysis developed earlier, in that the better the condition $f_o \ll f_s$ is satisfied, the more justified the SRA approximation is. A more general view of $\lambda(M, f_N, Q)$ is provided by the contour plots reported in Fig. 4.7b. The plot reports λ for values of f_N between 0.01 and 0.1, and for values of Q comprised between 2 and $+\infty$. Notice that the y-axis is defined as $1/Q$ in order to explicitly depict the open-circuit condition $Q \to +\infty$. To generate the plot, $M = 0.125$ is chosen, which corresponds to the case study 3LFC converter later presented. The corresponding point of such case study on the plane is indicated by a cross. The contour plot of Fig. 4.7b confirms that λ is negative for all values of f_N and Q, and is consistent with Fig. 4.7a in regard to the behavior of λ as f_N decreases. Furthermore, the contour plot confirms open-circuit stability for the DPCMC controller, in that all contour lines remain strictly negative as $1/Q$ approaches zero. These considerations hold for other values of M, for which the contour plots are qualitatively similar.

4.4 Multi-sampled peak DPCMC

In an N-level flying-capacitor dc-dc converter operating at a switching frequency f_s, the output filter is excited with an *effective* switching rate equal to $(N-1)f_s$, a fact which opens up to the possibility of implementing a *multi-sampled* version of the DPCMC (MS-DPCMC) and, as a consequence, to significantly extend the bandwidth of the control loop. Following the development of the single-sampled case, the discussion on multi-sampled DPCMC starts from the *peak* current control case. Results for the *average* and *valley* controllers are discussed in the next chapter. The 3-LFC Buck converter circuit with multi-sampled DPCMC block diagram is illustrated in Fig. 4.8. In



(a)



(b)

Figure 4.7: *(a) Stability parameter λ as a function of the normalized resonant frequency f_N for different values of M ($Q \approx 8$), and (b) contour plots of $\lambda(f_N, Q)$ for $M = 0.125$. The cross refers to the case study 3LFC prototype later presented.*

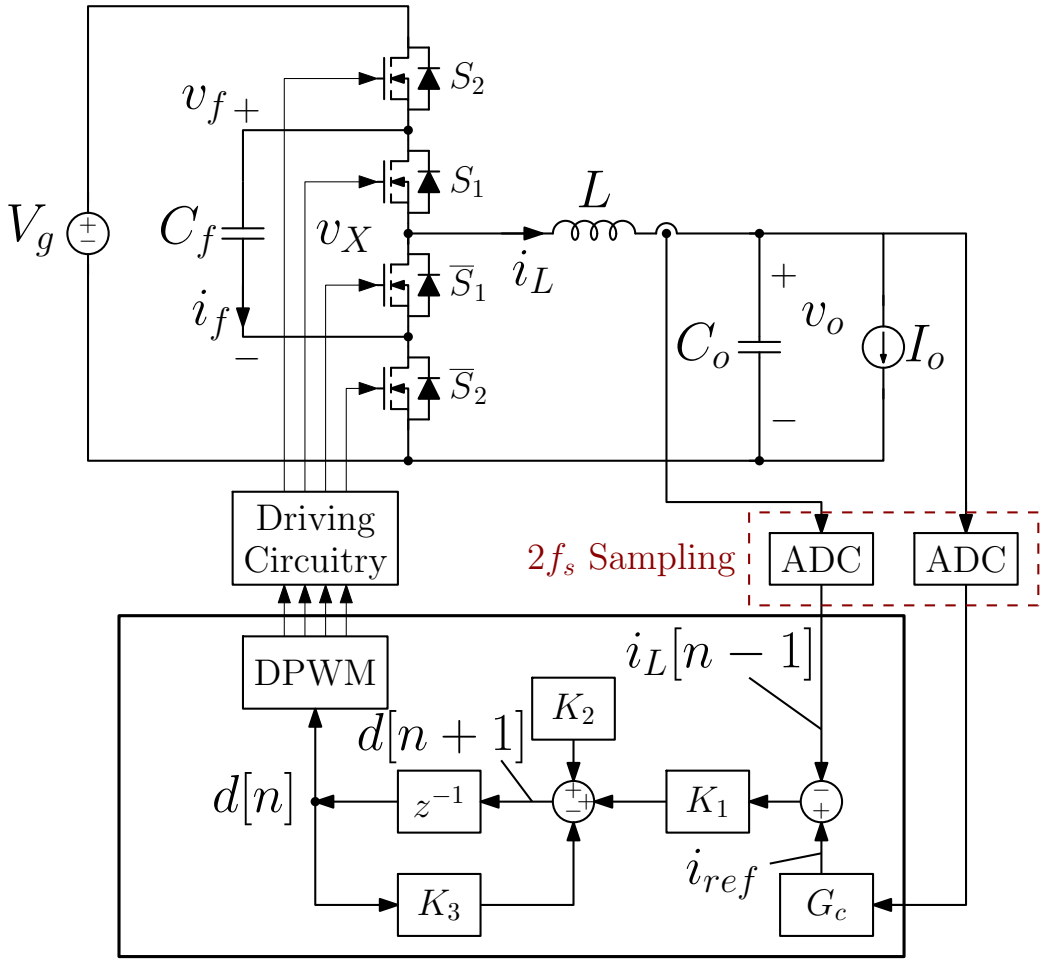


Figure 4.8: *Generic block diagram of a 3-LFC Buck converter with a multi-sampled digital predictive current-mode controller.*

this multi-sampled implementation, the sampling frequency is two times the switching rate (i.e., $f_{\text{sample}} = 2f_s$). As proven in this section, implementation of multi-sampled *peak* DPCMC as a straightforward extension of the single-sampled case is inherently *unstable* as long as $M < 0.5$ and would require some form of active stabilization. A stable variant of the *peak* MS-DPCMC through a *fast-update* of the duty cycle command is presented in the next section. The proposed fast-update multi-sampled *peak* DPCMC extends the dynamic capabilities of the converter and does not require dedicated sensing and circuitry for FC voltage stabilization.

4.4.1 Multi-sampled *peak* DPCMC - straightforward implementation

The implementation of *peak* MS-DPCMC for the 3LFC Buck requires to sample/update the inductor current *twice* per switching period. Fig. 4.9 exemplifies the case of multi-sampled *peak* current mode control based on a leading-edge PWM carrier. Using a similar approach discussed for the single-sampled case, the following control equation is derived

$$d[n+1] = \frac{2f_sL}{V_g}\left(I_{ref} - i_L[n-1]\right) + 2M - d[n]. \tag{4.34}$$

The time evolution of the perturbed current is still provided by (4.7). As expected, the inductor current is regulated in a dead-beat fashion over a time interval equal to T_s. This result is in line with what was previously discussed. Indeed, also for the multi-sampled case the considerations made about the pairing of carriers and control points apply. In particular by implementing the controller with an LE carrier based modulator, the errors at the control point and the one at the sampling point coincide. (4.34) is designed to guarantee the recovery of the error at the control point, but since it coincides, by construction of the modulator, with the sampling point the dead-beat behaviour is guaranteed.

With respect to the average FC current, the main difference between Fig. 4.6 and Fig. 4.9 lies in the values of the duty cycles during the charging and discharging phases of the FC. As already discussed, in the single-sampled DPCMC the two duty cycles are always equal within a given switching period T_s. Indeed, they are updated together once per switching cycle, and therefore the charging and discharging phases of the FC are always forced to be equal. Conversely, in the MS-DPCMC they are not. This difference has a strong impact on the stability of the average flying-capacitor voltage. As anticipated at the end of Section 4.3.2, the simple SRA-based approach is here sufficient to analyse the stability of the controller.

Using Fig. 4.9 as a reference, and assuming that the FC voltage is un-

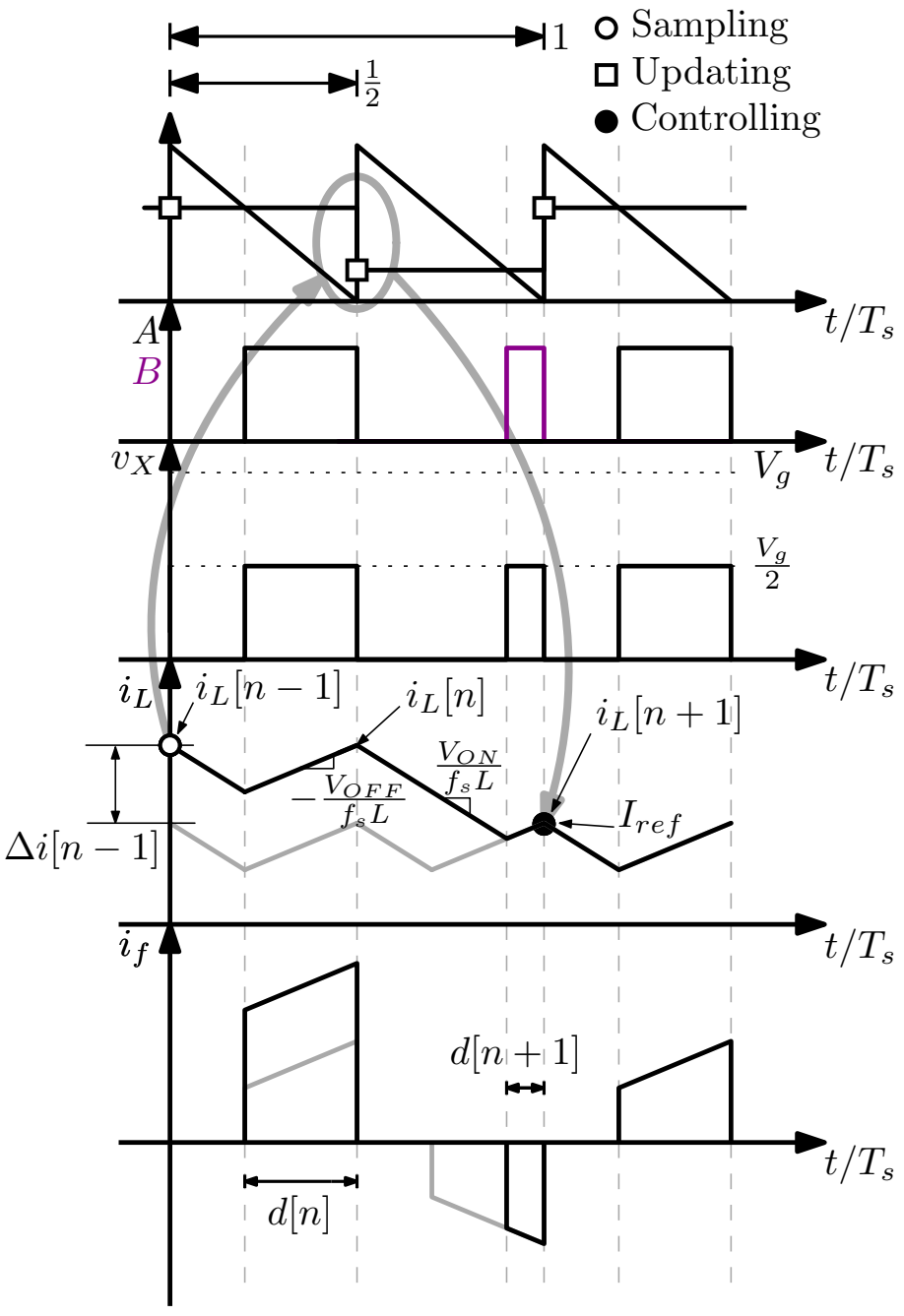


Figure 4.9: *Operation of the multi-sampled* peak *DPCMC with a LE carrier.*

balanced, i.e., $V_f = \frac{V_g}{2} + \hat{v}_f = \frac{V_g}{2}(1 + \hat{v}_N)$, the following expression can be derived

$$\begin{aligned} I_f \approx I_f\Big|_{\hat{v}_N=0} + \frac{dI_f}{d\hat{v}_N}\Big|_{\hat{v}_N=0} \hat{v}_N = 4M^2\left(2+\frac{3}{k}\right)\hat{v}_N \\ \implies \lambda = 4M^2\left(2+\frac{3}{k}\right), \end{aligned} \tag{4.35}$$

where the parameter k is defined as

$$k \triangleq \frac{2f_sLI_o}{V_o} = \frac{2f_sL}{R_o}. \tag{4.36}$$

From (4.35), the resulting stability parameter λ is always *positive*: although the discussed version of the multi-sampled DPCMC is a seemingly straightforward modification of the single-sampled approach to a sampling period equal to $T_s/2$, interaction between the predictive control law and the flying capacitor dynamics now results in an unstable FC voltage. This stability issue for $mode_1$ is solved by employing the strategy introduced in the next section.

By extending the proposed FC voltage stability analysis to $mode_2$, it is possible to prove that this multi-sampled control strategy ensures stable operation for $M > 1/2$ and for all values of the parameter k. Indeed, the λ expression can be written as

$$\lambda = -4M(1-M)\left(1+\frac{(M-1)^2}{Mk}\right) \tag{4.37}$$

(4.37) is always negative for all value of k and for $M > 1/2$. It is therefore possible to implement this type of multi-sampled control as long as the 3-LFC Buck operates with voltage conversion ratios always greater than 0.5.

One comment worth making here concerns the approach used to find (4.35): although a general method has been discussed in section 4.3.3, the SRA approach is enough in order to derive the first-order approximated expression of I_f. This allows reaching an expression of λ in closed form with

much less complexity of calculation. The more accurate analysis presented in 4.3.3 is therefore used in those specific cases where the SRA-based approach fails.

4.4.2 Multi-sampled *peak* DPCMC with fast-update

Fig. 4.10 shows the 3LFC Buck converter with a proposed modification of the *peak* MS-DPCMC, here referred to as *fast-update* multi-sampled DPCMC. The operation of the controller is exemplified in Fig. 4.11 for *peak* current-mode control with a leading-edge carrier. The key point is that $d[n]$ is updated *immediately after the sampling event*, in practice as soon as the digital controller has calculated the new duty cycle value. In Fig. 4.11 the duty cycle update occurs Δt_{calc} seconds after the sampling event. Observe that, while this type of control action is usually not possible using a microcontroller-based platform, it poses little technical difficulties in the context of custom, hardwired digital controllers targeted by this paper [33].

With the same approach used for (4.3), the control equation for the fast-update implementation can be derived as

$$d[n] = \frac{2f_sL}{V_g}\left(I_{ref} - i_L[n-1]\right) + M. \tag{4.38}$$

It can be shown that the evolution of the peak current perturbation is still governed by a dead-beat relationship. The stability of the FC voltage can be studied, once again, using the simplest SRA-based approach. From the fast-update predictive control law (4.38), and assuming that the FC voltage is unbalanced with a small perturbation $\hat{v}_N$ defined as usual, a first-order Taylor expansion of the average FC current, for $M < 1/2$, yields

$$I_f \simeq -4MI_o\left(\frac{1}{2} + M^2\frac{V_g}{4f_sLI_o}\right)\hat{v}_N. \tag{4.39}$$

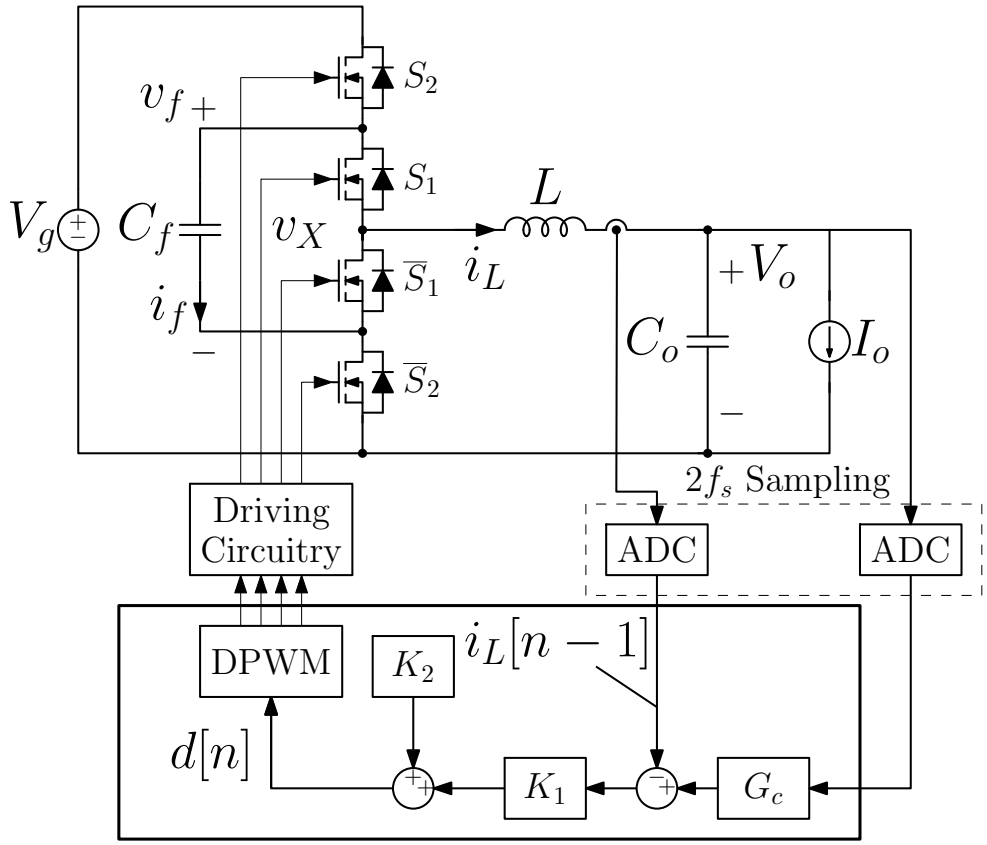


Figure 4.10: *Generic block diagram of a 3LFC Buck with fast-update multi-sampled DPCMC.*

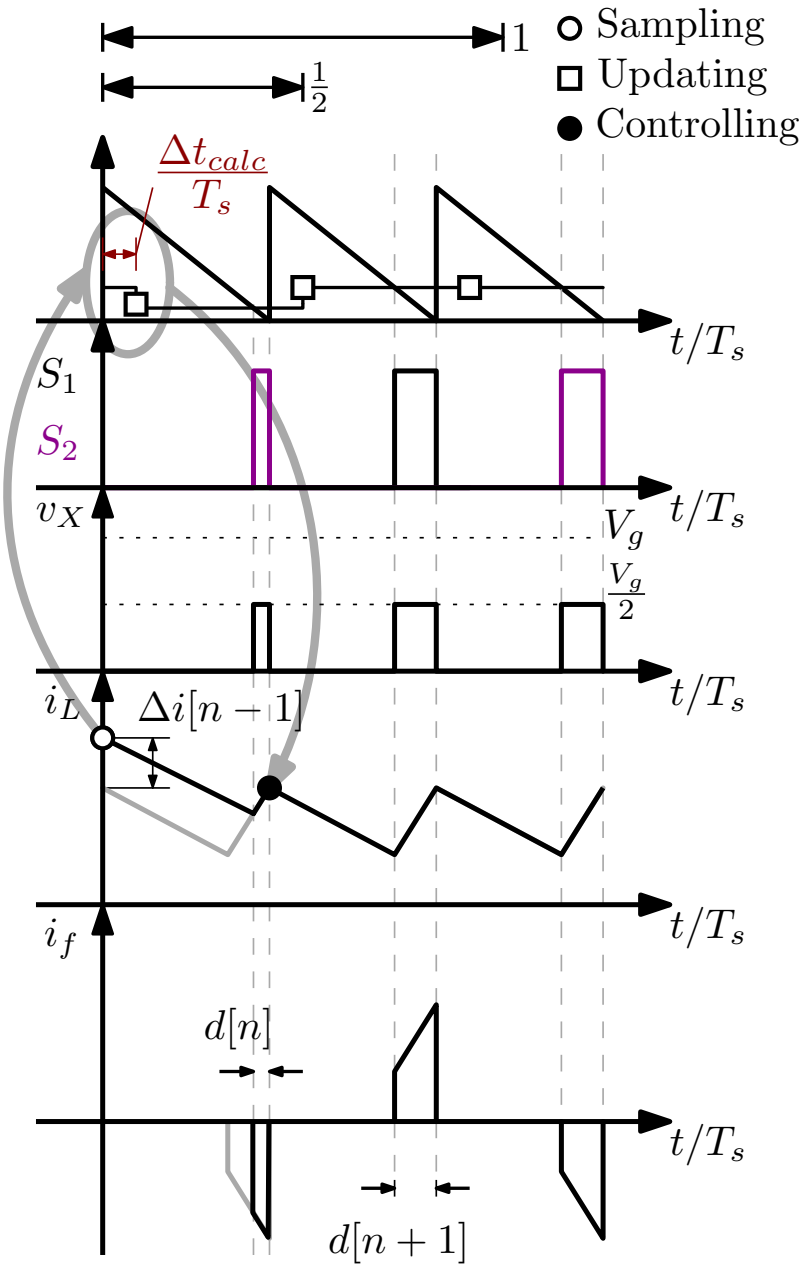


Figure 4.11: *Operation of fast-update* peak *multi-sampled DPCMC with a LE carrier.* Δt_{calc} *represents the maximum amount of time that the hardware requires to compute new duty-cycle values.*

Using the definitions (4.19), (4.20) and (4.36), the expression of λ becomes

$$\lambda = -4M^2 \left(1 + \frac{M}{k}\right). \tag{4.40}$$

Since the voltage conversion ratio M and the parameter k, are always positive, it is immediate to see that the stability parameter λ is always *negative*, indicating that the FC voltage is unconditionally stable. In other words, the fast-update *peak* MS-DPCMC can be implemented without dedicated sensing and circuitry to sense/balance the average FC voltage, exactly as with the single-sampled DPCMC. The possibility to stabilize the FC voltage naturally, by choosing the right inner current-loop technique, significantly reduce the cost and the complexity of the circuit and at the same time increase the reliability of the balancing technique.

Extending the simplified SRA based analysis for the FC voltage stability to the case $M > 1/2$, the following equation can be obtained

$$\lambda = 4M(1 - M) \left(1 + \frac{(M-1)^2}{2Mk}\right). \tag{4.41}$$

The parameter λ in (4.41) is always positive. Therefore, *peak* MS-DPCMC with the fast-update implementation cannot be used in $mode_2$ (i.e., $M > 1/2$). However, this is not a real disadvantage, since the practical applications to which this work refers move in the range $M < 1/2$. Also, for $M > 1/2$ one could use the multi-sampled DPCMC approach presented in the previous section. In this way, it is possible to implement a wide-band current control over the entire operating range for the voltage conversion ratio.

Remarks on duty cycle constraints in the fast-update MS-DPCMC

Since, in the fast-update MS-DPCMC, the duty cycle is updated Δt_{calc} seconds into the switching period, duty cycles $d[n]$ larger than $1 - \Delta t_{calc}/T_s$ cannot be correctly generated by the leading-edge PWM. It is therefore necessary to provide an upper saturation to the duty cycle command equal to

$$D_{max} = 1 - \frac{\Delta t_{calc}}{T_s}. \tag{4.42}$$

Such saturation limit does not pose practical problems as long as $\Delta t_{calc} \ll T_s$. This concept will be taken up in the next chapter where it will be seen that in the case of fast-update *average* DPCMC it will be necessary to limit also the minimum value of the duty-cycle. Even in that circumstance, however, the presence of the corresponding ΔT_{calc} will not represent a real limitation.

4.5 Simulation results

For the purpose of investigating the discussed DPCMC control approaches, a 500 kHz, 12 V-to-1.5 V, 500 mA 3-LFC Buck case study is considered. Converter parameters are summarized in Tab. 4.1. The voltage loop is compensated in order to achieve the *same* phase margin in both the single-sampled and multi-sampled cases, and by maximizing the loop gain crossover frequency subject to that constraint.

The case study converter is simulated in the Matlab®/Simulink®/PLECS® environment. In the simulation analysis presented below, a uniformly distributed ±25% tolerance is systematically included in the switches on-resistances. No stability nor appreciable balancing issues are observed in any of the DPCMC controllers under investigation. As for the sensitivity of DPCMC controllers to timing mismatches in the control signals, a dedicated Monte Carlo analysis is performed and described in section 4.5.2.

4.5.1 Dynamics and FC voltage stability

In this paragraph are reported a series of simulation tests to verify the theory developed so far. The tests are organized by control type in the following order: single-sampling, multi-sampled, and fast-update multi-sampled DPCMC. For each operating mode one test is considered. When possible, a simulation with the dynamic response to a load-step change is also be

Table 4.1: *Parameters of the 3LFC Buck Converter Case Study*

Converter parameters	
Input voltage V_g	12 V
Output voltage V_o	1.5 V
Output current I_o	500 mA
Filter inductance L	6.5 µH
Filter capacitance C_o	50 µF
Flying capacitance C_f	20 µF
Switching frequency	500 kHz
Voltage loop bandwidth and phase margin	
Single-sampled DPCMC	$f_s/18$, 50°
Multi-sampled DPCMC	$f_s/13$, 50°
Fast-update, multi-sampled DPCMC	$f_s/6$, 50° ($\Delta t_{calc} = 50$ ns)

proposed.

Single-sampled DPCMC

Single-sampled *peak* DPCMC is proved to be always stable, regardless the value of the voltage conversion ratio (except for $M \neq \frac{1}{2}$) and regardless the value of the average output current I_o, or equivalently regardless the value of the parameter k. Two simulations are here presented: one for $M < 0.5$, and another for $M > 0.5$. In each simulation, the feedback loop is closed at $t = 0.5\,\text{ms}$ to document the stability of the FC capacitor voltage. Successively, at $t = 1.5\,\text{ms}$, a $I_o = 500\,\text{mA} \rightarrow 0\,\text{A}$ load current step ($k = 0.4643 \rightarrow 0$) is applied to the system in order to document the dynamics of each controller and to show that stability does not depend on k. For both cases, the designed crossing frequency ω_c of the outer voltage loop is set at $\omega_c = 2\pi f_s/18$, and the phase margin is $\phi = 50^o$, as reported in Tab. 4.1.

Fig. 4.12 shows the case of single-sampled *peak* DPCMC for $M < 1/2$. As theoretically predicted the FC voltage remains stable and balanced throughout the transient. FC voltage stability character is maintained also in light-load operation, as confirmed by the theoretical analysis.

Fig. 4.13 shows the simulation results of single-sampled *peak* DPCMC for $M > 1/2$. Similar considerations to case $M < 1/2$ hold. Indeed, for all single-sampled DPCMC the λ expression does not depend on the operating point and its value is always negative whatever is M and k.

To better appreciate the behaviour of the control in the case of greatest practical interest (i.e., $M < 1/2$), an additional simulation is proposed below, precisely the transient response of single-sampled *peak* DPCMC to a 500 mA-to-0 A load step is shown in Fig. 4.14. Once again, this simulation confirms that the average FC voltage remains stable at $V_g/2$ throughout the transient. The finer time scale will allow a comparison between this control-technique and the other *multi-sampled* version presented in this chapter.

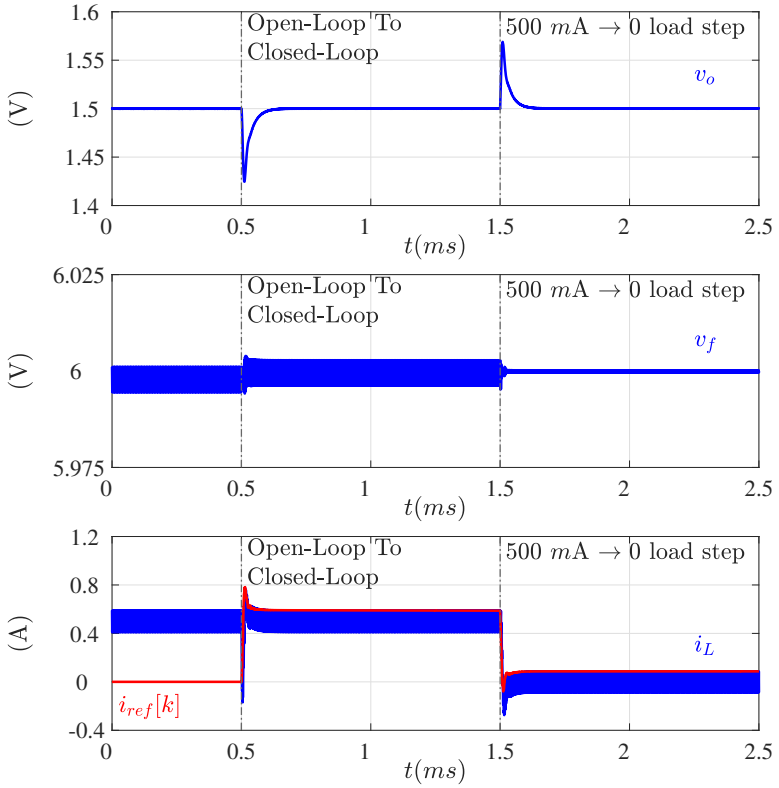


Figure 4.12: *Single-sampled* peak *DPCMC for* $M < 1/2$*: (top) output voltage, (middle) FC voltage, (bottom) inductor current and reference current. At* $t = 0.5ms$ *the feedback-loop is closed while at* $t = 1.5ms$ *the load steps:* $I_o = 500\,\text{mA} \rightarrow 0\,\text{A}$.

Multi-sampled DPCMC

According to the developed theory, the multi-sampled *peak* DPCMC is unstable for $M < 0.5$ and stable for $M > 0.5$. In order to further validate this, three simulations are proposed. For $M < 1/2$ this control-technique is unstable for all value of I_o; this is documented solely by an open-loop to closed-loop transition, after which the FC voltage is seen drifting away from the equilibrium value. Two simulations are proposed for this operating mode: one for $I_o = 0\,\text{A}$ and another one for $I_o = 500\,\text{mA}$. For $M > 1/2$, *peak* MS-DPCMC is stable. One simulation is here provided with an open-loop to closed-loop transition followed by a load step transient. For both multi-sampled DPCMC the crossing frequency of the outer voltage-loop is

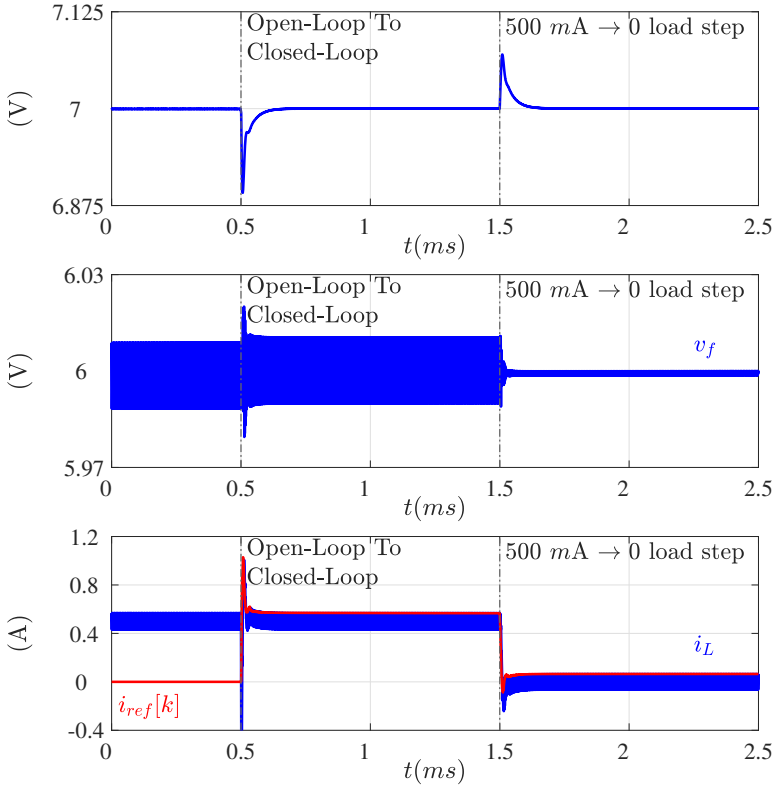


Figure 4.13: *Single-sampled* peak *DPCMC for* $M > 1/2$*: (top) output voltage, (middle) FC voltage, (bottom) inductor current and reference current. At* $t = 0.5ms$ *the feedback-loop is closed while at* $t = 1.5ms$ *the load steps:* $I_o = 500\,\text{mA} \rightarrow 0\,\text{A}$.

$\omega = 2\pi f_s/13$ while the resulting phase margin is $\phi = 50^o$, as in the previous cases.

Fig. 4.15 shows the operation for $I_o = 500\,\text{mA} \implies k = 0.4643$ while Fig. 4.16 the operation for $I_o = 0 \implies k = 0$. For this control-technique λ is always positive for $M < 1/2$ and always negative for $M > 1/2$. Therefore, the *peak* MS-DPCMC leads to unstable FC voltage operation for $M < 1/2$ and for all value of the output current as documented with tests reported in Fig. 4.15 and Fig. 4.16.

Fig. 4.17 shows the simulation results of the *peak* MS-DPCMC for $M > 1/2$. In this case λ is always negative: for all voltage conversion ratio $1/2 < M < 1$ and for all average output current I_o. The control therefore guarantees

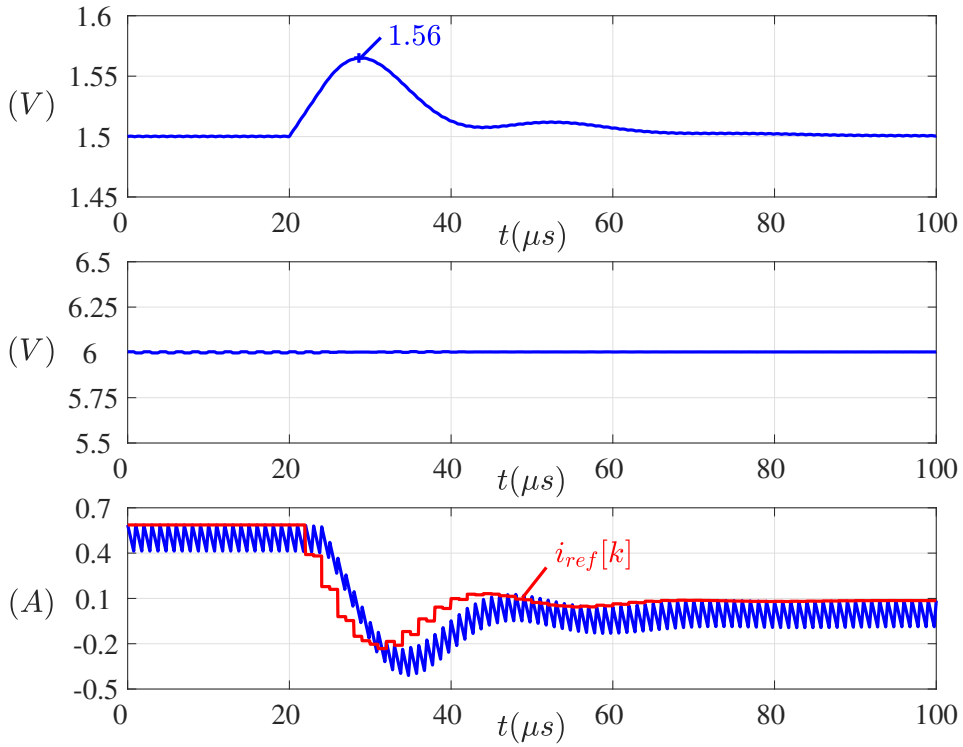


Figure 4.14: *Single-sampled* peak *DPCMC with LE carrier: simulated response to a* 500 mA-*to-*0 A *load step. (top) output voltage, (middle) FC voltage, (bottom) inductor current and reference current.*

a stable FC voltage operation.

Fast-update MS-DPCMC

Fast-update multi-sampled *peak* DPCMC is stable for $M < 0.5$ and unstable for $M > 0.5$. In this case the crossing frequency and the phase margin are $\omega_c = 2\pi f_s/6$ and $\phi = 50^o$ respectively, as summarized in Tab. 4.1.

Fig. 4.18 shows the simulation results of fast-update multi-sampled *peak* DPCMC for $M < 1/2$. Using (4.40), is proved that the controller reach a stable FC voltage operation as also confirmed by this simulation.

Fig. 4.19 and Fig. 4.20 show simulations results of fast-update multi-sampling *peak* DPCMC for $M > 1/2$. As theoretically predicted this controller leads un unstable FC voltage for all values of k, indeed for both

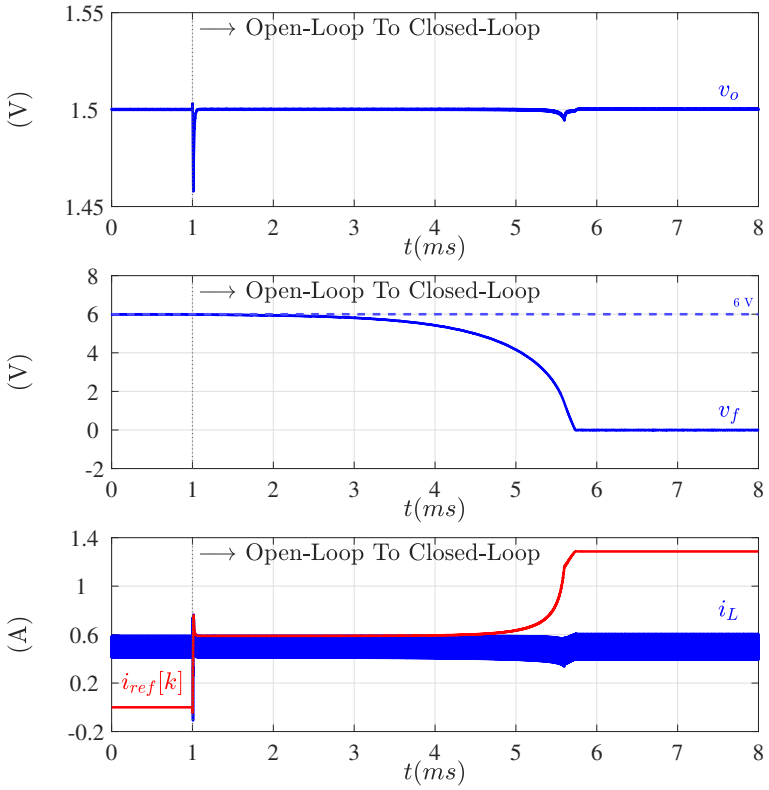


Figure 4.15: *Simulation of* peak *MS-DPCMC for* $M < 1/2$*: (top) output voltage, (middle) FC voltage, (bottom) inductor current and reference current.*$k = 0.4643$ *(*$I_o = 500\,\text{mA}$*). The feedback-loop is closed at* $t = 1\,\text{ms}$.

Fig. 4.19 and Fig. 4.20 the FC voltage drifts toward zero.

The simulation summarized in Fig. 4.21, reports the response for the fast-update multi-sampled *peak* DPCMC. As expected, the fast-update MS-DPCMC achieves a much faster dynamics and smaller overshoot with respect to the single-sampled implementation (see Fig. 4.14).

To further validate the FC voltage stability achieved by the fast-update approach, the system response to an abrupt (step-like) FC voltage perturbation is simulated and reported in Fig. 4.22. In the simulation model the flying capacitor is suddenly put in series with a constant voltage source, simulating a sudden variation of the FC voltage. The total voltage across the voltage source + flying-capacitor is then monitored throughout the subsequent transient. Although such abrupt variation is rather unrealistic in practice, it

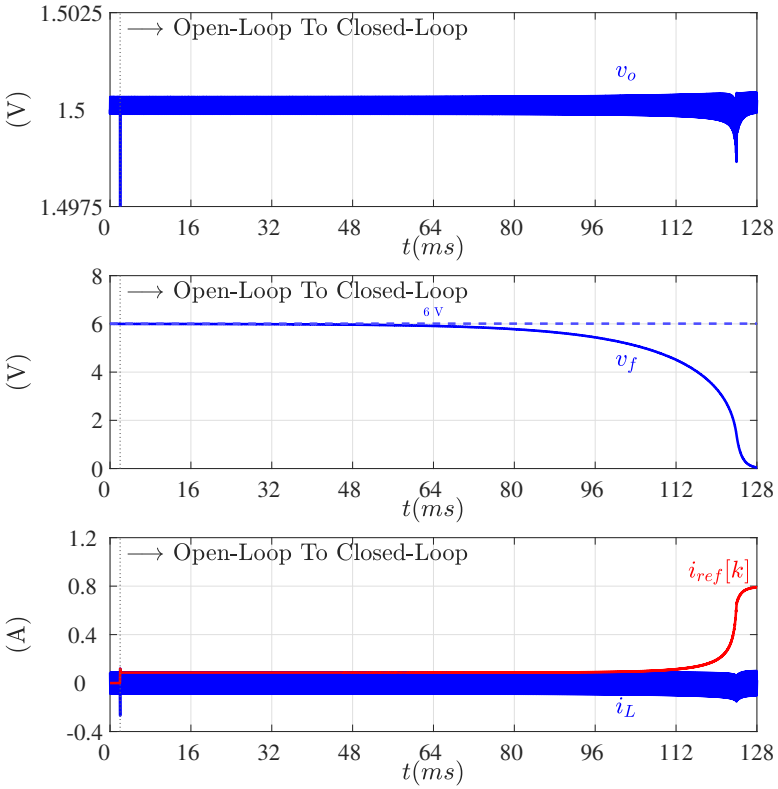


Figure 4.16: *Simulation of multi-sampled* peak *DPCMC for $M < 1/2$: (top) output voltage, (middle) FC voltage, (bottom) inductor current and reference current. $k = 0$ ($I_o = 0$). The feedback-loop is closed at $t = 1$ ms.*

nonetheless represents a good simulation test to assess the conclusions of the theoretical section. Waveforms in Fig. 4.22 indeed confirm that the average FC voltage asymptotically converges back to the initial value even in such extreme case.

4.5.2 DPCMC sensitivity to timing mismatches

In order to assess the impact of timing mismatches in the control signals on FC voltage balancing, a Monte Carlo simulation is carried out. In each simulation run, a uniformly distributed ±5% variation of the gate drivers propagation delay is randomly generated. Simulations are performed both closed-loop and open-loop, with the open-loop modulating signal of the

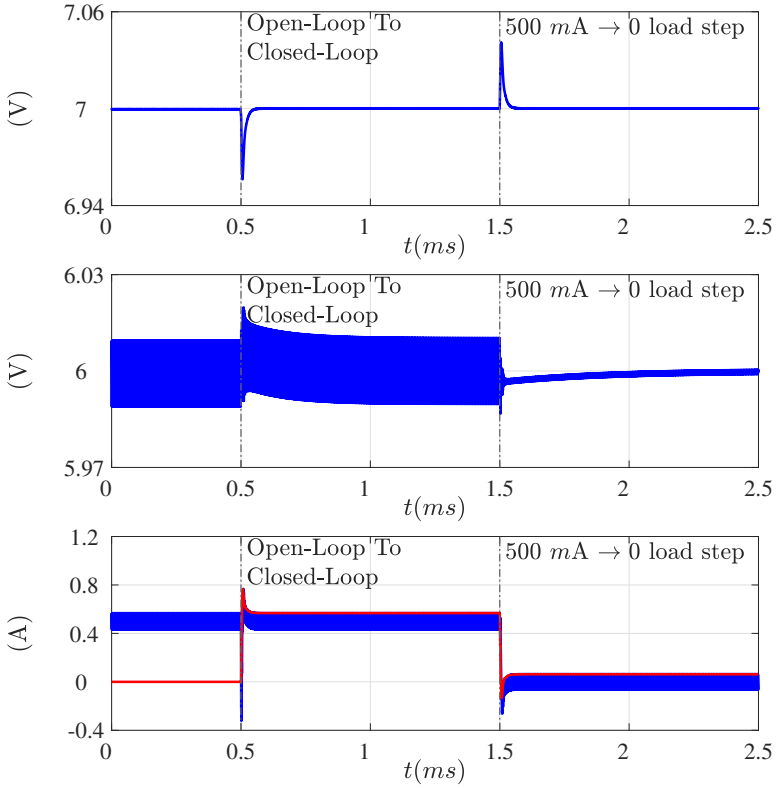


Figure 4.17: *Multi-sampled* peak *DPCMC for* $M > 1/2$*: (top) output voltage, (middle) FC voltage, (bottom) inductor current and reference current. At* $t = 0.5ms$ *the feedback-loop is closed while at* $t = 1.5ms$ *the load steps:* $I_o = 500\,\mathrm{mA} \rightarrow 0\,\mathrm{A}$.

DPWM adjusted to produce, in steady-state, the nominal output voltage $V_o = 1.5\,\mathrm{V}$. After each simulation run the relative steady-state imbalance

$$\delta V_f \triangleq \frac{V_f - V_g/2}{V_g/2} \tag{4.43}$$

is recorded.

Fig. 4.23 reports the simulation results for *peak* DPCMC, comparing the single-sampled case with the fast-update multi-sampled case. As seen in the figure, sensitivity of the single-sampled *peak* DPCMC is identical to the open-loop condition. In other words, no inherent balancing action is produced by the single-sampled controller in presence of significant timing mismatches.

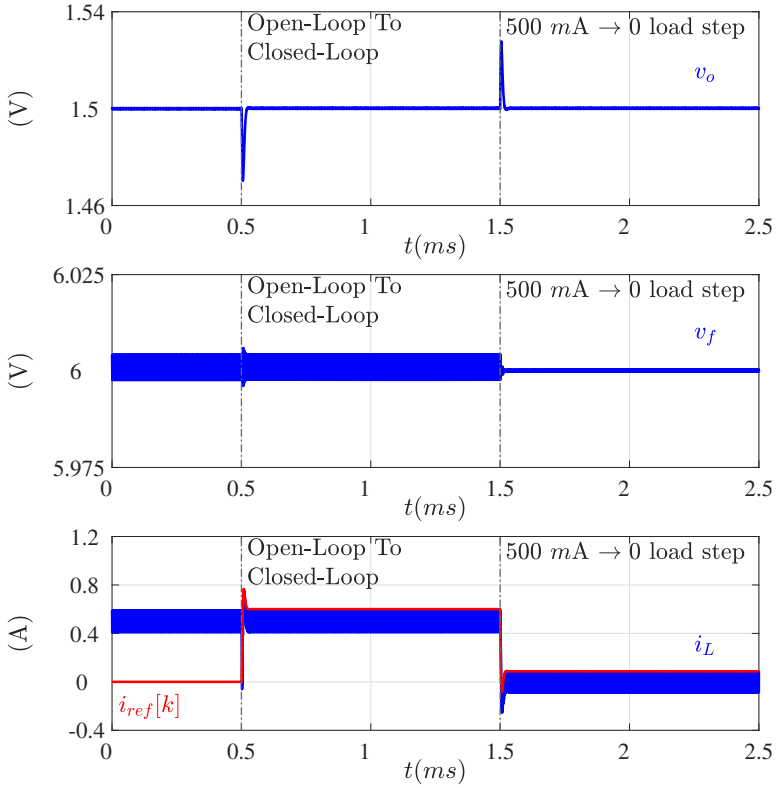


Figure 4.18: *Fast-update multi-sampled* peak *DPCMC for $M < 1/2$: (top) output voltage, (middle) FC voltage, (bottom) inductor current and reference current. At $t = 0.5ms$ the feedback-loop is closed while at $t = 1.5ms$ the load steps: $I_o = 500\,\text{mA} \rightarrow 0\,\text{A}$.*

This is probably due to the fact that in single-sampled controllers no corrective action of the charge and discharge FC phases can be thought of given that these two are forced by the control strategy to be always nominally equal. Therefore, by introducing an intentional mismatch in the control signals a steady-state with null average FC current even in the presence of FC voltage imbalance can be obtained.

The fast-update multi-sampled *peak* case is, on the other hand, significantly different, in that the closed-loop sensitivity is strikingly smaller than the open-loop one, and the open-loop imbalance is almost entirely corrected by the multi-sampled controller: the residual FC voltage imbalance δV_f for the fast-update MS-DPCMC is less than 0.3% for all simulation runs illus-

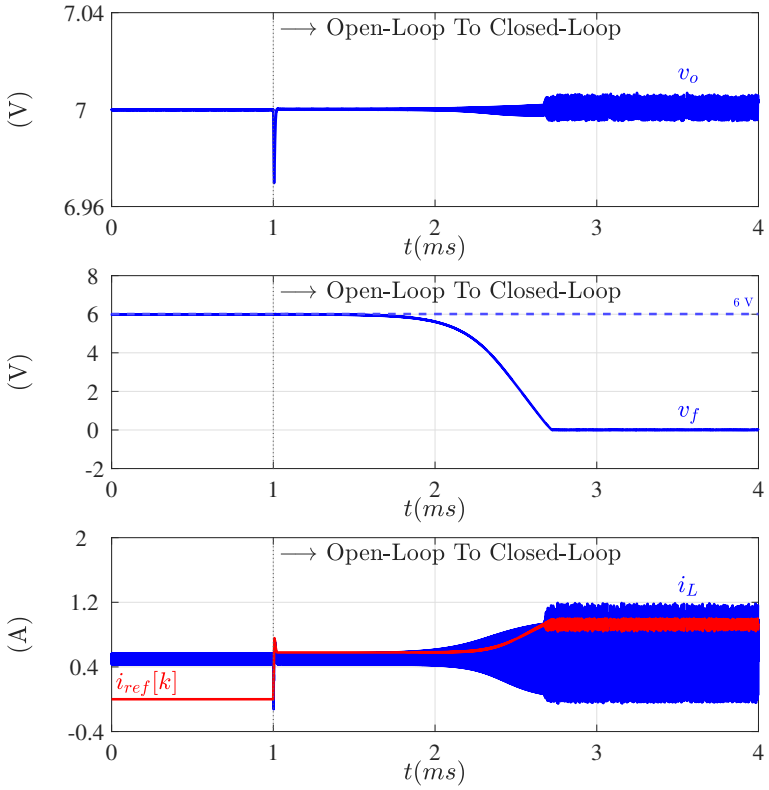


Figure 4.19: *Simulation of fast-update multi-sampled* peak *DPCMC for* $M > 1/2$*: (top) output voltage, (middle) FC voltage, (bottom) inductor current and reference current for* $k = 0.4643$ *(*$I_o = 500\,\text{mA}$*). The feedback-loop is closed at* $t = 1\,\text{ms}$.

trated in Fig. 4.23.

Such inherent *self-balancing* feature of the fast-update *peak* DPCMC can be justified by the fact that multi-sampled controllers are intrinsically capable of producing *different* duty cycles D_1 and D_2 within the switching period. The controller can therefore change the value of FC charging and discharging phases. During transients, the fast-update *peak* MS-DPCMC responds to non-zero FC voltage unbalance producing different duty-cycles. In this specific control the resulting action is a balancing reaction and in steady-state, a large amount of the FC voltage unbalance is recovered. As mentioned before, in the single-sampled implementation this action is simply not possible since the control always imposes the same duty cycle. Therefore

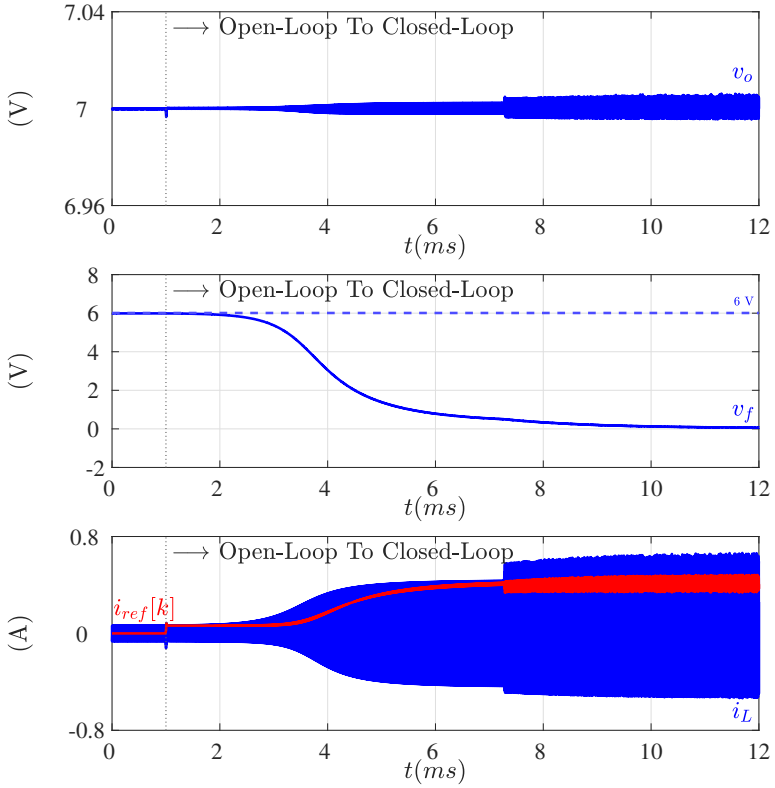


Figure 4.20: *Simulation of fast-update multi-sampled* peak *DPCMC for* $M > 1/2$*: (top) output voltage, (middle) FC voltage, (bottom) inductor current and reference current for* $k = 0$ *(*$I_o = 0$*). The feedback-loop is closed at* $t = 1\,\text{ms}$.

closed-loop unbalances coincide with the open-loop ones given that not even during transient is it possible introduce corrective actions on the FC charging and discharging phases.

4.5.3 Robustness with respect to the converter parameters

The predictive control equations discussed in this thesis depend on the converter parameters V_g, M, f_s and L – a fact shared with other predictive controllers previously reported [37] and which deserves a dedicated discussion. This topic, firstly introduced in Sec. 2.2.1, is now detailed as regard

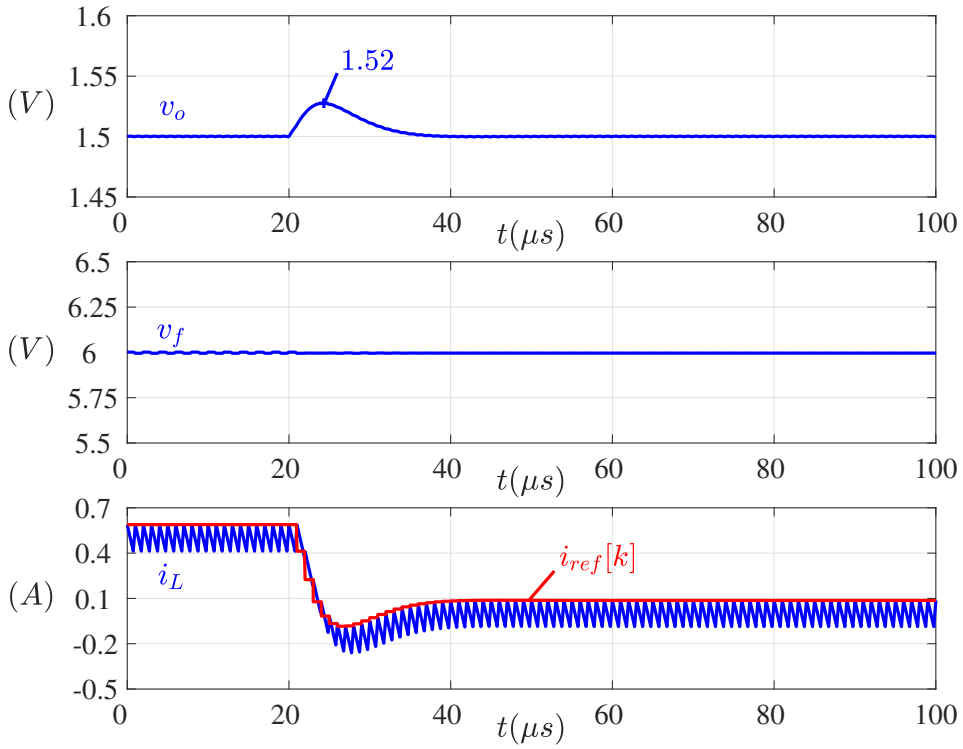


Figure 4.21: *Fast-update multi-sampled* peak *DPCMC with LE carrier: simulated response to a* 500 mA*-to-*0 A *load step. (top) output voltage, (middle) FC voltage, (bottom) inductor current and reference current.*

the application of DPCMC for multi-level converters. In order to get a more complete picture, some simulations are presented and discussed, followed by some experimental tests in which some parameters are deliberately different from the nominal values with which the control equation was constructed and implemented.

As stated in Sec. 2.2.1, one preliminary comment regards the applications targeted by this work. Indeed, in the integrated applications to which this work refers, a package pin is routinely reserved for input voltage sensing, as testified in several commercial integrated circuits datasheets [38–40]. Therefore, assuming that the information on V_g is available to the controller is consistent with the state-of-the art of commercial products. Furthermore, in the multilevel converters considered in this work one has $M = D$, i.e., the voltage conversion ratio is equal to the duty cycle, a signal always available

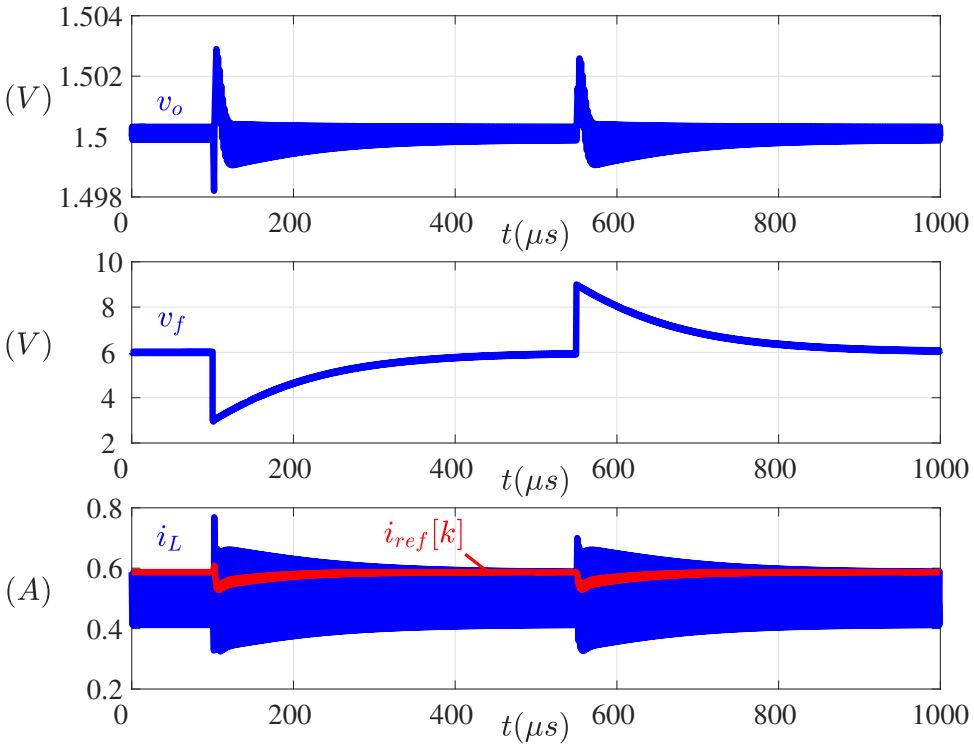


Figure 4.22: *Fast-update multi-sampled* peak *DPCMC with LE carrier: simulated response to an abrupt FC voltage perturbation* $V_f = 0.5V_g \rightarrow 0.25V_g$ *and* $V_f = 0.5V_g \rightarrow 0.75V_g$*: (top) output voltage* v_o*; (middle) instantaneous FC voltage* v_f*; (bottom) inductor current* i_L *and current loop reference signal* i_{ref}.

inside the digital controller. Also notice that an estimate of V_g can also be numerically obtained as V_o/M, eliminating the need for input voltage sensing altogether at the expense of a slight increase in hardware complexity. Overall, presence of V_g and M in the predictive control laws do not pose significant technical challenges to the application of DPCMC because all equations can be digitally implemented using measured or online-estimated coefficients.

Nonetheless, a simulation-based analysis is here presented assuming that variations of V_g occur without a corresponding adjustment or re-calculation of the predictive law coefficients. Fig. 4.24 shows a simulation where the input voltage V_g changes quickly from 12 V to 10.8 V. Subsequently the load current steps from 500 mA to 0 A. After the input voltage step, the FC

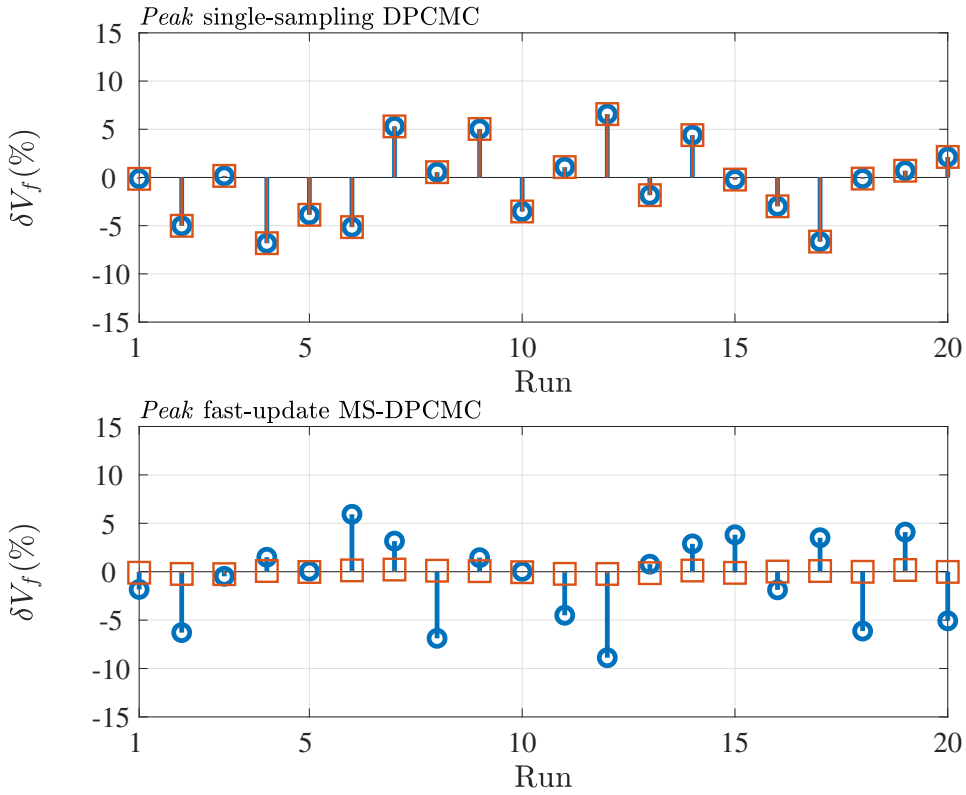


Figure 4.23: *Open-loop (circles) vs. closed-loop (squares) Monte Carlo simulation of (top) single-sampled* peak *DPCMC and (bottom) fast-update multi-sampled* peak *DPCMC.*

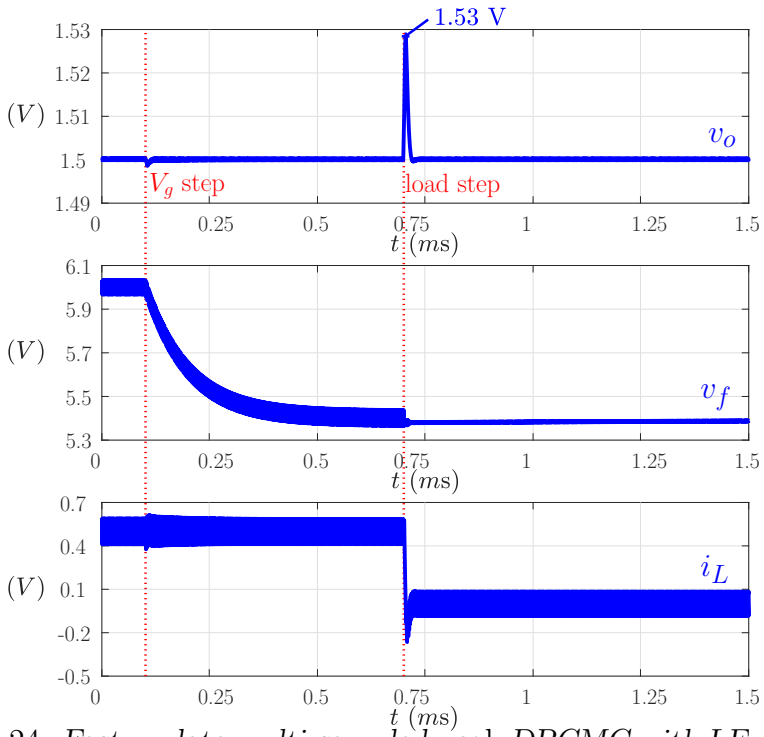


Figure 4.24: *Fast-update multi-sampled* peak *DPCMC with LE carrier: simulated response to an input voltage step* 12 V*-to-*10.8 V *followed by a* 500 mA*-to-*0 A *load step. (top) output voltage, (middle) FC voltage, (bottom) inductor current.*

voltage settles to the new balanced value, confirming that the controller is still able to guarantee a stable operation. After the load-step the overshoot of the output voltage v_o is slightly larger than the overshoot in Fig. 4.21, while the response time is practically unchanged.

In regard to the robustness of DPCMC against variations in L, Fig. 4.25 reports closed-loop simulation results for the fast-update *peak* MS-DPCMC assuming variations of the filter inductance with respect to the nominal value L_{nom} used in the predictive equations. In all cases the closed-loop response to a 500 mA-to-0 A load step is stable and the performances are almost unchanged. These results confirm that the fast-update *peak* MS-DPCMC operates normally while continuing to guarantee stability for both inductor current and FC voltage even in the presence of inductance and input voltage values deviating with respect to the nominal values.

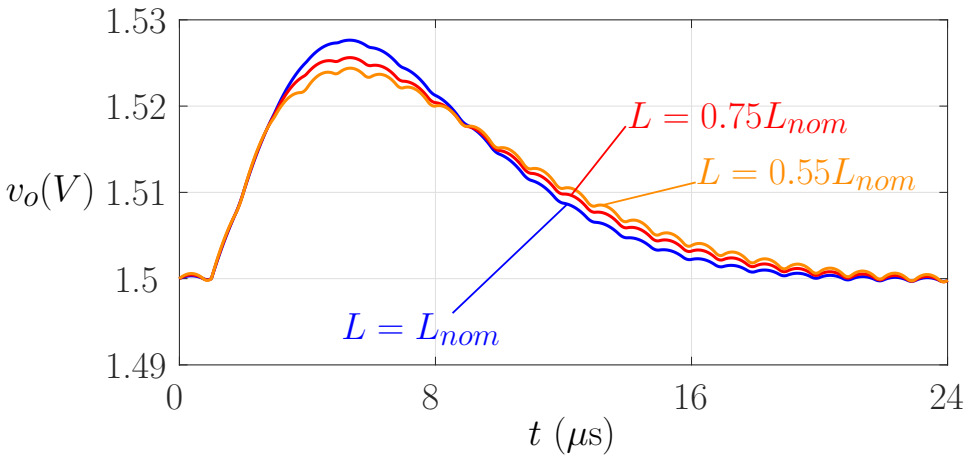


Figure 4.25: *Fast-update multi-sampled* peak *DPCMC with LE carrier: simulated output voltage response to a* 500 mA*-to-*0 A *load step with nominal and non-nominal inductance values.*

4.6 Experimental validation

The custom prototype shown in Fig. 4.26 is built in order to validate the developed theory for the chosen case study described in Tab. 4.1. The digital controller is VHDL-coded and synthesized on a commercial FPGA board interfaced with the 3-LFC prototype. With this custom prototype, it is possible to test the three dead-beat *peak* current control techniques described in this chapter, as well as the *average* and *valley* DPCMCs.

In the experimental measurements, no attempt is made to correct or compensate timing mismatches naturally present in the prototype.

The experimental response of the single-sampled *peak* DPCMC to a 500 mA-to-0 A load-step variation is reported in Fig. 4.27. As predicted theoretically and by the simulations, the average FC voltage remains stable throughout the transient. The same transient response is illustrated in Fig. 4.28 for the fast-update *peak* MS-DPCMC, illustrating a faster dynamics compared to the *peak* single-sampled DPCMC while still maintaining a stable FC voltage.

Although the system works as theoretically predicted, a small FC voltage

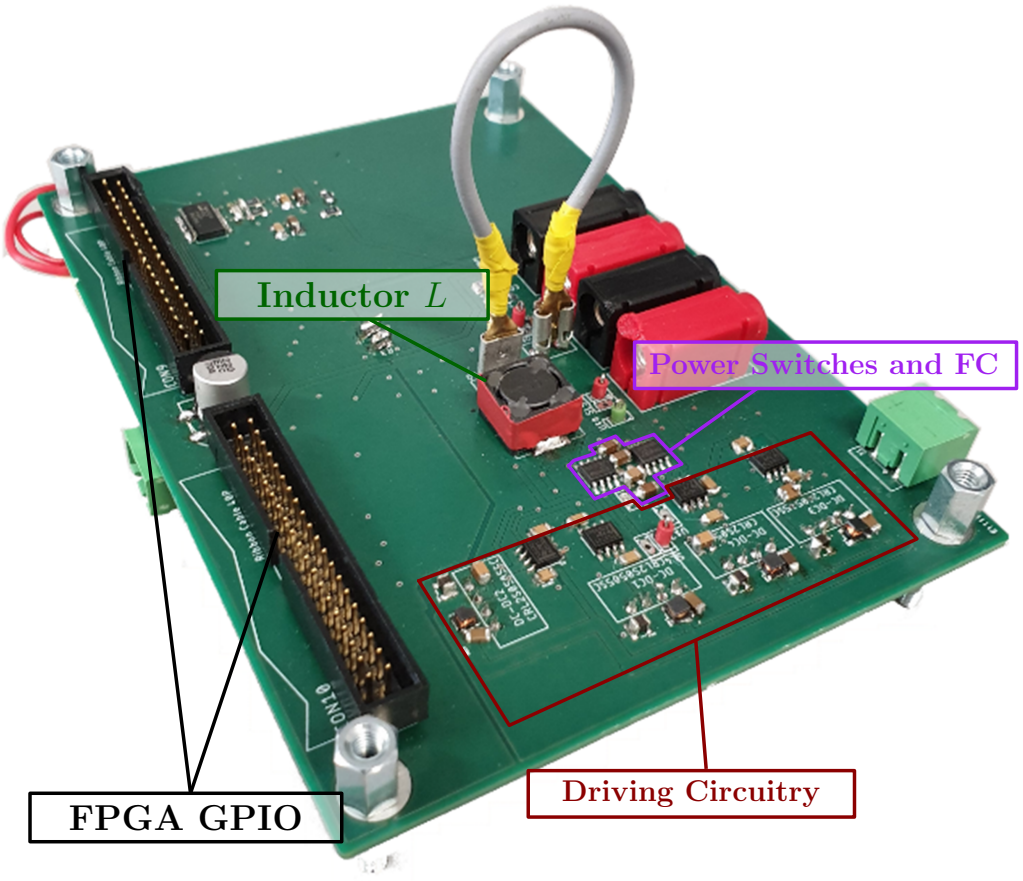


Figure 4.26: *Custom prototype of the* 500 kHz, 12 V-*to*-1.5 V, 500 mA *3-LFC Buck converter.*

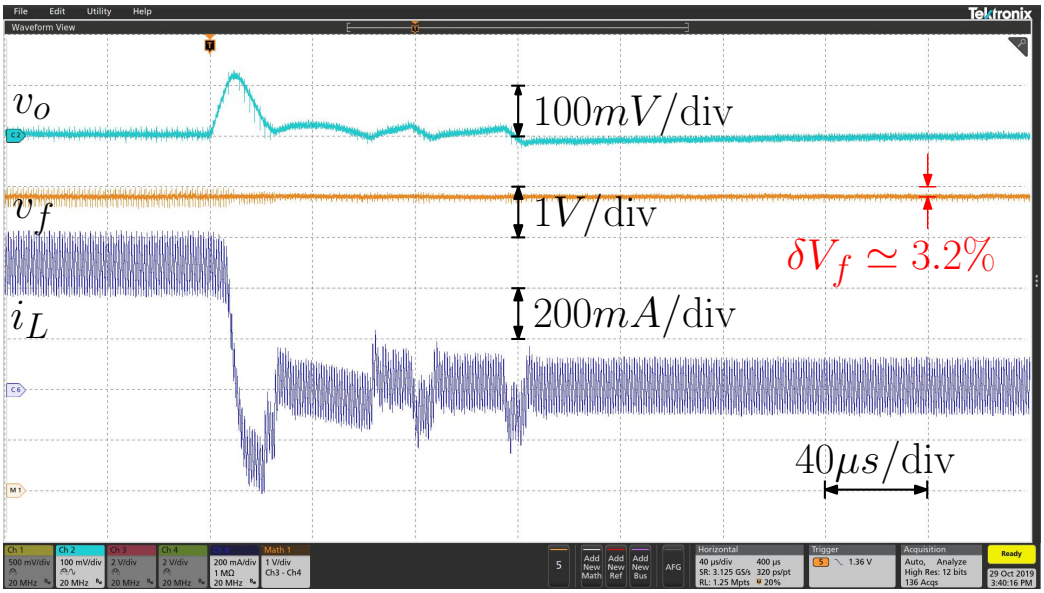


Figure 4.27: *Experimental response of single-sampled* peak *DPCMC to a* $500\,\text{mA} \rightarrow 0$ *load step. Output voltage* v_o *(ac-coupled):* $100\,\text{mV/div}$*; flying capacitor voltage* v_f*:* $1\,\text{V/div}$*; inductor current* i_L*:* $200\,\text{mA/div}$.

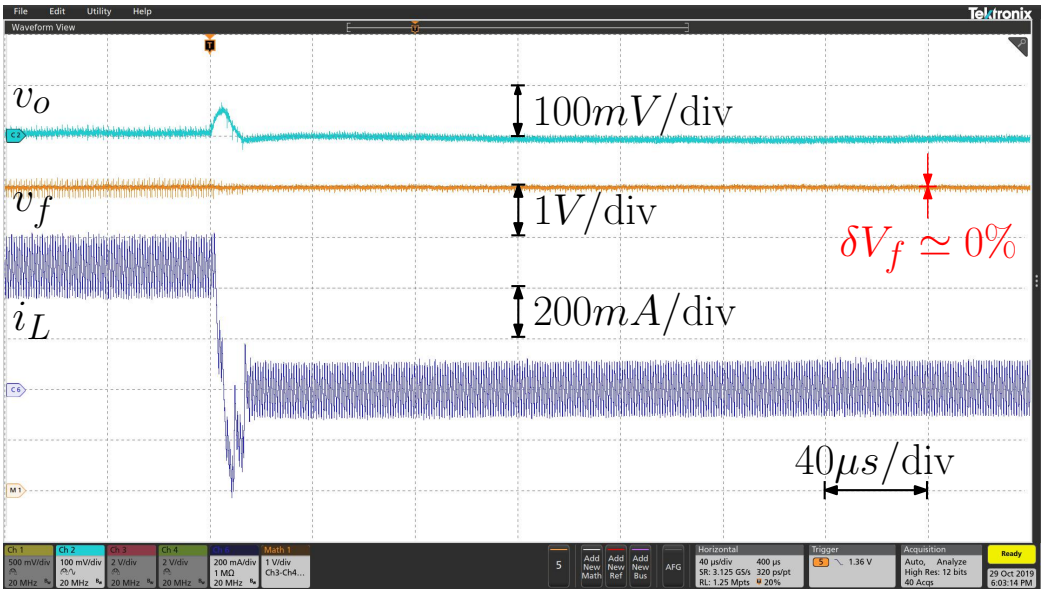


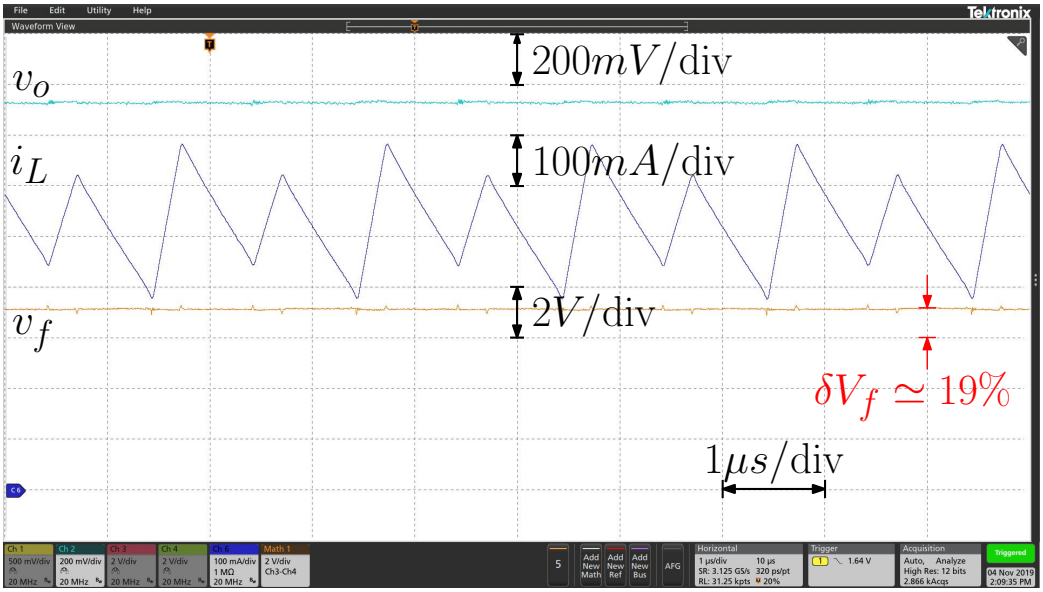
Figure 4.28: *Experimental response of fast-update multi-sampled* peak *DPCMC to a* $500\,\text{mA} \rightarrow 0$ *load step. Output voltage* v_o *(ac-coupled):* $100\,\text{mV/div}$*; flying-capacitor voltage* v_f*:* $1\,\text{V/div}$*; inductor current* i_L*:* $200\,\text{mA/div}$.

imbalance can be observed in the experimental test sketched in Fig. 4.27 while this FC voltage imbalance is completely recovered in Fig. 4.28. These results confirm what discussed in section 4.5.2 about the robustness of the *peak* fast-update MS-DPCMC. This self-balancing FC voltage property is now further verified with another important experimental test.

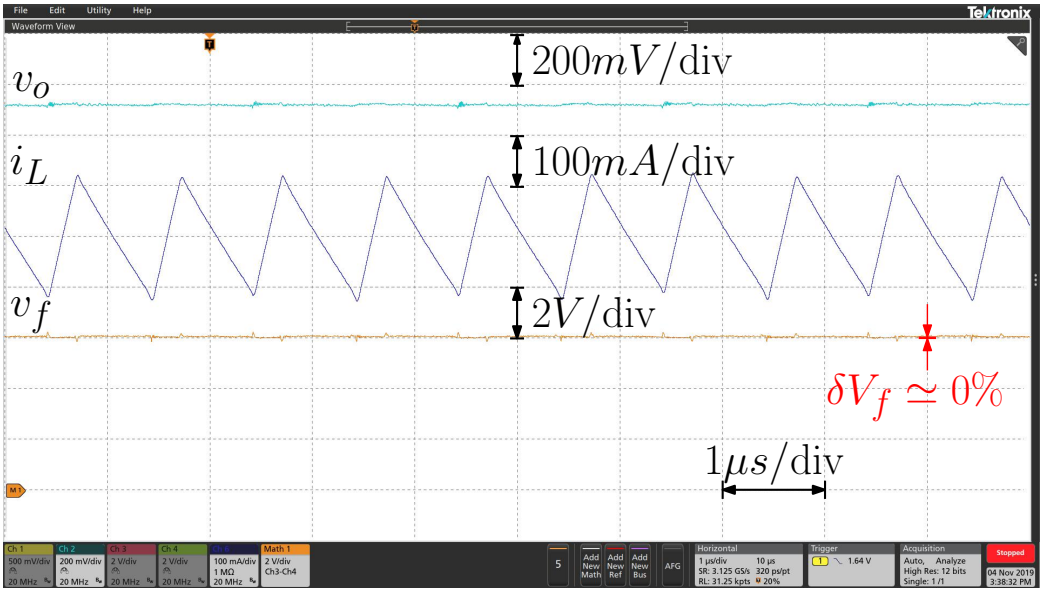
An *intentional* timing mismatch is introduced in the control signals in order to produce a large open-loop FC voltage imbalance. This imbalance is therefore compared with the closed-loop one. Such intentional mismatch is obtained by adding a turn-on delay of switch S_2 (see Fig. 4.10 as reference) and causes the duration of the discharging phase of the FC to be reduced by 2.5 ns. As a result, the measured open-loop FC voltage imbalance becomes $\delta V_f = 19.5\%$ ($V_f = 7.17\,\mathrm{V}$).

Fig. 4.29a and Fig. 4.29b respectively report the experimental open-loop and closed-loop situation for the fast-update multi-sampled *peak* DPCMC in presence of such intentional mismatch. The multi-sampled controller almost fully eliminates the open-loop imbalance: measured average FC voltage in the closed-loop condition is $V_f = 6.01\,\mathrm{V}$, corresponding to a residual imbalance of $\delta V_f = 0.17\%$.

This chapter is closed by a final experimental test in which the input voltage V_g is intentionally changed from its nominal value. Instead, the coefficient K_2 on Fig. 4.10 is left at the nominal value. In this way the robustness of the controller with respect to non-nominal values of the parameter K_2 or equivalently of the input voltage can be tested. Fig. 4.30 shows a load-step transient similar to the one proposed on Fig. 4.28 but with a non-nominal input voltage $V_g = 10.8\,\mathrm{V}$ and with no re-calculation of the predictive law coefficients. The experimental average FC voltage correctly settles to the balanced value $10.8\,\mathrm{V}/2 = 5.4\,\mathrm{V}$. The dynamics of the inductor current is very similar to the nominal condition and no stability issues are seen.



(a)



(b)

Figure 4.29: *Experimental comparison between (top) open-loop and (bottom) closed-loop FC voltage imbalance with fast-update multi-sampled* peak *DPCM in presence of an intentional timing mismatch of the control signals. Output voltage v_o:* 200 mV/div*; flying-capacitor voltage v_f:* 2 V/div*; inductor current i_L:* 100 mA/div.

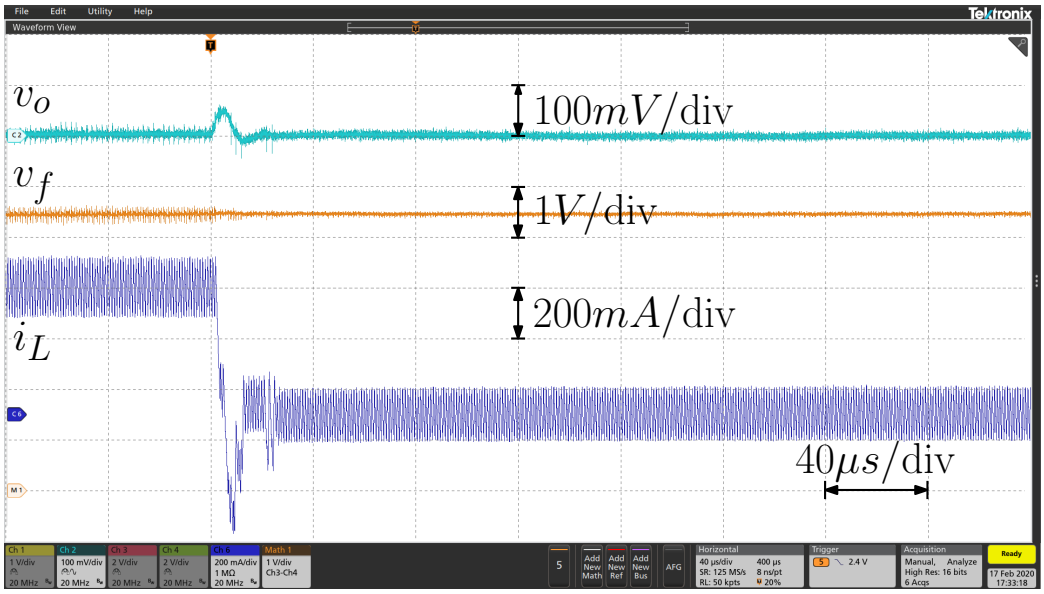


Figure 4.30: *Experimental response of fast-update multi-sampled* peak *DPCMC to a* 500 mA $\rightarrow$ 0 *load step for non-nominal value of the input voltage* $V_g = 10.8$ V. *Output voltage* v_o *(ac-coupled):* 100 mV/div*; flying capacitor voltage* v_f*:* 1 V/div*; inductor current* i_L*:* 200 mA/div.

Summary of inductor current and FC voltage stability

Tab. 4.2 reports the inductor current propagation error ratio $\frac{\Delta i[n+1]}{\Delta i[n-1]}$, for the 3-LFC Buck converter operating with *peak* DPCMC for different implementation of the DPWM. The only DPWM implementation that guarantees dead-beat behavior and a single control equation for both operating mode is obtained with the leading-edge carrier implementation.

Table 4.2: *Summary of the inductor current propagation error ratio* $\frac{\Delta i[n+1]}{\Delta i[n-1]}$*, for* peak *DPCMC implemented with LE, TTE and TE carrier.*
(*) Indicates the dead-Beat behaviour.

	LE carrier	TE carrier	TTE carrier
$M < \frac{1}{2}$	0^*	$\frac{M}{1-M}$	$-\frac{1-2M}{3-2M}$
$M > \frac{1}{2}$	0^*	$\frac{2M-2}{3-2M}$	$-\frac{2M-1}{5-2M}$

Tab. 4.3 summarizes the λ expression for the single-sampling, multi-sampling and fast-update multi-sampled *peak* DPCMC. The table shows only the results obtained with modulator implemented with LE carrier. The other cases are not of interest as far as this thesis is concerned and will not be further analyzed either here or in subsequent chapters [3].

Table 4.3: *Summary of λ expressions for the FC voltage stability analysis. (*) Inequalities are proved using the more accurate FC stability analysis presented in 4.3.3*

	DPCMC	MS-DPCMC	fast-update MS-DPCMC
$M < \frac{1}{2}$	$\lambda < 0^*$	$4M^2\left(2+\frac{3}{k}\right)$	$-4M^2\left(1+\frac{M}{k}\right)$
$M > \frac{1}{2}$	$\lambda < 0^*$	$4\left(M^2-M\right)\left(1+\frac{(M-1)^2}{Mk}\right)$	$4(M-M^2)\left(1+\frac{(M-1)^2}{2Mk}\right)$

The following list summarizes the most important findings captured in this chapter:

- All proposed *peak* DPCMC with a LE carrier based DPWM implements a digital dead-beat controller as regard as the inductor current regulation error.
- the single-sampled *peak* DPCMC provides a stable FC voltage operation for both operating modes.
- The fast-update multi-sampled *peak* DPCMC, guarantees a stable FC operation for $M < 1/2$. This control-technique also exhibit strong self-balancing capabilities, resulting in a marked improvement of the converter sensitivity to timing mismatches over the open-loop condition

[3] Applying the analytical tools developed in this chapter, it is possible to show that while the inductor current does not present any stability issue in the case TE o TTE based digital pulse-width modulators, the FC voltage presents instability or conditionally stable operation. Moreover, for this cases the inductor current is not controlled with a dead-beat fashion and the entity of the current error correction depends on the operating mode.

- Single-sampled *peak* DPCMC techniques exhibit a closed-loop sensitivity to timing mismatches which is identical to that of the open-loop converter.

Chapter 5

Average and valley DPCMC for 3-LFC Buck converter

As shown in the previous chapters, digital predictive current-mode control is a simple and fast approach for controlling the inductor current in a dead-beat fashion. Depending on which point of the inductor current waveform is to be regulated, one usually distinguishes between *peak*, *average* and *valley* DPCMC. In the context of multi-level converters, implementation of the DPCMC concept is subject to the constraint that the FC voltage(s) remain stable. As showed, this entails a dedicated analysis aimed at understanding how the predictive control law interacts with the FC voltage dynamics, and at identifying potential instability issues. Application of *peak* DPCMC to a 3-LFC-Buck is presented in the previous chapter and in [47,50]. Both single-sampled and multi-sampled versions of the approach are disclosed, and the main stability properties of the inductor current and of the FC voltage are analysed in relation to the converter parameters, operating point and load current. This chapter extends those results to the cases of *average* and *valley* digital predictive current-mode controllers, considering both single-sampled and multi-sampled implementations and FC voltage stability.

5.1 Single-sampled average DPCMC

Fig. 4.1 shows the general block diagram of a DPCMC controller for 3-LFC Buck converter. This structure applies for all single-sampled DPCMC and therefore also for the *average* current-mode control. Fig. 5.1 illustrates the operation of single-sampled *average* DPCMC based on a trailing triangle-edge (TTE) carrier. The figure exemplifies how the initial perturbation of the average inductor current value, $\Delta i[n-1] = i_L[n-1] - I_{ref}$, is corrected. The control equation can be derived assuming that the FC voltage V_f is balanced at $V_f = V_g/2$. With this assumption the value of $i_L[n+1]$ can be written as a function of the sampled current, the inductor current slopes and the two duty cycles $d[n]$ and $d[n+1]$,

$$\begin{aligned} i_L[n+1] =& i_L[n-1] + \frac{2V_{ON}}{f_s L} d[n] - \frac{V_{OFF}}{f_s L}(1-2d[n]) + \\ &+ \frac{2V_{ON}}{f_s L} d[n+1] - \frac{V_{OFF}}{f_s L}(1-2d[n+1]) \end{aligned} \tag{5.1}$$

where V_{ON} and V_{OFF} are the voltages across the inductor during the on and off phases respectively. Assuming that the voltage conversion ratio M is less than 0.5, the duty cycle $d[n+1]$ required to regulate the average current value at I_{ref} is solved from (5.1) as

$$d[n+1] = \frac{f_s L}{V_g}\left(I_{ref} - i_L[n-1]\right) + 2M - d[n]. \tag{5.2}$$

The same control equation holds for $M > 0.5$ [47, 50, 54], which extends the validity of (5.2) to $0 < M < 1$[1].

5.1.1 Static stability of the inductor current

The perturbation of the sampled current is defined, as shown in Fig. 5.1, as $\Delta i[n] = i_L[n] - I_{ref}$. In order to assess the static stability of the inductor

[1]Please note that the developed analysis does not takes into account the operating point corresponding to $M = 1/2$.

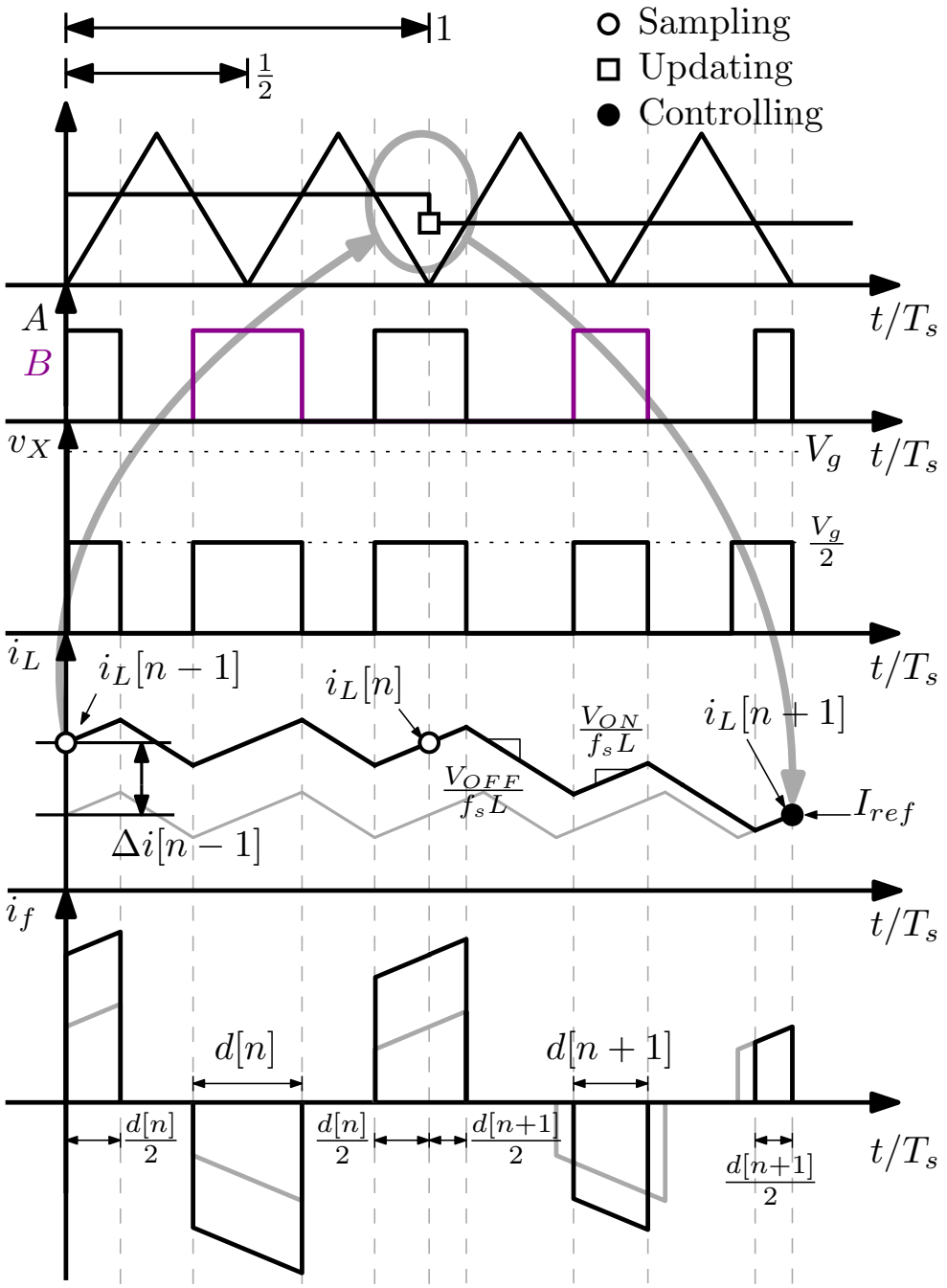


Figure 5.1: *Operation of the single-sampled* average *DPCMC for* $M < 0.5$. *From top to bottom: TTE carrier and modulating signal, control signals, inductor current waveform and FC current.*

current, the time-domain evolution of such perturbation is evaluated [37, 47, 50]. Considering the perturbed waveforms sketched in Fig. 5.1, the regulation error at the end of the $n+1$ cycle can be written as

$$\Delta i[n+1] = \Delta i[n-1] + \frac{2d[n+1]}{f_s L}(V_{OFF} + V_{ON}) - \frac{V_{OFF}}{f_s L}. \tag{5.3}$$

By replacing $d[n+1]$ with (5.2) one obtains

$$\frac{\Delta i[n+1]}{\Delta i[n-1]} = 0. \tag{5.4}$$

Consequently, the error $\Delta i[n+1]$ is zero independently of the value $\Delta i[n-1]$ and of the operating point. Static stability of the inductor current is therefore confirmed and, as expected, the average value of the inductor current is regulated in a dead-beat fashion.

5.1.2 Remarks on the definition of average inductor current

Equation (5.2) implements an average current controller by sampling the inductor current at the carrier valley points. The control equation, the inductor current dynamics and the stability properties change when a different definition of average current is used. This is mentioned in chapter 2 referring to the *two-level* case. Nevertheless, for the 3-LFC Buck case, the inductor current slopes are different and the corresponding stability properties could be different (e.g., as showed in Sec. 4.2). For instance, a different type of average current controller would be obtained by using the following definition of average current [37]

$$\langle i_L(t) \rangle_{T_s} = \frac{1}{T_s} \int_0^{T_s} i_L(\tau) d\tau \tag{5.5}$$

The predictive control equation is therefore developed with the objective to regulate $\langle i_L(t)\rangle_{T_s}$ rather than the sampled current. By doing so one has

$$d[n+1] = \frac{2f_sL}{V_g}\left(I_{ref} - i_L[n-1]\right) + 2M - d[n]. \tag{5.6}$$

By replacing (5.6) in (5.3) one has:

$$\frac{\Delta i[n+1]}{\Delta i[n-1]} = -1, \tag{5.7}$$

resulting in a marginally stable controller. Therefore, different definitions of the *average current* could lead to different control equations and thus, as in this case, to static stability issues on the inductor current operation. From here on, the average current to be controlled by the control equation is always understood to be the midpoint of the current during the on phase. Control with the same static stability properties could be achieved by using the midpoint during the off phase and implementing the modulator with a Leading-traingle edge carrier.

5.2 Multi-sampled average DPCMC

In the single-sampled *average* DPCMC just discussed the sampling/updating frequency is the same as the switching frequency f_s. As discussed in the previous chapter, for an N-level flying-capacitor Buck converter, the output filter is excited with an effective switching rate equal to $(N-1)f_s$, leading to the possibility of implementing wide-bandwidth, multi-sampled versions of the DPCMC. Following a similar approach used for the case of *peak* current control in the previous chapter, the multi-sampled and fast-update multi-sampling *average*current control implementations are now analysed.

5.2.1 *Average* multi-sampled DPCMC

The corresponding waveforms for *average* MS-DPCMC are sketched in Fig. 5.2. Here, the inductor current is sampled/updated twice per switching cycle. Following the same methodology developed in section 5.1 the multi-sampled control equation can be written as

$$d[n+1] = \frac{2f_sL}{V_g}\left(I_{ref} - i_L[n-1]\right) + 2M - d[n]. \tag{5.8}$$

The static stability of the inductor current can be evaluated, as usual, by studying the propagation of the inductor current perturbation

$$\Delta i[n+1] = \Delta i[n-1] + \frac{d[n+1]}{f_sL}(V_{OFF} + V_{ON}) - \frac{V_{OFF}}{f_sL}. \tag{5.9}$$

Replacing (5.8) in (5.9) yields

$$\frac{\Delta i[n+1]}{\Delta i[n-1]} = 0. \tag{5.10}$$

The inductor current is inherently stable and controlled in a dead-beat fashion.

The FC voltage stability can be assessed through the analysis discussed in Sec. 4.3.3. Removal of the small-ripple approximation is once again necessary to capture the actual stability character of v_f. However, the calculation of λ yields *exactly* the same results as the single-sampled case, and therefore the same plots of Fig. 4.7a and Fig. 4.7b, confirming controller stability.

The reason why the same λ as the single-sampled case is obtained in the multi-sampled controller is that the unbalanced steady-state waveforms of the two systems are identical. In fact, duty cycles D_1 and D_2 of the charging and discharging phases remain equal to each other in the multi-sampled case even if $\hat{v}_N \neq 0$, due to the TTE modulation. Consequently, the calculation of I_f for the multi-sampled case is not analytically different than the single-sampled one. Indeed, using the SRA approach the corresponding steady

state of the average MS-DPCMC is the same of the *average* single-sampled DPCMC: the two duty-cycles are equal in steady-state regardless the value of $\hat{v}_N$. This property holds because a trailing triangle carrier is used. Using Fig. 5.2 as a reference, when the modulating is changed, the leading edge of the controlling signal B is moved (delayed) in according with the (5.8). Also the trailing edge of the controlling signal A is moved (anticipated) by the same quantity. This implies that the duration of the half FC charging phase is forced to be equal to the duration of the half FC discharging phase.

Therefore, even in this case Fig. 4.7a and Fig. 4.7b can be used to describe the λ trend and therefore ultimately the stability of the FC voltage.

5.2.2 Fast-update multi-sampled DPCMC

An even faster version of the MS-DPCMC is obtained by updating the modulating signal *immediately* after the sampling event. In practice, the updating event occurs Δt_{calc} seconds after sampling, as soon as the control calculations are concluded. Operation of such *fast-update* MS-DPCMC is exemplified in Fig. 5.3. The control equation for the average fast-update MS-DPCMC can be written as

$$d[n] = \frac{2f_sL}{V_g}\left(I_{ref} - i_L[n-1]\right) + M. \tag{5.11}$$

Fig. 4.10 shows the generic block diagram of *all* fast-update MS-DPCMC. Stability analysis of the fast-update *average* MS-DPCMC proceeds along the same lines as before, yielding the same results. In particular, plots illustrated in Fig. 4.7a and Fig. 4.7b still represent the behaviour of λ, confirming the stability of the controller.

5.3 Extension to *valley* DPCMC

The above analysis provides insight on the stability properties of *average* DPCMC in its single-sampled and multi-sampled versions. This section

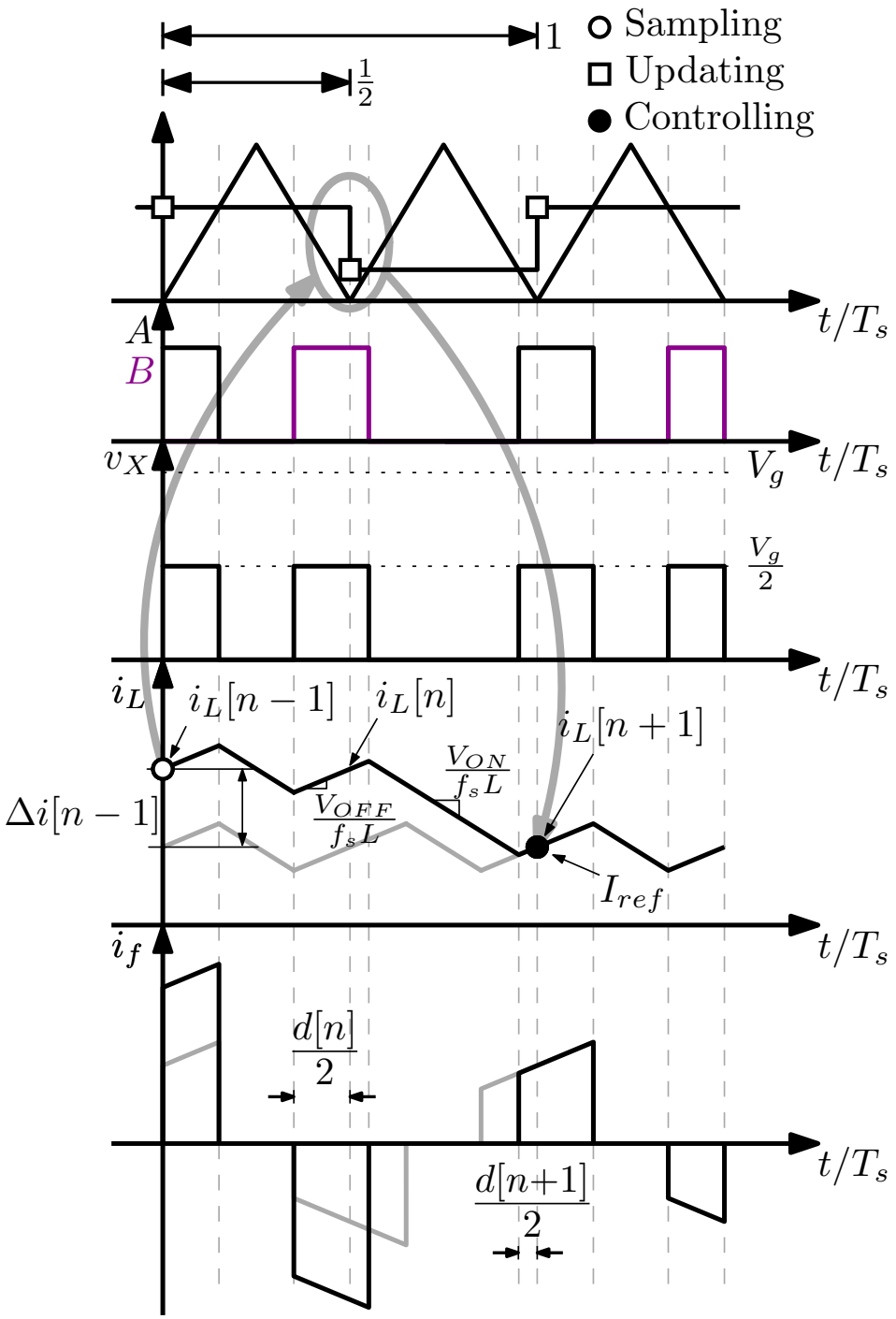


Figure 5.2: *Operation of multi-sampled average DPCMC for* $M < 0.5$

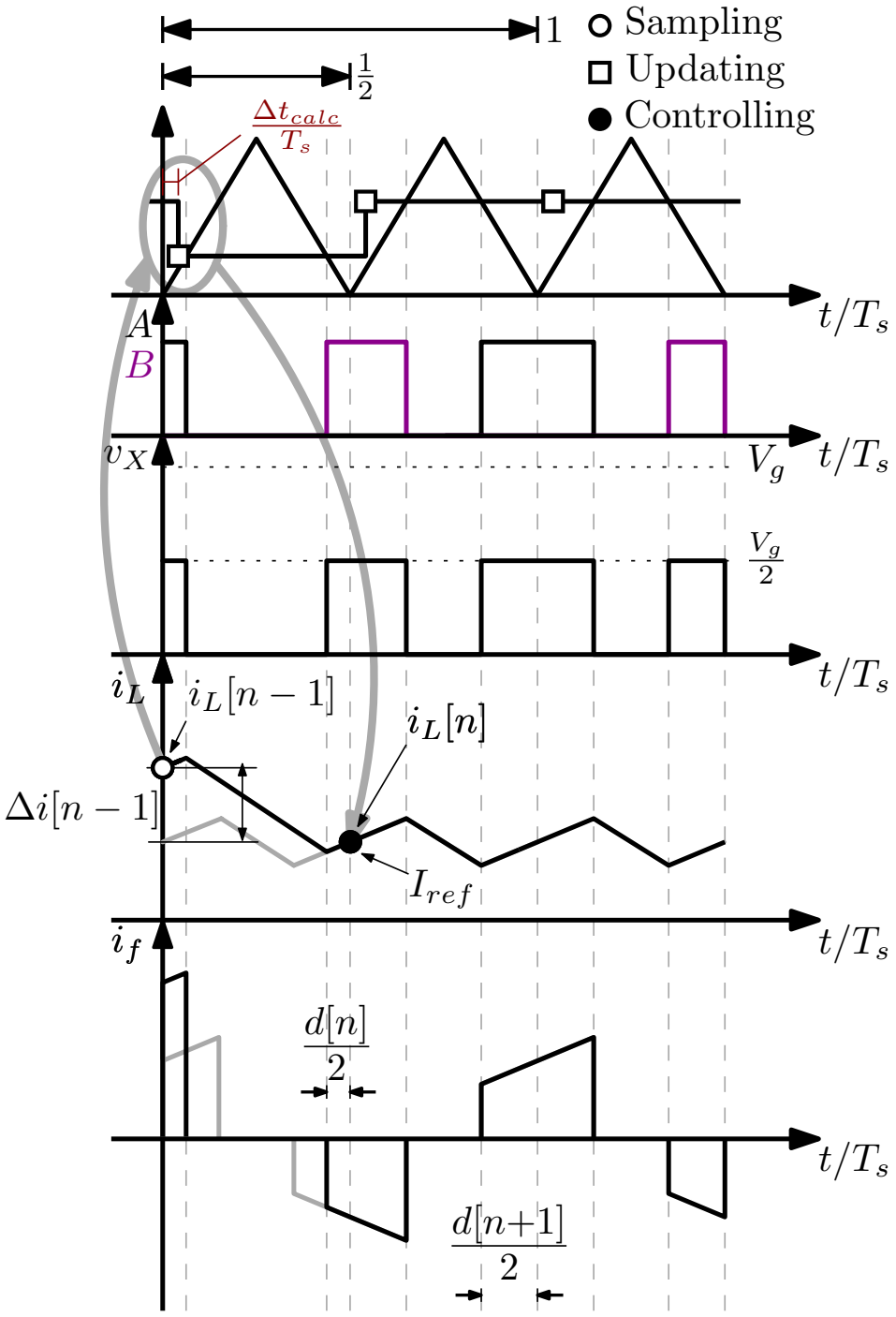


Figure 5.3: *Operation of fast-update multi-sampled* average *DPCMC for* $M < 0.5$

summarizes the findings by combining these results with those disclosed in the previous chapter and in [47,50] in regard to *peak* DPCMC. Furthermore, for completeness, stability results for *valley* DPCMC are also disclosed.

This summary will only address those cases which yield a dead-beat regulation of the sampled inductor current. These are *peak* DPCMC with leading-edge (LE) carrier, *valley* DPCMC with trailing-edge (TE) carrier, and *average* DPCMC with trailing-triangle (TTE) carrier. While none of these cases presents inductor current static instabilities, their FC voltage stability properties strongly depend on the controller type and the DPWM carrier used.

5.3.1 Single-sampled *valley* DPCMC

Fig. 5.4 illustrates the operation of single-sampled *valley* DPCMC based on a trailing-edge carrier. The control equation is equal to (5.2), derived for the *average* single-sampled DPCMC. The inductor current is inherently stable and controlled in a dead-beat fashion. Furthermore, FC voltage stability can be proved once again by removing the SRA approximation according to the approach discussed in Sec. 4.3.3.

5.3.2 Multi-sampled *valley* DPCMC

In regard to the multi-sampled version of the *valley* DPCMC, results indicate that even if the inductor current is inherently stable, FC voltage stability is not always achieved. For instance, assuming $M < 1/2$ and solving the steady-state for $\hat{v}_N \neq 0$, the duty cycles for the charging and discharging phases are respectively given by

$$D_1 = \frac{M}{1+\hat{v}_N} \quad \text{and} \quad D_2 = \frac{M}{1-\hat{v}_N}. \tag{5.12}$$

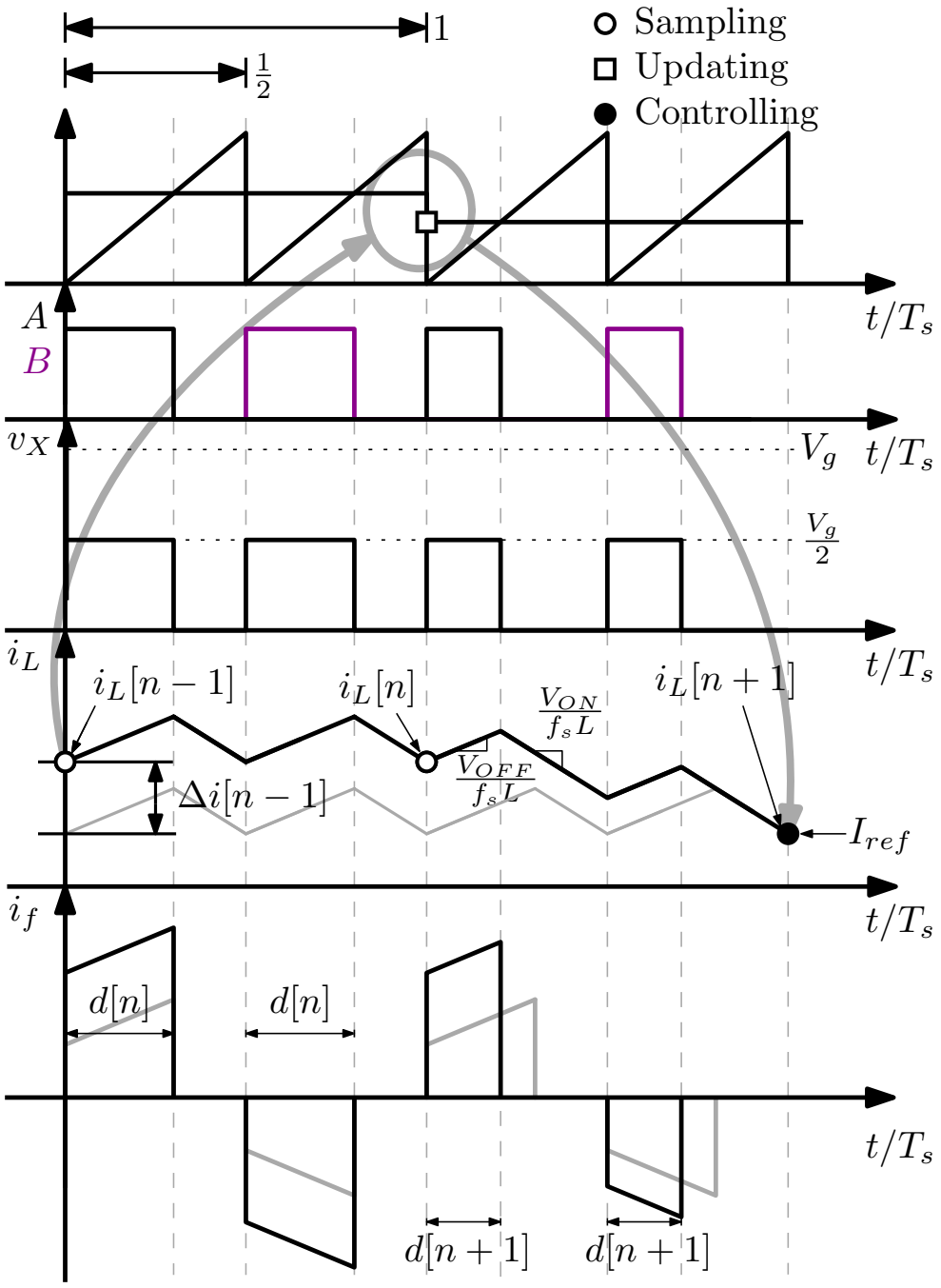


Figure 5.4: *Operation of single-sampled* valley *DPCMC for* $M < 0.5$.

Using this result for computing (4.25) and then (4.19), one obtains

$$\lambda = 4M^2 \left(2 + \frac{1-2M}{k}\right), \tag{5.13}$$

which is always positive. In other words, *valley* MS-DPCMC is always unstable for $M < 1/2$.

For $M > 1/2$ the duty-cycles of the charging and discharging phase are

$$D_1 = \frac{M + \hat{v}_N}{1 + \hat{v}_N} \quad \text{and} \quad D_2 = \frac{M - \hat{v}_N}{1 - \hat{v}_N}. \tag{5.14}$$

Using this expression for computing (4.25) and following the definition (4.19) the expression of λ can be derived. In this case one has

$$\lambda = -4M(1-M)\left(\frac{(M-1)^2}{2Mk} - 1\right), \tag{5.15}$$

Therefore *valley* MS-DPCMC leads to a stable FC voltage when

$$\frac{2 + k - \sqrt{k^2 + 4k}}{2} < M < \frac{2 + k + \sqrt{k^2 + 4k}}{2}.$$

Note that the previous condition implies that stability is lost in open-circuit conditions (i.e., $k = 0$).

5.3.3 Fast-update *valley* MS-DPCMC

As for the fast-update *valley* MS-DPCMC, solving the steady-state under the small-ripple approximation and following the disclosed approach, one has conditional stability expressed by $M < k$ if $M < 1/2$. The *valley* fast-update MS-DPCMC with $M > 1/2$ leads to a conditional stability expressed by

$$M < \frac{2 + k - \sqrt{k^2 + 4k}}{2} \ \vee \ M > \frac{2 + k + \sqrt{k^2 + 4k}}{2}.$$

Once again, stability is lost in open-circuit operation.

5.4 Flying-capacitor voltage stability summary

Tab. 5.1 and Tab. 4.3 respectively summarizes the stability analysis results developed in this and in the previous chapter. The following general remarks can be drawn:

- Single-sampled *peak*, *valley* or *average* always guarantee FC voltage stability.
- Multi-sampled *average* DPCMC also guarantees FC voltage stability. In particular, the fast-update option strongly improves the dynamic capabilities of the converter.
- Multi-sampled *peak* DPCMC implemented using the fast-update approach is always stable for $M < 0.5$. Although stability is not achieved throughout the entire range of M, this option is nonetheless extremely interesting in a number of relevant cases – e.g., automotive scenarios – in which M is already constrained to be small by the application.

5.5 Simulation Results

The foregoing analysis is validated in simulation on the 500 kHz, 12 V-to-1.5 V, 500 mA 3LFC-Buck case study illustrated in the previous chapter. Tab. 4.1 reports the values of the output filter and the other converter parameters.

5.5.1 Simulation results for the *average* DPCMC

The *average* DPCMC is first simulated in order to assess the dynamic properties of its single-sampled and multi-sampled versions. Fig. 5.5 illustrates a simulated transient response to a load step-down event. As expected, the fast-update MS-DPCMC achieves a much faster dynamics and smaller overshoot with respect to the single-sampled implementation. Fig. 5.6 shows

Table 5.1: *Expressions of λ and FC voltage stability properties for* average *and* valley *DPCMC.*
(*) Inequalities are proved using the more accurate FC stability analysis presented in 4.3.3.

		average DPCMC	*valley* DPCMC
DPCMC	$\forall M$	$\lambda < 0^*$ (stable)	$\lambda < 0^*$ (stable)
MS-DPCMC	$M < 1/2$	$\lambda < 0^*$ (stable)	$\lambda = 4M^2\left(2 + \frac{(1-2M)}{k}\right)$ (unstable)
	$M > 1/2$	$\lambda < 0^*$ (stable)	$\lambda = 4(M^2 - M)\left(1 - \frac{(M-1)^2}{Mk}\right)$ (conditionally stable)
fast-update MS-DPCMC	$M < 1/2$	$\lambda < 0^*$ (stable)	$\lambda = -4M^2\left(1 - \frac{M}{k}\right)$ (conditionally stable)
	$M > 1/2$	$\lambda < 0^*$ (stable)	$\lambda = 4(M^2 - M)\left(\frac{(M-1)^2}{Mk} - 1\right)$ (conditionally stable)

the simulation results for the three proposed implementations. Even if the MS-DPCMC and the fast-update MS-DPCMC have the same sampling frequency, there is a substantial difference between the two techniques, in that in the fast-update the updating instant takes place in the same cycle as the sampling one. This implies that the inductor current error is corrected in $T_s/2$ in the fast-update implementation while in the simple MS-DPCMC is addressed in T_s. This is the main reason why the outer voltage-loop bandwidth, shown in the last row of Tab. 4.1, can be significantly extended with respect to the bandwidth of the MS-DPCMC.

Since the *average* DPCMC is stable for all its implementations and for

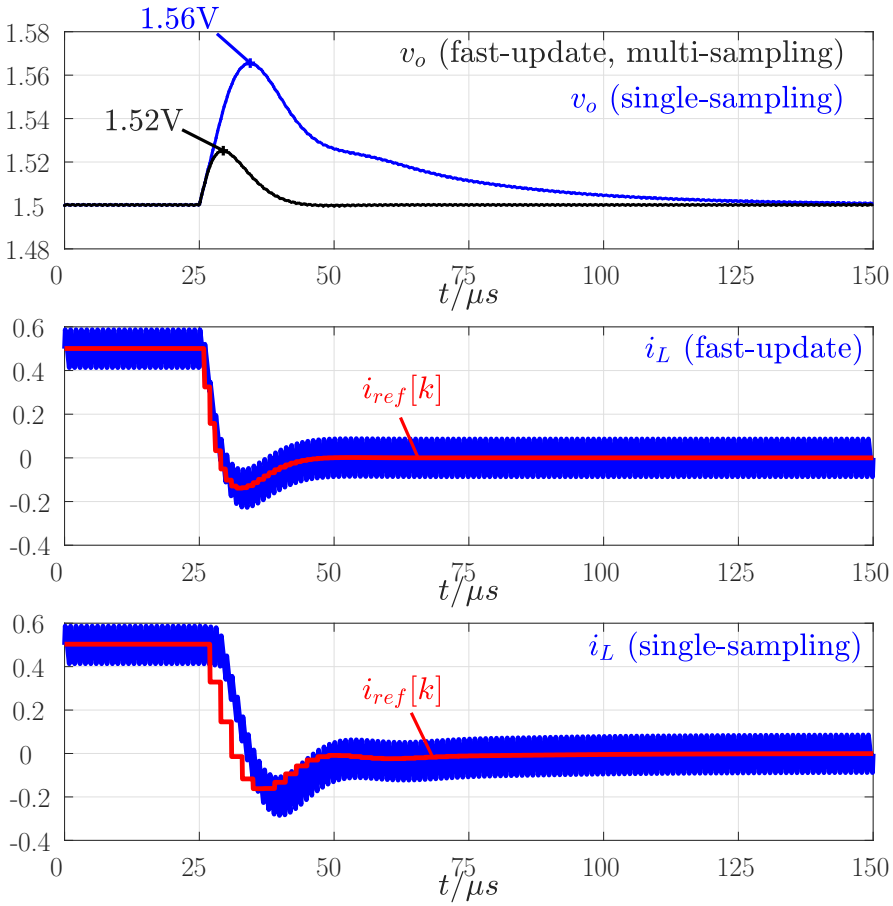


Figure 5.5: Average *DPCMC*: *simulated response to a* 500 mA → 0 *load step; (top) output voltage response, single-sampled vs. fast-update multi-sampled case; (middle) inductor current response and current loop reference signal for the fast-update controller; (bottom) inductor current response and current loop reference signal for the single-sampled controller.*

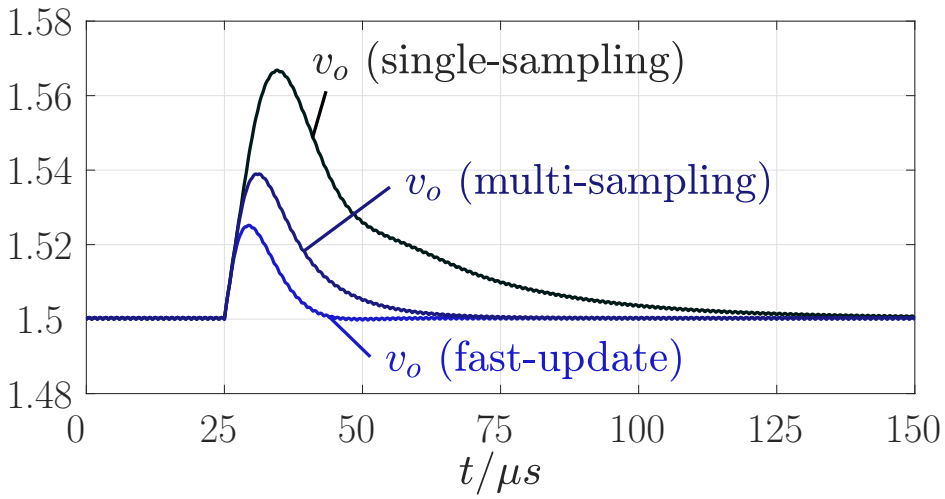


Figure 5.6: Average *DPCMC: simulated output voltage response to a* $500mA \rightarrow 0$ *load step; single-sampled, multi-sampled and fast-update multi-sampled cases.*

all values of M, a simulation test with the fast-update *average* MS-DPCMC for $M > 1/2$ is now analysed. Fig. 5.7 reports the closed-loop response of this fast-update controller to a 0 A-to-500 mA load-step variation. In order to test the inductor current and the FC voltage stability for the operating conditions $M > 1/2$, the average output voltage is regulated at $V_o = 7\,\text{V}$. The test confirms that the fast-update *average* MS-DPCMC guarantees stability of both the inductor current and FC voltage, in agreement with the developed theory.

5.5.2 Simulation results for the *valley* DPCMC

Fig. 5.8 illustrates a simulation transient response to a load step-down event $500\,\text{mA} \rightarrow 0$ applied at $t = 25\,\mu\text{s}$ for the fast-update *valley* MS-DPCMC. The simulation confirms the open-circuit instability previously proved. Indeed, when k tends to zero, the value of λ become positive and therefore FC stability is lost for this fast-update *valley* control-technique. Precisely, prior to the load step one has $k = 2.17$, satisfying the stability condition $M < k$. Conversely, after the load step one has $k = 0$ and there-

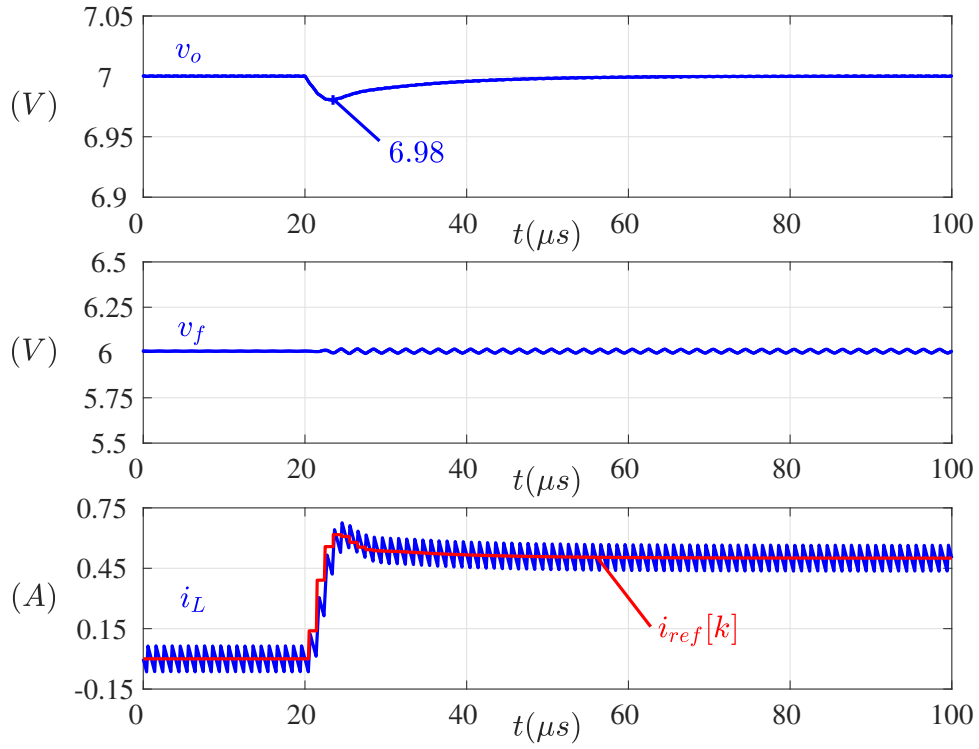


Figure 5.7: *Fast-update multi-sampled* average *DPCMC with TTE carrier: simulated response to a* $0 \rightarrow 500\,\text{mA}$ *load-step, for* $M > 1/2$. *(top) output voltage, (middle) FC voltage, (bottom) inductor current and reference current.*

fore $\lambda > 0$.

5.5.3 Sensitivity to timing mismatches

As done for the *peak* DPCMC in the previous chapter, in order to assess the impact of timing mismatches in the control signals on FC voltage balancing, a Monte Carlo simulation is carried out. For each simulation run, a uniformly distributed $\pm 5\%$ variation of the gate drivers propagation delay is randomly generated. Simulations are performed both closed-loop and open-loop, with the open-loop modulating signal of the DPWM adjusted to produce, in steady state, the nominal output voltage $V_o = 1.5\,\text{V}$. After each simulation run the relative steady-state imbalance, defined as (4.43), is

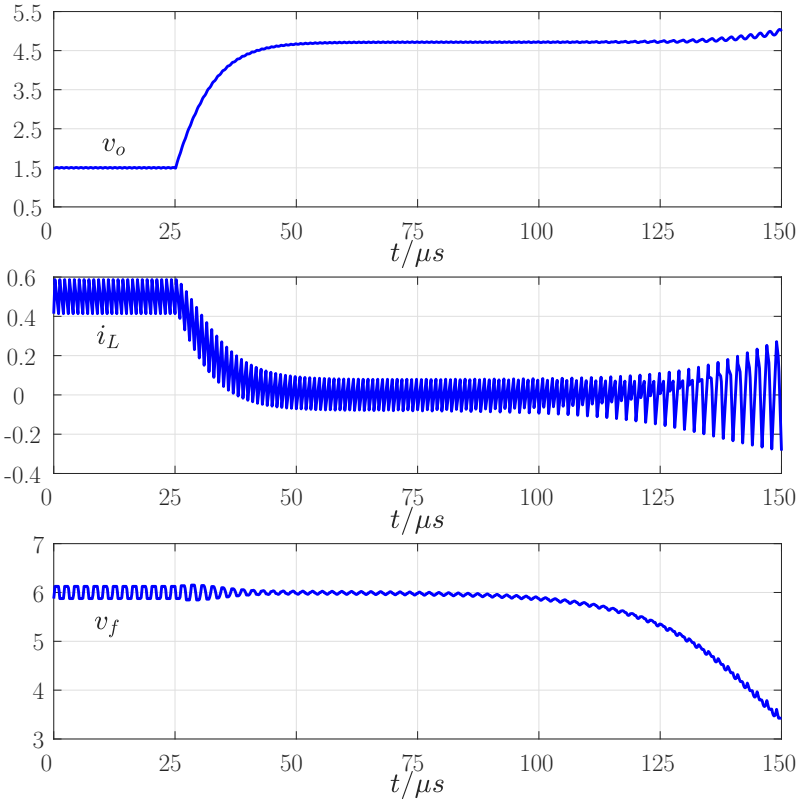


Figure 5.8: Valley *fast-update MS-DPCMC: simulated response to a* 500 mA $\rightarrow$ 0 *load step; (top) output voltage, (middle) inductor current and (bottom) flying-capacitor voltage.*

recorded.

Since all proposed *average* DPCMC leads to a stable FC operation, the comparison between the two multi-sampled implementations is possible. Monte Carlo analysis and comparison between the multi-sampled and fast-update multi-sampled *average* DPCMC is shown in Fig. 5.9. As seen, multi-sampled *average* controllers also exhibit some degree of self-balancing, although less marked than the *peak* case depicted in the previous chapter, and with the multi-sampled case being slightly more robust than the fast-update one: the worst-case FC voltage imbalance δV_f is always less than 2.6% in the former, and less than 6% in the latter. Nonetheless, the closed-loop imbalance is strongly improved over the open-loop condition in all cases.

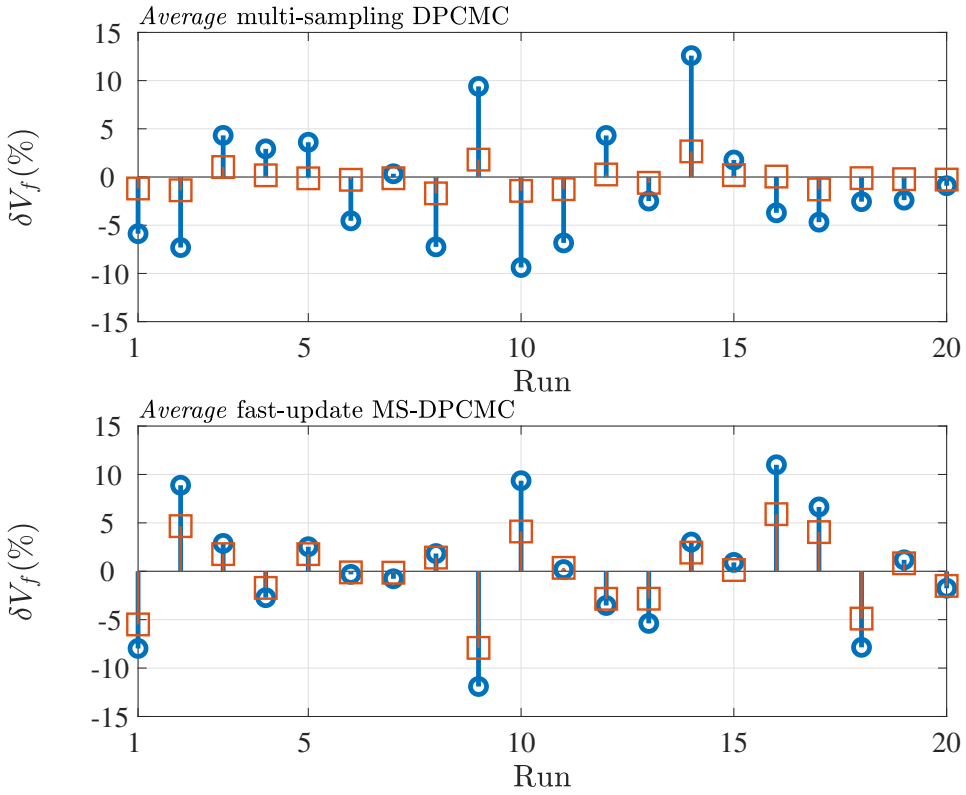


Figure 5.9: *Open-loop (circles) vs. closed-loop (squares) Monte Carlo simulation of (top) multi-sampled* average *DPCMC and (bottom) fast-update multi-sampled* average *DPCMC.*

Results presented in this section can be summarized as follows:

- Single-sampled DPCMC techniques exhibit a closed-loop sensitivity to timing mismatches which is identical to that of the open-loop converter.
- When stable, multi-sampled *peak* and *valley* DPCMC (either in their simple or fast-update forms) exhibit strong self-balancing capabilities, resulting in a marked improvement of the converter sensitivity to timing mismatches over the open-loop condition.
- Multi-sampled *average* DPCMC also exhibit self-balancing properties, although to a lesser extent than their *peak* or *valley* counterparts, and with the regular multi-sampled implementation being slightly less sensitive than the fast-update one.

5.6 Experimental Results

The custom prototype of the case study summarized in Tab. 4.1 and shown on 4.26 is used for the experimental validation of single-sampled and fast-update multi sampled *average* DPCMC control approaches previously discussed. Once again, the digital controller is VHDL-coded and synthesized on a commercial FPGA board interfaced with the 3LFC-Buck prototype. The experimental response of the single-sampled average DPCMC to a load-step variation is reported in Fig. 5.10. As predicted theoretically, the FC voltage remains stable throughout the transient. The same transient response is illustrated in Fig. 5.11 for the fast-update MS-DPCMC, confirming the much faster dynamics compared to the single-sampled DPCMC while maintaining a stable FC voltage.

Unlike the fast-update multi-sampled *peak* DPCMC, fast-update multi-sampled *average* DPCMC control is predicted to be stable for $M > 1/2$ as well. The experimental test reported in Fig. 5.12 documents the closed-loop response of the fast-update multi-sampled *average* DPCMC to a 0 A-to-500 mA load-step variation for $V_o = 7\,\mathrm{V}$. Main conclusions regarding

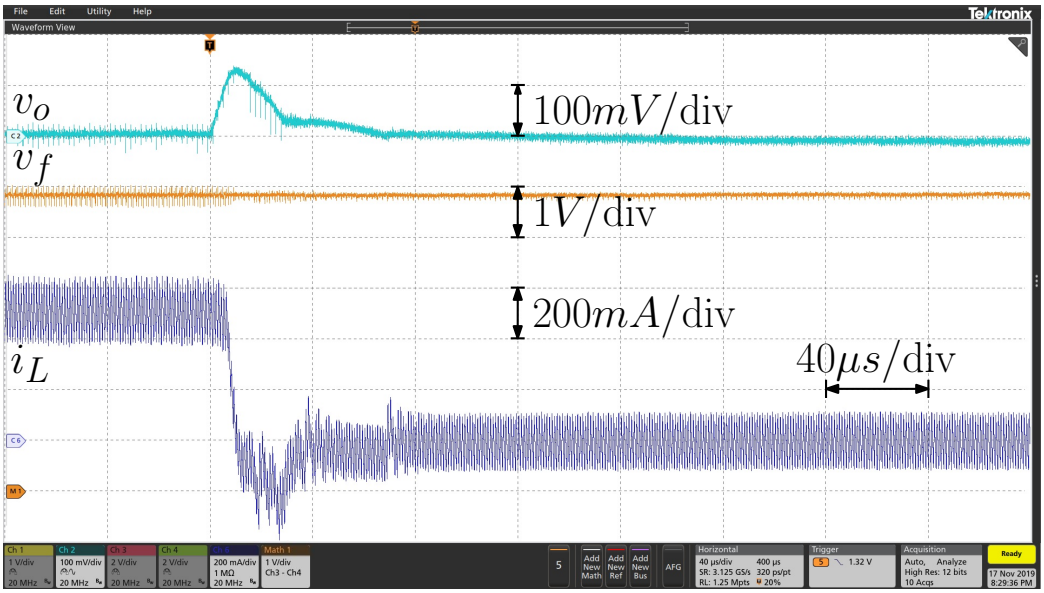


Figure 5.10: *Experimental response to a* $500\,\text{mA} \rightarrow 0$ *load step with the single-sampled* average *DPCMC; (top) output voltage* v_o *(*$100\,\text{mV}/\textit{div}$*, ac-coupled); (middle) flying-capacitor voltage* v_f *(*$6\,\text{V}/\textit{div}$*); (bottom) inductor current* i_L *(*$200\,\text{mA}/\textit{div}$*).*

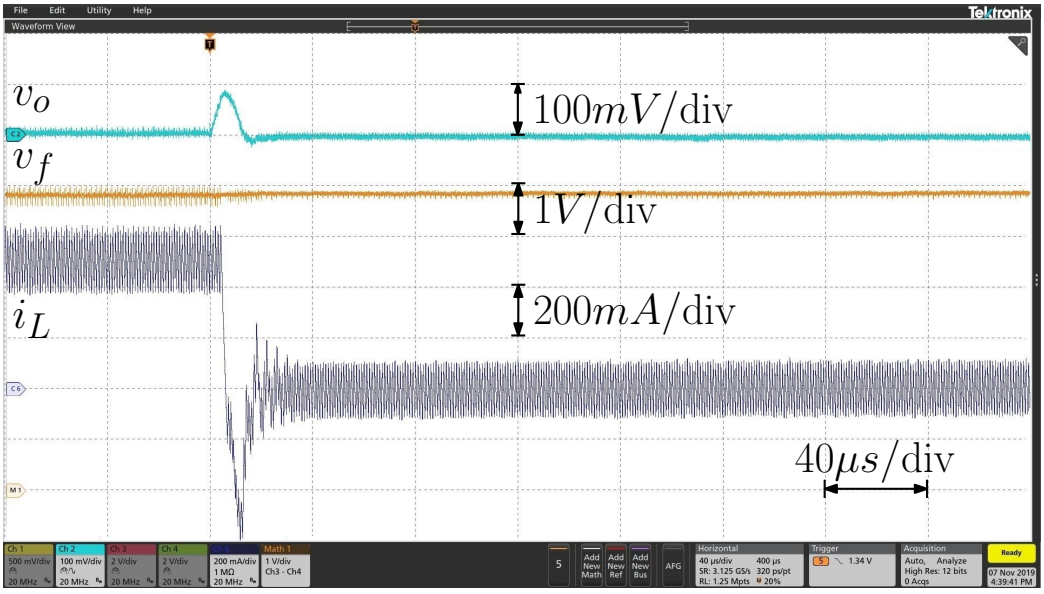


Figure 5.11: *Experimental response to a* $500\,\text{mA} \rightarrow 0$ *load step with the fast-update multi-sampled* average *DPCMC; (top) output voltage* v_o *(*$100\,\text{mV}/\textit{div}$*, ac-coupled); (middle) flying-capacitor voltage* v_f *(*$6\,\text{V}/\textit{div}$*); (bottom) inductor current* i_L *(*$200\,\text{mA}/\textit{div}$*).*

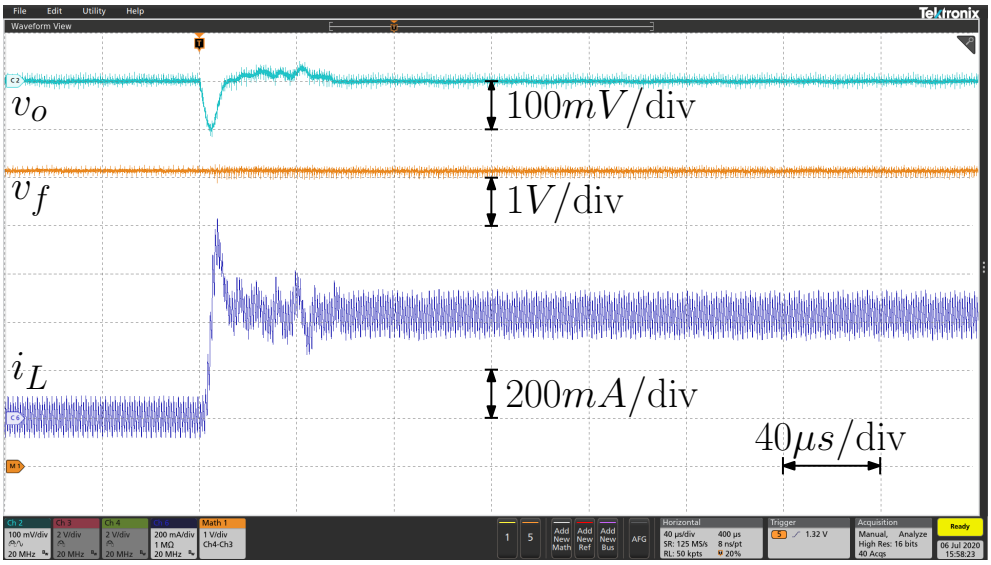


Figure 5.12: *Experimental response of fast-update multi-sampled* average *DPCMC to a* $500\,\text{mA} \rightarrow 0$ *load step and for* $M = 7/12$*. Output voltage* v_o *(ac-coupled):* $100\,\text{mV/div}$*; flying-capacitor voltage* v_f*:* $1\,\text{V/div}$*; inductor current* i_L*:* $200\,\text{mA/div}$.

FC voltage stability and dynamic capabilities of the controller are therefore experimentally verified for both $M < 1/2$ and $M > 1/2$ cases.

Open-circuit instability theoretically predicted for multi-sampled *valley* controllers is verified in Fig. 5.13. Specifically, the figure reports the experimental behaviour of fast-update *valley* MS-DPCMC when, starting from an initially open-loop situation, the inner inductor current-loop is suddenly closed. In the measurement, the converter operates in open-circuit conditions. Theoretical instability predicted in Tab. 5.1 is confirmed by the onset of FC voltage runaway as soon as the DPCMC loop is closed.

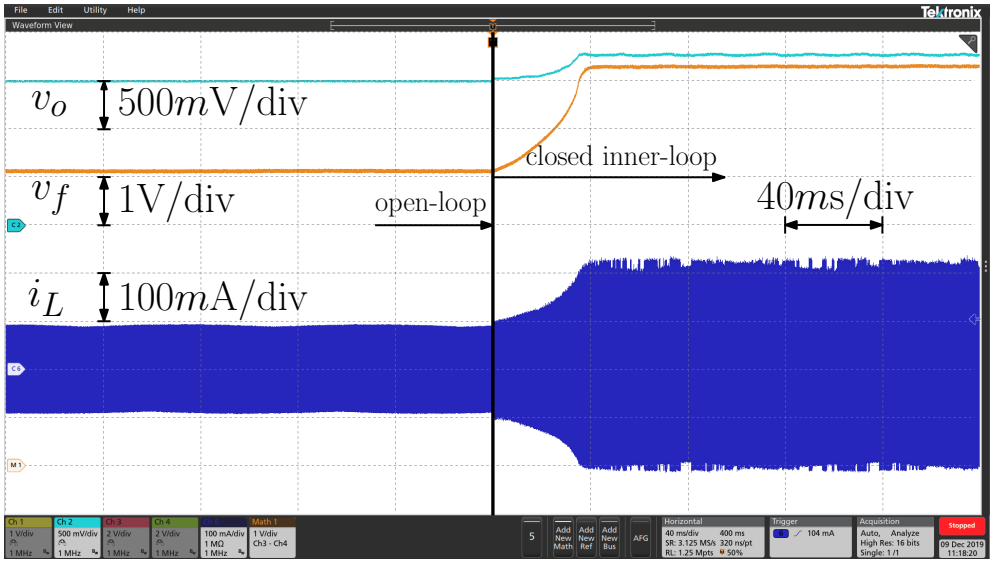


Figure 5.13: *Experimental open-circuit response of fast-update multi-sampled* valley *DPCMC when the inner current loop is suddenly closed from an initially open-loop condition. Output voltage* v_o*:* 500 mV/div*; flying capacitor voltage* v_f*:* 1 V/div*; inductor current* i_L*:* 100 mA/div.

Chapter 6

General approach for the stability analysis of N-LFC Buck Converter with DPCMC

The proposed FC voltage stability analysis can be extended to the generic N-LFC Buck converter. The major difficulty in extending the approach used in [47, 50, 54] is related to the study of the $N-2$ FCs voltages. Indeed, the stability properties of the inductor current remain unchanged for the carrier and control point pairings considered in this study. This Chapter proposed a unified analysis approach for the generic N-LFC Buck converter operating with DPCMC.

6.1 Digital predictive current-controls for the generic N-L case

The inductor current stability properties of the N-LFC Buck converter with *peak* DPCMC are analysed in the following. The circuit sketched in Fig. 3.4 and the DPWM implementation exemplified in Fig. 3.5a are used as

a reference. Following the approach used in Sec. 4, for $mode_1$ one has

$$\begin{aligned} i_L[n+1] =& i_L[n-1] - (N-1)\frac{V_{OFF}}{f_s L}\left(\frac{1}{N-1} - d[n]\right) + (N-1)\frac{V_{ON}}{f_s L}d[n] + \\ & - (N-1)\frac{V_{OFF}}{f_s L}\left(\frac{1}{N-1} - d[n+1]\right) + (N-1)\frac{V_{ON}}{f_s L}d[n+1]. \end{aligned} \tag{6.1}$$

For generic N, inductor voltages V_{ON} and V_{OFF} can be written as

$$\begin{aligned} V_{ON} &= \frac{V_g}{N-1} - V_o = \frac{V_g}{N-1}\left(1 - (N-1)M\right), \\ V_{OFF} &= V_o = MV_g \end{aligned} \tag{6.2}$$

From (6.1), by imposing that the new duty cycle $d[n+1]$ regulates the peak current at I_{ref}, one solves for $d[n+1]$ and obtains the control equation

$$\boxed{d[n+1] = \frac{f_s L}{V_g}\left(I_{ref} - i_L[n-1]\right) + 2M - d[n]}. \tag{6.3}$$

Control equation (6.3) holds for all operating modes[1].

Using the same approach, the control equations for the proposed multi-sampled controllers can be derived. For the *peak* MS-DPCMC one has

$$\boxed{d[n+1] = \frac{(N-1)f_s L}{V_g}\left(I_{ref} - i_L[n-1]\right) + 2M - d[n]}, \tag{6.4}$$

while for the fast-update *peak* MS-DPCMC

$$\boxed{d[n] = \frac{(N-1)f_s L}{V_g}\left(I_{ref} - i_L[n-1]\right) + M}. \tag{6.5}$$

Control equations (6.3) (6.4) and (6.5) hold for all $N-1$ operating modes and

[1]Please refer to Appendix A

for all types of controllers (i.e., *peak*, *valley* and *average* current controller).

6.1.1 Static stability on the inductor current and dead-beat behaviour

Inductor current stability and dead-beat behaviour are analysed as regard the general case. The perturbation of the sampled current is defined as $\Delta i[n] = i_L[n] - I_{ref}$. In order to assess the static stability of the inductor current, the time-domain evolution of $\Delta i[n]$ is analysed. The regulation error at the end of the $n+1$ cycle[2] can be generally written as

$$\Delta i[n+1] = \Delta i[n-1] + \frac{(N-1)d[n+1]}{f_s L}(V_{OFF} + V_{ON}) - \frac{V_{OFF}}{f_s L}. \tag{6.6}$$

By replacing $d[n+1]$ with (6.3) one obtains

$$\frac{\Delta i[n+1]}{\Delta i[n-1]} = 0. \tag{6.7}$$

As in the 3-L case, the inductor current error $\Delta i[n+1]$ is zero regardless the value of $\Delta i[n-1]$ and the operating point. Static stability of the inductor current is therefore confirmed and the peak inductor current value is regulated in a dead-beat fashion. The same results also apply to all operating modes, for the proposed multi-sampled implementations and to *valley* and *average* current-controllers.

6.2 Towards a general approach for the generic N-LFC Buck operating with DPCMC

The most challenging aspect of the proposed generalization regards the FCs voltages stability. The number of state variables involved in the problem depends on the number of levels. Precisely for the generic N-LFC Buck

[2]Waveforms in Fig. 22 can be used as a reference

converter, there are exactly N state variables: v_o, i_L, as in the traditional *two-level* Buck converter and the $N-2$ FCs voltages v_{f_i}. Therefore the complexity of the problem increases as N. The approach discussed in [49] while rigorous and exhaustive is extremely complicated to be used in this circumstance. The general stability analysis approach proposed in this thesis follows a simpler strategy based on the approach disclosed in Sec. 4.3. Precisely, the approach proposed about the 3-L case is extended and generalized. For the 3-LFC Buck converter, the stability character of the FC voltage is determined by studying the sign of the parameter λ defined as (4.19). The general case is much more complicated and needs some additional analytical tools. In order to obtain a simpler treatment, the following subsection details the 4-LFC Buck converter operating with fast-update *peak* MS-DPCMC. The developed theory is therefore extended to the general case.

6.2.1 Analysis of 4-LFC Buck operating in $mode_1$ with fast-update *peak* MS-DPCMC

The steady-state operation of the 4-LFC Buck converter with fast-update *peak* MS-DPCMC is shown on Fig. 6.1. From top to bottom the figure sketches the modulating signal with the LE carrier, the control signals, the inductor and FC currents. This general stability analysis requires the same hypotheses used in Sec. 4.3. SRA hypothesis is used for the input and output voltages and for FCs voltages. The resulting inductor current waveform is therefore piecewise linear.

The following steps describe the procedure to obtain the steady-state solution.

– All inductor current slopes are written as a function of FCs voltages, converter parameters and the operating point. In order to obtain simplest and general equations, the current axes are normalized with re-

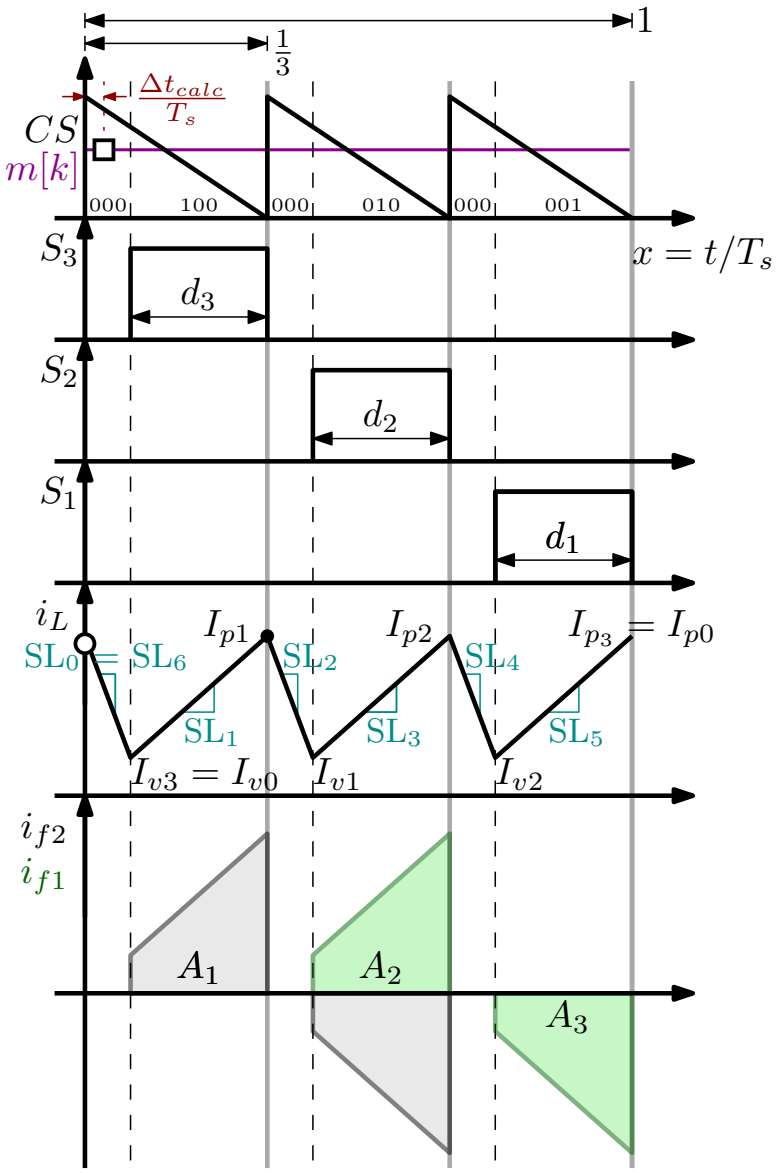


Figure 6.1: *Steady-state waveforms of the 4-LFC Buck converter operating with fast-update* peak *MS-DPCMC in* $mode_1$.

spect to the quantity $\frac{V_g}{(N-1)Lf_s}$. For $mode_1$ one has

$$\begin{aligned} SL_1 =& \left(\frac{V_g}{3Lf_s}\right)^{-1}\left(\frac{1}{Lf_s}\left(V_g - V_{f2} - v_o\right)\right) = 1 - \hat{v}_{N_2} - 3M \\ SL_3 =& 1 + v_{N_2} - v_{N_1} - 3M \\ SL_5 =& 1 - v_{N_1} - 3M \\ SL_0 =& SL_2 = SL_4 = -3M. \end{aligned} \tag{6.8}$$

Since the time axis is normalized with respect to the switching period T_s, the six normalized current slopes SL_i result in pure numbers. Inductor current slopes in (6.8) depend on the operating point (i.e., M) and on the normalized FCs voltage perturbations (i.e., $\hat{v}_{N_1}$ and $\hat{v}_{N_2}$).

– The *normalized* peak inductor current expressions are written as a function of the duty-cycles d_1, d_2, d_3 and the current slopes

$$\begin{aligned} I_{p1} = I_{p0} + SL_0\left(\frac{1}{3} - d_3\right) SL_1 d_3 =& I_{p0} + \frac{SL_0}{3} + d_3\left(SL_1 - SL_0\right) \\ I_{p2} =& I_{p1} + \frac{SL_2}{3} + d_2\left(SL_3 - SL_2\right) \\ I_{p3} = I_{p0} =& I_{p2} + \frac{SL_4}{3} + d_2\left(SL_5 - SL_4\right). \end{aligned} \tag{6.9}$$

– With the normalizations introduced in this section, the control equations (6.5) can be rewritten in a simpler form

$$\begin{aligned} d_3 =& I_{\mathrm{ref}_N} - I_{p0} + M \\ d_2 =& I_{\mathrm{ref}_N} - I_{p1} + M \\ d_1 =& I_{\mathrm{ref}_N} - I_{p2} + M. \end{aligned} \tag{6.10}$$

The normalized reference inductor current I_{ref_N} is defined as

$$I_{\mathrm{ref}_N} \triangleq \left(I_o + \frac{\Delta I_L}{2}\right)\left(\frac{V_g}{3Lf_s}\right)^{-1} = I_{o_N} + \left(1 - 3M\right)\frac{M}{2}, \tag{6.11}$$

whit $I_{o_N} = \dfrac{I_o}{V_g/(3Lf_s)}$.

– Equations (6.9) and (6.10) are solved with respect to the inductor current peaks and the duty-cycles. Knowing those, expressions of the normalized inductor current valleys can be founded

$$\begin{aligned} I_{v0} =& I_{p0} + SL_0\left(\frac{1}{3} - d_3\right) \\ I_{v1} =& I_{p1} + SL_2\left(\frac{1}{3} - d_2\right) \\ I_{v2} =& I_{p2} + SL_4\left(\frac{1}{3} - d_1\right). \end{aligned} \tag{6.12}$$

– Areas A_1, A_2 and A_3 defined as in Fig. 6.1 can be easily calculated using (6.9), (6.12) and the three duty cycles. Therefore, average FCs currents can be finally written as follows

$$\begin{cases} I_{f_2}\left(\hat{v}_{N_1}, \hat{v}_{N_2}\right) = & A_1 - A_2 \\ I_{f_1}\left(\hat{v}_{N_1}, \hat{v}_{N_2}\right) = & A_2 - A_3\ . \end{cases} \tag{6.13}$$

The average FCs currents in (6.13) are function of the operating point, the converter parameters and the FCs voltage perturbations.

– Expressions (6.13) can be approximated around the operating point obtained for $\hat{v}_{N_1} = \hat{v}_{N_1} = 0$. By using the first order Taylor-series approximation one has

$$\begin{cases} I_{f_2} \approx & I_{f_2}(0,0) + \hat{v}_{N_1}\left(\left.\dfrac{\partial I_{f_2}}{\partial \hat{v}_{N_1}}\right|_{\hat{v}_{N_1}=\hat{v}_{N_1}=0}\right) + \hat{v}_{N_2}\left(\left.\dfrac{\partial I_{f_2}}{\partial \hat{v}_{N_2}}\right|_{\hat{v}_{N_1}=\hat{v}_{N_1}=0}\right) \\ I_{f_1} \approx & I_{f_1}(0,0) + \hat{v}_{N_1}\left(\left.\dfrac{\partial I_{f_1}}{\partial \hat{v}_{N_1}}\right|_{\hat{v}_{N_1}=\hat{v}_{N_1}=0}\right) + \hat{v}_{N_2}\left(\left.\dfrac{\partial I_{f_1}}{\partial \hat{v}_{N_2}}\right|_{\hat{v}_{N_1}=\hat{v}_{N_1}=0}\right). \end{cases} \tag{6.14}$$

The terms $I_{f_2}(0,0)$ and $I_{f_1}(0,0)$ are always zero. Therefore the system

(6.14) can be written in the following matrix form

$$\boldsymbol{I_f} = \boldsymbol{\Omega} \cdot \boldsymbol{v_N}, \tag{6.15}$$

where $\boldsymbol{I_f}$ is the vector containing the normalized average FCs currents, $\boldsymbol{v_N}$ is the vector containing the normalized FCs voltage perturbations and the matrix $\boldsymbol{\Omega}$ is defined as

$$\boldsymbol{\Omega} \triangleq \begin{pmatrix} \left.\dfrac{\partial I_{f_2}}{\partial \hat{v}_{N_2}}\right|_{\hat{v}_{N_1}=\hat{v}_{N_1}=0} & \left.\dfrac{\partial I_{f_2}}{\partial \hat{v}_{N_1}}\right|_{\hat{v}_{N_1}=\hat{v}_{N_1}=0} \\ \left.\dfrac{\partial I_{f_1}}{\partial \hat{v}_{N_2}}\right|_{\hat{v}_{N_1}=\hat{v}_{N_1}=0} & \left.\dfrac{\partial I_{f_1}}{\partial \hat{v}_{N_1}}\right|_{\hat{v}_{N_1}=\hat{v}_{N_1}=0} \end{pmatrix}. \tag{6.16}$$

From the approach disclosed in Sec. 4.3.1, the general form of (4.17) is therefore obtained as

$$\boldsymbol{K} \cdot \frac{d\boldsymbol{v}_N}{dx} \approx \boldsymbol{I}_f = \boldsymbol{\Omega} \cdot \boldsymbol{v}_N. \tag{6.17}$$

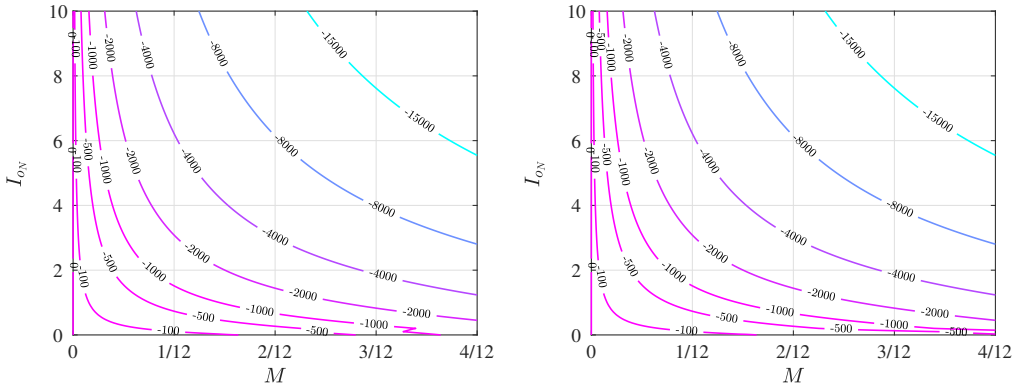
The FCs voltages stability character can be determined by studying the signs of the real part of the eigenvalues of $\boldsymbol{K}^{-1}\boldsymbol{\Omega}$.

The analytical expressions of $\boldsymbol{K}^{-1}\boldsymbol{\Omega}$, for the 4-LFC Buck converter operating with fast-update *peak* MS-DPCMC can be written as

$$\boldsymbol{\Omega} = -M \begin{pmatrix} I_{o_N} + \dfrac{M}{2}(1+3M) & I_{o_N} + \dfrac{M}{2}(3M-2) \\ -2I_{o_N} + \dfrac{M}{2}(1-6M) & I_{o_N} + \dfrac{M}{2}(1+3M) \end{pmatrix}, \tag{6.18}$$

while the diagonal matrix $\boldsymbol{K}$ is defined as

$$\boldsymbol{K} \triangleq f_s^2\, L \begin{pmatrix} C_{f_2} & 0 \\ 0 & C_{f_1} \end{pmatrix}. \tag{6.19}$$



(a) (b)

Figure 6.2: *Contour plot of the real part of eigenvalues ω_1 (on left) and ω_2 (on right) of $\boldsymbol{K}^{-1}\boldsymbol{\Omega}$ with respect to M (on x-axis) and I_{o_N} (on y-axis).*

Summary plots are proposed in the following. Fig. 6.2 shows the contour plot of the real part of the eigenvalues of $\boldsymbol{K}^{-1}\boldsymbol{\Omega}$ obtained for $C_{f_1} = C_{f_2}$. The x-axis represents the voltage conversion ratio M while the y-axis the normalized output current I_{o_N}. Both eigenvalues exhibit a negative real part in the overall range[3].

The proposed FCs voltages stability analysis can be used to analyse the impact of different flying-capacitor values. This analysis is straightforward for the 4-L case. Indeed, for finite and non-null FCs values, the matrix $\boldsymbol{K}$ can be written as follows

$$\boldsymbol{K} = LC_{f_2}\, f_s^2 \begin{pmatrix} 1 & 0 \\ 0 & \dfrac{C_{f_1}}{C_{f_2}} \end{pmatrix}. \tag{6.20}$$

The FCs voltages stability character is determined by studying the sign of

[3]The case under analysis is the 4-LFC Buck converter in $mode_1$ (i.e. $0 < M < \frac{1}{3}$).

the real part of the eigenvalues of the following matrix

$$-\frac{M}{LC_{f_2}\, f_s^2}\begin{pmatrix} 1 & 0 \\ 0 & \dfrac{C_{f_2}}{C_{f_1}} \end{pmatrix}\begin{pmatrix} I_{o_N}+\dfrac{M}{2}(1+3M) & I_{o_N}+\dfrac{M}{2}(3M-2) \\ -2I_{o_N}+\dfrac{M}{2}(1-6M) & I_{o_N}+\dfrac{M}{2}(1+3M) \end{pmatrix}. \tag{6.21}$$

The multiplicative constant $\frac{M}{LC_{f_2}\, f_s^2}$ is always positive and does not change the stability properties of the system. The *analytical* study of (6.21) proves that for all values of $C_N = C_{f_2}/C_{f_1}$, M and I_{o_N}, the real part of the two eigenvalues is always negative. Therefore, stability is guaranteed throughout $mode_1$ also for $C_{f_1} \neq C_{f_2}$.

Plots in Fig. 6.3, Fig. 6.4, Fig. 6.5 and Fig. 6.6 summarize what stated. For all figures the range of $C_N = C_{f_2}/C_{f_1}$ is $[0.1, 10]$. Plots in Fig. 6.3 and Fig. 6.4 represent the real part of eigenvalues ω_1 and ω_2 of $\boldsymbol{A} = \boldsymbol{K}^{-1}\boldsymbol{\Omega}$ with respect to C_N (on x-axis) and M (on y-axis); the normalized output current is used as parameter with values: $I_{o_N} = 0$, $I_{o_N} = 0.1$, $I_{o_N} = 1$ and $I_{o_N} = 10$. Plots in Fig. 6.5 and Fig. 6.6 represent the real part of eigenvalues ω_1 and ω_2 of $\boldsymbol{A}$ with respect to C_N (on x-axis) and I_{o_N} (on y-axis); the voltage conversion ratio is used as parameter with values $M = 0.01$, $M = 0.1$, $M = 0.25$ and $M = 0.3$.

The x-axis of Fig. 6.3, Fig. 6.4, Fig. 6.5 and Fig. 6.6 are in logarithmic scale as well the colormap in order to provide more comprehensible plots. For all plots, the sign of the real part of eigenvalues ω_1 and ω_2 does not change as C_N varies. Therefore, the 4-LFC Buck converter with fast-update *peak* MS-DPCMC can stably operate in $mode_1$.

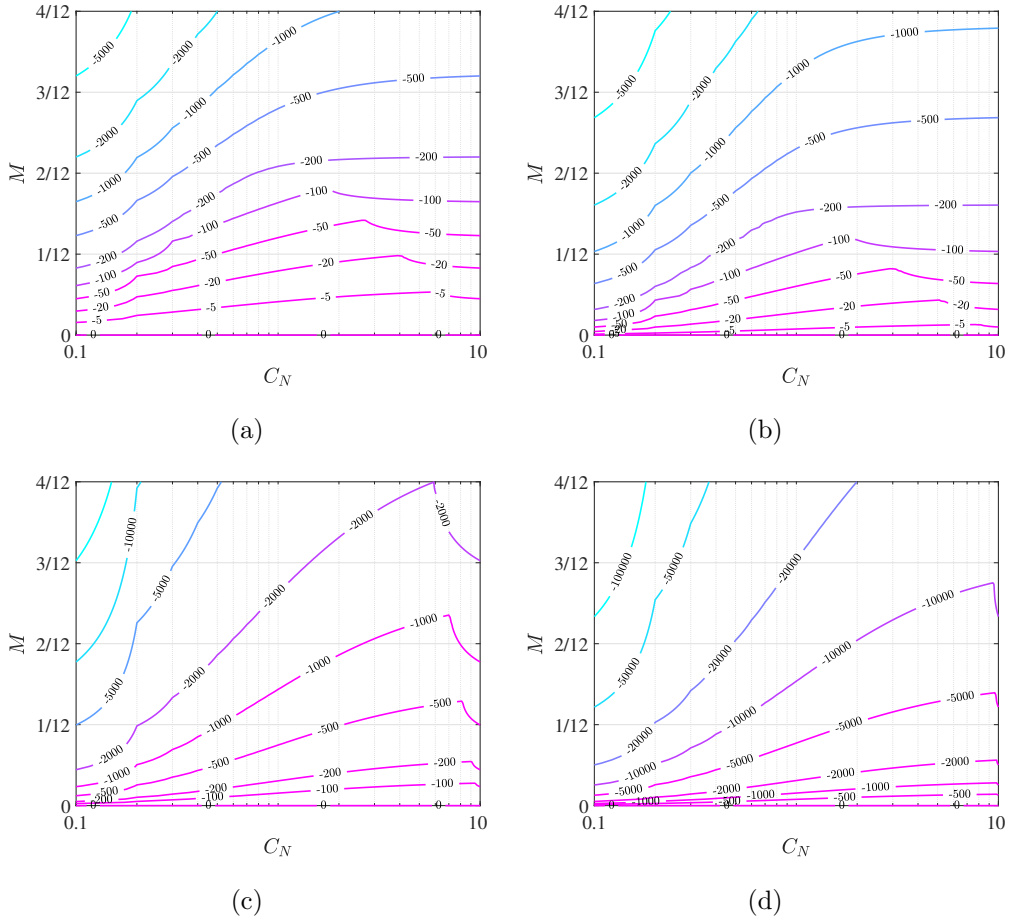


Figure 6.3: *Contour plots of the real part of the eigenvalue* ω_1 *of* $\boldsymbol{A} = \boldsymbol{K}^{-1}\boldsymbol{\Omega}$ *with respect to* C_N *(x-axis) and* M *(y-axis) for different values of the normalized output current (from top-left to bottom-right)* $I_{o_N} = 0$, $I_{o_N} = 0.1$, $I_{o_N} = 1$ *and* $I_{o_N} = 10$. *X-axes are in logarithmic scale.*

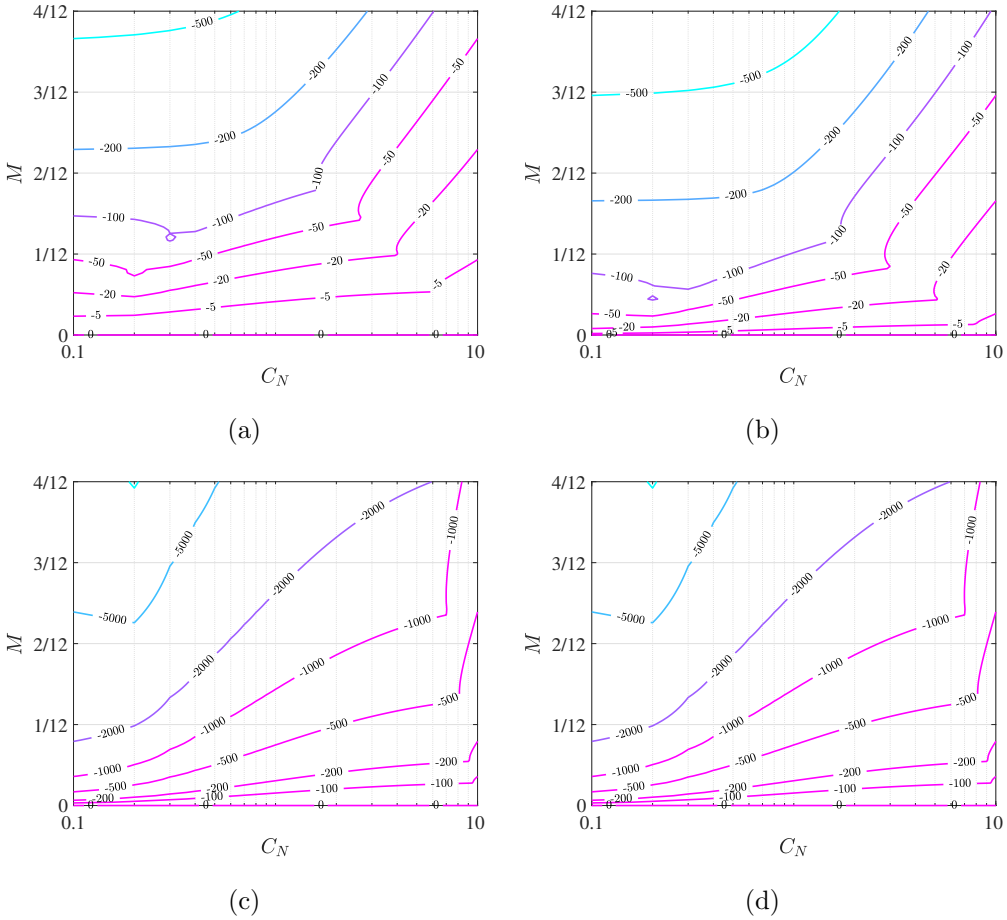


Figure 6.4: *Contour plots of the real part of eigenvalue* ω_2 *of* $\boldsymbol{A} = \boldsymbol{K}^{-1}\boldsymbol{\Omega}$ *with respect to* C_N *(x-axis) and* M *(y-axis) for different values of the normalized output current (from top-left to bottom-right)* $I_{o_N} = 0$, $I_{o_N} = 0.1$, $I_{o_N} = 1$ *and* $I_{o_N} = 10$. *X-axes are in logarithmic scale.*

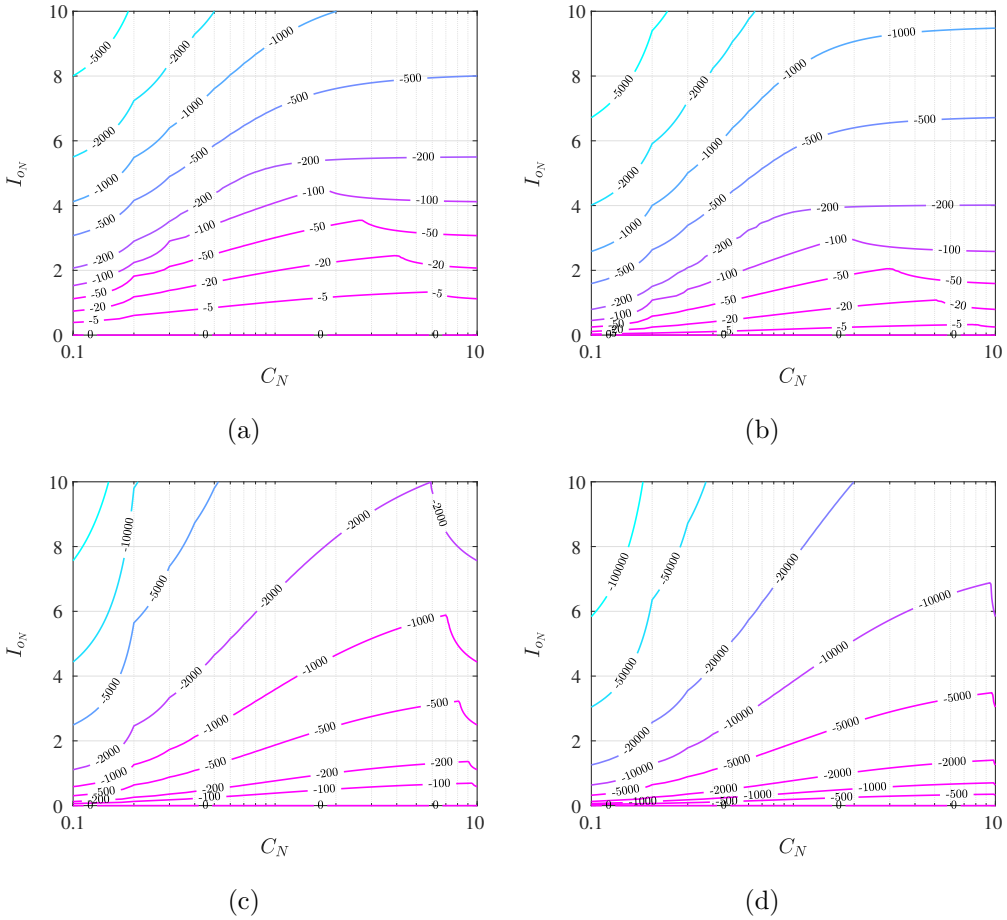


Figure 6.5: *Contour plots of the real part of eigenvalue* ω_1 *of* (6.21) *with respect to* C_N *(x-axis) and* I_{o_N} *(y-axis) for different values of the voltage conversion ratio (from top-left to bottom-right)* $M = 0.01$, $M = 0.1$, $M = 0.25$ *and* $M = 0.3$. *X-axes are in logarithmic scale.*

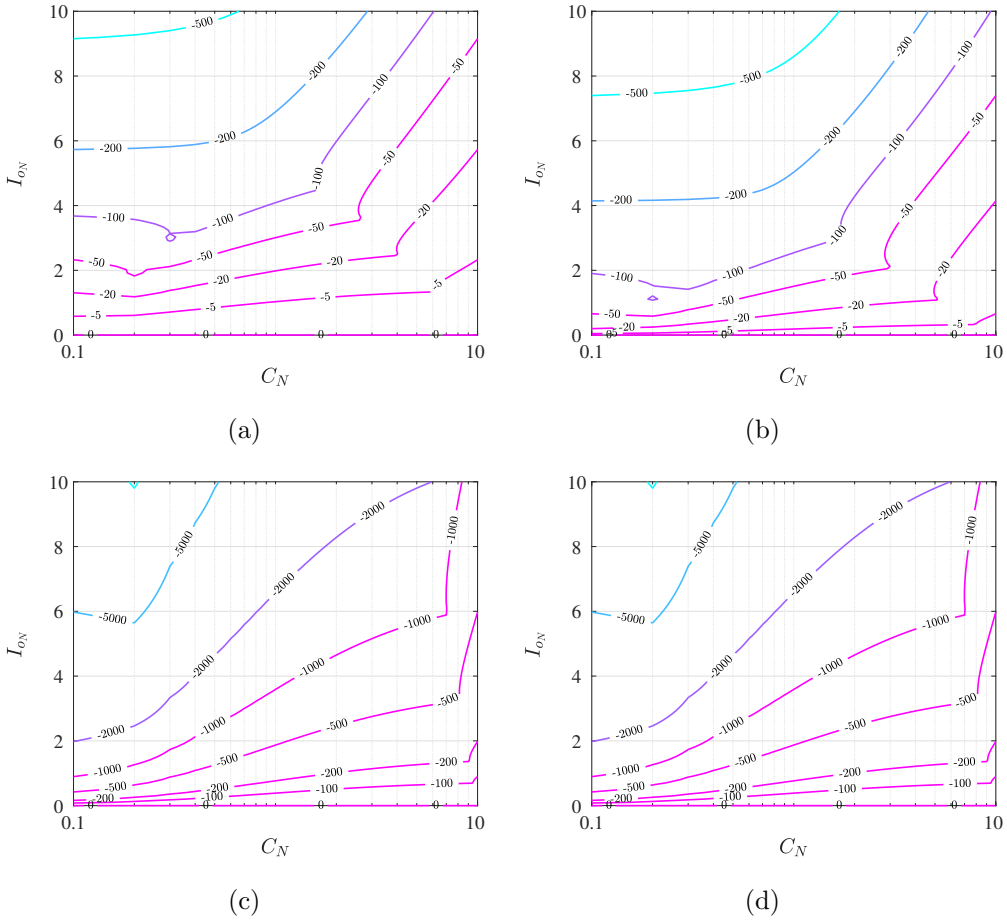


Figure 6.6: *Contour plots of the real part of eigenvalue* ω_2 *of* (6.21) *with respect to* C_N *(x-axis) and* I_{o_N} *(y-axis) for different values of the voltage conversion ratio (from top-left to bottom-right)* $M = 0.01$, $M = 0.1$, $M = 0.25$ *and* $M = 0.3$. *X-axes are in logarithmic scale.*

6.2.2 FC voltage stability analysis: general case

The FCs voltages stability analysis discussed with respect to the 4-L case is now extended to the general case where a generic number of levels are considered. The first problem regards how to switch from expressions related to $mode_1$ to the generic $mode_i$, whit $i = 1, 2, ...N-1$. For simplicity of presentation, the 4-L case is still considered as example. However, the expressions developed in this section are general.

Fig. 6.7 shows the main waveform of the three operation operating modes for the 4-LFC Buck converter with a fast-update *peak* MS-DPCMC. The edges updated by predictive control have been highlighted with a red arrow. For simplicity, carriers and modulating signals have been omitted. The following general approach for FCs voltages stability analysis is divided in two parts. In the first one the steady-state of the converter is solved. In the second part steady-state informations are used to derive the average FC currents as a function of the FCs voltage unbalances. Stability properties are determined by extending the approach disclosed in Sec. 6.2.1.

Steady-state analysis

The inductor current slopes, normalized with respect to $\frac{V_g}{(N-1)Lf_s}$ are written below. Expressions are therefore compared in order to highlights patterns or rules to relate them. For operating $mode_1$ one has

$$\begin{aligned} &\text{Inductor current slopes for } mode_1 \\ &\qquad SL_0 = 0 - 3M \\ &\qquad SL_1 = 1 - 3M - \hat{v}_{N_2} \\ &\qquad SL_2 = 0 - 3M \\ &\qquad SL_3 = 1 - 3M + v_{N_2} - v_{N_1} \\ &\qquad SL_4 = 0 - 3M \\ &\qquad SL_5 = 1 - 3M + v_{N_1}. \end{aligned} \tag{6.22}$$

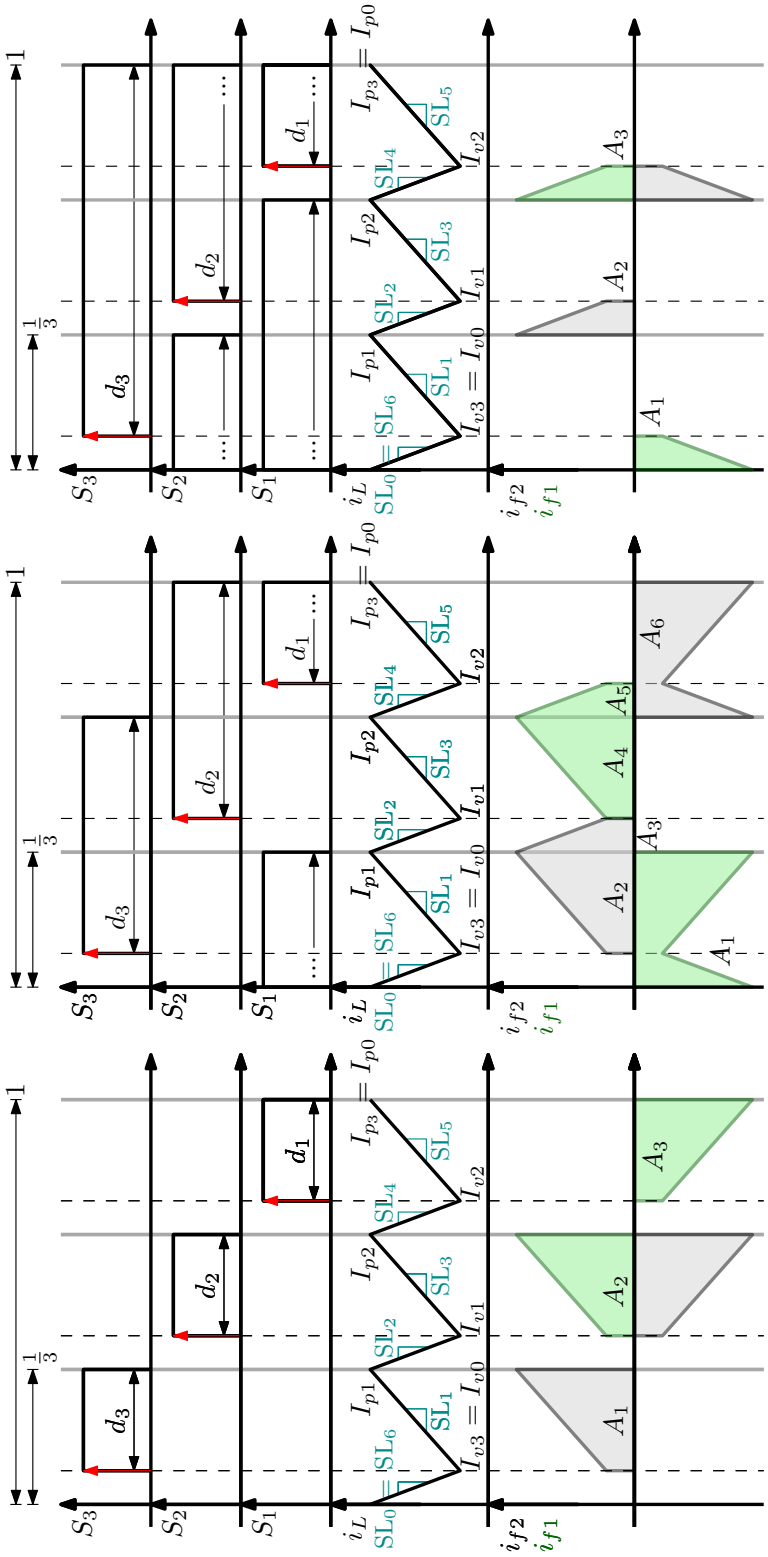


Figure 6.7: *Steady-state waveforms of the 4-LFC Buck converter operating with fast-update* peak *MS-DPCMC in (bottom to top) mode*$_1$*, mode*$_2$ *and mode*$_3$*.*

In $mode_1$, even-index slopes do not depend on FCs voltage perturbations. This fact is general and applies whatever the value of $N \geq 3$.
In $mode_2$ all current slopes are function of the FCs voltage unbalances

Inductor current slopes for $mode_2$

$$\begin{aligned} SL_0 =& 1 - 3M + \hat{v}_{N_1} \\ SL_1 =& 2 - 3M - \hat{v}_{N_2} + \hat{v}_{N_1} \\ SL_2 =& 1 - 3M - \hat{v}_{N_2} \\ SL_3 =& 2 - 3M - v_{N_1} \\ SL_4 =& 1 - 3M + \hat{v}_{N_2} - \hat{v}_{N_1} \\ SL_5 =& 2 - 3M + v_{N_2}. \end{aligned} \tag{6.23}$$

In $mode_3$, odd-index slopes do not depend on FCs voltage perturbations

Inductor current slopes for $mode_3$

$$\begin{aligned} SL_0 =& 2 - 3M + v_{N_2} \\ SL_1 =& 3 - 3M \\ SL_2 =& 2 - 3M - \hat{v}_{N_2} + \hat{v}_{N_1} \\ SL_3 =& 3 - 3M \\ SL_4 =& 2 - 3M - v_{N_1} \\ SL_5 =& 3 - 3M. \end{aligned} \tag{6.24}$$

From (6.22), (6.23) and (6.24) patterns can be recognized. Before continuing, additional definitions are required to write the general inductor current slope expression in a more compact form.

The vector containing switch states (i.e., 1 when the corresponding switch is on and 0 when off) for the sub-topology i is defined as

$$\boldsymbol{S}_i \triangleq (S_3, S_2, S_1)_i \tag{6.25}$$

For instance, using (6.25) the sequence of the switch states for the operating

$mode_1$ can be summarized as follows

$$\boldsymbol{Seq_S}_{mode_1} = [(0,0,0),(1,0,0),(0,0,0),(0,1,0),(0,0,0),(0,0,1)] \tag{6.26}$$

The vector $\boldsymbol{v}$ is defined as follows

$$\hat{\boldsymbol{v}} = (0, \hat{v}_{N_2}, \hat{v}_{N_1}, 0)\,. \tag{6.27}$$

Using (6.27), the following sequence can be founded

$$\boldsymbol{Seq}_{\hat{\boldsymbol{v}}} = (-\hat{v}_{N_2}, \hat{v}_{N_2} - \hat{v}_{N_1}, \hat{v}_{N_1}), \tag{6.28}$$

where the i-th element of $\boldsymbol{Seq}_{\hat{\boldsymbol{v}}}$ is defined as

$$Seq_{\hat{v}_i} \triangleq \hat{v}_i - \hat{v}_{i+1} \tag{6.29}$$

Now, from (6.22), (6.23) and (6.24) and using the definitions (6.25) and (6.29), one can deduce the following general expression for the normalized inductor current slope SL_i, with $i = 0, 1, ...2(N-1)$, in operating mode $n = 1, 2, ...N-1$

$$\boxed{SL_i = n - \left(\frac{1}{2} + \frac{(-1)^i}{2}\right) - (N-1)M + \boldsymbol{Seq}_{\hat{\boldsymbol{v}}} \cdot \boldsymbol{Seq}_{\boldsymbol{S}_i}^{\top}}\,. \tag{6.30}$$

The symbol $\top$ indicates the transposition operation, while $\cdot$ the scalar-product between vectors. Even though (6.30) is found for the 4-L case, this general expression is valid for all N-LFC Buck converter.

The N-1 predictive equations can be easily generalized as follows

$$\boxed{d_{N-i} = I_{\mathrm{ref}_N} - I_{p_{i-1}} + M}\,, \tag{6.31}$$

whit $i = 1, 2, ..., N-1$. Please note that both I_{ref_N} and $I_{p_{i-1}}$ are normalized with respect to $\frac{V_g}{(N-1)Lf_s}$. The normalized inductor peak expressions can be

generally written as

$$\boxed{I_{p_i} = I_{p_{i-1}} + \frac{SL_{i-1}}{N-1} + d_{N-i}\left(SL_i - SL_{i-1}\right)}, \tag{6.32}$$

whit $i = 1, 2, ..., N-1$. Please note that, since the steady-state operation is considered, the expression of I_{p0} is provided by $I_{p_{N-1}}$. The steady-state solution of the converter is obtained by solving the system of $2(N-1)$ equations in $2(N-1)$ unknowns that is obtained with (6.31) and (6.32). In vector notation one has

$$\boxed{\begin{cases} \boldsymbol{d} & = (I_{iref} + M)\,\boldsymbol{u}_{N-1} - \boldsymbol{R}\cdot\boldsymbol{I_p} \\ \boldsymbol{I_p} & = (\boldsymbol{I}-\boldsymbol{R})^{-1}\left(\boldsymbol{R}\cdot\dfrac{\boldsymbol{SL}}{N-1}\right) + (\boldsymbol{I}-\boldsymbol{R})^{-1}\cdot[\boldsymbol{R}\cdot((\boldsymbol{d}\circ(\boldsymbol{I}-\boldsymbol{R}))\cdot\boldsymbol{SL})] \end{cases}}, \tag{6.33}$$

where $\boldsymbol{u}_{N-1}$ is a vector with all $N-1$ components equal to 1, $\boldsymbol{I}$ is the identity matrix and $\boldsymbol{R} \in \mathbb{R}^{(N-2)\times(N-2)}$ is defined as follows

$$\boldsymbol{R} \triangleq \begin{pmatrix} 0 & 1 & 0 & ... & 0 & 0 \\ 0 & 0 & 1 & ... & 0 & 0 \\ ... & ... & ... & ... & ... & ... \\ 0 & 0 & 0 & ... & 1 & 0 \\ 0 & 0 & 0 & ... & 0 & 1 \\ 1 & 0 & 0 & ... & 0 & 0 \end{pmatrix}. \tag{6.34}$$

The symbol $\circ$ indicates the element-to-element[4] product defined as follows

$$\text{with } \boldsymbol{u}, \boldsymbol{v} \in \mathbb{R}^{\nu} \rightarrow \boldsymbol{u}\circ\boldsymbol{v} = \begin{pmatrix} u_1\ v_1 \\ u_2\ v_2 \\ ... \\ u_\nu\ v_\nu \end{pmatrix} \tag{6.35}$$

[4]Also known as *Hadamard* product

The vector $\boldsymbol{d}$ is defined as

$$\boldsymbol{d} \triangleq (d_{N-1}, d_{N-2}, ..., d_2, d_1)^\top , \tag{6.36}$$

while the normalized peak inductor current vector $\boldsymbol{I_p}$ and the inductor current slope $\boldsymbol{SL}$ vector, are respectively defined as follows

$$\begin{aligned} \boldsymbol{I_p} &\triangleq \left(I_{p1}, I_{p2}, ..., I_{p(N-2)}, I_{p(N-1)}\right)^\top \\ \boldsymbol{SL} &\triangleq (SL_1, SL_2, ..., SL_{N-2}, SL_{N-1})^\top \end{aligned} \tag{6.37}$$

For the generic N-LFC Buck converter operating in $mode_i$, the general definition of I_{ref_N} can be easily deduced using (3.35)

$$\boxed{I_{\text{ref}_N} = I_{o_N} + \frac{1}{2}\left(i - (N-1)M\right)\left(M - \frac{i-1}{N-1}\right)} . \tag{6.38}$$

For all operating modes, system (6.33) constitutes an *algorithm* for solving the steady-state of the generic N-LFC Buck converter operating with the fast-update *peak* MS-DPCMC. It is important to stress that the problem has been normalized in current with respect to the constant $\frac{V_g}{(N-1)Lf_s}$. In other words, the inductor current and the FC currents are considered in the following normalized form

$$\begin{aligned} i_L \rightarrow & i_{L_N} \triangleq \frac{(N-1)Lf_s}{V_g} i_L \\ i_{f_i} \rightarrow & i_{f_{i_N}} \triangleq \frac{(N-1)Lf_s}{V_g} i_{f_i} \quad \text{with} \quad i = 1, 2, ...N-2. \end{aligned} \tag{6.39}$$

The subscript $_N$ for indicating the *normalization* in (6.9), (6.12) and (6.32) has been omitted to avoid overcomplicating the final notation.

The solution of (6.33) can be now used to calculate the average FCs currents and therefore the matrix $\boldsymbol{\Omega}$ for the general case. Once found the steady-state expression of $\boldsymbol{I_p}$ and $\boldsymbol{d}$ as a function of the system inputs and converter parameters, the valley inductor current vector $\boldsymbol{I_v}$ can be founded

following the methodology used in 6.12. Indeed, for the general N-LFC Buck case, operating in $mode_i$, one has

$$\boxed{\boldsymbol{I_v} = \boldsymbol{I_p} + \boldsymbol{SL} \circ \left(\frac{mode_i}{N-1} \boldsymbol{u}_{N-1} - \boldsymbol{d} \right)} . \tag{6.40}$$

Trapezoidal areas, highlighted in Fig. 6.7, can be now calculated. The $N-2$ average FCs currents I_{f_i} are obtained by algebraically summing these areas. Having now available the lengths of bases and heights (i.e., $\boldsymbol{I_p}$, $\boldsymbol{I_v}$ and $\boldsymbol{d}$), the calculation of each area is straightforward. However, although for the 4-L case, the calculation of FC currents may be quite simple, the general case presents additional difficulties. In fact, for the generic N-L case, the calculation I_{f_i} requires to sum appropriate areas taken whit appropriate signs. This problem is illustrated by the following example regarding the 4-L case operating in $mode_2$ (i.e., $\frac{1}{3} < M < \frac{2}{3}$).
The expressions of A_i, with $i = 1, ..6$ in Fig. 6.7 can be written as follows

$$\begin{aligned}
A_1 =& \frac{I_{v3} + I_{p3}}{2} \left(\frac{2}{3} - d_3 \right) \\
A_2 =& \frac{I_{v3} + I_{p1}}{2} \left(d_3 - \frac{1}{3} \right) \\
A_3 =& \frac{I_{v1} + I_{p1}}{2} \left(\frac{2}{3} - d_2 \right) \\
A_4 =& \frac{I_{v1} + I_{p2}}{2} \left(d_2 - \frac{1}{3} \right) \\
A_5 =& \frac{I_{v2} + I_{p2}}{2} \left(\frac{2}{3} - d_1 \right) \\
A_6 =& \frac{I_{v2} + I_{p3}}{2} \left(d_1 - \frac{1}{3} \right) .
\end{aligned} \tag{6.41}$$

The expression of I_{f_2} and I_{f_1} are given by

$$\begin{aligned}
I_{f_2} =& A_2 + A_3 - A_5 - A_6 \\
I_{f_1} =& A_4 + A_5 - A_1 - A_3 .
\end{aligned} \tag{6.42}$$

Areas A_3 and A_5 are present in both expressions of (6.42) but their contribution change depending on whether I_{f_1} or I_{f_2} is computed. For the 4-L case, the graphical representation of areas (6.41) is relatively simple and (6.42) can be easily deduced from it. However, as the number of levels increases and for some operating modes, the problem begins to get quite complicated. The following expression fix this issue, automatically assigning the proper sign for each area as well as the correct area for each average FC current

$$I_{f_i} \triangleq -\sum_{\nu=1}^{2(N-1)} A_\nu \frac{\partial SL_\nu}{\partial \hat{v}_{N_i}}. \tag{6.43}$$

Therefore, the general calculation of the $N-2$ FC currents can be performed using the following expressions

$$\boxed{\boldsymbol{A} \triangleq \begin{cases} \dfrac{\boldsymbol{RI_p} + \boldsymbol{RI_v}}{2} \circ \left(\dfrac{mode_i}{N-1} \boldsymbol{u}_{2(N-1)} - \boldsymbol{d} \right) & \text{odd index} \\ \dfrac{\boldsymbol{I_p} + \boldsymbol{RI_v}}{2} \circ \left(\boldsymbol{d} - \dfrac{mode_i - 1}{N-1} \boldsymbol{u}_{2(N-1)} \right) & \text{even index} \end{cases}}, \tag{6.44}$$

$$\boxed{\boldsymbol{I}_f = \left(I_{f_{(N-2)}}, I_{f_{(N-3)}}, ..., I_{f_1} \right), \text{ with } \quad I_{f_i} \triangleq -\sum_{\nu=1}^{2(N-1)} A_\nu \frac{\partial SL_\nu}{\partial \hat{v}_{N_i}}}. \tag{6.45}$$

Expression (6.45) and (6.44) complete the proposed algorithm to solve the steady-state of the generic N-LFC Buck converter operating with the fast-update *peak* MS-DPCMC. This approach can be easily extended to the other digital-predictive controllers proposed in this thesis, by replacing in (6.33) the specific control equation of the controller under analysis. In addition, the discussed algorithm can be also extended to others digital controllers that use a different sequence of topological states, by modifying (6.26). Indeed, (6.29) and the scalar product in (6.30) automatically add the appropriate FC voltage perturbation to the corresponding inductor current slopes.

FCs voltages stability properties

The $N-2$ average FC currents I_{f_i} in (6.45) are function of the $N-2$ FC voltage perturbations $\hat{v}_{N_i}$. Similarly to the procedure used in (6.14), for small values of $\hat{v}_{N_i}$, the average FCs currents can be linearized using the Taylor-series. For the general case, one has

$$\begin{cases} I_{f_{N-2}} & \approx I_{f_{N-2}}\Big|_{\boldsymbol{v}_N=\boldsymbol{0}} + \hat{v}_{N_1}\left(\dfrac{\partial I_{f_{N-2}}}{\partial \hat{v}_{N_1}}\Big|_{\boldsymbol{v}_N=\boldsymbol{0}}\right) + ... + \hat{v}_{N_2}\left(\dfrac{\partial I_{f_{N-2}}}{\partial \hat{v}_{N_{N-2}}}\Big|_{\boldsymbol{v}_N=\boldsymbol{0}}\right) \\ I_{f_{N-3}} & \approx I_{f_{N-3}}\Big|_{\boldsymbol{v}_N=\boldsymbol{0}} + \hat{v}_{N_1}\left(\dfrac{\partial I_{f_{N-3}}}{\partial \hat{v}_{N_1}}\Big|_{\boldsymbol{v}_N=\boldsymbol{0}}\right) + ... + \hat{v}_{N_2}\left(\dfrac{\partial I_{f_{N-3}}}{\partial \hat{v}_{N_{N-2}}}\Big|_{\boldsymbol{v}_N=\boldsymbol{0}}\right) \\ & ... \\ I_{f_1} & \approx I_{f_1}\Big|_{\boldsymbol{v}_N=\boldsymbol{0}} + \hat{v}_{N_1}\left(\dfrac{\partial I_{f_1}}{\partial \hat{v}_{N_1}}\Big|_{\boldsymbol{v}_N=\boldsymbol{0}}\right) + ... + \hat{v}_{N_2}\left(\dfrac{\partial I_{f_1}}{\partial \hat{v}_{N_{N-2}}}\Big|_{\boldsymbol{v}_N=\boldsymbol{0}}\right). \end{cases} \tag{6.46}$$

The average FCs currents corresponding to the steady-state operation with null FCs voltage perturbations are always null (i.e., $I_{f_i}\big|_{\boldsymbol{v}_N=\boldsymbol{0}} = 0$) and thus (6.46) can be rewritten in the following general matrix form

$$\boxed{\boldsymbol{I}_f = \boldsymbol{K} \cdot \frac{\partial \hat{\boldsymbol{v}}_N}{\partial x} \approx \boldsymbol{\Omega} \cdot \hat{\boldsymbol{v}}_N}. \tag{6.47}$$

This is the general form already introduced in the previous section with (6.17) and previously in (4.17) with the scalar form regarding the 3-L case. The $(N-2)\times(N-2)$ matrix $\boldsymbol{K}$ is defined as follows

$$\boxed{\boldsymbol{K} \triangleq L f_s^2 \begin{pmatrix} C_{f_{N-2}} & 0 & ... & 0 & 0 \\ 0 & C_{f_{N-3}} & ... & 0 & 0 \\ ... & ... & ... & ... & ... \\ 0 & 0 & ... & C_{f_2} & 0 \\ 0 & 0 & ... & 0 & C_{f_1} \end{pmatrix}}. \tag{6.48}$$

In order to determine the stability properties of the FC voltages, all eigenvalues $\omega_i \in \mathbb{C}$ of the matrix $\boldsymbol{A} \triangleq \boldsymbol{K}^{-1}\boldsymbol{\Omega}$ has to satisfy at

$$\Re[\omega_i] \in \mathbb{R}^- \ , \tag{6.49}$$

where $\mathbb{R}^-$ denotes the set of negative real numbers. The next section presents some results obtained with this proposed general procedure.

6.3 Stability analysis examples

The stability properties of the 3-LFC Buck converter operating with single-sampled DPCMC, multi-sampled DPCMC and fast-update MS-DPCMC have been extensively analysed and verified by simulation and experimental tests in [47, 50, 54]. In order to verify the validity of the proposed *general* FC voltages stability analysis, further results and simulations are presented in relation to other N-LFC Buck converters.

6.3.1 4-LFC Buck converter operating with fast-update *peak* MS-DPCMC

The 4-LFC Buck converter has often been used as a reference for notation and presentation of the study methodology. This subsection discusses its FC voltages stability properties with respect to fast-update *peak* MS-DPCMC. Results are obtained for the most common practical case obtained for $C_{f_1} = C_{f_2}$. As shown in Sec. 6.2.1, also the general case obtained with different FCs values can be analysed with the proposed tools. For all results presented in this section, there are no changes in the FC voltages stability properties as the relative values of the FCs change.

Fig. 6.8 shows a summary stability plot. The voltage conversion ratio M is represented on the x-axis while the normalized output current I_{o_N} on y-axis. The yellow areas correspond to operating points where both system eigenvalues have negative real part while blue areas correspond to operating

point where at least one eigenvalue has non-negative real part. The following statement summarizes the meaning of yellow and blue areas of Fig. 6.8

$$\begin{aligned} \Re[\omega_1] < 0 \text{ and } \Re[\omega_2] < 0 \ &\rightarrow \text{yellow areas} \\ \Re[\omega_1] \geq 0 \ \text{ or } \ \Re[\omega_2] \geq 0 \ &\rightarrow \text{blue areas} \ , \end{aligned} \tag{6.50}$$

where ω_1 and ω_2 are the eigenvalues of $\boldsymbol{A} = \boldsymbol{K}^{-1}\boldsymbol{\Omega}$.

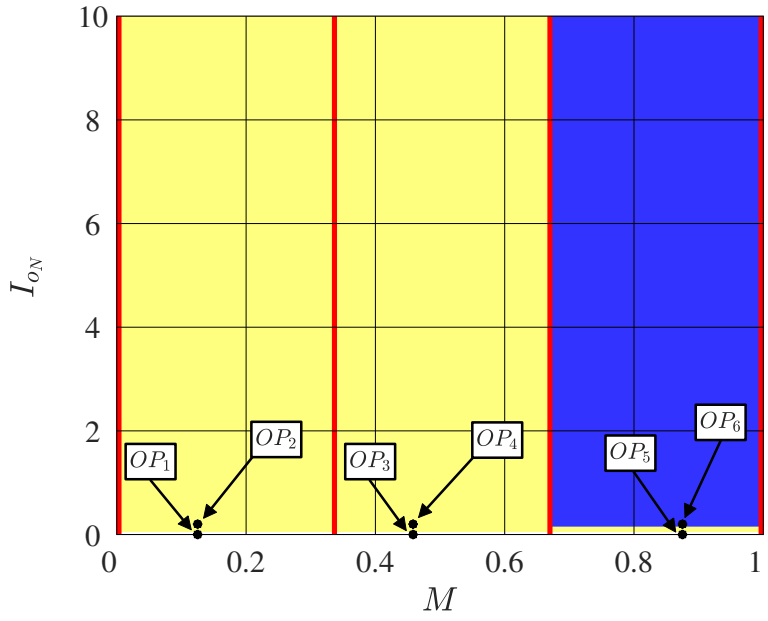


Figure 6.8: *Summary plot of the FC voltages stability properties for the 4-LFC Buck converter with fast-update* peak *MS-DPCMC. The voltage conversion ratio M is represented on the x-axis, while the normalized output current I_{o_N} is represented on y-axis. Stable operating point are represented in yellow while unstable operating point in blue. Red vertical lines denote operating points corresponding at $M = \frac{i}{N-1}$, with $i = 1, 2, ..., N-1$. Operating points used in simulations tests are highlighted with corresponding labels.*

Results in Fig. 6.8 predicts stable behaviour for $mode_1$ and $mode_2$. For operating $mode_3$, the proposed analysis indicates that FCs voltages stability depends on the normalized output current I_{o_N}: stable operation in no-load operation (i.e., $I_{o_N} = 0$) and unstable operation for higher values of I_{o_N}.

In order to verify whether the behaviour predicted by the proposed stability analysis coincides with the actual FCs voltages stability character, three simulations are proposed. The simulating operating points are indicated in Fig. 6.8. For these tests output capacitance $C_{o\,\text{4-L}}$ and inductance $L_{\text{4-L}}$ are halved with respect to the 3-L case previously analysed (i.e., $L_{\text{3-L}} = 6.5\,\mu\text{H}$, $C_{o\,\text{3-L}} = 50\,\mu\text{F}$, $L_{\text{4-L}} = 3.2\,\mu\text{H}$ and $C_{o\,\text{4-L}} = 25\,\mu\text{F}$). The designed bandwidth of the output voltage control-loop is $f_c = f_s/4$ while the phase margin is $\phi_m = 50°$. As shown by the following simulations, although the size of the output filter is decreased compared to the 3-L case, the overall system performances are quite similar. This confirms the benefits as the number of levels increases.

Simulation of the 4-LFC Buck converter with fast-update *peak* MS-DPCMC in $mode_1$

Fig. 6.9 and Fig. 6.10 show the simulating response to a $500\,\text{mA} \rightarrow 0$ load step variation. In Fig. 6.9 the time-interval is 8 ms while in Fig. 6.10 is 100 µs. The longer time-interval in the first figure allows to verify that both FC voltages rise to their balanced average values after the load-step (i.e., $V_{f_2} \rightarrow 8\,\text{V}$ and $V_{f_1} \rightarrow 4\,\text{V}$). As predicted theoretically this digital-predictive controller is able to operate without FC voltages stability issues.

A comparison with the results obtained with the same type of control applied to the 3-LFC Buck converter discussed in the 4.4.2 and in [47, 50] is now possible. In the 3-L case, the system is able to operate without stability FC voltage issues in $mode_1$ while the operation in $mode_2$ leads to unstable FC voltage operation. Simulations in the next subsection show a different behaviour for the 4-L case. These differences on the FCs voltages stability properties of multi-level converters with respect to the same type of controller emphasizes the relevance of the unified approach proposed in this chapter.

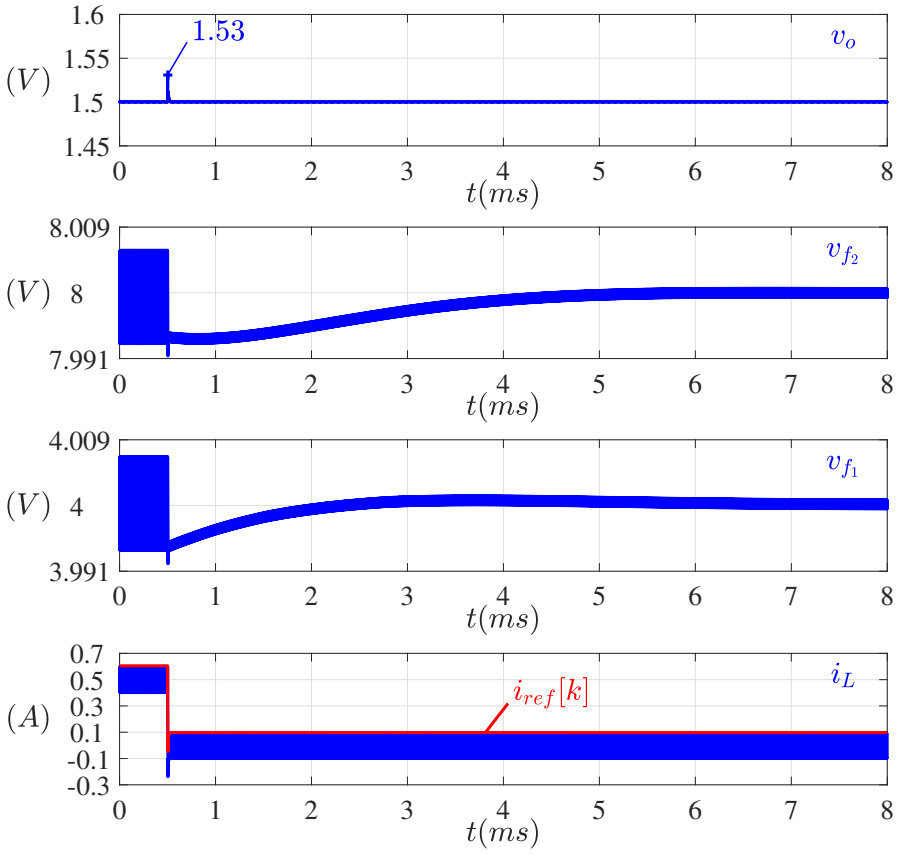


Figure 6.9: *Simulating response to a* $500\,\text{mA}(OP_2) \rightarrow 0(OP_1)$ *load step variation for the 4-LFC Buck converter with fats-update* peak *MS-DPCMC in* $mode_1$*. From top to the bottom: output voltage, FC voltage of* C_{f_2}*, FC voltage of* C_{f_1}*, inductor and reference currents.*

Simulation of the 4-LFC Buck converter with fast-update *peak* MS-DPCMC in $mode_2$

Fig. 6.11 and Fig. 6.12 show the simulating response to a $500\,\text{mA} \rightarrow 0$ load step variation. For these simulations the reference output voltage is changed in order to regulate the output voltage at 5.5 V. The simulation time is 8 ms for Fig. 6.11 and 100 µs for Fig. 6.12. As theoretically predicted, the fast-update *peak* MS-DPCMC in $mode_2$ operates without FCs voltages stability issues.

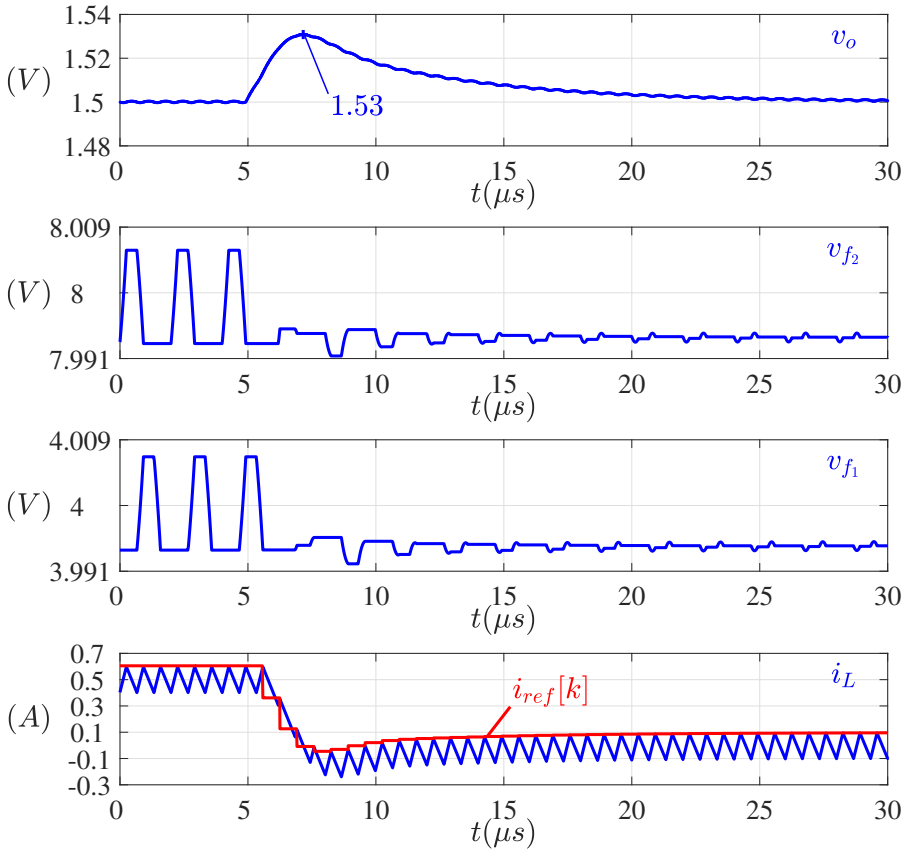


Figure 6.10: *Simulating response to a* $500\,\mathrm{mA}(OP_2) \rightarrow 0(OP_1)$ *load step variation for the 4-LFC Buck converter with fats-update* peak *MS-DPCMC in* $mode_1$ *(shorter time scale). From top to the bottom: output voltage, FC voltage of* C_{f_2}*, FC voltage of* C_{f_1}*, inductor and reference currents.*

Simulation of the 4-LFC Buck converter with fast-update *peak* MS-DPCMC in $mode_3$

Fig. 6.13 shows the simulating response to a $0 \rightarrow 500\,\mathrm{mA}$ load step variation. For these simulations the reference output voltage is changed in order to regulate the output voltage at 10.5 V. Results obtained with the proposed methodology and summarized by Fig. 6.8 indicate that for the $mode_3$, stable FCs voltages operation can be reached for null output current. For higher values of the output current both eigenvalues of the corresponding matrix $\boldsymbol{A}$ exhibit non-negative real part and the system is therefore unstable.

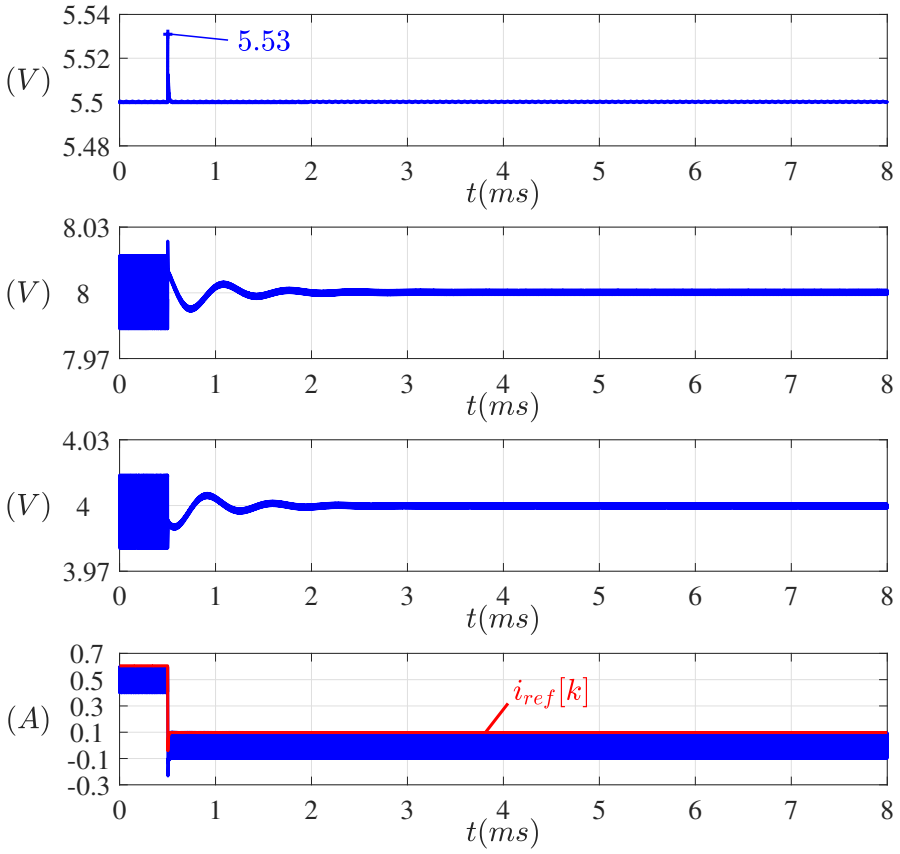


Figure 6.11: *Simulating response to a* $500\,\text{mA}(OP_4) \rightarrow 0(OP_3)$ *load step variation for the 4-LFC Buck converter with fats-update* peak *MS-DPCMC in* $mode_2$. *From top to the bottom: output voltage, FC voltage of* C_{f_2}, *FC voltage of* C_{f_1}, *inductor and reference currents.*

Fig. 6.13 shows the response to a $0 \rightarrow 500\,\text{mA}$. Since for $t = 0$, $I_o = 0\,\text{mA}$, the system starts at OP_5. The converter reaches the steady-state without FCs voltages stability issues. Once the load is abruptedly connected, the output current rise to the nominal value $I_o = 500\,\text{mA}$, and the converter works at the operating point OP_6. This is an unstable operating point for the converter and therefore, as predicted in Fig. 6.8, both FCs voltages diverge.

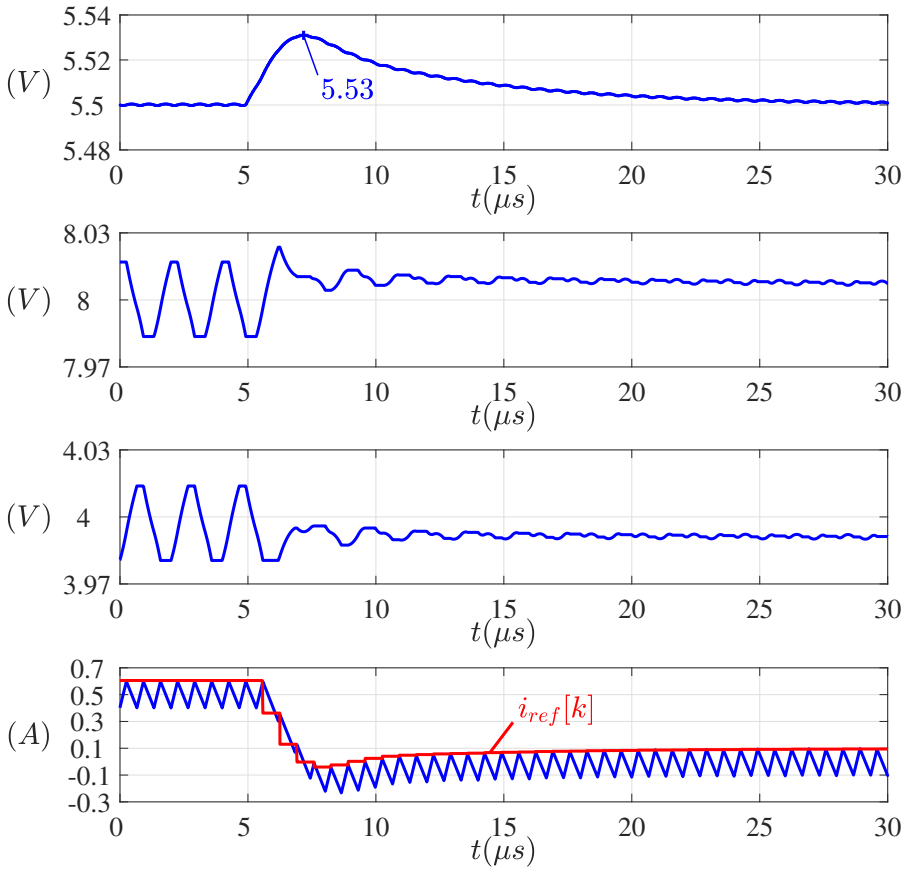


Figure 6.12: *Simulating response to a* $500\,\mathrm{mA}(OP_4) \rightarrow 0(OP_3)$ *load step variation for the 4-LFC Buck converter with fats-update* peak *MS-DPCMC in mode*$_2$ *(shorter time scale). From top to the bottom: output voltage, FC voltage of* C_{f_2}*, FC voltage of* C_{f_1}*, inductor and reference currents.*

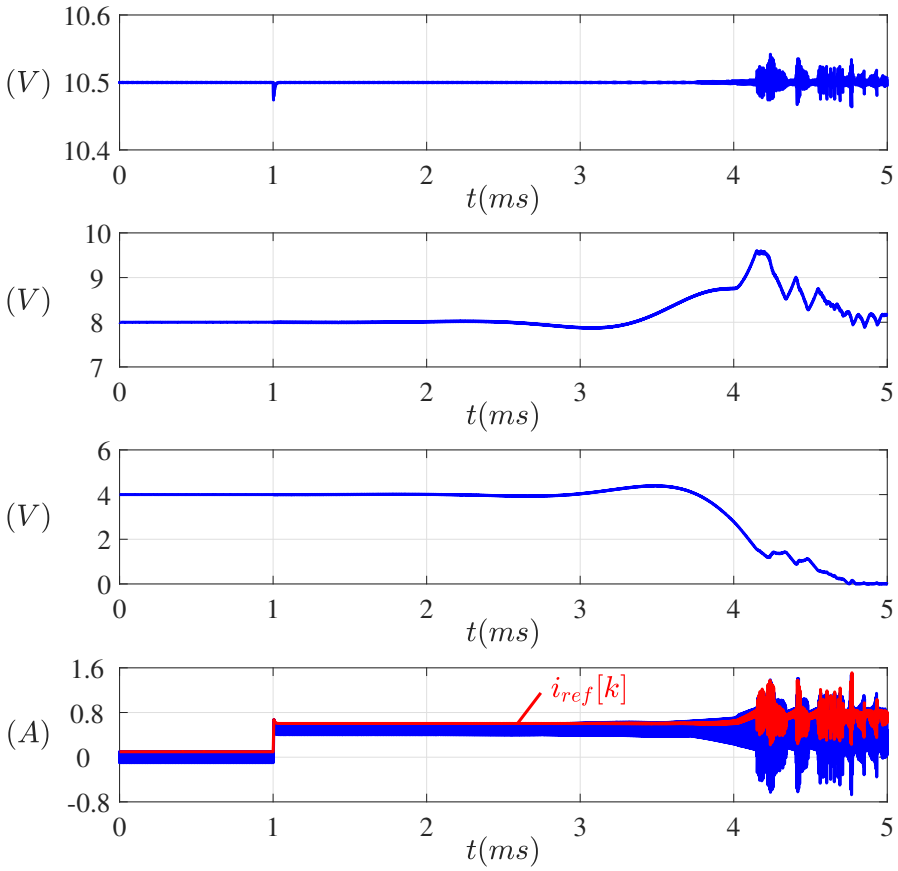


Figure 6.13: *Simulating response to a* $0(OP_5) \rightarrow 500\,\text{mA}(OP_6)$ *load step variation for the 4-LFC Buck converter with fats-update* peak *MS-DPCMC in mode*$_3$. *From top to the bottom: output voltage, FC voltage of* C_{f_2}, *FC voltage of* C_{f_1}, *inductor and reference currents.*

6.3.2 4-LFC Buck converter operating with fast-update *average* MS-DPCMC with *double-update* of the modulating signal

Thanks to the intrinsic shape of the TTE carriers, when the available hardware allows it, the modulating signal can be sampled twice per switching cycle: once on the valley and once on the peak of the TTE carrier. Applying the same approach to the N-LFC Buck converters[5], one can sample and update at higher frequency (i.e., $f_{\text{sample}} = f_{\text{update}} = 2f_s(N-1)$). This provides an even faster inner-current controlling action and thus further increases the *available* bandwidth for the outer output voltage control loop. This control strategy is now applied to the 4-LFC Buck converter. The resulting control strategy is referred as fast-update *average* MS-DPCMC with *double-update* of the modulating signal.

Following the approach disclosed in Chapter 5 and previously in [54], one can derive the following control equation

$$d[n] = \frac{2\,(N-1)\,f_s L}{V_g}\,(I_{ref} - i_L[n-1]) + M. \tag{6.51}$$

Using the approach developed in this thesis, can be easily proved that the system implements a digital dead-beat inductor current controller. The main concerns are about the FCs voltages stability. The stability properties predicted with the general proposed approach and their comparison with the simulation results are proposed below.

Fig. 6.14 shows the summary stability plot for the 4-LFC Buck converter operating with fast-update average MS-DPCMC with double-update of the modulating signal. The voltage conversion ratio M is represented on the x-axis while the normalized output current I_{o_N} on y-axis. Once again, yellow areas correspond to operating point where all eigenvalues of the relative matrix $\boldsymbol{A}$, have negative real part while blue areas correspond to operating

[5]Please refer to Appendix B.

point where at least one of its eigenvalues has real non-negative part.

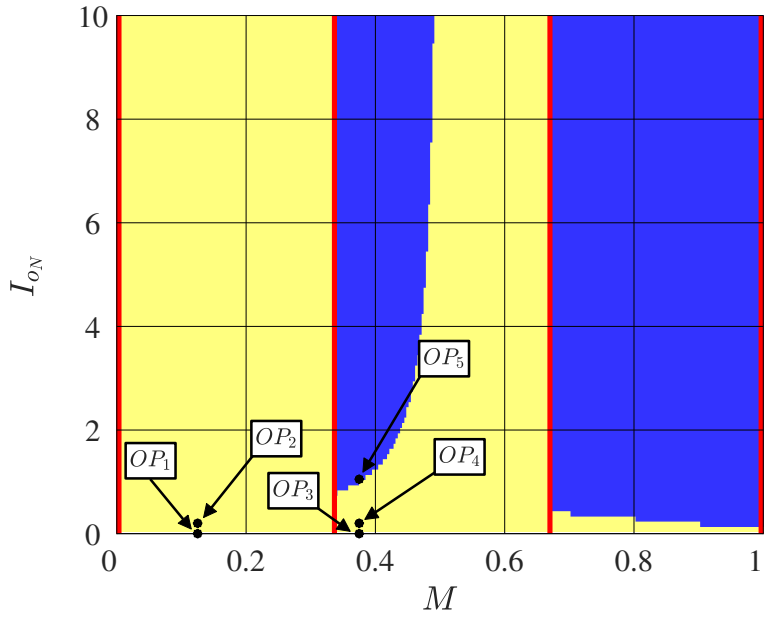


Figure 6.14: *Summary plot of the FC voltages stability properties for the 4-LFC Buck converter with fast-update* average *MS-DPCMC with* double-update *of the modulating signal. The voltage conversion ratio M is represented on the x-axis, while the normalized output current I_{o_N} is represented on y-axis. Stable operating point are represented in yellow while unstable operating point in blue. Red vertical lines denote operating points corresponding at $M = \frac{i}{N-1}$, with $i = 1, 2, ..., N-1$. Operating points used in simulations tests are highlighted with corresponding labels.*

The summary plot Fig. 6.14 is obtained by a numerical substitution procedure: both eigenvalues are numerically evaluated for each numerical value of the couple M and I_{o_N}. However, with the proposed approach, one can derive the analytical model in closed form and use it to make a design of the inductor so has to stabilize the operation even in $mode_2$. Using the developed

approach one can find the following expressions for $\boldsymbol{\Omega}$ and $\boldsymbol{A}$

$$\boldsymbol{\Omega} = \frac{I_{o_N}}{4}(1-2M) + \begin{pmatrix} -\dfrac{M(1-M)}{4} & \dfrac{1}{6} - 3I_{o_N}\dfrac{1-2M}{4} - M(1-M) \\ -\dfrac{1}{6} + 5M\dfrac{1-M}{4} & -\dfrac{M(1-M)}{4} \end{pmatrix}, \tag{6.52}$$

and

$$\boldsymbol{A} = \frac{1}{L\, f_s^2} \begin{pmatrix} \dfrac{1}{C_{f_2}} & 0 \\ 0 & \dfrac{1}{C_{f_1}} \end{pmatrix} \boldsymbol{\Omega}. \tag{6.53}$$

Eigenvalues ω_1 and ω_2 of $\boldsymbol{A}$ exhibit real negative part for

$$I_{o_N} < \frac{M(1-M)}{1-2M}. \tag{6.54}$$

Expression (6.54) can be rewritten as a function of the ratio between inductor current peak-to-peak ripple $\Delta i_{L_{\text{p-p}}}$ over the average output current I_o

$$\frac{\Delta i_{L_{\text{p-p}}}}{I_o} > \frac{6\left(\frac{2}{3} - M\right)\left(\frac{1}{2} - M\right)\left(M - \frac{1}{3}\right)}{M(1-M)}. \tag{6.55}$$

The condition (6.55) can be used as a design equation for the inductor. In each case for the application to which this thesis refers, the previous condition is always verified. Therefore it is possible to implement this *average* current control also in $mode_2$ obtained both, the advantages given by the fast-update MS-DPCMC approach and the advantages given by the double carrier update, allowed due to the trailing-triangle carrier.

Fig. 6.15 shows the simulating response to a $500\,\text{mA}(OP_2) \rightarrow 0(OP_1)$ load step variation. As theoretically predicted, this digital-predictive controller is able to operate without any problem related to FC voltages stability. Operating points OP_1 e OP_2 considered for this simulation are highlighted in Fig. 6.14.

Fig. 6.16 shows the simulating response to a $500\,\text{mA}(OP_4) \rightarrow 0(OP_3)$

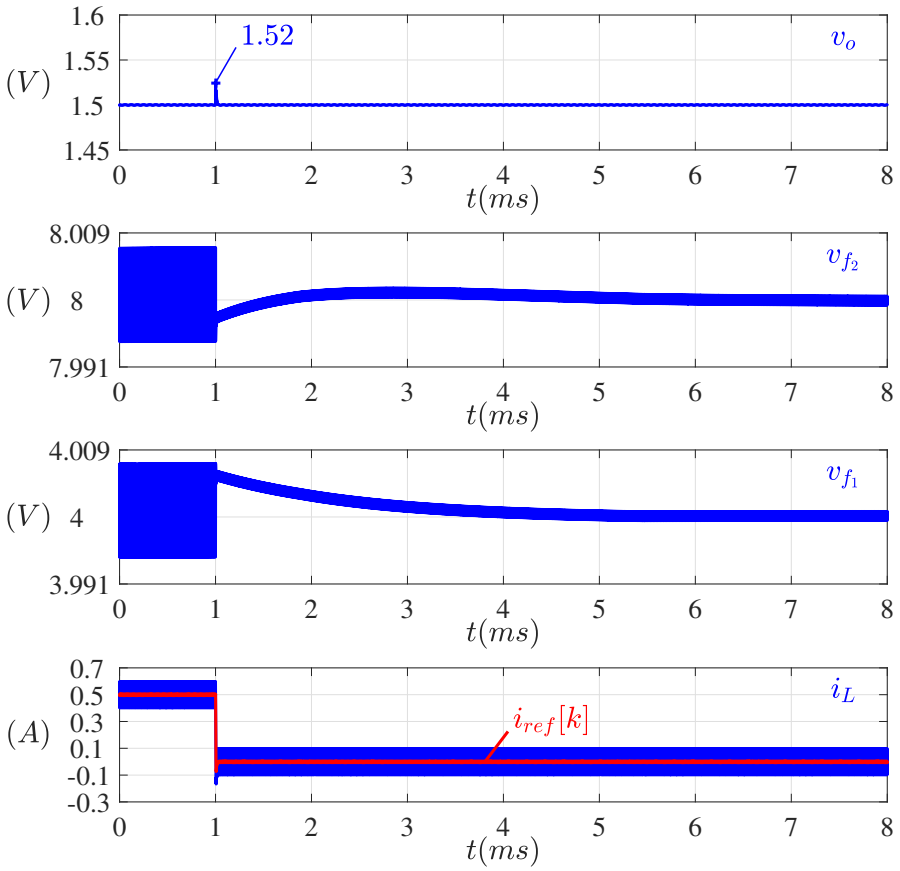


Figure 6.15: *Simulating response to a* $500\,\text{mA}(OP_2) \rightarrow 0(OP_1)$ *load step variation for the 4-LFC Buck converter with fats-update* average *MS-DPCMC with* double-update *of the modulating signal in* $mode_1$. *From top to the bottom: output voltage,* C_{f_2} *voltage,* C_{f_1} *voltage, inductor and reference currents.*

load-step variation for operating $mode_2$. Condition (6.55) is verified for both operating points and the converter operate stably, without any FCs voltages issue. It is interesting to analyse what happens when condition in (6.55) is no longer verified. For the chosen design, the developed stability condition is violated when the output I_o current exceeds $\approx 2.4\,\text{A}$. The simulation test summarized in Fig. 6.17 shows what happens under such conditions. Precisely, the figure shows the simulating response to a $500\,\text{mA}(OP_4) \rightarrow 2.5\,\text{A}(OP_5)$ load-step variation. The operating point OP_4 before the load-

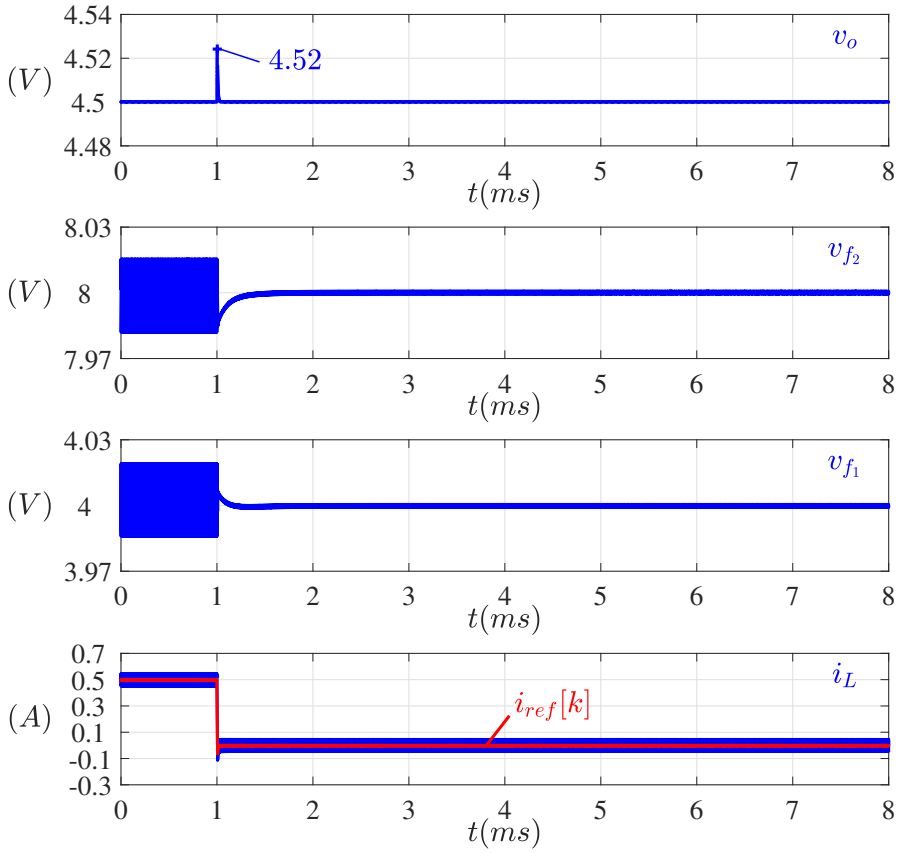


Figure 6.16: *Simulating response to a* $500\,\mathrm{mA}(OP_4) \rightarrow 0(OP_3)$ *load step variation for the 4-LFC Buck converter with fats-update* average *MS-DPCMC with* double-update *of the modulating signal in* $mode_2$. *From top to the bottom: output voltage, FC voltage of* C_{f_2}, *FC voltage of* C_{f_1}, *inductor and reference currents.*

step ensures system stability. In contrast, the resulting operating point OP_5 violates the condition (6.55) and therefore the system becomes unstable. Again, forecasts obtained by the developed approach correctly predicted the actual FC voltages stability properties.

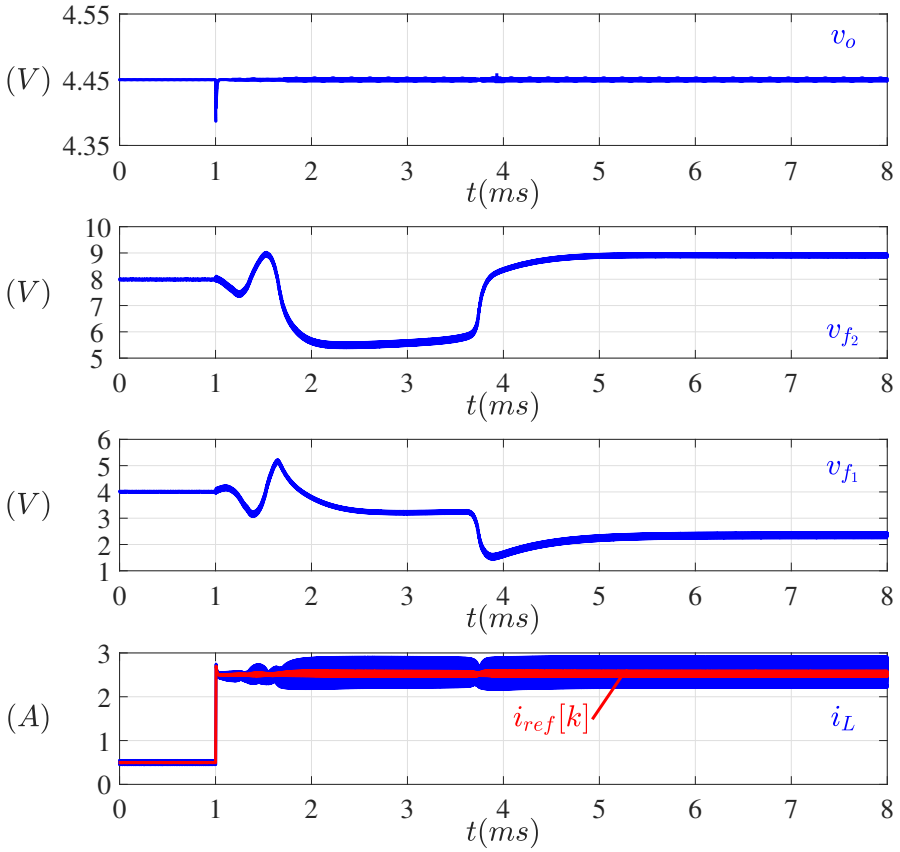


Figure 6.17: *Simulating response to a* $500\,\mathrm{mA}(OP_4) \rightarrow 2.5\,\mathrm{A}(OP_5)$ *load step variation for the 4-LFC Buck converter with fats-update* average *MS-DPCMC with* double-update *of the modulating signal in* $mode_2$. *From top to the bottom: output voltage, FC voltage of* C_{f_2}, *FC voltage of* C_{f_1}, *inductor and reference currents.*

6.3.3 5-LFC Buck converter operating with fast-update *peak* MS-DPCMC

Fig. 6.18 shows the summary stability plot for the 5-LFC Buck converter operating with fast-update *peak* MS-DPCMC. As in Fig. 6.8, the voltage conversion ratio M is represented on the x-axis while the normalized output current I_{o_N} on y-axis. The system operates stably in operating modes 1 and 3, while in modes 2 and 4 stability is not guaranteed, also for zero output current. The red vertical lines indicate the operating points at zero current ripple through the inductor.

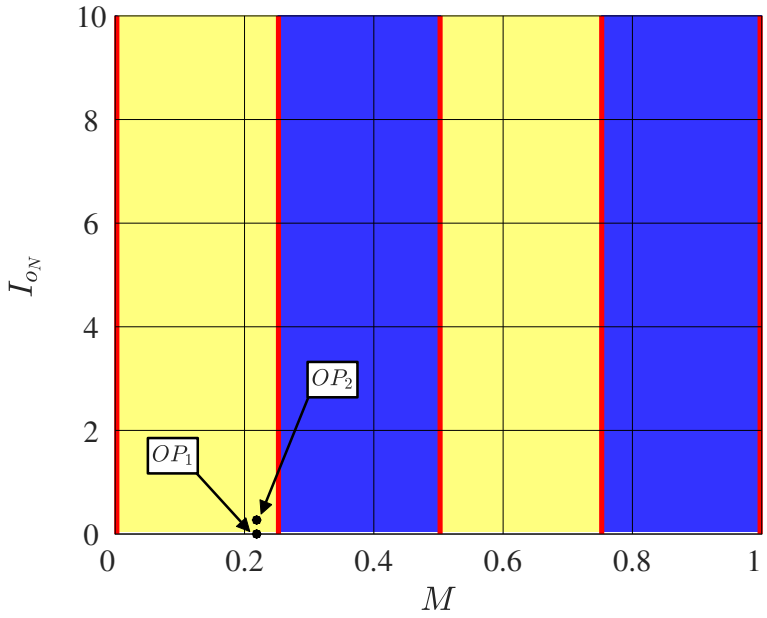


Figure 6.18: *Summary plot of the FC voltages stability properties for the 5-LFC Buck converter with fast-update* peak *MS-DPCMC. The voltage conversion ratio M is represented on the x-axis, while the normalized output current I_{o_N} is represented on y-axis. Stable operating point are represented in yellow while unstable operating point in blue. Red vertical lines denote operating points corresponding at $M = \frac{i}{N-1}$, with $i = 1, 2, ..., N-1$. Operating points used in simulations tests are highlighted with corresponding labels.*

Operating points OP_1 and OP_2 highlighted in the figure are relative to

the chosen case-study and are used in the following simulation test. Fig. 6.19 shows the simulating response to a $500\,\mathrm{mA}(OP_2) \rightarrow 0(OP_1)$ load-step variation. With such load-step variation the system moves from operating point OP_2 to operating point OP_1. According to the stability summary reported in Fig. 6.18, both operating points ensure stable FC voltages operation. Simulation results confirm that average FC voltages are stable and lead back to their balanced values also after the transient. Others predicted stability properties summarized by Fig. 6.18 are tested with several PLECS/Matlab® simulations. No discrepancies between the predicted FC voltages stability and the behaviour observed in the simulations emerged.

Stability properties can be more complex. Indeed, as show in the next subsection, the fast-update approach applied to the 8-L case leads to a rather complicated dependence of the FC voltages stability with respect to the operating point.

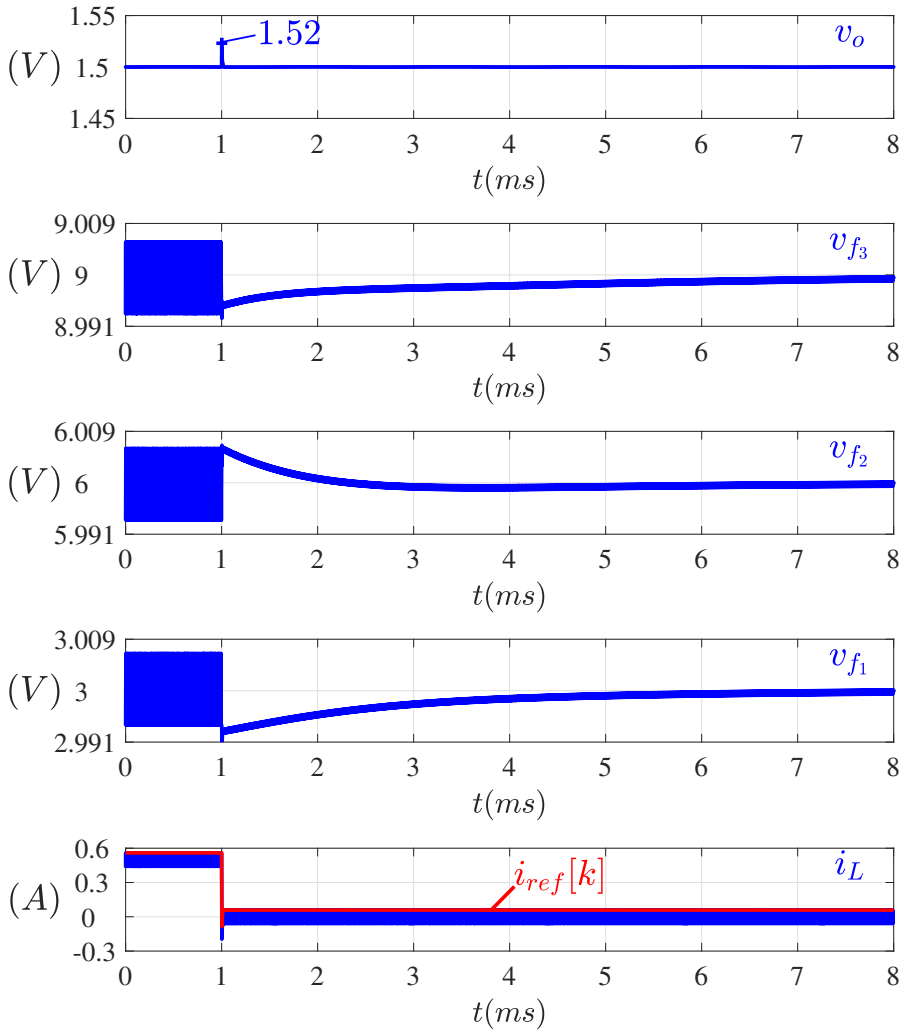


Figure 6.19: *Simulating response to a* $500\,\mathrm{mA}(OP_2) \rightarrow 0(OP_1)$ *load step variation for the 5-LFC Buck converter with fats-update* peak *MS-DPCMC in* $mode_1$. *From top to the bottom: output voltage, FC voltages of* C_{f_3}, C_{f_2} *and* C_{f_1}, *inductor and reference currents.*

6.3.4 8-LFC Buck converter operating with fast-update *peak* MS-DPCMC

Fig. 6.20 shows the summary stability plot for the 8-LFC Buck converter operating with fast-update *peak* MS-DPCMC. The figure shows that the fast-update controller can stably operate in $mode_7$. For other operating modes there is a fairly complicated dependence of the FC voltages stability properties with respect to the operating point. Such behaviour makes the fast-update control approach practically inapplicable to the 8-LFC Buck converter.

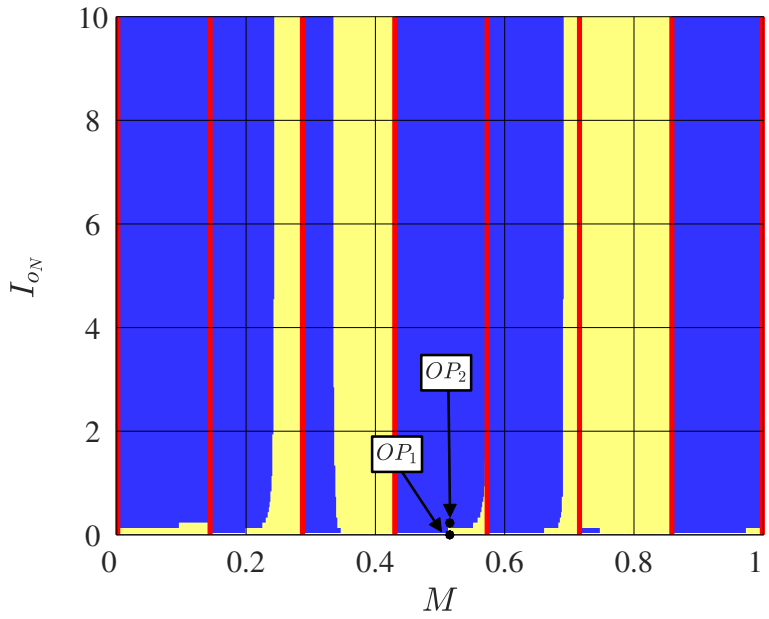


Figure 6.20: *Summary plot of the FC voltages stability properties for the 8-LFC Buck converter with fast-update* peak *MS-DPCMC. The voltage conversion ratio M is represented on the x-axis, while the normalized output current I_{o_N} is represented on y-axis. Stable operating point are represented in yellow while unstable operating point in blue. Red vertical lines denote operating points corresponding at $M = \frac{i}{N-1}$, with $i = 1, 2, ..., N-1$. Operating points used in simulations tests are highlighted with corresponding labels.*

The output inductance and capacitance values used in this test are four

times smaller than the design used in the 3-L case (i.e., $L_{3\text{-L}} = 6.5\,\mu\text{H}$, $C_{o\,3\text{-L}} = 50\,\mu\text{F}$, $L_{8\text{-L}} = 1.6\,\mu\text{H}$ and $C_{o\,8\text{-L}} = 12.5\,\mu\text{F}$). Fig. 6.21 shows the simulating response to a $0 \rightarrow 500\,\text{mA}$ load step variation. With such load-step variation the system moves from operating point OP_1 to operating point OP_2. These points are also highlighted in Fig. 6.20.

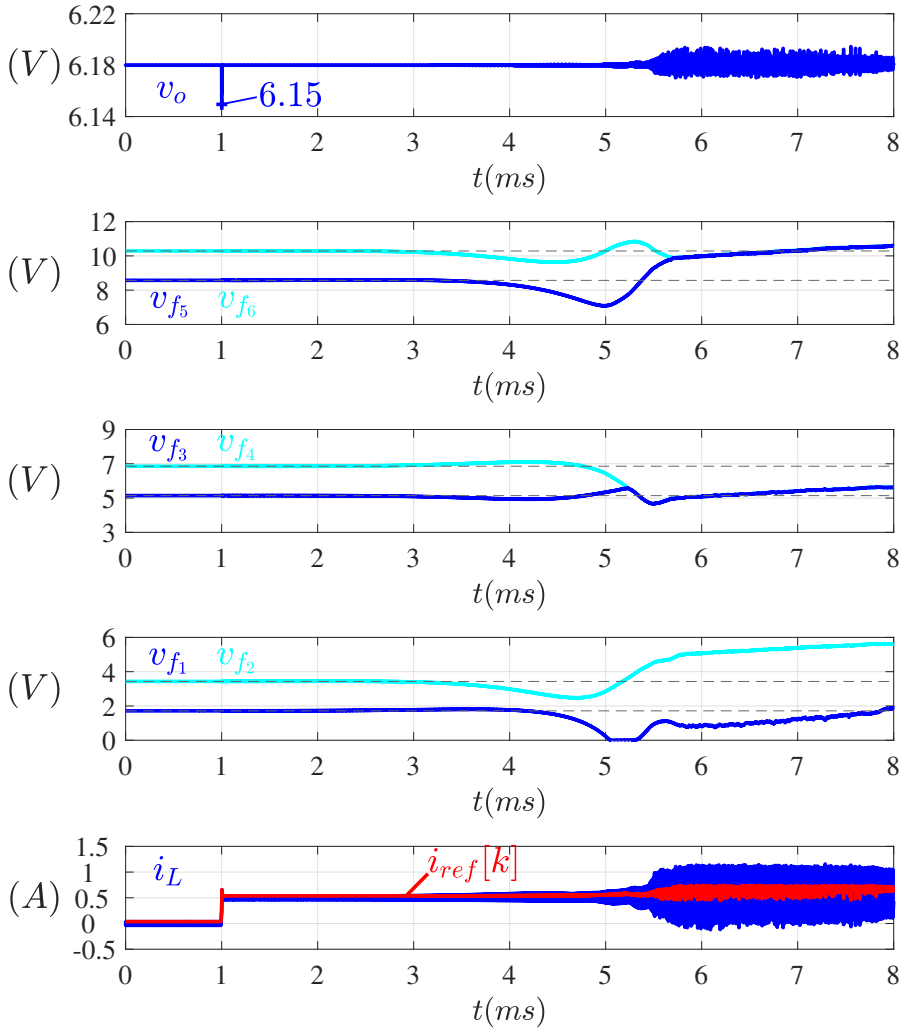


Figure 6.21: *Simulating response to a* $500\,\text{mA} \rightarrow 0$ *load step variation for the 8-LFC Buck converter with fats-update* peak *MS-DPCMC in* $mode_4$. *From top to the bottom: output voltage, FC voltages of* C_{f_6}, C_{f_5}, C_{f_4}, C_{f_3}, C_{f_2}, C_{f_1}, *inductor and reference currents. Dashed lines indicate balanced average FC voltages.*

According to forecasts summarized in Fig. 6.20 before the load-step variation the system works at a stable operating point and all FC voltages arise their balanced values. After the load-step the system works at an unstable operating point and thus FC voltages become unstable. Once again, what theoretically predicted finds confirmation in simulation testing.

From the comparisons reported in this chapter and from other simulations omitted for reasons of space, no discrepancies ever emerged between what theoretically predicted by the proposed general FC voltage stability analysis for the generic N-LFC Buck converter and the observed simulating behaviour.

Conclusion

A complete and exhaustive study on the application of digital predictive current-mode controls applied to multi-level converters is made. This study includes investigating the inductor current stability properties and how they change with different implementations of the digital pulse-width modulator. In particular, pairs of controlling points and DPWM implementation have been identified in order to ensure both the static inductor current stability and the dead-beat controller behaviour. In addition to the inductor current stability study, the resulting research work leads to the formulation of a unified analysis strategy for predicting the FCs voltages issue. In addition to a detailed investigation of all the inherent issues in applying digital-predictive current-mode controls to N-LFC Buck converters, taking advantage of the unique properties of MLFC converters, other two DPCMC have been successfully studied and implemented: the multi-sampled DPCMC and the fast-update multi-sampled DPCMC. The corrective action that allows the DPCMC to eliminate the sampled error on the inductor current requires two switching periods in the DPCMC. In the multi-sampled DPCMC implementation, this time is reduced to $2\frac{T_s}{N-1}$. In the control that uses the fast-update of the modulating signal, this time is even further reduced to $\frac{T_s}{N-1}$. Being able to act rapidly in recovering the error on the inductor current with respect to the reference value, making it possible to achieve a faster inner-loop, which in turn made it possible to implement a faster external outer-voltage control loop. Both new implementations allow faster controls thanks to the multi sampling in the inductor current. To understand how parametric variation

could change the stability properties of the controllers, several simulation and experimental tests were conducted on the 3-LFC Buck converter. On the latter, *peak* and *average* DPCMC have been tested in both single-sampled and multi-sampled implementations. The instability of the FC voltage for low load-current values of the *valley* DPCMC, previously documented by the theoretical study, has also been ascertained experimentally.

A well-known critical aspect of multi-level converters is the sensitivity of the FC voltage balancing properties to mismatches in the control signals. Monte Carlo type simulations were conducted for this purpose and the emerged properties are therefore verified experimentally. Precisely, the behaviour of 3-LFC Buck converter with DPCMC in the presence of large intentional mismatches in the control signals is experimentally observed. Tests show that the DPCMC in its single-sampled implementation does not allow to recover the FC voltage imbalance. In contrast, MS-DPCMC implementations allow to partial recovery it. Additionally, the fast-update *peak* MS-DPCMC proved to be able to recover practically all the FC voltage imbalance intentionally created through very pronounced mismatches in the control signals. Thus, fast-update MS-DPCMC and MS-DPCMC not only allow to obtain a much faster corrective action on the inductor current with respect to the single-sampled DPCMC but also ensure a much lower sensitivity of the FC voltages with respect to mismatch in the control signals. For the experimental tests, a custom prototype is built and all controllers are implemented in VHDL on a commercial FPGA. The analysis methodology initially used to study the stability of the FC voltage in the 3-LFC Buck converter operating with digital-predictive controllers is extended to all N-LFC Buck converters and for all operating modes.

Appendix A

In this Appendix the basic steps to obtain the control equation in the case of DPCMC applied to the Buck N-LFC converter are detailed. N is a generic integer number higher than 2. Fig. 22 exemplifies the control response and recovery of an initial inductor current error of the N-LFC Buck converter with *peak* DPCMC operating in $mode_1$ (i.e., $0 < M < \frac{1}{N-1}$). Notation is this figure is used as a reference in the following steps.

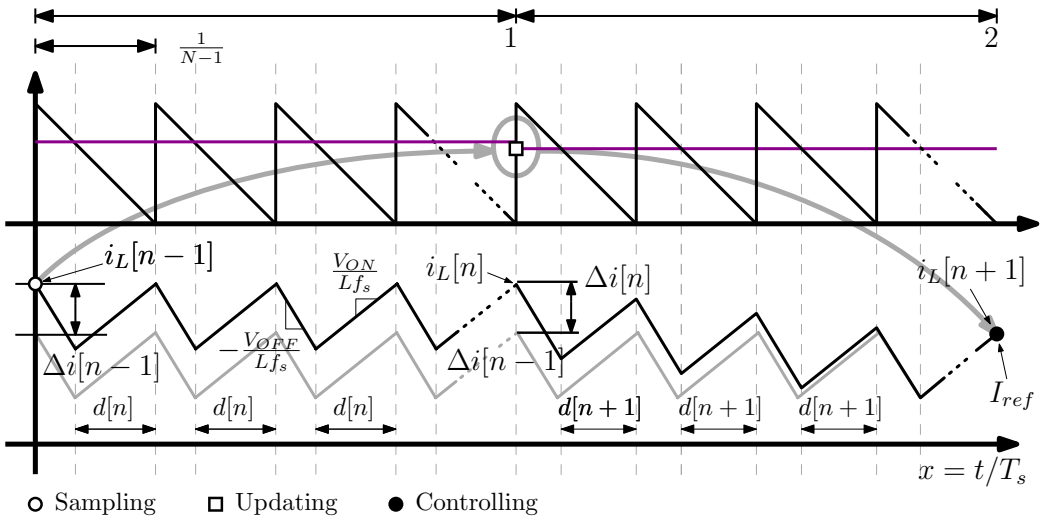


Figure 22: *Operation of N-LFC Buck converter with* peak *DPCMC. Representation of modulating signal (on top) and inductor current (on bottom) behaviours during the correction of an initial inductor current perturbation.*

The final inductor current value $i_L[n+1]$ can be written as a function of the initial sampled $i_L[n-1]$ the duty cycles $d[n]$ and $d[n+1]$ and the current

slopes

$$i_L[n+1] = i_L[n-1] + \left(-\frac{V_{OFF}}{Lf_s}\left(\frac{1}{N-1} - d[n]\right) + \frac{V_{ON}}{Lf_s}d[n]\right)(N-1) + \\ + \left(-\frac{V_{OFF}}{Lf_s}\left(\frac{1}{N-1} - d[n+1]\right) + \frac{V_{ON}}{Lf_s}d[n+1]\right)(N-1). \tag{1}$$

By simplifying some products, one has

$$i_L[n+1] = i_L[n-1] + \frac{d[n]}{Lf_s}(V_{OFF} + V_{ON})(N-1) - \frac{V_{OFF}}{Lf_s} + \\ + \frac{d[n+1]}{Lf_s}(V_{OFF} + V_{ON})(N-1) - \frac{V_{OFF}}{Lf_s}. \tag{2}$$

The expression of V_{OFF} and V_{ON} are

$$V_{OFF} = V_o = M(N-1)\frac{V_g}{(N-1)} \quad \text{and} \quad V_{ON} = \frac{V_g}{(N-1)}(1-(N-1)M). \tag{3}$$

Using (3) in (2), one has

$$i_L[n+1] = i_L[n-1] + \frac{V_g}{Lf_s}(d[n] + d[n+1]) - \frac{2MV_g}{Lf_s}. \tag{4}$$

Imposing that the new duty cycle $d[n+1]$ controls the inductor current $i_L[n+1]$ to be equal to I_{ref}, the final control equation is obtained

$$\boxed{d[n+1] = \frac{f_s L}{V_g}(I_{ref} - i_L[n-1]) + 2M - d[n]}. \tag{5}$$

In according to the definition (2.15), the expression that describes the propagation of the initial inductor current perturbation $\Delta i_L[n-1]$ in (6.6), can be easily obtained by subtracting the steady-state peak inductor current expression in (4).

As has already been shown throughout the thesis for selected pairings of DPWM carrier (i.e., time-position of sampling instant of the inductor

current) and controlling point, control equations and static inductor current properties do not change. Therefore, the expression (5) and the consequent dead-beat behaviour hold also for *valley* and *average* DPCMC.

Appendix B

In this Appendix is analysed the fast-update *average* MS-DPCMC with double modulating signal update. Fig. 23 exemplify the operation for the 4-L case operating in $mode_1$ (i.e., $0 < M < \frac{1}{N-1}$). The modulating signal is sampled twice for each sub-period (i.e., once per $\frac{T_s}{2(N-1)}$). The duty-cycle update occurs immediately after the sampling instant. Clearly, between the sampling and the update instant, the minimum amount of time necessary to calculate the new duty-cycle value must be waited. In Fig. 23, this time is indicated with Δt_{calc}. The inductor current sample, acquired on the valley of the TTE carrier, that contains the information regarding the average inductor current during the on-phase, is used to control the average inductor current during the next off-phase. Instead, the inductor current sample, acquired on the peak of the TTE carrier, is used to control the next average inductor current during the on-phase. With respect to the notation in Fig. 23, I_{r0} is used in order to modulate the position of the trailing-edge of S_3 in order to regulate $I_{f0} = I_{\mathrm{ref}_N}$ while I_{f0} is used to modulate the position of the leading-edge of S_2 in order to obtain $I_{r1} = I_{\mathrm{ref}_N}$.

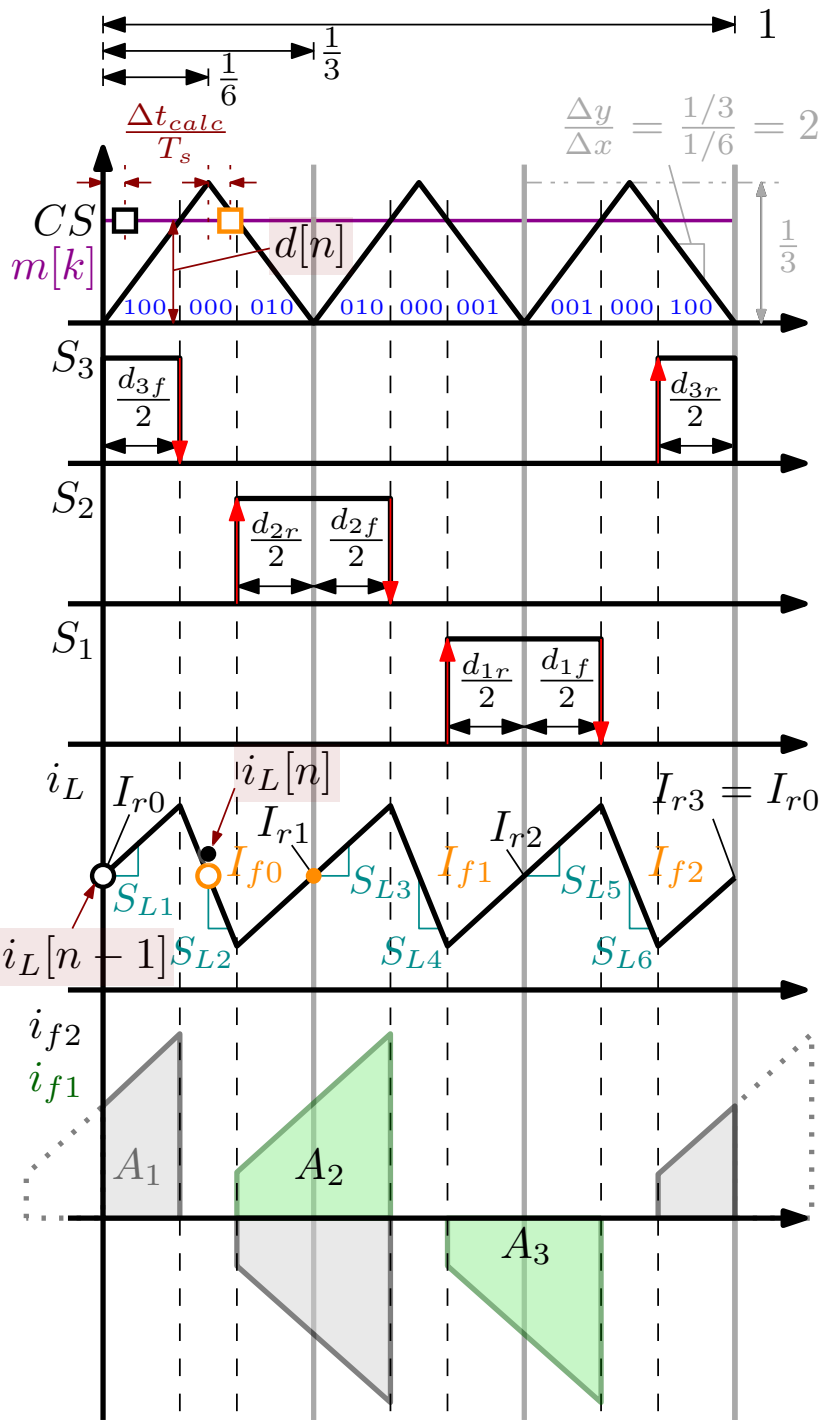


Figure 23: *Operation of 4-LFC Buck converter with fast-update* average *MS-DPCMC with double update modulating signal update.*

The following steps detail how to get the control equation. Fig. 23 is used as a reference. Currents in figure are normalized with respect to the constant $\frac{V_g}{(N-1)Lf_s}$. The normalized inductor current value $i_L[n]$ can be written as a function of the initial sampled $i_L[n-1]$ the actual duty cycles $d[n]$ and the current slopes

$$i_L[n] = i_L[n-1] + \frac{d[n]}{2} SL_1 + \left(\frac{1}{6} - \frac{d[n]}{2}\right). \tag{6}$$

By simplifying some products, one has

$$i_L[n] = i_L[n-1] + \frac{d[n]}{2}\left(SL_1 - SL_2\right) + \frac{SL_2}{2}. \tag{7}$$

The expression of the normalized inductor curent slopes SL_1 and SL_2 are respectively given by

$$SL_1 = 1 - (N-1)M \quad \text{and} \quad SL_2 = -\frac{V_o}{Lf_s}\left(\frac{V_g}{(N-1)Lf_s}\right)^{-1} = -(N-1)M. \tag{8}$$

Using (8) in (7), one has

$$i_L[n] = i_L[n-1] + \frac{d[n]}{2} - \frac{M}{2}. \tag{9}$$

Imposing that the new duty cycle $d[n]$ controls the average inductor current $i_L[n]$ to be equal to I_{ref}, the final control equation is obtained

$$\boxed{d[n] = 2\left(I_{\text{ref}_N} - i_L[n-1]\right) + M}. \tag{10}$$

Same control equation holds for the case in which the sampled current $i_L[n-1]$ is the average inductor current during the turn-off and the controlled point is on the middle on the next on-phase (e.g. $i_L[n-1] \leftarrow I_{f0}$ and $i_L[n] \leftarrow I_{\text{ref}}$). The reason why the duty-cycle $d[n]$ appears halved in (6) lies in slope values of the used TTE carrier. Indeed, as showed in Fig. 23 the slope of the TTE carrier is $\Delta y/\Delta x = 2$, thus when the modulating signal is equal to $d[n]$ the

corresponding time interval is $\frac{d[n]}{2}$.

Next steps prove the static stability on the inductor current. Fig. 23 is used as a reference. The propagation of an inductor current error on $i_L[n-1]$ can be generically described with the following equation

$$\Delta i_L[n+1] = \Delta i_L[n-1] + \frac{d[n]}{2} SL_1 + SL_2 \left(\frac{1}{2(N-1)} - \frac{d[n]}{2} \right) + \\ + \frac{d[n+1]}{2} SL_3 + SL_2 \left(\frac{1}{2(N-1)} - \frac{d[n+1]}{2} \right), \tag{11}$$

where $\frac{d[n+1]}{2}$ is supposed to be $\frac{d_{2_r}}{2}$ of Fig. 23. Using the expression of current slopes one has

$$\Delta i_L[n+1] = \Delta i_L[n-1] + \frac{1}{2}\left(d[n] + d[n+1]\right) - M. \tag{12}$$

Now, the predictive equation for $d[n+1]$ can be written as

$$d[n+1] = (I_{\mathrm{ref}_N} - I_{f0}) + M, \tag{13}$$

where

$$I_{f0} = i_L[n-1] + SL_1 \frac{d[n]}{2} + \left(\frac{1}{6} - \frac{d[n]}{2} \right) SL_2. \tag{14}$$

By substituting (14) in (13) one has

$$d[n] + d[n+1] = M - \frac{SL_2}{3} - 2\Delta i_L[n-1]. \tag{15}$$

Using (15) in (12) one finally has

$$\boxed{\frac{\Delta i_L[n+1]}{\Delta i_L[n-1]} = 0}. \tag{16}$$

Expression (16) proves the static stability of the inductor current and the dead-beat action of the fats-update *average*MS-DPCMC with double-update

of the modulating signal.

In order to apply the proposed FC voltage stability analysis described in Chapter 6, one has to consider that unlike other controllers studied in this thesis, for the fast-update *average* MS-DPCMC with double-update of the modulating signal *two* sets of control equations must be considered. Precisely, with the normalized-current notation one has

$$\begin{aligned} d_{3f} &= 2\left(I_{\mathrm{ref}_N} - I_{r0}\right) + M & & & d_{3r} &= 2\left(I_{\mathrm{ref}_N} - I_{f2}\right) + M \\ d_{2f} &= 2\left(I_{\mathrm{ref}_N} - I_{r1}\right) + M & & \text{and} & d_{2r} &= 2\left(I_{\mathrm{ref}_N} - I_{f0}\right) + M \\ d_{1f} &= 2\left(I_{\mathrm{ref}_N} - I_{r2}\right) + M & & & d_{1r} &= 2\left(I_{\mathrm{ref}_N} - I_{f1}\right) + M. \end{aligned} \tag{17}$$

The definition of I_{f_i} and I_{r_i} with $i = 1, 2, ...(N-1)$, can be easily inferred from Fig. 23. Also, the sequence of the status vector defined in (6.25) has to be changed. The new sequence can be founded in Fig. 23 (i.e., the blue numbers under the TTE carrier). Final results of the FC voltages stability analysis are discussed in Sec. 6.3.2.

Bibliography

[1] A. G. O. (EEA), C. Guerreiro, and N. Joana Soares (Norwegian Institute for Air Research, *Air quality in Europe — 2020 report*, 1st ed. Luxembourg: Publications Office of the European Union, 2020.

[2] V. Masson-Delmotte, P. Zhai, H.-O. Pörtner, D. Roberts, J. Skea, and P. R. S. et. al, *Global warming of 1.5˚ — IPCC Special report*, 1st ed. Intergovernmental Panel on Climate Change, 2019.

[3] P. Gueguen, "How power electronics will reshape to meet the 21st century challenges?" in *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, 2015, pp. 17–20.

[4] M. Gaboriault, "Us merchant markets and applications for internal ac/dc switching power supplies and dc/dc converters," in *APEC 2000. Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.00CH37058)*, vol. 1, 2000, pp. 59–63 vol.1.

[5] S. D. Mitchell, S. M. Ncube, T. G. Owen, and M. H. Rashid, "Applications and market analysis of dc-dc converters," in *2008 International Conference on Electrical and Computer Engineering*, 2008, pp. 887–891.

[6] I. Technologies, *Automotive application guide*, 2021. [Online]. Available: https://www.infineon.com/cms/en/applications/automotive/

[7] ——, *AURIX(TM) 32-bit microcontrollers for automotive and industrial applications*, 2020. [Online]. Available: https://www.infineon.com/cms/en/product/microcontroller/

[8] T. Instruments, *Power Supply Reference Design for Automotive Microcontroller in Gateway and Body Control Module*, 2018. [Online]. Available: https://www.ti.com/tool/TIDA-01412

[9] S. M. Ahsanuzzaman, A. Prodić, and D. A. Johns, "An integrated high-density power management solution for portable applications based on a multioutput switched-capacitor circuit," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4305–4323, 2016.

[10] B. Nguyen, N. Tang, W. Hong, Z. Zhou, and D. Heo, "High-efficiency fully integrated switched-capacitor voltage regulator for battery-connected applications in low-breakdown process technologies," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6858–6868, 2018.

[11] R. Jain, B. M. Geuskens, S. T. Kim, M. M. Khellah, J. Kulkarni, J. W. Tschanz, and V. De, "A 0.45–1 v fully-integrated distributed switched capacitor dc-dc converter with high density mim capacitor in 22 nm tri-gate cmos," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 917–927, 2014.

[12] Z. Tianting, Z. Yue, and C. Baoxing, "An isolated dc-dc converter with fully integrated magnetic core transformer," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, 2017, pp. 1–4.

[13] S. Dietrich, L. Liao, F. Vanselow, R. Wunderlich, and S. Heinen, "A 1mv voltage ripple 0.97mm¡sup¿2¡/sup¿ fully integrated low-power hybrid buck converter," in *2013 Proceedings of the ESSCIRC (ESSCIRC)*, 2013, pp. 395–398.

[14] I. Park, J. Oh, and C. Kim, "A power management system based on adaptive low-dropout voltage regulator with optimal reference pre-compensation technique," in *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2021, pp. 1–4.

[15] D. W. Lee, K.-P. Hwang, and S. X. Wang, "Fabrication and analysis of high-performance integrated solenoid inductor with magnetic core," *IEEE Transactions on Magnetics*, vol. 44, no. 11, pp. 4089–4095, 2008.

[16] X. Fang, R. Wu, L. Peng, and J. K. O. Sin, "A novel integrated power inductor with vertical laminated core for improved l/r ratios," *IEEE Electron Device Letters*, vol. 35, no. 12, pp. 1287–1289, 2014.

[17] R. Wu and J. K. O. Sin, "A novel silicon-embedded coreless inductor for high-frequency power management applications," *IEEE Electron Device Letters*, vol. 32, no. 1, pp. 60–62, 2011.

[18] S. Prabhakaran, Y. Sun, P. Dhagat, W. Li, and C. Sullivan, "Micro-fabricated v-groove power inductors for high-current low-voltage fast-transient dc-dc converters," in *2005 IEEE 36th Power Electronics Specialists Conference*, 2005, pp. 1513–1519.

[19] X. Fang, R. Wu, L. Peng, and J. K. O. Sin, "A novel silicon-embedded toroidal power inductor with magnetic core," *IEEE Electron Device Letters*, vol. 34, no. 2, pp. 292–294, 2013.

[20] C. Ahn, Y. Kim, and M. Allen, "A fully integrated planar toroidal inductor with a micromachined nickel-iron magnetic bar," *IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A*, vol. 17, no. 3, pp. 463–469, 1994.

[21] Y. Ding, X. Fang, R. Wu, and J. K. O. Sin, "A new fan-out-package-embedded power inductor technology," *IEEE Electron Device Letters*, vol. 41, no. 2, pp. 268–271, 2020.

[22] Y. Ding, X. Fang, Y. Gao, Y. Cai, X. Qiu, P. K. T. Mok, S. W. R. Lee, K. M. Lau, and J. K. O. Sin, "A power inductor integration technology using a silicon interposer for dc-dc converter applications," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2018, pp. 347–350.

[23] S. M. Ahsanuzzaman, A. Prodić, and D. A. Johns, "An integrated high-density power management solution for portable applications based on a multioutput switched-capacitor circuit," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4305–4323, 2016.

[24] Y. Sugawa, K. Ishidate, M. Sonehara, and T. Sato, "Carbonyl-iron/epoxy composite magnetic core for planar power inductor used in package-level power grid," *IEEE Transactions on Magnetics*, vol. 49, no. 7, pp. 4172–4175, 2013.

[25] J. Lee, Y.-K. Hong, S. Bae, J. Jalli, J. Park, G. S. Abo, G. W. Donohoe, and B.-C. Choi, "Integrated ferrite film inductor for power system-on-chip (powersoc) smart phone applications," *IEEE Transactions on Magnetics*, vol. 47, no. 2, pp. 304–307, 2011.

[26] C. A. Pardue, M. L. F. Bellaredj, H. M. Torun, M. Swaminathan, P. Kohl, and A. K. Davis, "Rf wireless power transfer using integrated inductor," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 5, pp. 913–920, 2019.

[27] F. Zhang, F. Peng, and Z. Qian, "Study of the multilevel converters in dc-dc applications," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, vol. 2, 2004, pp. 1702–1706 Vol.2.

[28] S. Buso and P. Mattavelli, *Digital Control in Power Electronics, 2nd Edition*, 2nd ed. Morgan and Claypool Publishers, 2015.

[29] K. Sozański, *Digital Signal Processing in Power Electronics Control Circuits*, 2nd ed. Springer, 2013.

[30] N. Mohan, T. M. Undeland, and W. P. Robbins, *Converters Applications, and Design*, 2nd ed. John Wiley and Sons, inc., 1995.

[31] R. W. Erickson and D. Maksimovič, *Fundamental of Power Electronics*, 2nd ed. Kluwer Academic Publishers, 2001.

[32] S. K. Mitra, *Digital Signal Processing*, 2nd ed. McGraw-Hill, 2000.

[33] L. Corradini, D. Maksimovič, P. Mattavelli, and R. Zane, *Digital Control of High-Frequency Switched-Mode Power Converters*, 2nd ed. Wiley, 2015.

[34] B. A. Mather and D. Maksimovič, "Quantization effects and limit cycling in digitally controlled single-phase pfc rectifiers," in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 1297–1303.

[35] M. Bradley, E. Alarcòn, and O. Feely, "Analysis of limit cycles in a pi digitally controlled buck converter," in *2012 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2012, pp. 628–631.

[36] ——, "Design-oriented analysis of quantization-induced limit cycles in a multiple-sampled digitally controlled buck converter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 4, pp. 1192–1205, 2014.

[37] J. Chen, A. Prodic, R. Erickson, and D. Maksimovič, "Predictive digital current programmed control," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 411–419, 2003.

[38] T. Instruments, *TPS6215xA-Q1 3-V to 17-V 1-A Step-Down Converter with DCS-Control*, Jul. 2019. [Online]. Available: http://www.ti.com/lit/ds/symlink/tps62152a-q1.pdf

[39] ——, *TPS6217x 3-V to 17-V, 0.5-A Step-Down Converters with DCS-Control*, May 2017. [Online]. Available: http://www.ti.com/lit/ds/symlink/tps62170.pdf

[40] ——, *TPS560200-Q1 4.5-V to 17-V Input, 500-mA Synchronous Step-Down Converter With Advanced Eco-mode*, May 2019. [Online]. Available: http://www.ti.com/lit/ds/symlink/tps560200-q1.pdf

[41] C. Newton and M. Summer, "Multi-level convertors a real solution to medium/high-voltage drives?" *Power Engineering Journal*, vol. 12, no. 1, pp. 21–26, 1998.

[42] T.-J. Kim, D.-W. Kang, Y.-H. Lee, and D.-S. Hyun, "The analysis of conduction and switching losses in multi-level inverter system," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, vol. 3, 2001, pp. 1363–1368 vol. 3.

[43] T. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference*, 1992, pp. 397–403 vol.1.

[44] ——, "Multilevel converters and derived topologies for high power conversion," in *Proceedings of IECON '95 - 21st Annual Conference on IEEE Industrial Electronics*, vol. 1, 1995, pp. 21–26 vol.1.

[45] T. Meynard, H. Foch, F. Forest, C. Turpin, F. Richardeau, L. Delmas, G. Gateau, and E. Lefeuvre, "Multicell converters: derived topologies," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 978–987, 2002.

[46] E. Abdelhamid, G. Bonanno, L. Corradini, P. Mattavelli, and M. Agostinelli, "Stability properties of the 3-level flying capacitor buck converter under peak or valley current programmed control," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 8031–8044, 2019.

[47] G. Bonanno and L. Corradini, "Digital predictive peak current-mode control for three-level buck converters," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019, pp. 1–7.

[48] J. Celikovic, R. Das, H.-P. Le, and D. Maksimovic, "Modeling of capacitor voltage imbalance in flying capacitor multilevel dc-dc converters," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019, pp. 1–8.

[49] H. Visser and P. van den Bosch, "Modelling of periodically switching networks," in *PESC '91 Record 22nd Annual IEEE Power Electronics Specialists Conference*, 1991, pp. 67–73.

[50] G. Bonanno and L. Corradini, "Digital predictive current-mode control of three-level flying capacitor buck converters," *IEEE Transactions on Power Electronics*, vol. 36, no. 4, pp. 4697–4710, 2021.

[51] E. Abdelhamid, L. Corradini, P. Mattavelli, G. Bonanno, and M. Agostinelli, "Sensorless stabilization technique for peak current mode controlled three-level flying-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 3208–3220, 2020.

[52] N. Vukadinovic, A. Prodic, B. A. Miwa, C. B. Arnold, and M. W. Baker, "Extended wide-load range model for multi-level dc-dc converters and a practical dual-mode digital controller," in *Proc. 31st IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 1597–1602.

[53] J. S. Rentmeister, C. Schaef, B. X. Foo, and J. T. Stauth, "A flying capacitor multilevel converter with sampled valley-current detection for multi-mode operation and capacitor voltage balancing," in *in Proc. 8th IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2016, pp. 1–8.

[54] G. Bonanno and L. Corradini, "Stability properties of digital predictive current-mode controllers for three-level flying capacitor converters," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 312–319.

Acknowledgements

I would like to thank my supervisor Luca Corradini and the whole group of Power Electronics here at the Department of Information Engineering in Padua, for their welcome, kindness, trust and cooperation. I would also like to express my affectionate appreciation to my fellow adventurers during these years, thank you dear: Eslam, Francesco, Ivan, Qing, Simone, Stefano, Yuchen. A special thanks go to Anita and Clara for their timeless and endless affection and support. Lastly, I would like to thank my family. Those who taught me the meaning of perseverance and honesty, two gifts of immeasurable value.