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Radiation Tolerant Multi-Bit Flip-Flop System with Embedded Timing Pre-Error Sensing

Abhishek Jain[1], *Member, IEEE,* Andrea Mario Veggetti[2], Dennis Crippa[2], Antonio Benfante[2], Simone Gerardin[3], *Member, IEEE,* and Marta Bagatin[3], *Member, IEEE*

***Abstract*— This paper presents the design, implementation methodology, and validation of a multi-bit flip-flop system that provides tolerance against Single Event Upsets (SEU) and Single Event Transients (SET) caused by radiation strikes. The proposed solution also has embedded timing pre-error sensing capability, which enables closed-loop integration of digital systems to work at optimal operating point (OPP) without any fail. It allows efficient real-time Dynamic Voltage Frequency Scaling (DVFS) implementation in the digital system. It helps detect aging-related and Total Ionizing Dose (TID) induced timing degradation in digital circuits. It can be implemented with any standard digital cell library (non-rad-hard), thereby providing a cost-effective solution for rad-hard applications. The design is implemented in ST BCD 90 nm technology in multiple configurations of bit sizes. A digital system based on ARM cortex M4 microprocessor has also been implemented with the proposed Flip-Flop (FF) and put on silicon for testing to validate various capabilities of the proposed design. The results are presented based on simulations, electrical characterization, and radiation tests.**

***Index Terms*— Soft error-tolerant flip-flop, single-event effects, in-situ delay monitors, radiation-tolerant digital circuits.**

I. INTRODUCTION

HIGH resilient systems which are tolerant against radiation-induced soft errors and adaptable to other device wear-out arising during product life-cycle like Negative and Positive Bias Temperature Instability (NBTI/PBTI) aging effects, TID effects, electromigration, etc. are gaining interest with the increased penetration of electronic devices in critical applications like medical, automotive, space, etc. These systems require innovative methods, architectures, and building blocks to achieve the designed tolerance level with minimal or no impact on cost, performance, and power consumption. FF being the basic building block of any digital system, indeed requires innovative and efficient solutions to enable designing such systems as the standard solutions fail to do so.

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[1]A. Jain is with STMicroelectronics Pvt Ltd. Greater Noida, India, and Ph.D. student at department of information engineering, University of Padova, Italy. (Email: abhishek.jain@st.com, abhishek.jain@studenti.unipd.it).

[2]A. Veggetti, D. Crippa and A. Benfante are with STMicroelectronics S.r.l, Agrate Brianza, Italy. (Email: {andrea.veggetti, dennis.crippa, antonio.benfante}@st.com)

[3]S. Gerardin and M. Begatin are with department of information engineering, University of Padova, Italy, (Email: simone.gerardin, marta.bagatin}@dei.unipd.it)

Depending upon the target application and radiation environment it will operate in, various hardening techniques can be deployed in flip-flops to achieve the required tolerance target [2,3,4]. For low radiation terrestrial applications, techniques such as BISER [5], Hysteresis [6], Charge Steering [7], etc., can be used to meet the target error rate acceptable by the application. These methods provide resilience to radiation to some extent but are not entirely immune. Other methods targeted for either terrestrial or space application but require very high tolerance and immunity against radiation are based on spatial and temporal redundancy. One of the most common hardened circuit architectures based on spatial redundancy is dual interlocked storage cell (DICE) [8]. Here, the interleaving provides dual node feedback to each storage node, making it difficult to change the state in case of a radiation strike. It is proven to be effective against SEU, but with lower feature sizes its prone to multi-node upsets [1,2] on single radiation strikes. Another variant of DICE, known as LEAP-DICE [9], where LEAP stands for Layout Design through Error-Aware Transistor Positioning, aims to mitigate the impact of multi-node charge collection but is not entirely adequate. Other cell-based methods where the redundant element is packed in single-cell are QUATTRO latch [10], Single Phase Clock Based radiation-tolerant flip-flop [11], etc.; all these structures are susceptible to multi-node charge sharing and requires the design of specific radiation-hardened cells. Another method proven to be very effective against SEU and multi-bit upsets (MBU) is Triple Modular Redundancy (TMR) [12]. This methodology is based on triplicating the FFs spatially and voting out the erroneous ones, thereby overcoming SEU faults. Its variant Delta TMR [13,14], based on temporal and spatial redundancy, deals with SET faults [2] along with SEU. Other TMR variants such as scannable TMR, latch-based TMR TSPC TMR, and self-correcting TMR, including delta TMR, were reported in [15], wherein delta TMR solution was found to be an effective rad-hard solution for space applications. Another self-correcting TMR solution called Temporal Self Voting Logic (TSVL) was reported in [16]. These TMR-based methodologies are proven to be very effective against radiation effects but are very costly to implement in terms of area, power, and timing overheads. There are robust multi-bit solutions that aim to reduce effective per-bit cost by grouping multiple bits and sharing added logic across multiple bits. One such system based upon temporal pulse clocked multi-bit TMR flip-flop was presented in [17]. The clock generation circuitry is shared across multiple bits, reducing the effective cost. Such a mechanism of sharing redundant logic across multi-bits is cost-

effective and exploited in the proposed methodology. Another limitation with the solutions, as mentioned earlier, is that they are effective against soft errors only; there is no mechanism to protect against slow device degradations caused by radiation-induced TID effects and aging effects. The standard technique of taking extra design margins during the implementation phase is used for these effects.

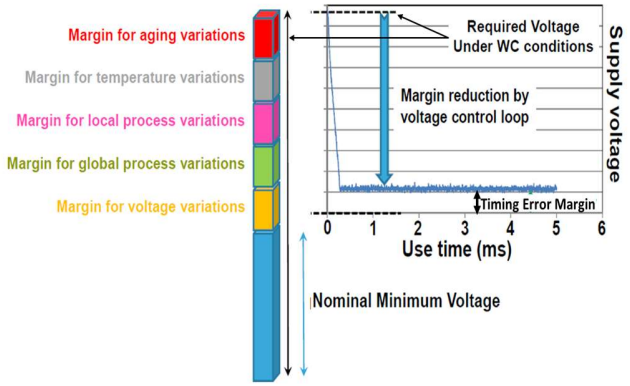

Fig. 1. Margins for semi-custom designs account for various variations and applications of in-situ delay monitors [8].

Conventionally semi-custom design flow used for the implementation of digital systems is based on the design for worst-case scenarios. During the design phase, margins are taken to account for voltage, process, and temperature variations. Additional margins are taken for aging effects as well. This margin leaves the enormous scope of optimization (shown in Fig. 1) as the worst scenarios may never occur during the product life cycle. In-situ monitoring timing monitoring circuits are targeted to exploit these margins to make the device work on the optimal operating point. There are techniques based on detecting timing errors and correcting them after they have occurred, known as Razor. It was first introduced with Razor-1 in [18], whose improved version Razor-II was reported in [19], and a low-cost iRazor solution was reported in [20]. The key idea of Razor is that data is stored in the main flip-flop and a shadow latch/flip-flop, which is sampled later. The mismatch between the two outputs reveals the occurrence of timing error. Here, the timing fault is allowed to occur in the main flip-flop; after that, advanced error correction and recovery mechanisms such as global clock gating, micro rollbacks, pipeline flushing, architectural replays, etc., are deployed to restore the system to a normal state. These mechanisms can be very costly, design specific, and do not guarantee complete error recovery in all scenarios, such as higher error rates. Due to inherent error detection capability, some of such designs also offer detection of soft errors. In razor-II [19], SEU effectiveness of razor-II flip-flop is presented. The errors detected by Razor-II flip-flops are recovered through an architectural replay mechanism that is very specific to microprocessors. It can be suitable for lower robustness applications as it offers no protection against SETs and multi-bit errors. Also, it requires designing of specific razor cell, which is not available in the standard cell library. There is another class of circuits which are based and other based on detection of timing pre-error conditions arising when data transitions start occurring close to active clock edge wherein FF main flip-flop data is not corrupted; these are called canary flip-flops [18,19,20,21]. The former requires complex error recovery mechanisms such as local micro rollbacks, pipeline flushing, etc., which may or may not recover errors leading to system reset. This methodology ensures that the circuit operates with a good safety margin. As demonstrated in [21,22,23,24], the canary-based in-situ monitors can be effectively and reliably used to provide prior setup violations, enabling automatic voltage frequency regulation to overcome cost impact, enhance performance, and adapt to device wear-outs.

The proposed brand-new FF system innovatively exploits the spatial and temporal redundancy methodology and embedded timing pre-error detection and multi-bit groupings to provide a low-cost, efficient, and reliable robust solution that can be implemented in any digital system with any non-rad-hard standard cell library. The paper is organized as follows: Section II illustrates a multi-bit FF system with the help of a 2-Bit example; Section III shows the design and implementation of various variants and their CAD results; Section IV presents test-chip implementation and silicon validation results; finally, Section V concludes the paper.

II. Multi-Bit Flip-Flop System

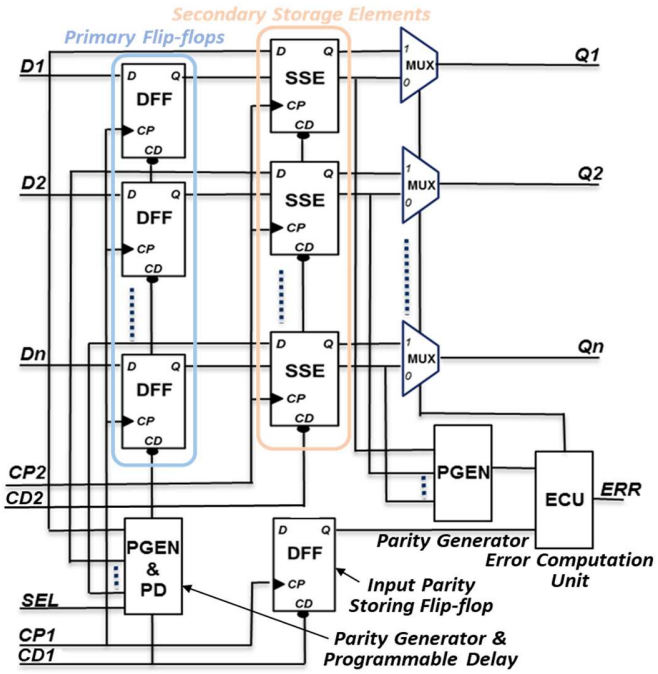

Fig. 2. Proposed Multi-bit FF System Block Diagram.

In Fig. 2, an n-bit system block diagram is shown. It mainly comprises of:

- Primary FFs: any standard D FF can be used.
- Replica Secondary Storage Element (SSE) for each Primary FF in original system. Here, SSE can be D FF or a simple latch as well. However, latch-based designs would require large hold margins. In the present scope

of paper, we concentrate only on FF based SSE.

- PGEN: n-bit Parity Generator. It can be an even or an odd parity generator.
- PD: Programmable Delay with select lines to fix the timing margin.
- Error Computation Unit (ECU) based on basic XOR gates. Its purpose is to compare the input parity stored in FF with parity computed from data stored in primary FFs.
- Output selection unit (MUX or similar logic): depending upon error condition it selects whether data stored in primary FF should pass through (ERR=0) or from SSE (ERR=1).
- The clock CP2 is skewed with respect to CP1 to provide multiple sampling times for D inputs so that any transient event due to radiation on D inputs can be filtered.
- Separate reset lines CD1 and CD2 for primary FFs and SSE respectively enable the circuit to avoid SET-induced faults on reset tree.

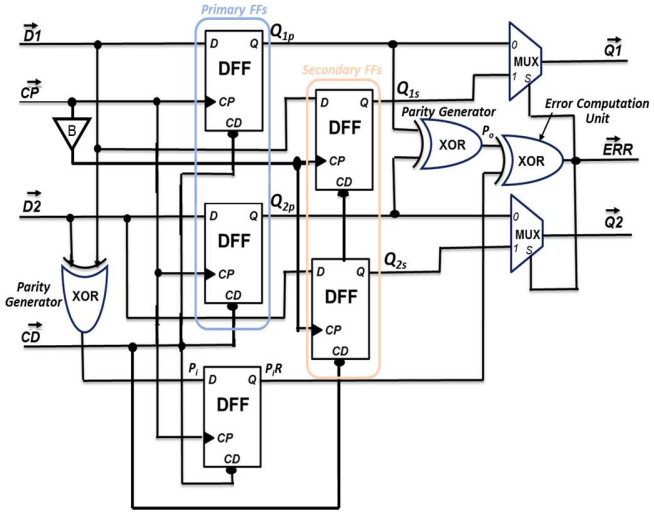

Fig. 3. 2-Bit Even Parity Proposed FF System Circuit Diagram with common reset and skewed clock.

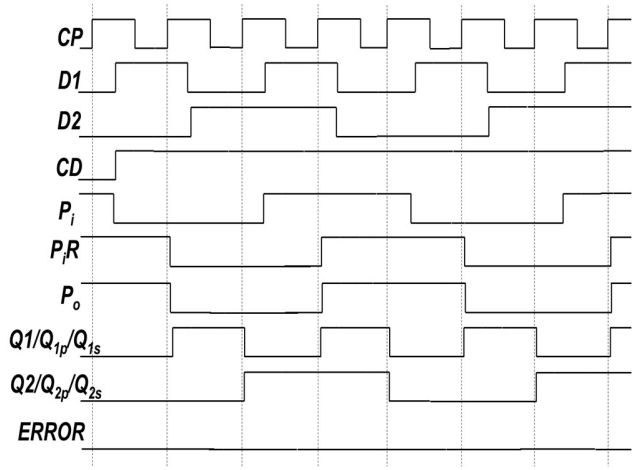

Fig. 4. 2-Bit Even Parity Flip-Flop System Signal Waveforms in normal operation mode.

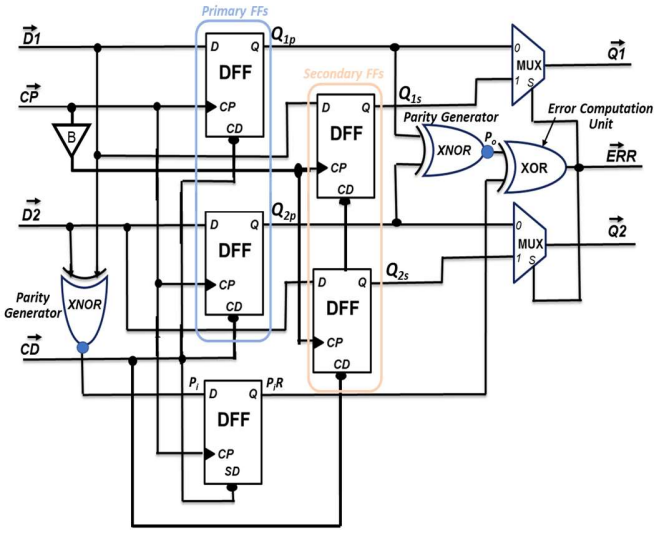

Fig. 5. 2-Bit Odd Parity Proposed FF System Circuit Diagram with common reset and skewed clock

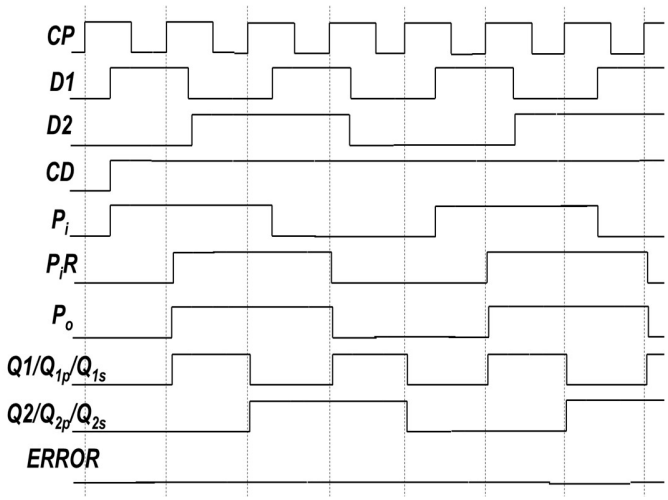

Fig. 6. 2-Bit Odd Parity FF System Signal Waveforms in normal operation mode.

To explain the system's working under various scenarios, we have taken an example of a 2-bit flip-flop system as a reference. Two implementations based on even and odd parity are shown in Fig. 3 and Fig. 5, respectively. Fig. 4 and Fig. 6 show the waveforms of various signals under regular operation for the two variants. The parity generators used are XOR (for the first implementation) and XNOR (for the second implementation) gates. The clock going to secondary FFs is skewed with respect to the primary clock. The window of timing error detection is based on XOR and XNOR gate delay, respectively; no additional delay has been added. To understand the system's working, we need to consider different scenarios that could arise during the FF operation. These are classified as the normal operation mode, radiation strike resulting in SEU in one of the FFs, radiation strike resulting in SET in different parts of the system, timing error detection, and multiple event upsets. Each of the scenarios is explained in detail below.

A. *Normal Operating Mode:* as shown in Fig. 4 and Fig. 6, the primary and secondary FFs samples D1 and D2 at clock edge. Parity generation based on D1 and D2 (P_i) occurs before the clock edge and stores in parity FF (P_{iR}). The same is computed based on the output of primary FFs (Po) and is compared with the stored parity bit (P_{iR}). Under regular operation, they are same, and the error signal is low. With the error signal low, the output of primary FFs is passed to Q1 and Q2 outputs. This is regular working model assuming no-fault condition arises.

B. *Radiation Strike Causing SEU:* in case of a radiation event, the data stored on one of the FFs could get disturbed. Here, only a single bit upset is considered, as, during physical implementation, we are making sure that all the FFs belonging to one group are placed at a safe distance from one another so that multi-bit upset (MBU) conditions can be avoided as explained demonstrated in [12]. More details on placement constraints are given in section III. Below we consider the SEU event on different FFs present in the circuit.

B1. *Radiation Strike upsets one of the primary FFs*: on upset in one of the primary DFFs, their output changes, resulting in change of output parity signal P_o and the input parity bit P_{iR} stored in register remains unchanged. Thereby resulting in the assertion of the error signal. With error signal high, the secondary FF output that hold correct data are passed to Q1 and Q2 through MUX. Thus, SEU fault gets filtered out and final outputs Q1 and Q2 remain correct even if output of one of the primary DFFs is altered. An example of such scenario is shown in Fig. 7 in error conditions 1 and 2.

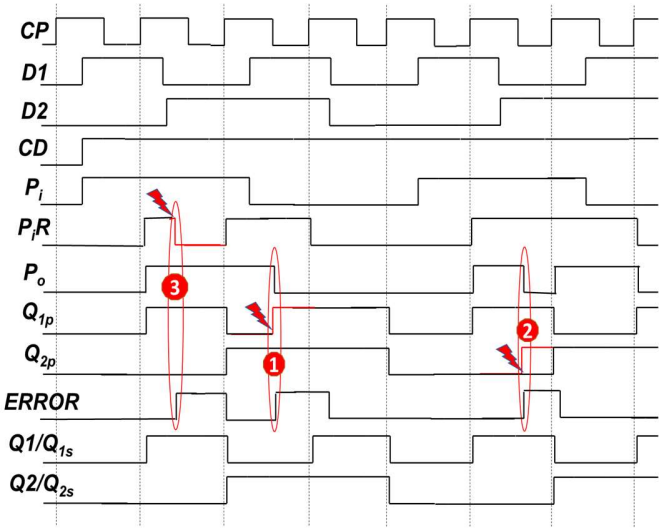

Fig. 7. 2-Bit Even Parity FF System Signal Waveforms showing radiation strike events resulting in SEU faults in different FFs. Condition 1 illustrates the SEU in primary DFF Q_{1p}, condition 2 shows SEU in primary DFF Q_{2p} and condition 3 shows SEU on parity storing DFF.

B2. *Radiation Strike upsets one of the secondary FFs (i.e., SSE)*: as shown in Fig. 8, on upset in one of the secondary FFs there is no impact on parity generation and comparison logic. Hence, no error signal is generated, and the primary FF output continue to pass through MUX to Q1 and Q2.

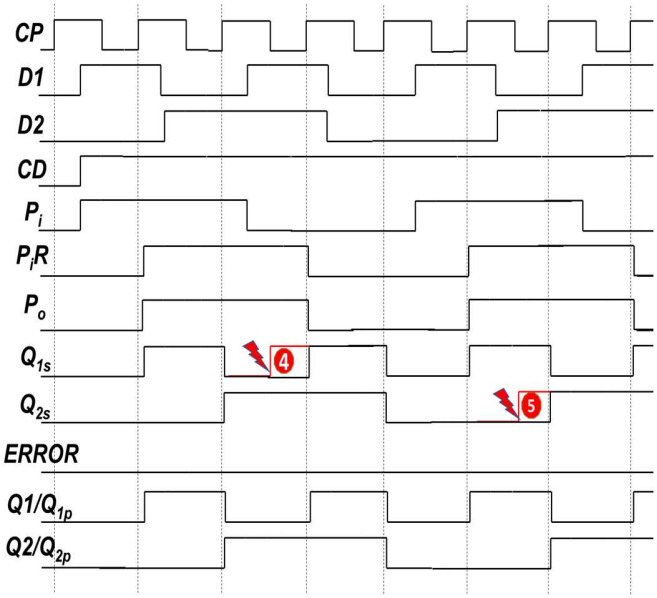

Fig. 8. 2-Bit Even Parity FF System Signal Waveforms showing radiation strike events resulting in SEU faults in Secondary FFs. Condition 4 illustrates the SEU in secondary DFF Q_{1s} and condition 5 shows SEU in secondary DFF Q_{2s}.

B3. *Radiation Strike upsets the parity storing FF*: as shown in Fig.7 (error condition 3) an upset in parity storing DFF results in change of P_{iR}, and P_o retains its previous value. This will result in error signal assertion, but both primary FF and SSE have corrected data stored in them, so Q1 and Q2 do not change.

C. *Radiation Strike Causing SET:* A transient pulse SET could occur on any combinational path if radiation strikes on combinational logic cells. This may or may not result in change of state of FF. However, since the probability is not zero, as illustrated in [2], the system must take care of SET events as well. We consider different paths below where SET can occur and how the impact can be mitigated.

C1. *SET event on Data Inputs*: one of the paths, D1 or D2, could get a glitch arising due to radiation strike close to the rising edge of FF, resulting in incorrect data being latched. Multiple sampling points in the proposed circuit effectively detects the error introduced due to SET. Different scenarios showing SET on the D1 path captured by different FFs are shown in Fig. 9. The same is true for D2 input as well. In cases when SET is not captured in FFs, there will be no impact on the system. In error condition 6, when parity FF gets corrupted due to a glitch, the error signal goes high, but there is no impact on final outputs Q1 and Q2. In case of error condition 7, when primary FF gets corrupted and Q_{1p} changes its state resulting in a change of P_o and subsequently assertion of the error signal, the outputs Q1 and Q2 comes through Q_{1s} and Q_{2s}, which store good values because they are sampling data on skewed clock CP_{Skew}. If SSE (Q_{1s}) gets corrupted (error condition 8), there is no effect on the rest of the circuit, and the output holds a good value.

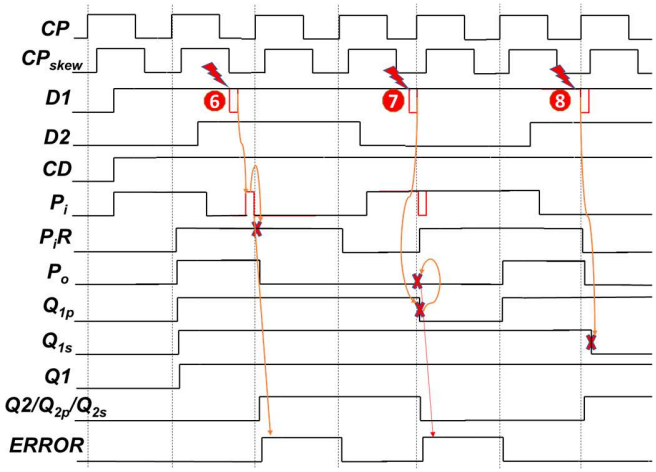

Fig. 9. 2-Bit Even Parity FF System Signal Waveforms showing radiation strike event resulting in SET faults in Data Path D1 at various time intervals. Condition 6 illustrates the SET captured by parity storing DFF, condition 7 illustrates SET captured by Primary DFF Q_{1p} and condition 8 shows SET event captured by secondary DFF Q_{1s}.

C2. *SET event on Clock paths*: Clock paths are susceptible to SET as the data paths. However, due to the construction of balanced tree networks to minimize skew, the capacitance on nodes is relatively higher, which requires higher energy particles to cause meaningful transient on clock path resulting in failures. Experimental results reported in [25, 26] on 28nm and 90nm technology nodes respectively show that burst errors due to SET in clock tree start to occur for particles with LET > 10 $MeVmg^{-1}cm^2$. The SET on the clock path could result in either clock jitter or radiation induced clock race. The probability of radiation-induced clock jitter resulting in setup violation in flip-flop, is very low, and the same can be detected and corrected with the timing pre-error detection mechanism of the proposed solution. On the other hand, radiation-induced clock race could cause an error in the given system. Robust clock tree solution such as mesh type [25], hardened clock spine [27], etc., can be adopted to mitigate these types of errors. These methods are proven to be effective for higher LETs (> 10 $MeVmg^{-1}cm^2$). In order to make the system more robust specially for low capacitance clock nodes, it is best to deploy SET mitigation at leaf cell level i.e., the clock input of FF. In the proposed system, the clock inputs to primary FFs can be connected to clock network through delay filters based on guard gates [28] (Fig. 10). These can filter out unwanted transient pulses on clock lines. The SSE does not require such filters.

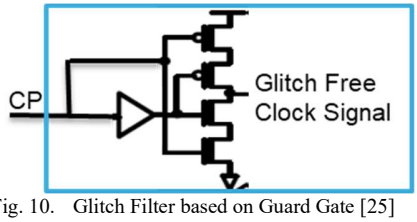

Fig. 10. Glitch Filter based on Guard Gate [25]

C3. *SET event on RESET path*: - Single Event Transient on Reset path could result in localized resetting of flip-flops as reset buffer tree could have low capacitance points having less critical charge. To avoid this, separate reset paths can be used inside multi-bit system, as shown in fig. 11. In the case of even parity, the DFF storing parity should give "1" on reset (i.e., of SET type) and in the case of odd parity it should give "0". This is required to generate error condition, when SET event occurs on CD1 (as shown in Fig. 12), which eventually makes Q1-Q2 controlled by SSE. This requirement of specific polarity on reset also results in false error signal assertion in the actual reset condition. Normally, this false error assertion is automatically ignored by the system as the whole digital system will be under reset, but for some specific cases, system designer needs to take care of this. In the case of an event on CD2, there is no impact as Q1 and Q2 are driven by primary FFs, which are unaffected. CD1 and CD2 are controlled with same reset signal at the top but the buffer tree is different. Another way of managing this is to place glitch filtering at the input of each flip-flop reset but the penalty of that could be huge in terms of area and power.

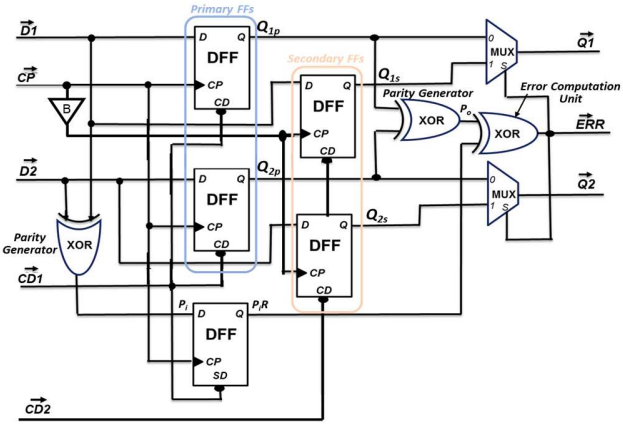

Fig. 11. 2-Bit Even Parity Proposed FF System Circuit Diagram with sperate reset and skewed clock.

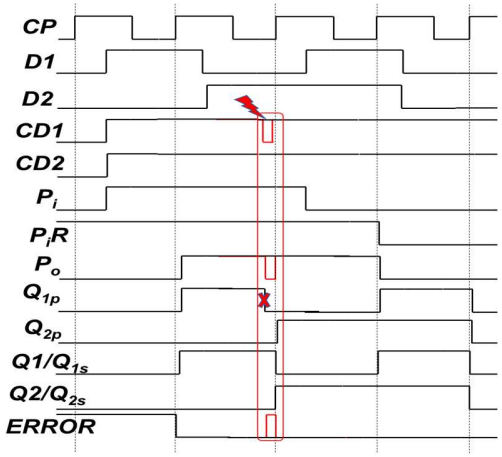

Fig. 12. 2-Bit Even Parity FF System Signal Waveforms showing radiation strike events resulting in SET on reset path CD1

C4. *SET event on added circuitry*: The added logic of parity computation, error detection, and correction is also prone to SET faults. Any SET event in the input party generation circuit would result in a glitch on Pi input which can be

latched and result in corruption of PiR. However this will be masked as explained in section B3, and will not affect the final output. SET on output parity computation and the error generation circuit would result in a glitch on the ERROR signal which again will not affect the final outputs and can be registered as error event by the system. Any SET event on output mux driving final output would result in a glitch on outputs which could eventually propagate to data inputs of subsequent stage FFs. They are treated like SET on data inputs for subsequent stage flip-flops and will be filtered by the mechanism already explained in section C1.

D. *Timing Pre-error Sensing Mode:* the parity generation and comparison logic also enable the timing pre-error sensing capability. The transitions on data inputs occurring very close to the clock edge can be detected. This concept is very well illustrated in [21]. The input parity bit computed from D1 and D2 gets delayed by XOR gate intrinsic delay and stored in parity FF, whereas the parity bit calculated from outputs of primary FF will be based upon the data sampled in primary FFs without any delay on the same clock edge. When D1 and D2 change very close to the clock rising edge, the two parity bits will be different, resulting in the assertion of the ERROR signal, as shown in Fig. 13. The ERROR signal arising due to timing is different in terms of periodicity with respect to error from radiation events. It is more systematic i.e., it will be asserted more frequently. The digital system can work in a closed-loop based on this feedback from the FFs as demonstrated in [24]. It can take corrective actions like scaling supply voltage, reducing clock frequency, etc., to reach the OPP. Here, the primary outputs Q1 and Q2 are not affected and store correct value, therefore no impact on system functionality. One limitation of this logic is that in a particular case, wherein D1 and D2 both change simultaneously, resulting in same parity computation, the timing sensing won't be able to detect the data alteration. Nevertheless, as timing faults are systematic faults, the error could get captured in subsequent clock cycles when parity change occurs. In order to tune the window of timing error detection, the delay on the input parity generation path can further be tuned by including a programmable delay in the path or a fixed delay in the path as per system and process requirements.

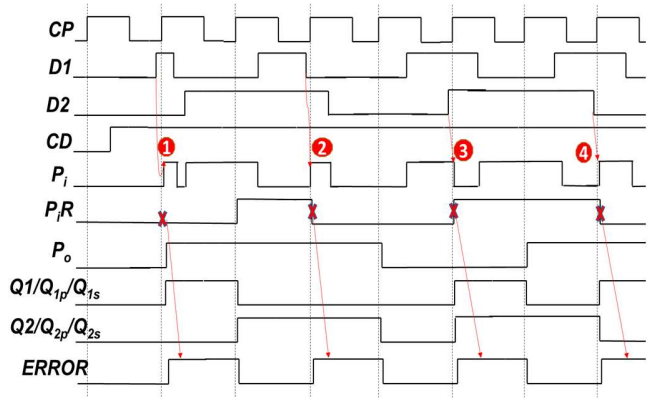

Fig. 13. 2-Bit Even Parity FF System Signal Waveforms showing timing pre-error sensing capability. Condition 1 and 2 illustrate the transitions on D1 input close to clock edge. Condition 3 and 4 illustrate the transition on D2 input close to clock edge.

E. *Multiple Event Upsets:* Apart from various scenarios discussed above, there is one particular scenario of multiple events wherein multiple strikes could result in the accumulation of bitflips in flip-flops. This condition would arise if the digital system is in power saving mode by applying clock gating, and no refresh cycle is provided to correct the data stored in primary and secondary FFs. The proposed system does not automatically correct the data stored in FFs. It only detects and masks the bit upsets introduced due to radiation event. Typically, such bit upsets are automatically corrected through subsequent clock pulses or dedicated refresh cycles, or dedicated self-correcting designs are needed, like self-correcting delta-TMR [15]. The detection capability of the proposed system allows the system designer to use the ERROR signal to detect radiation strike event and provide refresh cycles to the system so that accumulation of errors can be avoided and good functionality of the system can be maintained. However, an actual error condition might still happen if the ERROR signal is not asserted on the first radiation strike and the subsequent strike happens on the same flip-flop group, but the probability of such occurrence is very low.

We have explained the different working modes of the proposed system under various scenarios and demonstrated the single event error detection and mitigation capabilities of the system. Now, in the next section, we will look into the implementation of proposed FF and placement constraints which helps in avoidance multi-bit upsets due to multi-node upsets and charge sharing. Its application in digital systems and the impact on power, performance, and area. Its relative performance with respect to existing standard solutions.

III. Design, Implementation and Comparative Analysis

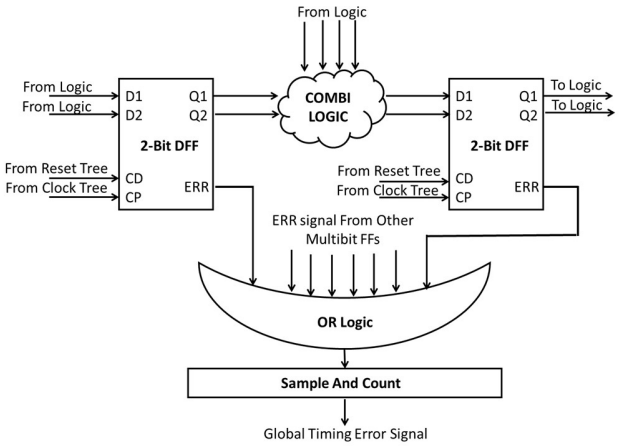

Fig. 14. Digital System based on Proposed 2-bit FF.

As mentioned earlier, the proposed circuit can be designed with standard library cells. It does not require the designing of specific rad-hard cells. With certain design constraints, any digital system can be implemented with standard semi-custom design flow using proposed FFs. In a generic digital design, the sequential elements can be replaced with proposed FF with grouping of FFs belonging to similar power and clock domains. An example of a typical digital system path with the proposed 2-bit implementation is shown in Fig. 14. The ERROR signals coming from different groups are combined with OR logic, then

passed to a sample and count circuit to generate the error signal. For timing error, count should be more than two in reasonable time window, whereas for other cases where the count is less than two, they can be treated as radiation error.

A. *Timing Constraints with Proposed Design:* Additional logic required for the proposed circuit does impose a timing penalty on the digital system along with particular constraints for the proper functioning of the system. The overall impact on performance and timing constraints required for the proposed methodology can be well understood by the below equations. For a standard digital system design, basic timing constraints are given by: -

$$T_{CKPeriod} > T_{pdFF} + T_{comb} + T_{setupFF} + T_{margin} - T_{skew} \quad (1)$$

$$T_{comb} + T_{skew} > T_{holdFF} \quad (2)$$

Where $T_{CKPeriod}$ is Clock Period, T_{pdFF} is CP-Q delay of STD launch FF, $T_{setupFF}$ is setup time of STD capture FF, T_{comb} is combinational delay between launch and capture FF, T_{skew} is clock skew between launch and capture FF clock, T_{holdFF} is hold time STD FF and T_{margin} is extra time margin taken to account for PVT variations, voltage drops, jitter, aging etc. as shown in Fig. 1. Maximum frequency of digital design is limited by equation 1 where T_{margin} has significant weight. In the proposed multibit system, timing margin can be squeezed with help of timing pre-error detection. The timing constraint equation for maximum frequency is given by equation 3 and for hold time equation 4.

$$T_{CKPeriod} > T_{pdFF} + T_{comb} + T_{setupFF} + T_{mux} + T_{PGdelay} + T_{error} - T_{skew} \quad (3)$$

$$T_{comb} + T_{skew} + T_{cpskew} > T_{holdFF} \quad (4)$$

$$T_{margin} > T_{mux} + T_{PGdelay} + T_{error} \quad (5)$$

$$T_{cpskew} < T_{pdFF} + T_{error} \quad (6)$$

Here, T_{cpskew} is introduced clock skew between primary and secondary FFs, T_{mux} is the delay of output mux of launch FF, $T_{PGdelay}$ is the delay of input parity generator of capture FF, T_{error} is the propagation delay of ERROR signal from output of primary launch FFs. For the system to be effective and efficient with no impact on the target frequency of original design, time margins taken during implementation should compensate for the increase in delay components as shown in equation 5. Usually, margins taken for the desired operating point are sufficient to offer optimization, even after compensating the additional delays [18-24]. This has been demonstrated in the subsequent sections with experimental data. The input and output parity generator delay becomes the timing margin window for detecting timing pre-errors and limiting factor to the number of bits that can be grouped. As for higher bit groups, the parity generator delay would be more.

As explained in section II-C-2, the width of SET that can be filtered on D inputs of FF is driven by clock skew introduced between primary and secondary FF. To filter wider pulses, more clock skew needs to be introduced. An increase in clock skew, firstly, impacts the hold timing constraints as per relation given in equation 4; secondly, it is also limited by internal cell delays as equation 6. Using this relation and knowing the desired pulse widths to be filtered, appropriate skew values can be introduced.

B. *Digital Design Flow with Proposed Design:* A standard digital implementation flow diagram is shown in Fig. 15, along with additional steps required to insert multi-bit FFs. The grouping of FFs is done after compiled netlist is available during synthesis flow. The grouping is done for FFs with common clock and power domain and at the same hierarchy level. After grouping, FFs are replaced with equivalent multi-bit FFs. Thereafter, a new netlist is generated along with additional timing constraints, without any change in cell list and placement constraints. The generated netlist is verified with respect to original netlist with a formal equivalence checking tool by setting appropriate black-box definitions and constraints on added logic. After checks with this new netlist and constraints, DFT insertion continues, and synthesis is completed. The gate-level netlist and constraints are passed to the backend implementation tool for the next steps.

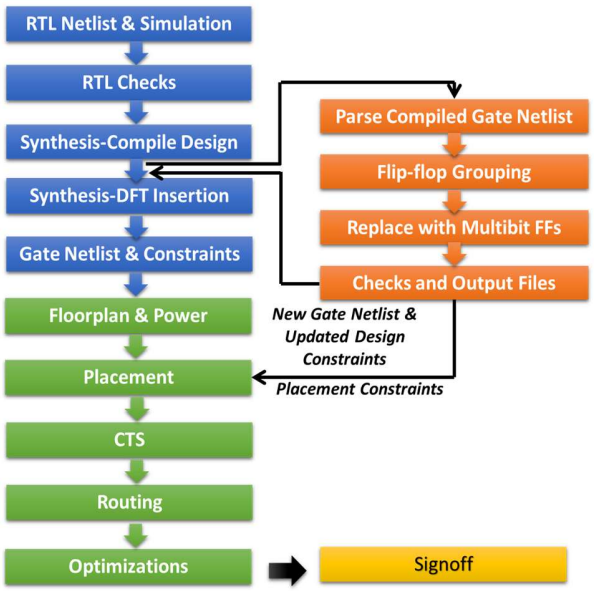

Fig. 15. Digital Implementation flow diagram.

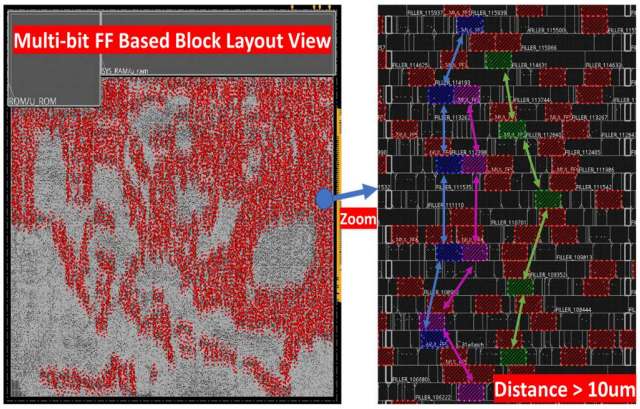

Fig. 16. Multi-bit FF based ARM blocks layout view showing placed cells. Instances in red colour are showing 2-bit grouped flip-flops. In the zoomed view, instances of three different 2-bit groups are shown as example in blue, magenta and green colour. With the help of placement constraint, a minimum distance of 10um is maintained within the cells belonging to same group.

The following backend implementation flow in green in fig. 15 is a standard one with just one additional placement

constraint during the placement step wherein spacing between cells belonging to one FF group is forced during the cell placement step to avoid multi-bit/multi-node upsets on cells of same group. *This is shown in fig.16 where cells of* the *same group are placed at least 10um apart from each other*, *avoiding* MBU within the *same group. This space is filled with other* design *cells*, *not causing any area penalty.* However, for higher bit groupings, the congestion issues do appear. Finally, signoff checks are performed on design after clock tree build-up, routing, and timing optimizations.

C. *Comparative Study:* The proposed system is implemented in 90 nm ST BCD technology based on a High Vt standard cell library. We performed a comparative analysis on standalone FFs and microcontroller (MCU) implementation trials based on different FFs.

C1. Standalone Flip-flop implementation and comparison: For comparative study, we have taken standard dual clock phase master-slave D FF (STD FF) shown in fig. 17 (a) as reference. Based on the same STD FF, 2-bit, 4-bit, and 8-bit even parity versions of the proposed system are implemented along with TMR and delta-TMR [15]. Simulations were caried out on all FFs to characterize various parameters of FFs under default working mode with no error condition. Table 1 summarizes the main characteristics of the architectures mentioned above.

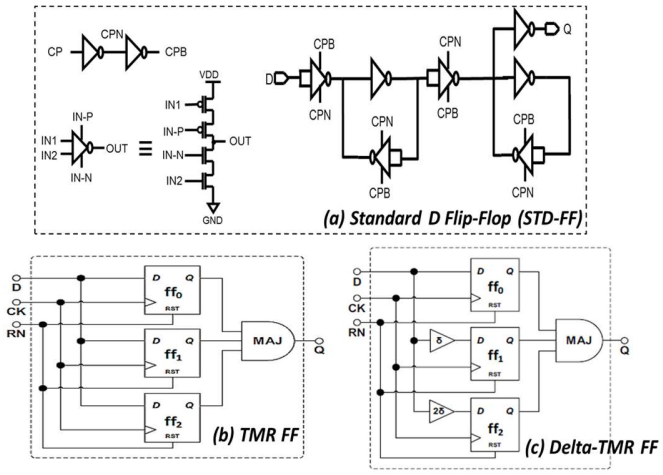

Fig. 17. Flip-flops under comparison (a) Standard D Flip-flop Circuit (STD FF), (b) TMR FF (c) Delta-TMR flip-flop

Effective per bit data of proposed FF on standalone basis shows 2x impact on CP-Q delay, ~3.5x increase in area, ~5x on switching power, and ~1.5x impact on setup time with respect to STD FF. These results are in line with other standard robust solutions TMR and delta-TMR. In delta-TMR FF, where temporal hardening is used by adding clock skew, the impact on timing is very high as it requires at least two flip-flops sampled to be resolved so that the majority voter could converge to valid output. In the proposed system, the setup time and propagation delay are independent of delay in input party logic and clock skew, as in default case of no error condition, the final outputs are governed by primary FFs passing through output mux. It is also observed that with higher bit groupings in the proposed methodology, the area and power show improvement and performance remain the same. Therefore, it is recommended to go for higher bit grouping configuration of the proposed system for the digital system design but upper limit is restricted by constraints mentioned earlier in section III-A and III-B.

Table 1. Standalone Simulation results for different FF variants at typical process, 1.0 V and 25°C. Data is normalized to STD FF data.

	STD FF	TMR FF	Delta-TMR FF	2-Bit FF*	4-Bit FF*	8-Bit FF*
CLK Cap	1	3.01	3.03	1.97	1.63	1.48
CP-Q Delay	1	1.86	1.88	2.04	2.02	2.03
Setup	1	1	7.05	1.46	1.46	1.46
Area	1	3.9	4.5	3.85	3.51	3.18
Switching Power 25% Data Activity	1	4.23	5.52	4.99	5.02	3.74
Min Captured Pulse Width on D inp	87.5 ps	87.5 ps	285.5 ps	142.5 ps	150 ps	165.5 ps
SET Tolerance	No	No	Yes	Yes	Yes	Yes
SEU Tolerance	No	Yes	Yes	Yes	Yes	Yes
Timing Pre-error Detection	No	No	No	Yes	Yes	Yes

* Data reported is scaled to single bit for one-to-one comparison with other FFs

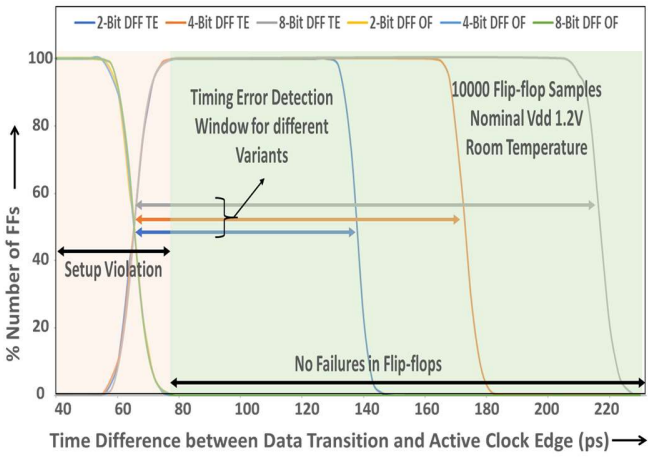

Fig. 18. Graph showing Number of FFs Failing with change in time difference between data and clock. Data obtained from Monte Carlo simulations at nominal operating conditions. TE suffix denotes number of FFs showing timing pre-error and OF denotes actual operation failures in FFs.

We also computed minimum SET pulse which different FFs can capture. The TMR and STD DFF can capture pulse widths more than 87 ps, delta-TMR can filter up to 285 ps, and the proposed DFF with single buffer clock skew can filter up to 142 ps, 150 ps, and 165 ps respectively for 2-, 4- and 8-bit implementation respectively. The same can be enhanced by increasing clock skew respecting timing constraints given in equations 4 and 6. The timing window for pre-error detection is shown in Fig. 18 for different implementation configurations. As discussed earlier, the input parity logic delay governs the window size, and it can be enhanced by adding additional delay in the path. It also impacts the optimization efficiency of the system as more margins would translate into a less efficient

system. The 8-bit FF has largest window size as input parity logic has more delay with respect to 4-bit and 2-bit configurations.

C2. *Digital system implementation and comparison*: A Digital MCU (shown in Fig. 19) based on ARM cortex M4, memory, and basic peripherals like GPIO, registers bank, counter, etc., is implemented with the proposed system to study its implications in an application. The design is approximately 200K gates having 4.82k FFs based on standard D ones. We replaced all the FFs in the design with the proposed robust FF system as per the design flow mentioned in section III-B. Only 2-, 4-, and 8-bit configuration are chosen as for higher 16-bit configuration trade-off is very poor. We also implemented TMR FF based MCU to benchmark against a standard radiation hardening methodology. Similar placement constraints are followed for TMR implementation as well.

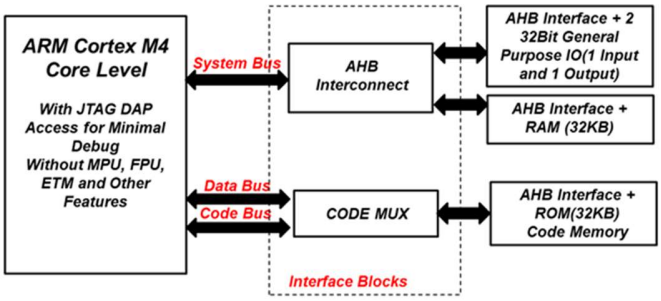

Fig. 19 Microcontroller (MCU) architecture implemented.

Table 2. Place & Route data from MCU implementation done with different FF variants. Data is normalized to STD. FF data.

Flip-flop Variant used	STD FF	TMR FF	2-Bit FF	4-Bit FF	8-Bit FF
Core Area (with Macros)	1	1.39	1.36	1.33	1.31
Core Area (without Macros)	1	1.78	1.71	1.64	1.60
Num. of FF	1	3.00	2.51	2.29	2.19
Leakage Power	1	1.43	1.49	1.43	1.37
Vector less Dynamic Power	1	1.84	1.91	2.11	2.16

Table 2 shows the results obtained with implementation trials using the Cadence Innovus tool at 18 ns clock period and signoff corner wc_1.00V_125C. The timing margin for robust MCUs is reduced by 300ps for implementation trials, to account for additional logic delay. We tried to minimize the area for the given target frequency till no timing and design rule checks (DRC) violations were observed. The results are in line with the hardening benchmark of TMR FF. With the higher grouping of FFs, the area, leakage power, and number of FFs added reduces, whereas vector less dynamic power reported by tool increases due to more switching in redundant logic. Fig. 20 shows the percentage share of different bit groupings formed in different implementations of the proposed multi-bit system. It shows that in the given design more than 95% of the flip-flops can be grouped in either 2-, 4- or 8-bit groups. Fig. 21 shows the number of paths and timing slack for different implementations. It shows that at worst corner wc_1.00V_125C, approximately 15% of the paths have slack < 500ps, and the rest have more than 500ps margin. Also, the worst critical path delay scenario may or may not occur during the device lifetime. Therefore, there is a sufficient margin for the typical operating range, which can be optimized with the help of timing pre-error detection, and OPP can be found.

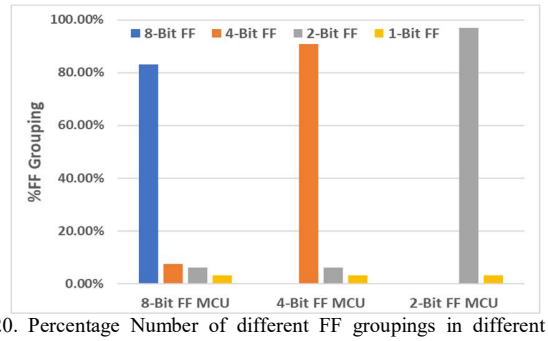

Fig. 20. Percentage Number of different FF groupings in different MCU implementation

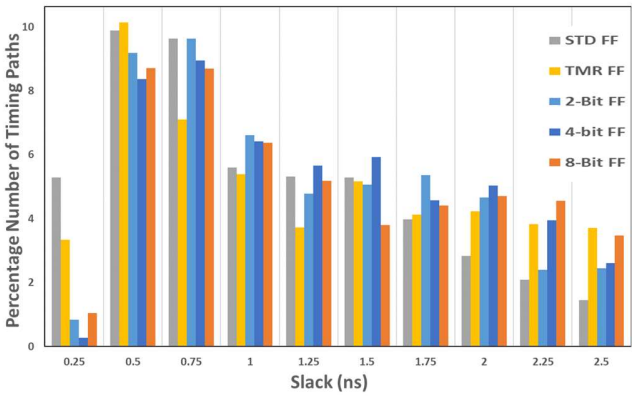

Fig. 21. Timing Graph showing timing slack vs number of paths at worst corner for different FF implementations.

IV. Test-Chip Implementation and Test Results

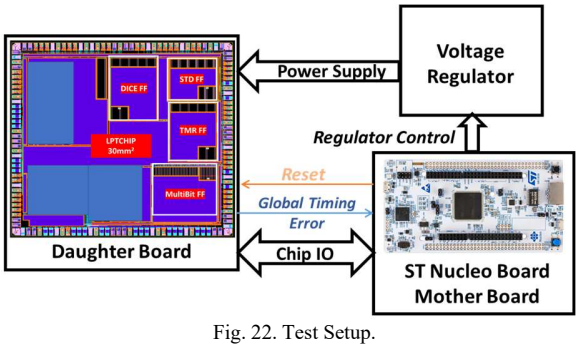

Fig. 22. Test Setup.

The LPTCHIP (30 mm^2) implemented in ST BCD 90 nm technology is based on multiple implementations of the same MCU, but with different FF variants, i.e., STD FF, DICE based FF [8], TMR FF [12,15], and the proposed multi-Bit FF system based on up to 2-bits of grouping with single buffer clock skew and common reset as shown in Fig. 3. In the MCU reported in

previous section in Fig. 19, the RAM used for storage is protected with single error correction and double error detection error-correcting codes (SECDED). If a single bit error condition is detected in memory, the peripheral logic automatically corrects and stores the correct data to avoid error accumulation in memory. The code stored in ROM is a mix of bubble sort, matrix multiplication, floating-point addition, and FIR filter. A failure is reported in case of wrong computation outcomes, or the MCU itself stops responding. The failures reported are mainly due to SET and SEU occurring in the digital logic of the CPU. For Multi-bit FF based implementation, error signal coming from MCU is observable through primary output of the chip and a closed-loop test system is implemented externally based on this signal, as shown in Fig. 22. The daughterboard, which hosts the Device Under Test (DUT) is controlled and observed with a motherboard containing ST Nucleo board with STM32 microcontroller. The power supply to the DUT can be controlled with an external voltage regulator, which provides precise voltage steps of 1 mV. This enables the automatic voltage regulation scheme based on timing error signal coming from DUT.

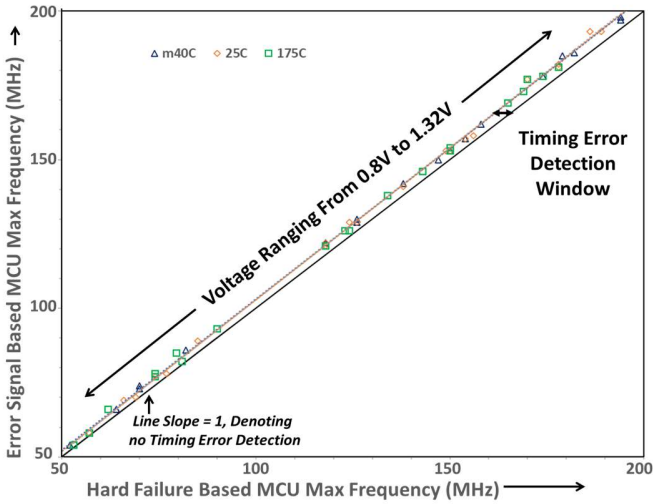

Fig. 23. Max Frequency Data of Multi-bit DFF based MCU.

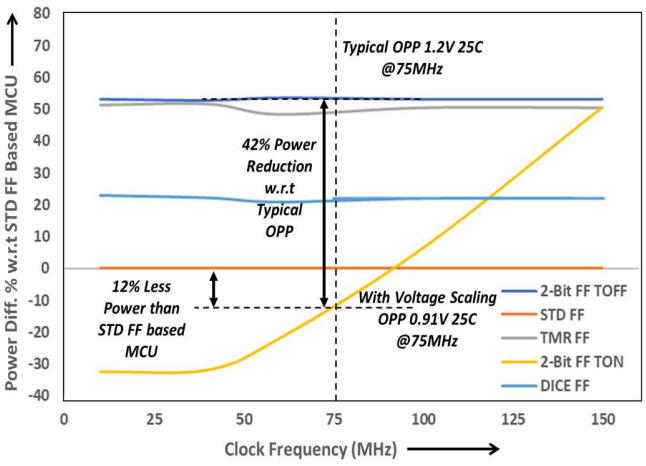

Fig. 24. Power Consumption at 1.2V room temperature for different MCUs at different clock frequencies.

Multiple packaged samples of the above-described test-chip have been characterized electrically and under radiation. CPGA144 package with no covering on top is used to avoid any effect of package material during radiation tests. We measured the maximum frequency of multi-bit MCU operation at various voltage and temperature points based on actual hard faults where the device gives incorrect responses and based on timing error signal. The data is plotted for multiple samples and shown in Fig. 23. It is observed that the error signal coming from the timing sensor always flags error before actual failures in design. The timing error margin window at the system level can also be computed with the help of the graph. In a typical corner (1.2 V and 25°C), it comes out to be around 350 ps. In Fig. 24 percentage differences of dynamic power with respect to reference FF are plotted at room temperature and 1.2 V operating voltage for various frequencies. It is noted that robust FF increases the consumption by 20% for dice DFF and by 50% for both TMR and the proposed FF. With automatic voltage regulation application in multi-bit MCU, power consumption can be brought down to 12% gain with respect to standard DFF MCU. The multi-bit MCU can operate at 0.91 V for a frequency target of 75 MHz as we move at higher performance operating points, the gain in power reduction reduces linearly. We reach the limit of lowering supply voltage at 0.8 V wherein memory minimum supply is hit, and supply cannot be scaled down further. Therefore, power gain becomes constant at lower operating frequencies.

Radiation tests are carried out mainly with Alpha particles. A radioactive Americium-241 (^{241}Am) source capable of generating 5.486MeV alpha particles 85% of the times [31] was used at the Dept. of Information Engineering, Padova, Italy, and the chip was irradiated at room temperature for 24hrs. At the nominal voltage of 1.2V, few failures were observed in STD FF based MCU, while others based on robust structures showed no fails. At 0.9 V, some failures are observed in robust structures; the results are shown in Table 3 in the form of an effective FIT rate. The FIT rate [2] is calculated as per the below equation: -

$$FIT = Natural_{RadFlux} \times \frac{\#errors \times (10^6 \times 10^9)}{Test_{RadFlux} \times TestTime \times \#cells} \quad (7)$$

The Failure in Time (FIT) rate is the number of errors expected on 1Mega cells in 1Giga hours. The natural radiation flux used for computation is 10^{-3} for alpha particles, and test flux is 18200 particles·cm^{-2}·s^{-1}. The FIT rate of different flip-flops implemented as shift-registers is reported in our previous work [11], according to which STD FF has FIT rate of 500 at 0.9V and negligible for robust flip-flops. In case of MCUs, the effective FIT rate for STD FF comes down much lower ~30 because of logical error masking. There are almost negligible errors in robust structures at lower frequencies but at higher clock frequencies they show few errors. These can be due to SET faults captured by FFs.

Table 3. Alpha radiation test results in terms of FIT rate at 0.9 V bias.

	STD FF	DICE FF	TMR FF	Multibit FF
1MHz	28.3	0.9	0.6	1
54MHz	31.6	6	4.9	5.3

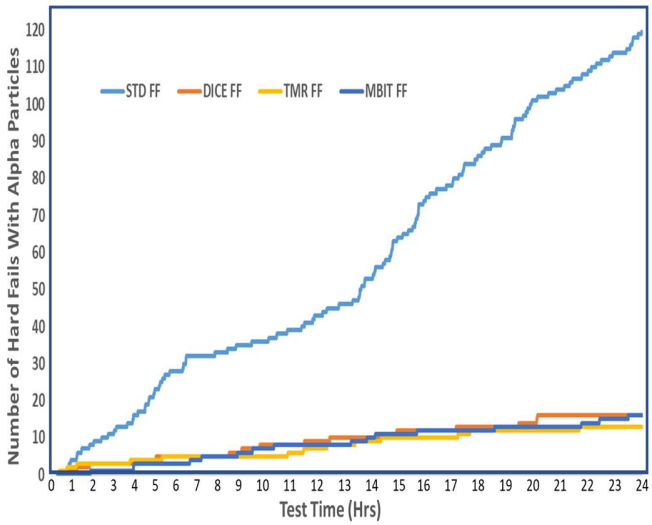

Fig. 25. Alpha particle radiation test results showing number of fails reported with test time at 0.9V room temperature.

Fig. 25 shows the number of fails reported with test time. It is noted that robust DFFs show good resilience with respect to standard DFF. But as test time progresses error accumulation in FFs and high probability of SET induced faults with time results in failures in robust solutions.

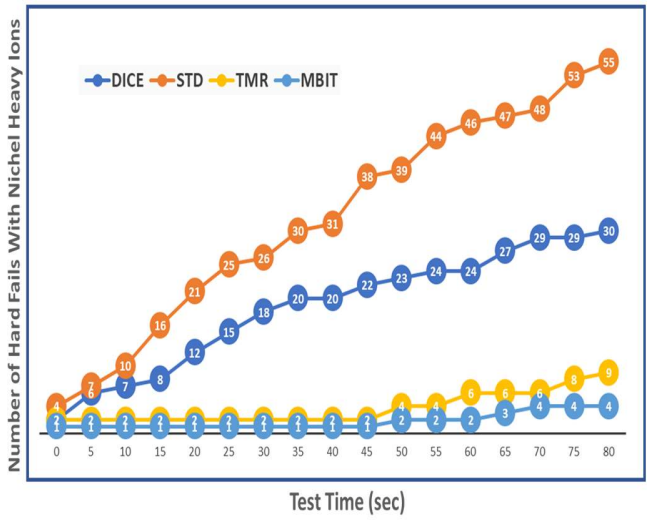

Fig. 26. Nickel Ion radiation results showing number of fails reported with test time at 0.9 V and room temperature.

Table 4. Nickel Heavy Ion Cross-Section (cm^2) at 0.9 V bias and room temperature.

STD FF	DICE FF	TMR FF	MBIT FF
1.15E-08	6.25E-09	1.87E-09	8.33E-10

Heavy ions tests are conducted at the SIRAD line of the TANDEM accelerator at the Laboratori Nazionali di Legnaro, Padova, Italy. The tests are performed with nickel heavy ion, which is a high LET particle (28.4 $MeVmg^{-1}cm^2$). It represents a worst-case for terrestrial application wherein particles are dominated by mainly alpha (LET below 1) and neutron byproducts (LET < 15 $MeVmg^{-1}cm^2$). Fig. 26 shows the number of failures observed over time on exposure to Nickel ions at room temperature and 0.9 V operating voltage. The tests were conducted for 80s only due to the limited availability of stable particle accelerator. Also, we calculated the effective bit cross-section [2] given by:

$$\sigma = \frac{\#errors}{Test_{RadFlux} \times TestTime \times \#cells} \qquad (8)$$

and measured in cm^2. Flux for nickel ions measured from test setup is 12450 particles·cm^{-2}·s^{-1}. The bit cross section indicates the sensitivity of a bit to a certain particle. The results are tabulated in table 4. The DICE and Standard FF based MCUs had many errors on exposure of few seconds due to SEU in FFs and SETs in clock, data path etc. while TMR and Multibit Based MCUs showed good resilience as SEUs are negligible. The errors reported are due to SETs in clock and data paths and error accumulation in FFs and memory.

V. Conclusion

A Multi-bit FF system has been presented, which can be adopted in any digital system with standard library cells and standard digital design flow. The functionality and design constraints required for the proposed system have been explained in detail. Through architectural explanations and experimental data, it has been shown that the proposed flip-flop has high tolerance against both SEU and SET. Further, the effectiveness of timing pre-error sensing has been demonstrated, which helps in efficient voltage and frequency regulation. Area overhead due to redundant logic is similar to standard robust solution TMR, delta-TMR, etc. Overall, the proposed system offers both radiation robustness and adaptability, a combination of which is missing in conventional robust architectures. Application developers can exploit this peculiarity to make resilient and efficient digital systems. Future work is planned to analyze implementations with higher bit configurations, and with proper circuit tuning for SET protection on silicon, and further tests need to be conducted to study aging effects, TID effects, and exposure to more radiation particles.

References

[1] Massengill et al., “Technology Scaling and Soft Error Reliability”, IEEE International Reliability Physics Symposium 2012.
[2] D. Kobayashi, “Basics of SEE Mechanisms and Predictions”, in IEEE NSREC Short Course Notebook, 2019.
[3] B. Narsimham, “Hardening Techniques for Digital Circuits” in IEEE NSREC short course Notebook, 2021.
[4] M. Nicolaidis et al., “Design for soft error mitigation,” *IEEE Trans. Device Mater. Reliab.*, vol. 5, no. 3, pp. 405–418, Sep. 2005.
[5] S. Mitra et al., "Robust system design with built-in soft-error resilience," IEEE Computer, vol. 38, no. 2, pp. 43-52, Feb. 2005.
[6] B. Narasimham et al., "A Hysteresis-Based D-Flip-Flop Design in 28 nm CMOS for Improved SER Hardness at Low Performance Overhead," IEEE Trans. Nuclear Science, vol. 59, no. 6, pp. 2847-2851, Dec. 2012.
[7] B. Narasimham et al., "Charge-Steering Latch Design in 16 nm FinFET Technology for Improved Soft Error Hardness," IEEE Trans. Nuclear Science, vol. 64, no. 1, pp. 353-358, Jan. 2017.
[8] T. Calin et al., "Upset hardened memory design for submicron CMOS technology," IEEE Trans. Nucl. Sci., vol. 43, pp. 2874-2878, Dec. 1996.
[9] Kelin et al., “LEAP: Layout Design through Error-Aware Transistor Positioning for soft-error resilient sequential cell design” IEEE International Reliability Physics Symposium IRPS 2010.

[10] Y. Q. Li et al., "A Quatro-Based 65-nm Flip-Flop Circuit for Soft-Error Resilience" IEEE Transactions on Nuclear Science, pp. 1554-1561, Volume: 64, Issue: 6, June 2017.
[11] A. Jain et al., "Single Phase Clock Based Radiation Tolerant D Flip-flop Circuit" IEEE 26th International Symposium on On-Line Testing and Robust System Design (IOLTS) 2020.
[12] Petrovic et al., "Design flow for Radhard TMR Flip-Flops", IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems, pp 204-208, 5Th December 2015.
[13] Schrape et al., "Aspects on Timing Modeling of Radiation-Hardness by Design Standard Cell-Based ΔTMR Flip-Flops" 22nd Euromicro Conference on Digital System Design (DSD), pp. 639-642, 2019
[14] D. Mavis et. al., "Soft Error Rate Mitigation Techniques for Modern Microcircuits", *Proc.* IEEE Int. Reliability Physics Symposium, pp. 216-225, 2002.
[15] O. Schrape, et. al., "Design and evaluation of radiation-hardened standard cell flip-flops". IEEE Transactions on Circuits and Systems I: Regular Papers, 68(11), pp.4796-4809. 2021.
[16] S. Alghareb et. Al., "Soft Error Effect Tolerant Temporal Self-Voting Checkers: Energy vs. Resilience Tradeoffs" IEEE Computer Society Annual Symposium on VLSI, pp: 571-576, 2016.
[17] Kumar, S., Chellappa, S. and Clark, L.T., 2015, May. Temporal pulse-clocked multi-bit flip-flop mitigating SET and SEU. In 2015 IEEE International Symposium on Circuits and Systems (ISCAS) (pp. 814-817). IEEE.
[18] D. Bull, et. al., "A Power Efficient 32-bit ARM processor using Timing-Error Detection and Correction for Transient Error Tolerance and Adaptation to PVT Variation", in IEEE J. of solid-state circuits, vol-46, No. 1, January 2011.
[19] D. Blaauw et al.," RazorII: In Situ Error Detection and Correction for PVT and SER Tolerance" IEEE J. Solid-State Circuits, Jan. 2009.
[20] Y Zhang et. Al. "iRazor: Current-Based Error Detection and Correction Scheme for PVT Variation in 40-nm ARM Cortex-R4 Processor" IEEE Journal of Solid State Circuits, vol. 53, No. 2, pp. 619-631, Feb. 2018.
[21] V. Huard et.al "Adaptive Wear out Management with in-situ aging monitors" IEEE Int. Reliability Physics Symposium 5th June 2014.
[22] T. Sato, et al., "A Simple Flip-Flop Circuit for Typical-Case Designs for DFM", 8th International Symposium on Quality Electronic Design, 2007.
[23] M. Saliva et. al, "Digital circuits reliability with in-situ monitors in 28nm fully depleted SOI", IEEE Design, Automation & Test in Europe Conference & Exhibition (DATE) 2015.
[24] A. Benhassain et al., "Timing in-situ Monitors: Implementation Strategy and Applications Results", IEEE Custom Integrated Circuits Conference (CICC) 2015.
[25] H. B. Wang et al., "Single-Event Transient Sensitivity Evaluation of Clock Networks at 28-nm CMOS Technology," in IEEE Transactions on Nuclear Science, vol. 63, no. 1, pp. 385-391, Feb. 2016.
[26] David L. Hansen et al., "Clock, Flip-Flop, and Combinatorial Logic Contributions to the SEU Cross Section in 90 nm ASIC Technology", IEEE Transactions on Nuclear Science, vol. 56, No. 6, Dec. 2009.
[27] S. Chellappa et al., "A 90-nm radiation hardened clock spine" IEEE Transactions Nuclear Science, vol. 59, pp. 1020–1026, 2012.
[28] A. Balasubramanian et al. "RHBD techniques for mitigating effects of single event hits using guard-gates", IEEE Transactions on Nuclear Science, vol. 52. no. 6, pp. 2531-2535, 2005.
[29] R. Dashet et al. "SEU hardened clock regeneration circuits". In: Proceedings of the 10th International Symposium on Quality of Electronic Design, San Jose, 2009. 806–813
[30] S. Jagannathan et. Al. "Frequency Dependence of Alpha-Particle Induced Soft Error Rates of Flip-Flops in 40-nm CMOS Technology", IEEE Transactions on Nuclear Science, pp. 2796-2802, Vol. 59, No. 6, Dec. 2012
[31] https://en.wikipedia.org/wiki/Americium-241.
[32] USPTO application no. 16867325, 10-12-2020.

Abhishek Jain (Member, IEEE) received the Bachelor of Engineering degree in Electronics and Telecommunication Engineering in 2005 from Netaji Subhas Institute of Technology, University of Delhi – India. He is pursuing industrial Ph.D. in Radiation effects on CMOS circuits at Information Engineering Department, Padova University – Italy from 2019.

He started to work with STMicroelectronics Pvt. Ltd. (ST) – India in 2005 as Design Engineer and currently, he is working as senior technical manager of Smart Power Technology R&D Group over there. He is member of technical staff at ST worldwide. His research work has been focused on on-chip monitoring circuits, low power design methodologies, adaptive and reliable circuit design for digital systems. Lately, his interests have been on ionizing radiation effects in advanced CMOS technologies and on their interplay with device aging and embedded no-volatile memory design. He has authored or co-authored about 20 articles published in various international conferences. He holds over 10 U.S. patents.

Andrea Mario Veggetti received the M.Sc. in computer science and microelectronics in 1994 from University of Milan – Italy.

He joined STMicroelectronics Central R&D in 1996 starting from digital design and CAD development. Since 2001 he has been working on Testchip development for IPs validation and Ultra Low Power design and test. Starting from 2008 he has been actively working on Soft error characterization due to Ionizing Radiation. In 2011 he started working on Flash memories dsign and validation adopting ARM microcontroller as reference for testchip architecture. He has coauthored more than 10 articles in various international conferences and is the holder several patents in radiation hardening and Ultra Low Power Design.

Dennis Crippa received the M.Sc. degree in electronics engineering in 2005 from Politecnico di Milano University, Milan, Italy.

Since 2006 he is with STMicroelectronics S.r.l. Milan - Italy in Smart Power Technology R&D group as senior design and test engineer. His current activity is the characterization of radiation effects (single events errors as well as total dose effects) on the technology platform and then implementation and analysis of design hardening techniques at system level. He is also involved in validation and characterization of non-volatile memories in smart power technologies. He has authored or co-authored about 5 articles published in various international conferences.

Antonio Benfante received the M.Sc. degree in Electronics and Photonics Engineering from University of Palermo, Italy, in 2014. In February 2018, he got a Ph.D. degree in Information and Communication Technologies from the same institution.

From October 2016 to June 2017, he was visiting student at the Institute of Nanotechnology (INT) of the Karlsruhe Institute of Technology, Germany, working on the design and fabrication of graphene-based transistors and detectors. From October 2013 to March 2014 and from January 2015 to July 2015, he was visiting scientist at the SLAC National Accelerator Laboratory, Menlo Park, CA, USA, where he was involved in the project, fabrication and characterization of X-ray detectors. He is currently with STMicroelectronics as R&D Hardware Design Senior Engineer working on the design of ARM-based test vehicles and rad-hardened solutions. He has coauthored about 20 articles between publications and conference contributions.

Dr. Benfante received “Mario Sannino Award for the best contribution in the field of electronics and electromagnetism applied to microwaves” by MECSA (Microwave Engineering Center for Space Applications) as part of his Ph.D. activities in 2017. In 2016 he received the “Selected poster Award” at the International School on Photonic integration: advanced materials, new technologies and applications by IEEE Photonics Society - Italy Chapter. In 2014, he received the “Best electronic engineering graduate for the academic year 2013-2014” award, conferred by the local section of AEIT (Associazione Italiana di Elettrotecnica, Elettronica, Automazione, Informatica e Telecomunicazioni).

Simone Gerardin (Member, IEEE) received the Laurea degree (cum laude) in Electronics Engineering in 2003, and a Ph.D. in Electronics and Telecommunications Engineering in 2007, both from the University of Padova – Italy, where he is now an Associate Professor of Electronics.

His research is focused on ionizing radiation effects in advanced CMOS technologies and on their interplay with device aging and electrostatic discharges, in the space, terrestrial and high-energy physics environments. Lately, his interests have been on innovative non-volatile memories and total dose effects at ultra-high levels.

Dr, Gerardin has authored or co-authored more than 200 peer-reviewed journal articles, book chapters, and conference presentations, of which more than ten were recognized with international awards. Simone has been an associate editor for the IEEE Transactions on Nuclear Science for seven years. He presented four tutorials at international conferences and co-edited a book about radiation effects in electronic devices. He has been the Short Course Chair and the Technical Program Chair for the Nuclear Space Radiation Effects Conference in 2018 and 2019, respectively. He is the General Chair of the 2022 Radiation and its Effects on Components and Systems (RADECS). He was member-at-large of the IEEE Radiation Effects Steering Group, and he is currently member of the RADECS Steering Group.

Marta Bagatin (Member, IEEE) received a Ph.D. in Information Science and Technology in 2010 from the University of Padova, Italy. Since March 2020, she is a Senior Assistant Professor in Electronics at the University of Padova.

Her research interests concern the experimental study and modeling of radiation effects and reliability issues on electronic devices for space, nuclear, and terrestrial applications, with a special focus on non-volatile semiconductor memories. She took part in numerous projects and collaborations with universities, space agencies, research laboratories, and companies. She spent time in several international laboratories and universities (INFN Legnaro National Laboratories, Rutherford Appleton Laboratories, ESA-ESTEC, Université Catholique de Louvain, the Svedberg Laboratory, the Paul Scherrer Institute, and GSI), where she used a large number of facilities for the irradiation of electronic components.

Dr. Begatin has regularly attended the IEEE NPSS Nuclear Space Radiation Effects Conference (NSREC) and the RADiation Effects on Components and Systems (RADECS) conference. She participated to several other IEEE-sponsored conferences on reliability and radiation effects, also as part of the technical (NSREC, RADECS, IRPS) or management committee (IRPS), serving as session chair, tutorial chair, and poster chair. She will be the RADECS 2022 technical program chair. MB is a regular reviewer for international journals, in particular for the IEEE Transactions on Nuclear Science. She is the author or co-author of 4 book chapters, more than 70 papers published in peer-reviewed journals, more than 80 presentations at international conferences (4 of them invited), and editor of one book. The results of her work were recognized with 10 awards at NSREC and RADECS conferences.