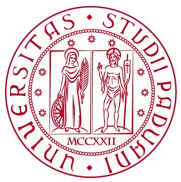

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Design and Development of a Digital Radio Frequency Control System for Linear Accelerators

Tesi redatta con il contributo finanziario dell' INFN – Laboratori Nazionali di Legnaro

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UNIVERSITY OF PADOVA

DOCTORAL THESIS

Design and development of a digital Radio Frequency control system for linear accelerators

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"... but you must wager. It is not optional."

Blaise Pascal

Abstract

The new control system for Radio Frequency (RF) structures at Legnaro National Laboratories (LNL) is presented in this document. LNL is one of the four national laboratories of the National Institute for Nucler Physics (INFN) and it is devoted to basic research in nuclear physics and nuclear-astrophysics, together with applications of nuclear technologies. The subject of this Ph.D. thesis is indeed the development of a fully digital RF feedback system, focusing on the validation of the RF controller, its programming and its integration in the particle accelerator control system. The RF controller interacts directly with the cavities and it works in a real-time closed loop. It is a set of analog and digital electronics which provides phase, amplitude and frequency corrections to stabilize the RF field in presence of disturbances and vibrations due to other subsystems of the accelerator. The control algorithm is implemented via a programmable device as an FPGA. This increases dramatically the flexibility and the programmability of the controller. The digital board of the RF controller can work in a wide range of the RF spectrum. It is a versatile tool, easy to adapt to 40/80/160/352 MHz resonators, thus spanning all types of cavities of the final SPES configuration. At LNL, it may be used to control RF cavities like bunchers to pulse the beam, superconducting cavities to accelerate the beam and RF quadrupoles (RFQ) to both accelerate and focus the beam. Most of them work in superconducting condition, while the other ones in normal condition. The controlling and the monitoring of the RF controller is done by the particle accelerator control system based on EPICS (Experimental Physics and Industrial Control System). It is a widely adopted software framework for control systems. EPICS is a set of tools, libraries and applications developed collaboratively and used worldwide to create distributed soft real-time control systems for scientific instruments such as particle accelerators.

Beam transport was carried out with the 8 cavities working in superconducting mode with the new instruments. The controller kept locked the cavities for few days. In this time the controller has proven to be more stable and reliable than the precedent system.

The first chapter of the document introduces the SPES and ALPI facility and the RF subsystem to a certain level of details: RF acceleration concepts and Low Level RF (LLRF) control for an optimum energy gain of the particle beam. In order to better understand the issues faced during the design of the control system it is useful to derive mathematical models of the RF cavities. This is the subject of the second chapter. In the third chapter the disturbance sources of the accelerating field are listed, besides clarifying the stability requirements, the frequency tuning of the cavities and their driving modes. Furthermore, the choice of the frequency sampling is outlined. The fourth chapter introduces the controller in detail. The boards functionalities are highlighted, the fundamental elements of the boards are described as well as the communication between components and boards. The fifth, sixth and seventh chapters describe the main contribution of this Ph.D. thesis. The firmware development for the Field Programmable Field Array, that is the heart of the RF controller, is covered in chapter five, emphasizing the module for the communication with the accelerator control system and the module that implements the control algorithms. The sixth chapter gives an overview of the EPICS framework, focusing on the driver support, the integration of the RF controller with the EPICS based control system is further expanded while in the last section the RF cavity tuning is explained. The seventh chapter is split in two sections. The first section lists the tests performed in order to qualify the boards of the RF controller. The second section analyzes some key parameters acquired during a successful beam test in real working conditions, where the performance of the new controller has been evaluated. Finally, a concluding chapter summarizes the results obtained so far and outlines improvements and future upgrades that can implement new functionalities in the Radio Frequency control system.

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List of Abbreviations

ADC	**A**nalog **D**igital **C**onverter
ALPI	**A**cceleratore **L**ineare **P**er **I**oni
CA	**C**hannel **A**ccess
CB	**C**harge **B**reeder
CGS	**C**ode **G**roup **S**ynchronization
CORDIC	**CO**ordinate **R**otation **DI**gital **C**omputer
CPM	**C**omplex **P**hase **M**odulator
CSS	**C**ontrol **S**ystem **S**tudio
CW	**C**ontinuos **W**ave
DAC	**D**igital **A**nalog **C**onverter
DDC	**D**irect **D**own **C**onversion
ENOB	**E**ffective **N**umber **O**f **B**its
EPICS	**E**xperimental **P**hysics and **I**ndustrial **C**ontrol **S**ystem
EVM	**EV**aluation **M**odule
FSM	**f**inite **s**tate **m**achine
FPGA	**F**ield **P**rogrammable **G**ate **A**rray
GDR	**G**enerator **D**riven **R**esonator
IC	**I**ntegrated **C**ircuit
ICh	**I**nput **Ch**annel
IIC	**I**nter **I**ntegrated **C**ircuit
ILA	**I**ntegrated **L**ogic **A**nalyzer
ILAS	**I**nitial **L**ane **A**lignment **S**equence
INFN	**I**stituto **N**azionale di **F**isica **N**ucleare
IOC	**I**nput **O**utput **C**ontroller
LFD	**L**orentz **F**orce **D**etuning
Linac	**Lin**ear **ac**celerator
LLRF	**L**ow **L**evel **R**adio **F**requency
LMFC	**L**ocal **L**evel **M**ulti**f**rame **C**lock
OCh	**O**utput **Ch**annel
ORC	**O**ctal **R**esonator **C**ontroller
PLL	**P**hase **L**ocked **L**oop
PI	**P**roportional **I**ntegral

PM	**P**ower **M**onitor
PV	**P**rocess **V**ariable
Q	**Q**uality factor
QWR	**Q**uarter **W**ave **R**esonator
RIB	**R**adioactive **I**on **B**eam
RF	**R**adio **F**requency
RF IOC	**R**adio **F**requency **I**nput **O**utput **C**ontroller
RFFE	**R**adio **F**requency **F**ront **E**nd
rms	**r**oot **m**ean **s**quare
sc	**S**upeconducting
SEL	**S**elf **E**xcited **L**oop
SINAD	**SI**gnal **N**oise **A**nd **D**istortion ratio
SNR	**S**ignal to **N**oise **R**atio
SPI	**S**erial **P**heripheral **I**nterface
SPES	**S**elective **P**roduction of **E**xotic **S**pecies
SRF	**S**upeconducting **R**adio **F**requency
THD	**T**otal **H**armonic **D**istortion
VHDL	**V**HSIC **H**adware **D**escription **L**anguage

1 Introduction

1.1 The SPES Project

SPES (Selective Production of Exotic Species) is one of the most important project supported by the INFN (Istituto Nazionale di Fisica Nucleare). The main goal is the development of a facility for neutron rich exotic beams production to perform forefront research in nuclear structure, reaction dynamics and interdisciplinary fields like medical, biological and material sciences [1]. The LNL (Laboratori Nazionali di Legnaro) was chosen as the site for the construction and operation of SPES.

Fig. 1.1 shows the layout of the SPES facility, from the Charge Breeder (CB) [2] and the new injector, to the linear accelerator (Linac) ALPI [3] and the transport lines to the experimental halls. The driver of the SPES accelerator is a proton cyclotron ($70MeV$, $700\mu A$) [4], that impinging the beam on a uranium carbide target, produces exotic species mostly via nuclear fission. The target is part of an ion source system, from which a q=1+ ion beam is extracted, the unwanted contaminants are removed using a Wien filter and a high resolution mass separator (HRMS) [5]. The purified beam is delivered, through an electrostatic focusing line, to an ECR type CB. The CB and a

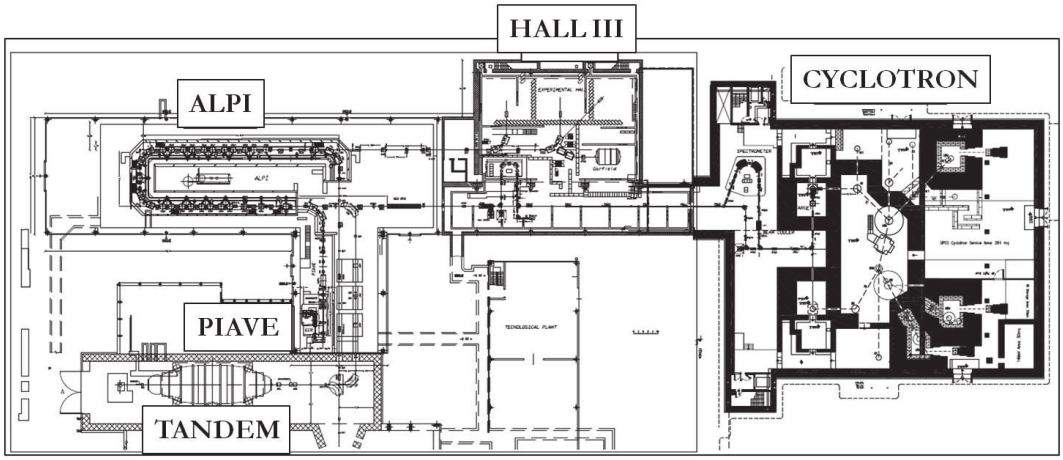


Figure 1.1: Layout of the SPES Facility.

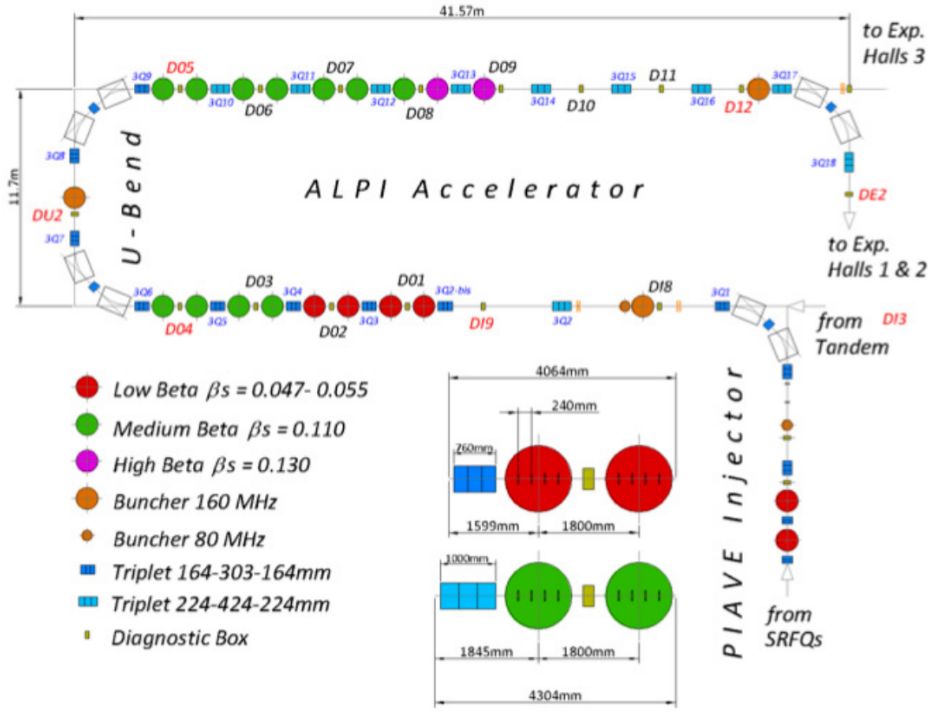


Figure 1.2: Layout of the ALPI Facility.

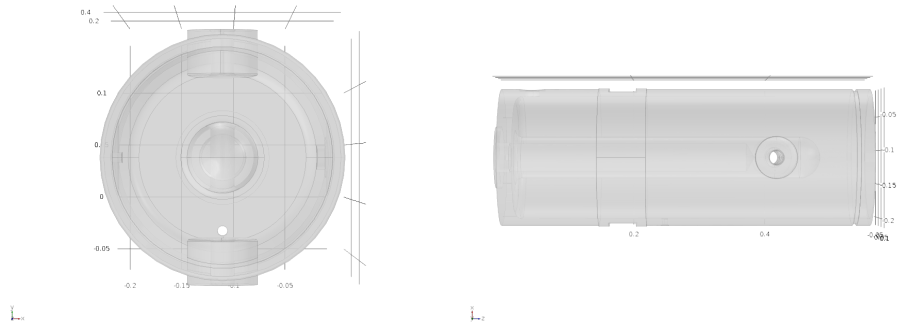
Continuous Wave (CW) RFQ [6], is the front end of a new injector complex into the superconducting (sc) linear accelerator ALPI. The Radioactive Ion Beam (RIB) is boosted through ALPI and sent to the three experimental halls of LNL for physics experiments. The upgrades which would make ALPI suitable as a RIB accelerator are in commissioning phase [7].

1.2 The "ALPI" Linear Accelerator

The ALPI Linac operates cavities under superconducting working conditions. Fig. 1.2 shows the layout of ALPI. ALPI cavities are manufactured in niobium (Nb) bulk or in Nb internally sputtered (coated) copper and they are submerged in a bath of liquid He in order to keep them at a temperature of 4 K because niobium achieves superconducting properties under a critical temperature of 9.2 K. This operating point allows maximum electromagnetic fields significantly higher than cavities working at room temperatures.

The ALPI cavities are QWR (Quarter Wave Resonator) [8]. They are assembled in groups of 4 into custom designed cryostats. The mechanical design of an ALPI cavity is reported in Fig. 1.3. The shape section is a coaxial cable, short-circuited at one end (where the RF magnetic field is maximum) and

open at the other (where the RF electric field is maximum). Ion bunches cross each QWR cavity where electric field is highest and get accelerated by the two gaps between the central drift tube electrode and the surrounding cylinder cavity. The Linac is divided into three sections according to bunch velocity and hence beam energy: the low beta section, whose QWR cavities resonate at 80 MHz, the medium and high beta section with QWR cavities resonating at 160 MHz.



(a) (b)

Figure 1.3: Mechanical design of a medium beta cavity. a) Front view b) lateral view.

Presently, ALPI can accelerate the beam coming from a Van Der Graaf injector and also from a second smaller Linac, more recently put into operation, called PIAVE (acronym for "Positive Ion Accelerator for very low VElocity ions").

In order to boost also the RIB coming from SPES, ALPI must be tuned. Most of its components need to be revisited: RF controllers, RF control system, RF power amplifiers and mechanical in the cavities: e.g. couplers, pick-ups and tuners.
The work presented here is focused on the RF controller and RF control system upgrade. The reasons are the following: the radioactive beam injected from SPES will be of very low intensity, down to $10^7 \div 10^9$ particles/s and re-acceleration by ALPI needs higher resolution and higher stability of the electromagnetic fields in the cavity, in order to minimize losses in the transport lines due to the inherent de-focusing and steering of magnetic and electrostatic lenses put along the beam path. Besides this, the existing analog controllers have reached the end of their useful life and cannot be maintained any longer.

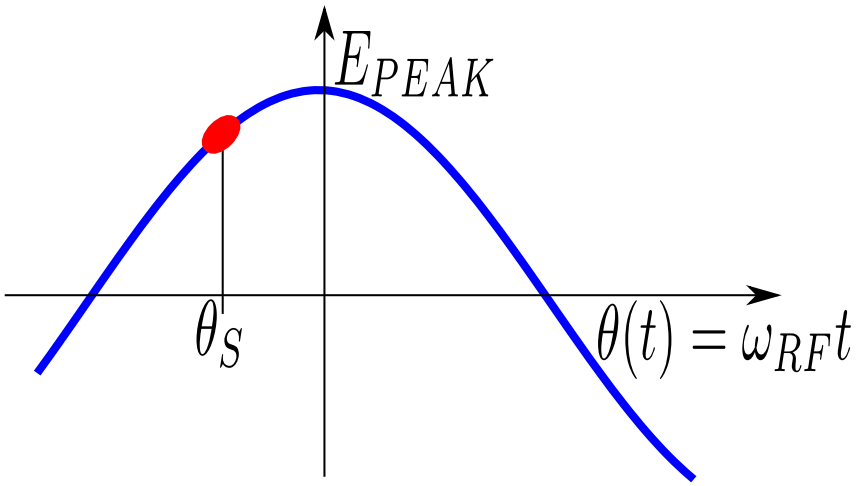


Figure 1.4: Acceleration in a RF gap.

1.3 Radio Frequency Acceleration

The RF system in a Linac has to focus the beam in the longitudinal direction, minimize the de-focusing on the transverse plane and add up energy to accelerate the beam. The phase between the RF signal and the beam is crucial for a proper acceleration. The following dissertation is more detailed in [9].

In a gap of length L including an electromagnetic gradient, the rate of energy gained by a particle crossing that section is:

$$\frac{dE}{dz} \approx \frac{\Delta E}{L} = q\frac{V_c}{l_c}\cos(\phi(t)) = qE_{PEAK}\cos(\phi(t)) \tag{1.1}$$

where $\phi(t)$ is the angle between beam and RF signal.
From Fig. 1.4, E_0 is defined as the energy gained by the synchronous particle passing through the cavity at ϕ_s:

$$\frac{dE_0}{d_z} = qE_{PEAK}\cos(\phi_s) \tag{1.2}$$

The particles in the bunch not synchronous with ϕ_s, gain an energy with differs from E_0 by a quantity:

$$\begin{aligned}\frac{d\epsilon}{dz} = \frac{d(E-E_0)}{d_z} = qE_{PEAK}[\cos(\phi(t)) - \cos(\phi_s)] = \\ = qE_{PEAK}[\cos(\phi_s + \theta(t)) - \cos(\phi_s)]\end{aligned} \tag{1.3}$$

Different energy gain, with the same initial conditions, means different velocities. You may rewrite:

$$\frac{d\theta(t)}{dz} = \omega_{RF}\frac{d}{dz}(t - t_s) = \omega_{RF}\left(\frac{1}{v(t)} - \frac{1}{v_s}\right) = -\omega_{RF}\left(\frac{v(t) - v_s}{v(t)v_s}\right) \tag{1.4}$$

The energy difference between a generic particle and the synchronous particle is:

$$\epsilon(t) = E(t) - E_0 = \frac{1}{2}m(v(t)^2 - v_s^2) \approx mv_s(v(t) - v_s) \tag{1.5}$$

Then equation 1.4, considering the previous approximation too, becomes:

$$\frac{d\theta(t)}{dz} = -\frac{\omega_{RF}}{mv_s^3}\epsilon(t) \tag{1.6}$$

The longitudinal dynamics of a generic particle with respect to the synchronous particle is defined by:

$$\begin{aligned} \frac{d\theta(t)}{dz} &= -\frac{\omega_{RF}}{mv_s^3}\epsilon(t) \\ \frac{d\epsilon(t)}{dz} &= qE_{PEAK}[\cos(\phi_s + \theta(t)) - \cos(\phi_s)] \end{aligned} \tag{1.7}$$

In order to analyze the stability of equilibrium points, equations 1.7 have to be linearized around them:

$$\frac{dx(t)}{dt} = f(x) \to f(\bar{x}) = 0 \Rightarrow \frac{d(x(t) - \bar{x})}{dt} = A(x(t) - \bar{x}) \tag{1.8}$$

At the equilibrium points, that is $\bar{x} : (\bar{\theta}, \bar{\epsilon}) = (0, 0)$, equations 1.7 linearized are:

$$\begin{aligned} \frac{d\theta(t)}{dz} &= -\frac{\omega_{RF}}{mv_s^3}\epsilon(t) \\ \frac{d\epsilon(t)}{dz} &= -qE_{PEAK}\sin(\phi_s)\theta(t) \end{aligned} \tag{1.9}$$

that is equivalent to:

$$\begin{bmatrix} \frac{d\theta(t)}{dz} \\ \frac{d\epsilon(t)}{dz} \end{bmatrix} = A \begin{bmatrix} \theta(t) \\ \epsilon(t) \end{bmatrix} = \begin{bmatrix} 0 & -\frac{\omega_{RF}}{mv_s^3} \\ -qE_{PEAK}\sin(\phi_s) & 0 \end{bmatrix} \begin{bmatrix} \theta(t) \\ \epsilon(t) \end{bmatrix} \tag{1.10}$$

The eigenvalues λ of A are defined by the characteristic equation:

$$det(\lambda I - A) = det \begin{bmatrix} \lambda & \frac{\omega_{RF}}{mv_s^3} \\ qE_{PEAK}\sin(\phi_s) & \lambda \end{bmatrix} = \lambda^2 + x^2 = 0 \tag{1.11}$$

with $x^2 = -qE_{PEAK}\frac{\omega_{RF}}{mv_s^3}\sin(\phi_s)$. Studying the real part value and sign of the eigenvalues, informations about the longitudinal dynamics stability are deduced:

- If $x^2 > 0$, $\phi_s = -\arccos\left(\frac{E_0}{qE_{PEAK}l_c}\right) + 2K\pi$. The equilibrium points are stable;
- If $x^2 < 0$, $\phi_s = \arccos\left(\frac{E_0}{qE_{PEAK}l_c}\right) + 2K\pi$. The equilibrium points are unstable.

Therefore to guarantee the stability of the particle motion it is necessary to keep the relative position between the bunch and the accelerating voltage phase to certain values. The choice of the synchronous phase in the positive slope of the RF voltage provides longitudinal focusing, thanks to the bunching effect and acceleration of the beam at the same time.

1.3.1 RF Acceleration in ALPI

In ALPI the RF accelerating structures are Quarter Wave Resonators (QWRs), basically equivalent to coaxial lines. The coaxial line has two conductors, center and outer, and it supports TEM modes. In the case of Linac QWRs the coaxial structure is short-circuited at one end, while at the opposite end the outer conductor is closed with a cap that forms a capacitor with the inner conductor (Fig. 1.5). In Fig. 1.6 there is a representation of a QWR considered as a transmission line. In this figure the capacitance C_L formed between inner conductor and final part of the outer conductor is outlined.

In a transmission line the relations between the voltage and the current along the line are expressed by the Telegrapher 's equations:

$$\begin{cases} V(z) = V_+e^{-\gamma z} + V_-e^{\gamma z} \\ I(z) = \frac{1}{Z_0}(V_+e^{-\gamma z} + V_-e^{\gamma z}) \end{cases} \tag{1.12}$$

with Z_0 the characteristic impedance of the cavity and $\gamma = j\beta_W$ its propagation constant. Since at one end the coaxial line is short-circuited, equations

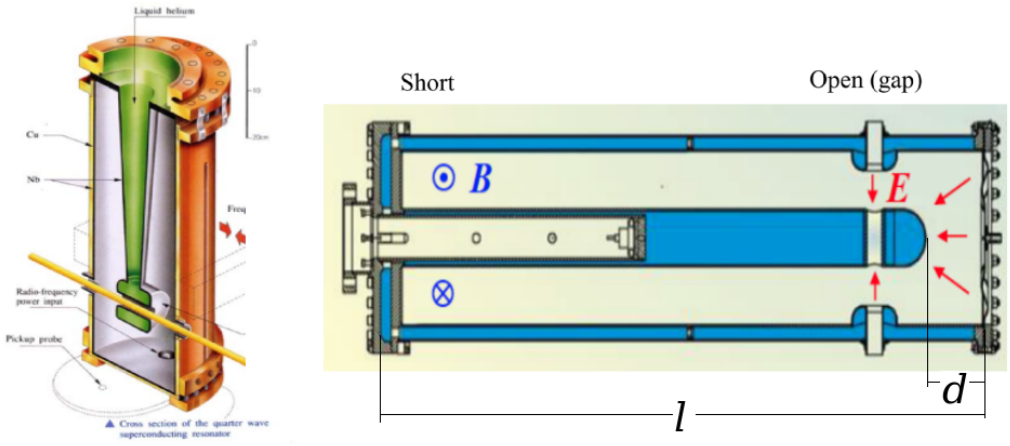


Figure 1.5: ALPI QWR (on the left) and its transverse section (on the right). [10]

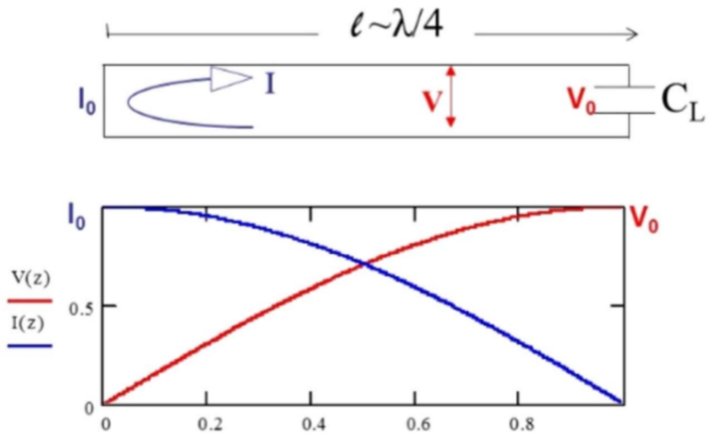


Figure 1.6: QWR transmission line electric model and current and voltage along the line. [10]

1.12 turn into:

$$\begin{cases} V(z) = V_+(e^{-\gamma z} - e^{\gamma z}) = -2jV_+ \sin(\beta_W z) \\ I(z) = \frac{1}{Z_0} V_+(e^{-\gamma z} + e^{\gamma z}) = 2\frac{V_+}{Z_0} \cos(\beta_W z) \end{cases} \tag{1.13}$$

From equations 1.13, the voltage V and hence the electric field E in the cavity has a maximum at the edge of the cavity opposite to the short-circuit: for $\beta_W z = \pi/2$. Rewriting β_W as:

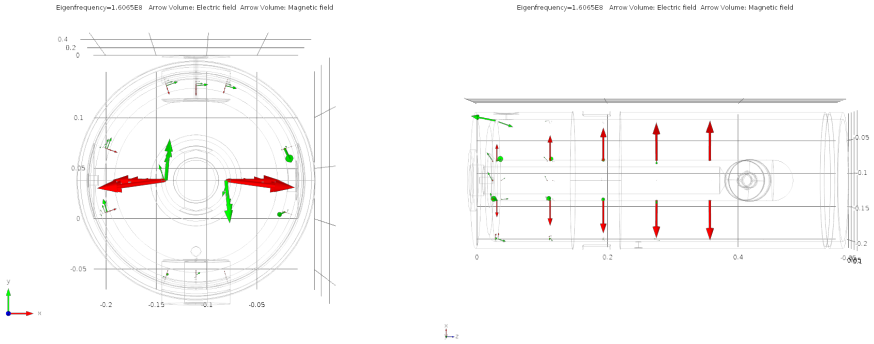
$$\beta_W = \frac{2\pi}{\lambda} \tag{1.14}$$

the beamline is placed at $z = l = \lambda/4$, where E is maximum and can be used

QWRs	Low Beta	Medium Beta	High Beta
f_0 [MHz]	80	160	160
L [cm]	18	18	18
β [% c]	0.056	0.11	0.13
G [Ω]	15.4	32	29
r_{sh} [MΩ/m]	20.4	24	24
E_a [MV/m]	6	5	4.1
P_c [W]	7	7	7
Q_0	$8 \cdot 10^8$	$3 \cdot 10^8$	$3 \cdot 10^8$
E_{peak}/E_a	4.9	4.7	4.9
B_{peak}/E_a [Gauss/(MV/m)]	100	104	106

Table 1.1: Parameters of the superconducting ALPI cavities.

to accelerate the charged particles. The fields are shown in Fig. 1.7. Therefore the highest energy gain of the beam can be achieved if the charged particle bunches pass the cavity cells when the electric field reaches its maximum (on-crest acceleration). Fluctuations in amplitude and phase lead to spread the beam energy gain.



(a) (b)

Figure 1.7: Distribution of electromagnetic field in a QWR cavity at its eigenfrequency. a) Front view b) lateral view.

In ALPI there are three kind of cavities. The main characteristics are listed in table 1.1.

1.4 Radio Frequency Cavity Control

When a resonator operates slightly off resonance, amplitude and phase of the field inside the cavity change with respect to the driving signal. The eigenfrequency of a cavity changes mainly because it:

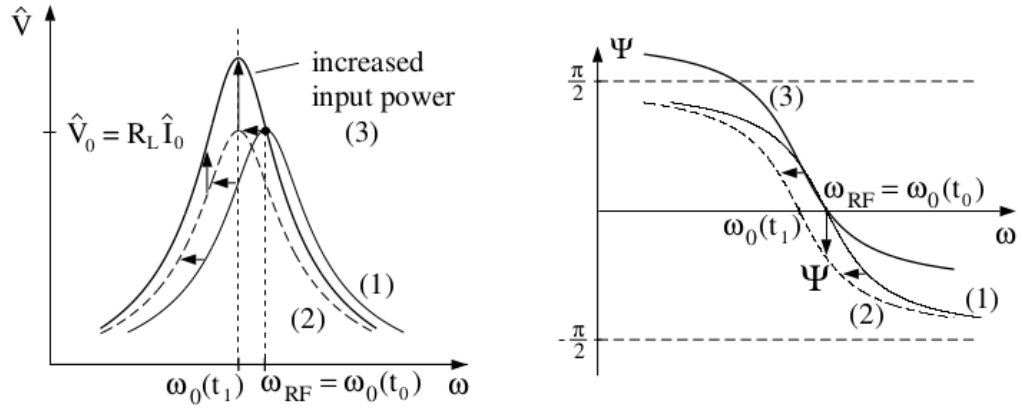


Figure 1.8: Principle of RF control. A frequency detuning corresponds to a decreasing of the amplitude and a phase shift. Therefore it is necessary a phase shift in the opposite direction and an adjusting of the input power. [11]

- changes its shape (i.e. due to vibrations);
- changes its dimensions (due to cooling, when it gets superconductivity);
- changes the stored electromagnetic energy (Lorentz force detuning);
- changes the dielectric: from air to empty;
- changes the charged distribution inside (i.e. multipactoring, quench).

ALPI cavities, due to their superconducting nature, resonate in a narrow bandwidth. Consequently, they are very susceptible to eigenfrequency changes and even small perturbations can result in massive field variations. Amplitude and phase fluctuations caused by these vibrations have to be compensated by an RF control system (see Fig. 1.8).
When the resonance frequency changes there is a magnitude decrease of the electric field inside the cavity, that has to be compensated by increasing the input power. At the same time the electric field undergoes also a phase shift that has to be correct applying a phase shift to the driving signal in opposite direction.

This operation has to be done by a so called Low Level Radio Frequency (LLRF) controller, that is part of the RF system: it is a fundamental part of the accelerator complex that performs a specific and critical function. It interacts directly with the cavity and other subsystems, and works in a real-time loop.
The controller is the main subject of this thesis. Field Programmable Gate Array (FPGA) replaces the previous analog controller by a novel digital RF

control system. Main part of this thesis covers the development and validation of this system.

1.5 The Linac Software

The control system of a particle accelerator allows the operation of the machine, the monitoring of its status and the handling of exceptional conditions. The control system makes possible to have access to the different devices of the infrastructure from a unique and remote control room. The status of the accelerator and beam lines can be displayed for each subsystem. In the case of the RF subsystem, for instance, the new LLRF controller allows the supervision of the signals picked up from the cavities, of the parameters of the control algorithms implemented in FPGA and of the signals sent back to the power amplifiers. The integration of these functionalities in the existing software control system has revealed to be impractical: that's why the whole control software has undergone a major revision moving to a modern software framework called EPICS (Experimental Physics and Industrial Control System) [12]. For the same reasons the LLRF control system has required an accurate and specific development for the integration in EPICS. This integration will be covered in next chapters.

2 The Radio Frequency Cavities

2.1 The Cavity Resonator

A cavity resonator is a closed metal structure that confines radio frequency electromagnetic fields. Resonant cavities are usually obtained from short-circuited sections of a waveguide or a coaxial line.

Electromagnetic energy is stored in the cavity and the only losses are due to finite conductivity of cavity walls and dielectric/ferromagnetic losses of material filling the cavity. In order to dramatically increase the quality factor Q of the resonator, it is necessary increase the conductivity of the cavity walls exploiting superconductivity. The cavity must have openings to allow beam passage.

2.1.1 From LC Circuit to Cavity Model

An LC circuit is the simplest form of RF resonator and it can be used as basic cavity model. This electric circuit and a resonant RF cavity share common aspects, as the fact that the energy is stored and periodically exchanged between the electric and magnetic fields. As shown in the cartoon in Fig. 2.1, an LC circuit can be transformed into a RF cavity by increasing the resonance frequency: this can happen by lowering L with the use of solid walls and lowering C exploiting cylindrical or elliptical geometries. Finally, the beam tubes have to be added to let the particles pass through.

2.2 Key Cavity Parameters

The dissertation done in this paragraph is detailed deeper in [13]. The stored energy in a cavity is given by:

$$U = \frac{1}{2}\mu_0 \int_V |H^2| dv = \frac{1}{2}\varepsilon_0 \int_V |E^2| dv \tag{2.1}$$

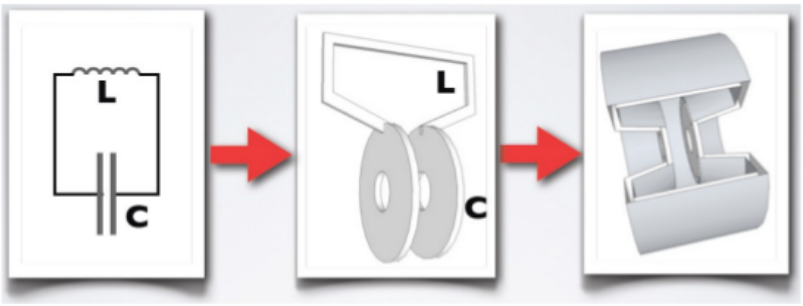


Figure 2.1: RLC representation of a RF cavity.

In any resonant system, one of the most important figure of merit is the quality factor Q, which it is defined as:

$$Q_0 = \frac{\omega_0 \times (\text{stored energy})}{P_c} = \omega_0 \frac{U}{P_c} = \omega_0 \tau_0 = \frac{\omega_0}{\Delta\omega_0} \tag{2.2}$$

Q is defined also as:

$$Q_0 = \frac{G}{R_s} \tag{2.3}$$

Where G is the geometric factor that depends only on the cavity shape and electromagnetic mode, but not on its size. On the other hand, R_s is the surface resistance and it can be expressed as:

$$R_s(T) = R_o + R_{BCS}(T) \tag{2.4}$$

with R_o the residual resistance, usually of few $n\Omega$, that comes from different extrinsic contributions as: impurities/defects in the surface, hydrides precipitates and trapped flux. Whereas the $R_{BCS}(T)$ for niobium cavities depends on the temperature according to the relation:

$$R_{BCS}(T) \approx 2 \cdot 10^{-4} \left(\frac{f[MHz]}{1500} \right)^2 \frac{1}{T} e^{-17.67/T} [\Omega] \tag{2.5}$$

A useful parameter is the shunt impedance that determines how much acceleration a particle can get for a given power dissipation in a cavity. A common definition is:

$$r_{sh} = \frac{E_{acc}^2}{P_c^I} \tag{2.6}$$

where P_c^I is the power dissipation per unit length and the shunt impedance is in $[\Omega/m]$.

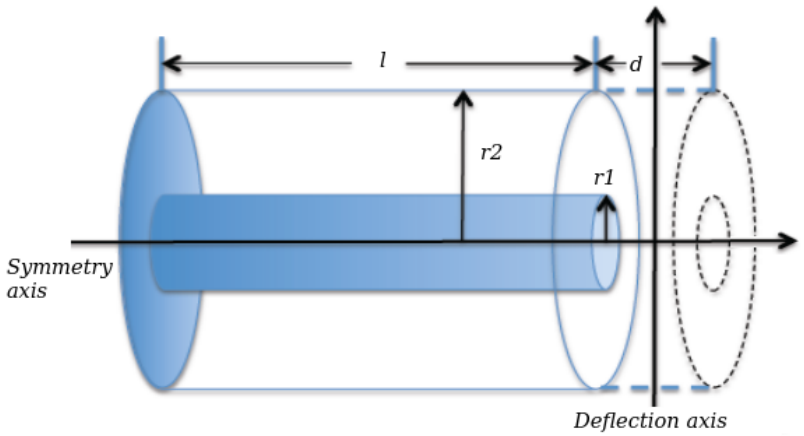


Figure 2.2: QWR cavity.

2.2.1 QWR Peculiarities

The characteristic impedance of a coaxial line is defined as:

$$Z_0 = \frac{\eta}{2\pi} ln\left(\frac{r_2}{r_1}\right) \tag{2.7}$$

with $\eta = \sqrt{\frac{\mu_0\mu_r}{\varepsilon_0\varepsilon_r}}$. Here μ_0, μ_r, ε_0 and ε_r are the magnetic permeability of free space, the relative permeability, the permittivity of free space and the relative permittivity, respectively.

As mentioned in previous chapter, a QWR cavity can be considered a coaxial line shorted at one hand and open at the opposite end. Therefore equation 2.7 is still valid for QWR cavities.
For these cavities the geometric factor is:

$$G = QR_s = \frac{2\pi\eta}{\lambda} \frac{ln(r_2/r_1)}{r_1^{-1} + r_2^{-1}} \tag{2.8}$$

Some characteristics of a QWR cavity are:

- The length of the inner conductor is $l = \lambda/4$;
- The E field is zero at the short end;
- The gap is very small compared to the total length. From Fig. 2.2 $d << l$;
- The resonance modes are at frequencies $\omega_n = 2(2n+1)\pi c/(4l)$;
- The lowest resonance frequency is $\omega_0 = \pi c/(2l)$.

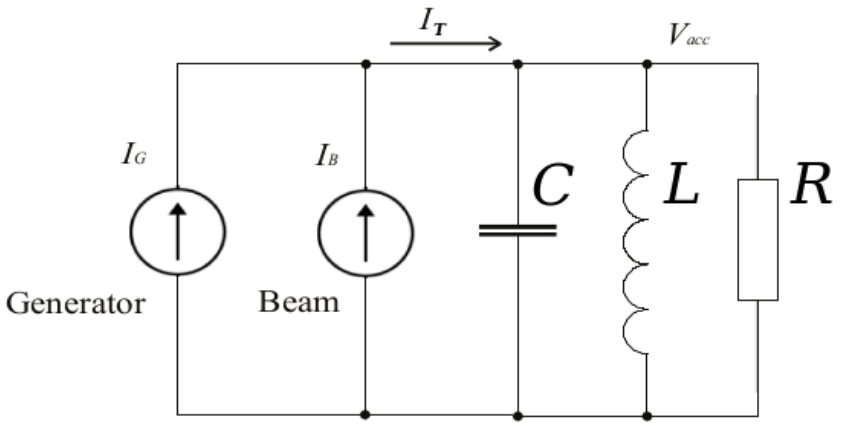


Figure 2.3: Equivalent circuit of a resonant mode RF cavity.

2.3 Cavity Steady State Model

Fig. 2.3 reports the RLC model of a RF cavity. The two current sources represent the current from the power amplifier (the generator) and from the beam current (the so called beam loading). Applying Kirkhoff's current law to the nodes of the model we obtain:

$$\begin{aligned} &\frac{1}{R}v_c(t) + \frac{1}{L}\int_0^T v_c(t)dt + C\frac{dv_c(t)}{dt} = i_G(t) + i_B(t) = i_T(t) \\ &\ddot{v_c}(t) + \frac{1}{RC}\dot{v_c}(t) + \frac{1}{LC}v_c(t) = \frac{1}{C}\dot{i_T}(t) \end{aligned} \tag{2.9}$$

In steady state conditions the following hold: $i_T(t) = I_T\cos(\omega_c t + \alpha) = \Re\{I_T e^{j\alpha}e^{j\omega_c t}\} = \Re\{\tilde{I_T}e^{j\omega_c t}\}$ and $v_C(t) = V_C\cos(\omega_c t + \beta) = \Re\{V_C e^{j\beta}e^{j\omega_c t}\} = \Re\{\tilde{V_C}e^{j\omega_c t}\}$, where ω_c is the carrier frequency.

Equation 2.9 can be rewritten as:

$$\begin{aligned} &(j\omega_c)^2\tilde{V_C}e^{j\omega_c t} + \frac{1}{RC}(j\omega_c)\tilde{V_C}e^{j\omega_c t} + \frac{1}{LC}\tilde{V_C}e^{j\omega_c t} = \frac{1}{C}(j\omega_c)\tilde{I_T}e^{j\omega_c t} \\ &\left(j\omega_c C + \frac{1}{R} + \frac{1}{j\omega_c L}\right)\tilde{V_c} = \tilde{I_T} \\ &\tilde{V_c} = \frac{1}{\left(j\omega_c C + \frac{1}{R} + \frac{1}{j\omega_c L}\right)}\tilde{I_T} = Z_c(\omega_c)\tilde{I_T} \end{aligned} \tag{2.10}$$

with:

$$Z_c(\omega_c) = \frac{R}{1 + jR\left(\omega_c C - \frac{1}{\omega_c L}\right)} = \frac{R}{1 - j\tan\Psi} \tag{2.11}$$

$$\frac{|Z_c(\omega_c)|}{R} = \frac{1}{\sqrt{1+\left[R\left(\frac{1}{\omega_c L}-\omega_c C\right)\right]^2}} = \frac{1}{\sqrt{1+\tan\Psi^2}} = \cos(\Psi) \tag{2.12}$$

Ψ is the angle between the driving current I_T and the cavity voltage V_c and it is defined as detuning angle of the cavity.

2.4 The Transient Model of the Cavity

For the control of the RF cavity, we have to modulate the amplitude/phase components of the generator current $i_G(t)$. Considering a generic sine wave of frequency f_c and amplitude X, that is $x(t) = X\sin(2\pi f_c t)$. Let $a_m(t)$ be the modulation waveform. Then the amplitude modulation results when the carrier $x(t)$ is multiplied by the positive quantity $(1 + a_m(t))$:

$$x_{AM}(t) = X(1 + a_m(t))\sin(2\pi f_c t) \tag{2.13}$$

Let now $\phi_m(t)$ be the modulation waveform. The phase modulation results when the argument of the carrier $x(t)$ is shifted by the quantity $\phi_m(t)$:

$$x_{PM}(t) = X\sin(2\pi f_c t + \phi_m(t)) \tag{2.14}$$

Combining the last two equations and applying them to $i_G(t)$ we get:

$$\begin{aligned} i_G(t) &= I_G(1 + a_m(t))\sin(\omega_c t + \phi_m(t)) \\ i_G(t) &= I_G(t)\cos(\phi_m(t))\cos(\omega_c t) - I_G(t)\sin(\phi_m(t))\sin(\omega_c t) \\ i_G(t) &= I_{G_{IN}}(t)\cos(\omega_c t) - I_{G_Q}(t)\sin(\omega_c t) \end{aligned} \tag{2.15}$$

Applying the Euler's formula, the signal $i_G(t)$ can be expressed in phasor representation as:

$$i_G(t) = \Re\{i_{GL}(t)e^{j2\pi f_c t}\} \tag{2.16}$$

where $i_{GL}(t) = I_{G_{IN}}(t) + jI_{G_Q}(t)$.
The notation $\tilde{i_G}(t) = i_{GL}(t)e^{j2\pi f_c t}$ in the following, for representing the signals is used.

Based on the initial differential equation representing the fundamental resonant mode of the cavity (equation 2.9), we need to get a model describing the dynamics of the modulation signals in $i_G(t)$, $i_B(t)$ and $v_c(t)$.
Equation 2.9 can be rewritten as:

$$\ddot{\tilde{v_c}}(t) + \frac{1}{RC}\dot{\tilde{v_c}}(t) + \frac{1}{LC}\tilde{v_c}(t) = \frac{1}{C}\dot{\tilde{i_T}}(t) \tag{2.17}$$

with $\tilde{v_c}(t) = v_{cL}(t)e^{j\omega_c t}$, $\tilde{i_T}(t) = i_{TL}(t)e^{j\omega_c t}$. Substituting in 2.17:

$$\ddot{v_{cL}}(t)e^{j\omega_c t} + 2j\omega_c\dot{v_{cL}}(t)e^{j\omega_c t} - \omega_c^2 v_{cL}(t)e^{j\omega_c t} + \frac{1}{RC}\left(\dot{v_{cL}}(t)e^{j\omega_c t} + j\omega_c v_{cL}(t)e^{j\omega_c t}\right) + \frac{1}{LC}v_{cL}(t)e^{j\omega_c t} = \frac{1}{C}\left(\dot{i_{TL}}(t)e^{j\omega_c t} + j\omega_c i_{TL}(t)e^{j\omega_c t}\right) \tag{2.18}$$

In equation 2.18 the terms $e^{j\omega_c t}$ can be simplified. As the bandwidth of the complex envelope signal is much lower than the carrier frequency $\omega_c/2\pi$ the terms including the second derivative of the complex envelope of the voltage and the first derivative of the complex envelope of the total current are negligible, that is:

$$\ddot{v_{cL}}(t) << \omega_c\dot{v_{cL}}(t)\ ,\ \ddot{v_{cL}}(t) << \omega_c^2 v_{cL}(t) \text{ and } \dot{i_{TL}}(t) << \omega_c i_{TL}(t)$$

Hence equation 2.18 becomes:

$$2j\omega_c\dot{v_{cL}}(t) - \omega_c^2 v_{cL}(t) + \frac{1}{RC}\left(\dot{v_{cL}}(t) + j\omega_c v_{cL}(t)\right) + \frac{1}{LC}v_{cL}(t) = \frac{1}{C}i_{TL}(t) \tag{2.19}$$

and grouping the terms involving $\dot{v_{cL}}(t)$ and $v_{cL}(t)$:

$$\left(2j\omega_c + \frac{1}{RC}\right)\dot{v_{cL}}(t) = \left(-\frac{j\omega_c}{RC} + \omega_c^2 - \frac{1}{LC}\right)v_{cL}(t) + \frac{j\omega_c}{C}i_{TL}(t) \tag{2.20}$$

Since $\omega_c >> 1/RC$ and dividing by $2j\omega_c$, the equation simplifies to:

$$\dot{v_{cL}}(t) = \left(-\frac{1}{2RC} + \frac{\omega_c^2 - \omega_0^2}{2j\omega_c}\right)v_{cL}(t) + \frac{1}{2C}i_{TL}(t) \tag{2.21}$$

Assuming that $\omega_c \approx \omega_0$:

$$\dot{v_{cL}}(t) = -\left(\frac{1}{2RC} + j(\omega_c - \omega_0)\right)v_{cL}(t) + \frac{1}{2C}i_{TL}(t) \tag{2.22}$$

Introducing the definition $\frac{\omega_0 R}{2Q_L} = \frac{1}{2C}$, $\frac{1}{2RC} = \frac{\omega_0}{2Q_L} = \omega_{1/2}$ the cavity bandwidth and $\Delta\omega = \omega_c - \omega_0$ the cavity frequency detuning, the final equation is:

$$\dot{v_{cL}}(t) = -\left(\omega_{1/2} + j\Delta\omega\right)v_{cL}(t) + \frac{\omega_0 R}{2Q_L}i_{TL}(t) \tag{2.23}$$

Substituting the complex envelope by the in-phase/quadrature components $v_{cL}(t) = v_{c_{IN}}(t) + jv_{c_Q}(t)$, $i_{TL}(t) = i_{T_{IN}}(t) + ji_{T_Q}(t)$ and separating the differential equation into real and imaginary parts:

$$\begin{bmatrix} \dot{v_{c_{IN}}}(t) \\ \dot{v_{c_Q}}(t) \end{bmatrix} = \begin{bmatrix} -\frac{\omega_0}{2Q_L} & \omega_c - \omega_0 \\ -\omega_c + \omega_0 & -\frac{\omega_0}{2Q_L} \end{bmatrix} \begin{bmatrix} v_{c_{IN}}(t) \\ v_{c_Q}(t) \end{bmatrix} + \frac{\omega_0 R}{2Q_L} \begin{bmatrix} i_{T_{IN}}(t) \\ i_{T_Q}(t) \end{bmatrix}$$
$$\begin{bmatrix} \dot{v_{c_{IN}}}(t) \\ \dot{v_{c_Q}}(t) \end{bmatrix} = \begin{bmatrix} -\omega_{1/2} & \Delta\omega \\ -\Delta\omega & -\omega_{1/2} \end{bmatrix} \begin{bmatrix} v_{c_{IN}}(t) \\ v_{c_Q}(t) \end{bmatrix} + \omega_{1/2} R \begin{bmatrix} i_{T_{IN}}(t) \\ i_{T_Q}(t) \end{bmatrix} \tag{2.24}$$

Taking the Laplace transform and assuming initial conditions equal to zero:

$$\begin{bmatrix} sV_{c_{IN}}(s) \\ sV_{c_Q}(s) \end{bmatrix} = \begin{bmatrix} -\frac{\omega_0}{2Q_L} & \omega_c - \omega_0 \\ -\omega_c + \omega_0 & -\frac{\omega_0}{2Q_L} \end{bmatrix} \begin{bmatrix} V_{c_{IN}}(s) \\ V_{c_Q}(s) \end{bmatrix} + \frac{\omega_0 R}{2Q_L} \begin{bmatrix} I_{T_{IN}}(s) \\ I_{T_Q}(s) \end{bmatrix} \tag{2.25}$$

then:

$$\begin{bmatrix} s + \frac{\omega_0}{2Q_L} & -\omega_c + \omega_0 \\ \omega_c - \omega_0 & s + \frac{\omega_0}{2Q_L} \end{bmatrix} \begin{bmatrix} V_{c_{IN}}(s) \\ V_{c_Q}(s) \end{bmatrix} = \frac{\omega_0 R}{2Q_L} \begin{bmatrix} I_{T_{IN}}(s) \\ I_{T_Q}(s) \end{bmatrix} \tag{2.26}$$

Finally:

$$\begin{aligned} &\begin{bmatrix} V_{c_{IN}}(s) \\ V_{c_Q}(s) \end{bmatrix} = \frac{\omega_0 R}{2Q_L} \begin{bmatrix} s + \frac{\omega_0}{2Q_L} & -\omega_c + \omega_0 \\ \omega_c - \omega_0 & s + \frac{\omega_0}{2Q_L} \end{bmatrix}^{-1} \begin{bmatrix} I_{T_{IN}}(s) \\ I_{T_Q}(s) \end{bmatrix} = \\ &= \frac{\omega_0 R}{2Q_L} \frac{1}{(s + \frac{\omega_0}{2Q_L})^2 + (\omega_c - \omega_0)^2} \begin{bmatrix} s + \frac{\omega_0}{2Q_L} & \omega_c - \omega_0 \\ -\omega_c + \omega_0 & s + \frac{\omega_0}{2Q_L} \end{bmatrix} \begin{bmatrix} I_{T_{IN}}(s) \\ I_{T_Q}(s) \end{bmatrix} = \\ &= \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_{T_{IN}}(s) \\ I_{T_Q}(s) \end{bmatrix} \end{aligned} \tag{2.27}$$

where:

$$\begin{aligned} Z_{11} = Z_{22} &= \frac{\omega_0 R}{2Q_L} \frac{s + \frac{\omega_0}{2Q_L}}{s^2 + \frac{\omega_0}{Q_L} s + (\frac{\omega_0}{2Q_L})^2 + (\omega_0 - \omega_c)^2} \\ Z_{21} = -Z_{12} &= \frac{\omega_0 R}{2Q_L} \frac{\omega_0 - \omega_c}{s^2 + \frac{\omega_0}{Q_L} s + (\frac{\omega_0}{2Q_L})^2 + (\omega_0 - \omega_c)^2} \end{aligned} \tag{2.28}$$

Hence we can define the transfer function $\tilde{Z}_c(s)$ [14] as:

$$\tilde{Z}_c(s) = Z_{11}(s) + jZ_{21}(s) = \frac{\omega_0 R}{2Q_L} \frac{s + \frac{\omega_0}{2Q_L} + j(\omega_0 - \omega_c)}{s^2 + \frac{\omega_0}{Q_L} s + (\frac{\omega_0}{2Q_L})^2 + (\omega_0 - \omega_c)^2} \tag{2.29}$$

The bode diagrams of these transfer functions are represented in Fig. 2.4, Fig. 2.5 and 2.6. Fig. 2.4 shows Z_{11} or equivalently Z_{22} when the frequency detuning is zero. In this condition the RF cavity at its own resonance mode

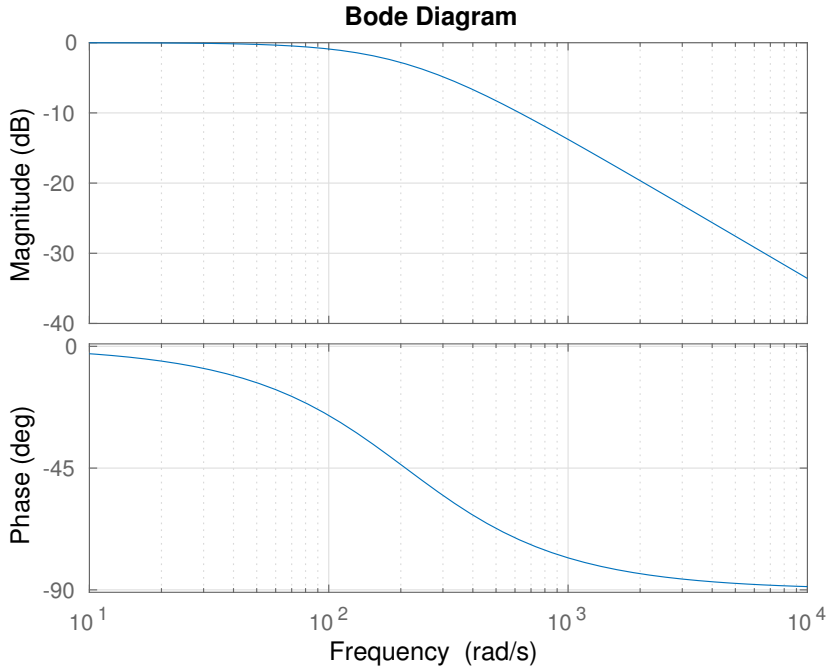


Figure 2.4: Z_{11} transfer function with zero detuning. This was obtained substituting to 2.28 the typical values for an ALPI medium beta cavity.

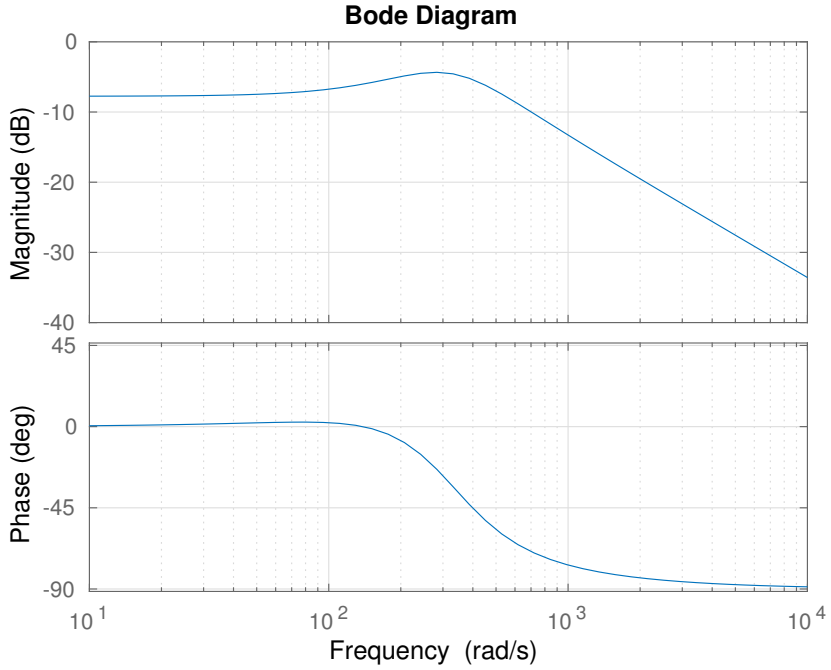


Figure 2.5: Z_{11} transfer function with $50/2\pi$ Hz of detuning. This was obtained substituting to 2.28 the typical values for an ALPI medium beta cavity.

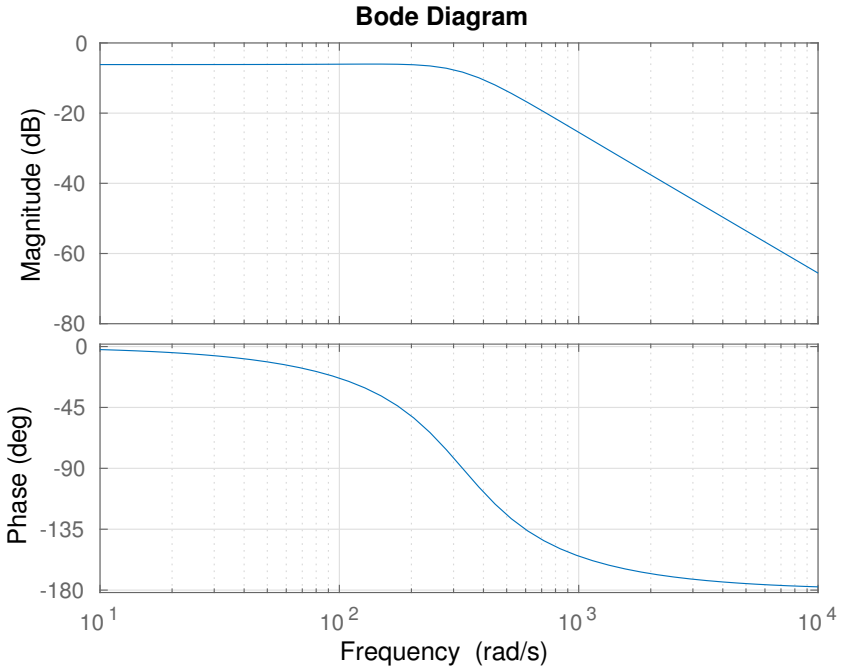


Figure 2.6: Z_{12} transfer function with $50/2\pi$ Hz of detuning. This was obtained substituting to 2.28 the typical values for an ALPI medium beta cavity.

is well described by a first order low-pass filter. Furthermore, the in-phase and quadrature components are decoupled.
In Fig. 2.5 and Fig. 2.6 Z_{11} and Z_{12}, with a frequency detuning of $50/2\pi$ Hz, are shown respectively. The in-phase and quadrature are coupled and the cavity model is not time invariant since $\Delta\omega = \Delta\omega(t)$. In particular Z_{12} shows that the coupling between the two components is a second order low-pass filter.

2.5 Coupling

To excite a resonant mode, the cavity has to be connected to an RF power source via an input coupler through a cavity port. The input coupler is modeled as an ideal transformer, as shown in Fig. 2.7. If RF source is turned off, the stored energy will be dissipated now not only in R, but also in $Z_0 n^2$, that is the generator impedance referred to the secondary. Thus:

$$\begin{aligned} &P_{tot} = P_0 + P_{ext} \\ &P_0 = P_c = \frac{V_c^2}{R} = \frac{V_c^2}{R/Q_0 \cdot Q_0} \quad P_{ext} = \frac{V_c^2}{Z_0 n^2} = \frac{V_c^2}{R/Q_0 \cdot Q_{ext}} \end{aligned} \tag{2.30}$$

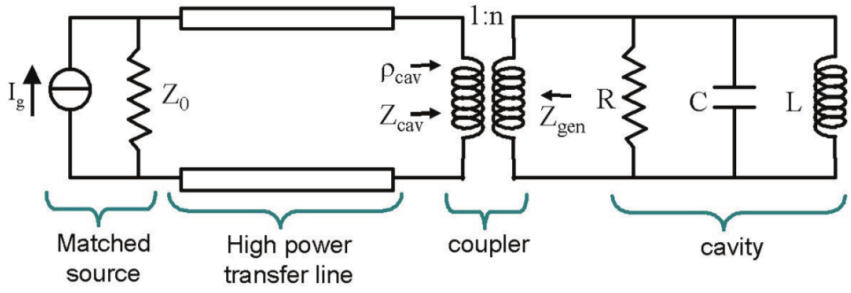


Figure 2.7: Equivalent circuit of a cavity coupled with an RF source. [15]

where Q_{ext} is an external quality factor associated with an input coupler. The external Q factors depend also on RF probe, beam pipes and dielectric. Then the total power loss can be associated with the loaded Q factor, which is:

$$\frac{1}{Q_L} = \frac{1}{Q_0} + \frac{1}{Q_{ext}} + \frac{1}{Q_{ext1}} + \frac{1}{Q_{ext2}} + ... \tag{2.31}$$

For each port a coupling parameter can be defined as:

$$\beta = \frac{Q_0}{Q_{ext}} \tag{2.32}$$

The parameter β, referred to the input coupler, quantifies how strongly the coupler interact with the cavity.
For heavy ion superconducting Linac, like ALPI, the RF power to inject into cavities is mainly determined by the necessity to reach a sufficient overcoupling to guarantee an acceptable bandwidth in the order of a few tens of Hz. Indeed if the coupling coefficient increases, the loaded Q decreases and hence the bandwidth $\Delta\omega$ becomes wider, as can be seen from equation 2.2.

2.6 Forward/Reflected Power

The cavity voltage is determined by the forward and reflected waves at the load:

$$V_c = V_{forw} + V_{refl} \tag{2.33}$$

In this section the beam current will be taken into account. In Fig. 2.3, it is represented by I_B, with a magnitude I_b and a beam phase ϕ_0 with respect to the generator phase.
According to the dissertation by Sergey Belomestnykh, reported for the sake

of clarity in appendix A, the forward voltage, the reflected voltage and the forward power are respectively:

$$V_{forw} = \frac{I_b R/QQ_{ext}}{2}(\cos(\phi_0) + j\sin(\phi_0)) + \frac{V_c}{2}\frac{\beta+1}{\beta}(1 + j\tan\Psi') \tag{2.34}$$

$$V_{refl} = -\frac{I_b R/QQ_{ext}}{2}(\cos(\phi_0) + j\sin(\phi_0)) + \frac{V_c}{2}\frac{\beta+1}{\beta}\left(\frac{\beta-1}{\beta+1} - j\tan\Psi'\right) \tag{2.35}$$

$$P_{forw} = \frac{V_c^2}{4R/QQ_{ext}}\frac{(\beta+1)^2}{\beta^2}\left[\left(1 + \frac{I_b R/QQ_L}{V_c}\cos(\phi_0)\right)^2 + \left(\tan\Psi' + \frac{I_b R/QQ_L}{V_c}\sin(\phi_0)\right)^2\right] \tag{2.36}$$

with

$$\tan\Psi' = 2Q_L\frac{\Delta\omega}{\omega} \tag{2.37}$$

where Q_L is the loaded Q factor and $\Delta\omega$ is the cavity resonance detuning from the RF frequency.

3 Radio Frequency Control Design

3.1 Introduction

Radio frequency control, as applied to Linacs, generally implies the measurement of the key parameters of the RF field (amplitude, phase and frequency) and the processing of those parameters formalized to its regulation. The smart I/O controller discussed here, is the embodiment of the above concepts with the task of controlling and maintaining a specified phase, amplitude and frequency stability of the electric field in QWR cavity during beam transport, despite the presence of different kinds of perturbations. The cavities act as filters, with an extremely huge Q due superconducting conditions. They exhibit a narrow frequency bandwidth and their capacity to store energy decreases rapidly when moving away from the resonance frequency. Hence it becomes essential to extend the frequency range to compensate small perturbations that have frequencies from a few Hz up to some KHz. These perturbations have to be compensated by the low level RF control system. This chapter details the main sources of disturbances, the influence on the field regulation, the compensation used, the key components of a general RF application and the choices that have been taken to implement the components of the LLRF control system.

3.2 Sources of Disturbances

The basic disturbances affecting a superconducting cavity working in a CW Linac are:

- beam loading;
- static Lorentz Force Detuning (LFD);
- microphonics;
- slow frequency drift.

Tuning, compensation	Type
Very slow	**Quasi-stastic, pre-tuning**
	Niobium plunger
	Three stub tuner
	Pneumatic bellows
Slow	**< 1Hz, compensation of Helium pressure fluctuation and beam loading**
	Warm motor + lever + tuning plate
	Cold motor driven lever
Fast	**Microphonic and LFD compensation**
	None / overcoupling
	Variable reactance
	Mechanical with piezo actuator

Table 3.1: Compensation type. [13]

These disturbances belong to two groups: the repetitive ones and the non-repetitive ones. The repetitive components are regular and can be fixed by a feedforward control. Non-repetitive disturbances are not predictable and they have to be compensated by a feedback controller. The main disturbance contributions are described in the next sections.

Depending on the frequency of the disturbances, the tuning and the compensation can be done in different ways as summarized in Tab. 3.1.

3.2.1 Beam Cavity Interaction

When bunches cross the cavities they transfer electromagnetic energy to the field resonating in cavity. These phenomena are described in terms of wake-fields [13]. Long range wake fields, or Higher Order Modes (HOMs), lead to a longitudinal and transverse emittance spread. If the HOMs do not decay sufficiently between bunches, fields from subsequent bunches can interfere, causing various instabilities. In order to obtain the total cavity voltage at the fundamental frequency, taking account of the beam cavity interaction, we need to consider the beam induced voltage. This was already done in the previous chapter and in appendix A. In equation 2.36 the two terms correspond to active and reactive parts of the beam loading. This disturbance depends on the beam current magnitude, the repetition rate, amplitude and phase of the particle beam with respect to the RF field phase in cavity. Usually these parameters remain unchanged during operation, e.g. they can be classified as a repetitive disturbance source.

3.2.2 Lorentz Force Detuning

The Lorentz force detuning (LFD) is another repetitive disturbance. The electromagnetic field exerts forces on thin cavity walls, changing its geometry. The entity of the changes is proportional to the electric and magnetic energy stored in the cavity. The detuning represents a constant drift of the cavity eigenfrequency. If the system operates in CW mode, the detuning reaches a final steady state when the induced deformations and the stiffness of the cavity match. To overcome this problem one could simply detune the cavity by the RF field induced frequency shift.

3.2.3 Microphonics

Microphonics are mechanical vibrations of cavity's wall, excited by external factors as in the cooling system, vacuum pumps and motors. Usually these disturbances oscillate within few hundred hertz. These mechanical vibrations perturb the cavity shape, moving its eigenfrequency, as shown in Fig. 3.1. The small changes in the resonance frequency, due to the high Q, have a non negligible effect on the field, since the RF drive frequency is fixed. Therefore the field magnitude decreases and its frequency shifts with respect to the reference. These detuning consequences must be compensated by the feedback controller.

3.2.4 Slow Frequency Drift

Generally, slow frequency drifts are identified with the pressure fluctuation in the cryogenic system. Helium pressure in cryostats fluctuates causing pressure changes on the cavity walls, which induces detuning of the resonant frequency. This disturbance source changes in a slow time scale and is not predictable. This can be classified as a non-repetitive disturbance source.

3.3 Disturbances at LNL

In the previous section the main disturbances have been described. In this section the impact of these disturbances is evaluated in order to understand

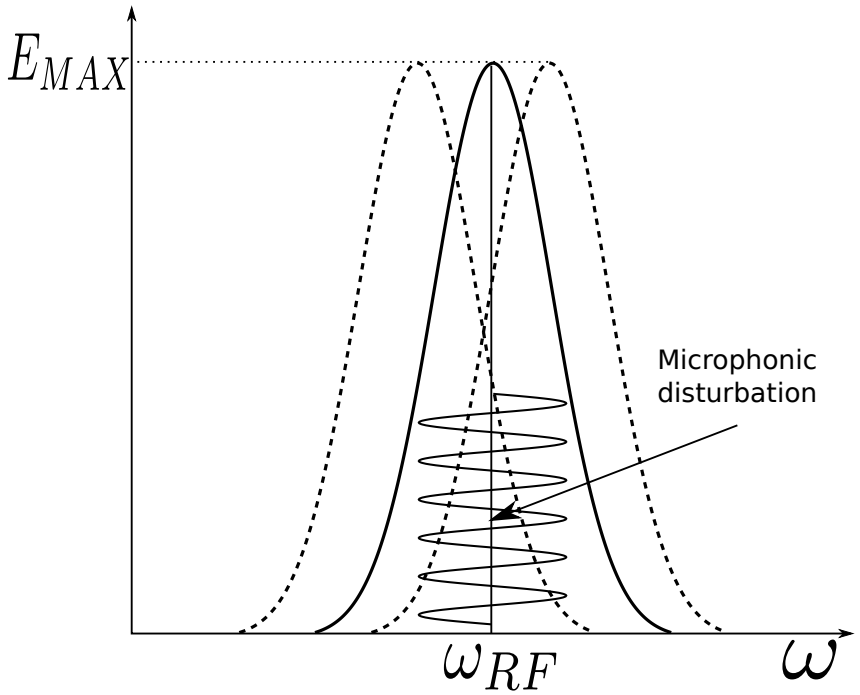


Figure 3.1: Microphonics effects on cavity resonance frequency.

why a mechanical frequency tuning control and an electronic feedback for field control are necessary.

3.3.1 Beam Cavity Interaction

Combining equations 2.36 and 2.37, one can see that in order to compensate the reactive part of the beam impedance, the cavity has to be detuned in such a way that:

$$I_b R/Q Q_{ext} \sin(\phi_0) + V_c \frac{\beta + 1}{\beta} \tan \Psi' = 0 \tag{3.1}$$

$$\Delta\omega = -\frac{I_b R/Q \omega sin(\phi_0)}{2V_c} \tag{3.2}$$

Substituting in equation 3.2 the values in table 1.1 and knowing that the typical beam current at LNL is in the order of tens to hundred nA, one finds that:

$$\frac{I_b R/Q \omega sin(\phi_0)}{2V_c} \approx \frac{1}{100}$$

Therefore the beam interaction with respect to the accelerating field in the cavity is negligible .

3.3.2 Lorentz Force Detuning

The QWRs used are mechanically stable and thanks to their symmetric and circular structure they have a satisfactory stiffness. The frequency detuning due to the Lorentz force detuning it has been measured to be:

$$\frac{\Delta f}{E_a^2} = 1\frac{Hz}{(MV/m)^2} \tag{3.3}$$

Furthermore Lorentz force detuning is almost constant during operation since the Linac is operated in cw mode. Therefore the frequency drift due to LFD is an offset that can be neglected for a feedforward compensator.

3.3.3 Microphonics

With microphonics we mean mechanical vibrations of the cavities in the range of few Hz to hundreds of Hz. As described in table 3.1, these frequency disturbances are compensated by overcoupling the QWR cavity to enlarge its bandwidth and through the RF power injected in the cavity (equation. 3.4). To perform this compensation the power amplifiers have an extra power budget. The power dissipated in the cavity to keep the gradient field for a correct acceleration is $P_c \approx 7W$. Low beta cavities are excited by 1 KW power amplifiers, meanwhile medium and high beta ones are excited by 100 W power amplifiers. The forward power sourced by the power amplifier is:

$$P_{forw} = \frac{V_c^2}{4R/Q_0 Q_{ext}} \frac{(\beta+1)^2}{\beta^2} \left[1 + \left(2Q_L \frac{\Delta\omega}{\omega}\right)^2\right] \tag{3.4}$$

It was obtained from eq. 2.36 without considering the beam load. The dependence of the forward power depending on the frequency detuning in a low beta cavity is shown in Fig. 3.2.

So using only an electronic feedback control we can compensate microphonic disturbances that detune the cavity resonance frequency up to 200Hz.

3.3.4 Slow Frequency Drift

In superconducting cavities, slow frequency drifts are basically due to pressure changes Δp in the liquid helium bath. The medium and high beta SRF

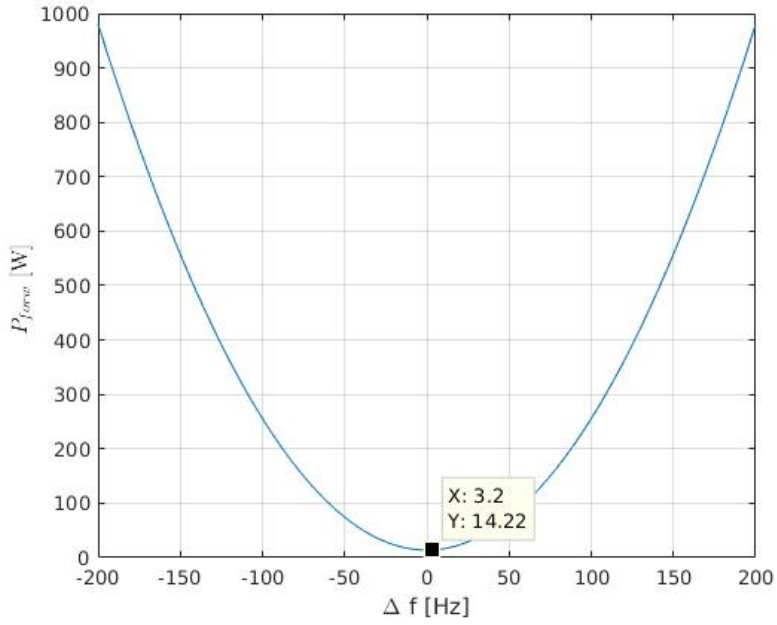


Figure 3.2: Forward power vs. detuning frequency for a low beta cavity.

cavities exhibit a shift of their eigenfrequency due to Δp of:

$$\frac{\Delta f}{\Delta p} = \frac{1}{100}\frac{Hz}{mbar} \tag{3.5}$$

while the low beta cavities:

$$\frac{\Delta f}{\Delta p} = 1\frac{Hz}{mbar} \tag{3.6}$$

The pressure in the helium tank is stabilized at 50 mbar and in typical working condition there can be a pressure variation of 5 mbar/min. Hence, looking at the table 3.1, we need a slow compensation system. This is accomplished using warm motor + lever + tuning plate, e.g a mechanical tuning.

3.4 RF Key Components

Each LLRF controller can control at the same time up to eight cavities. The RF signals picked up from the cavities are sampled by RF ADCs. The digitized signals are fed into a field programmable gate array (FPGA) which implements the control loop. The signals processed by the FPGA are in-phase/quadrature modulated and sent to power amplifiers and hence to the cavities. The main feature of the new control system is an all digital control

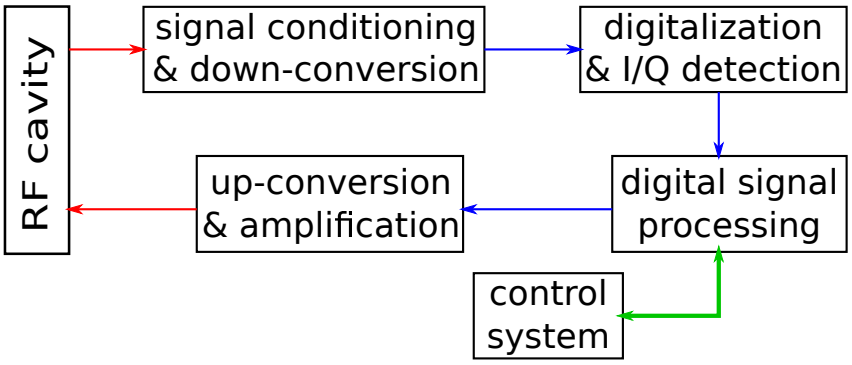


Figure 3.3: Key components of a digital RF application.

loop that originates from direct sampling of the antenna RF signal. In-phase and quadrature components are obtained by a suitable choice of the undersampling frequency, while control of the amplitude and phase field in the cavity is based on a digital Complex Phase Modulator (CPM).

Fig. 3.3 shows the main blocks of a LLRF control application. In the next sections, the key aspects of the LLRF controller implementation and programming are analyzed.

3.5 The Undersampling Technique

Signals picked up from the cavities are affected by disturbances whose frequencies are much lower with respect to the eigenfrequency of the cavity. The detection of the components will be illustrated in this section.
The maximum Nyquist frequency available with the Analog Digital Converters (ADC) can be smaller than the RF frequencies of interest. The RF signal frequencies, in the context of this work, lie in the second or third Nyquist zone. The idea behind undersampling technique is sample the RF signals in order to obtain a replica of the signal at baseband, without requiring an additional down-conversion [16].
In order to extract the I/Q information from the samples, the sampling frequency f_s for a correct down-conversion, has to be chosen following the relations [17]:

$$f_s > 2B \tag{3.7}$$

$$f_s = \frac{4f_{RF}}{2 \cdot N - 1} \tag{3.8}$$

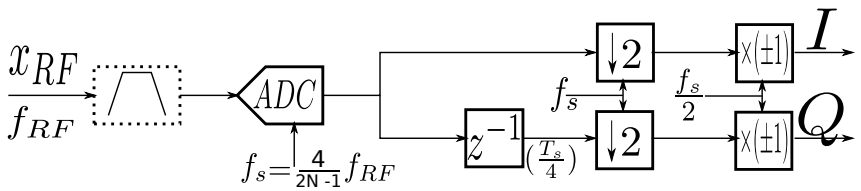


Figure 3.4: Block diagram of an I/Q demodulator.

where f_{RF} is the resonance frequency of the cavities and B the bandwidth of the RF signal. These conditions ensure that a non overlapped alias will appear centred at $f_s/4$. In our study, the inequality 3.7 is always met.

Conceptually the digitalization of the signal works as in Fig. 3.4.

The RF signal, if needed, is band-pass filtered in order to avoid aliasing effects. Then it is sampled directly with an ADC operating at a frequency as described in equation 3.8. The ADCs generate a digital sequence of I, Q, -I, -Q etc. This stream of values is separated into a data stream of I and Q components, respectively, by an I/Q demodulator (Fig. 3.4). The alternating signs are removed otherwise the CORDIC algorithm (section 5.8.2) can have ambiguities during signal processing. The output signals are the I and Q values [18].

The drawback of this technique is that for signals sampled outside the first Nyquist zone, the clock and aperture jitter have a larger impact on the resulting error.

3.6 Cavity Control

The basic functionality of a feedback control system is illustrated by Fig. 3.5. The controlled system (plant) can be affected by several disturbances. The controlled variable is compared to the set-point by estimating the difference between the plant output and the set-point. The resulting difference is called tracking error. The controller derives the control signal from the tracking error and sends it to the actuator to control the system.

The main requirements in the design of a control system are:

- stability;
- rejection of disturbances and noise effects;
- ability to track the reference signal.

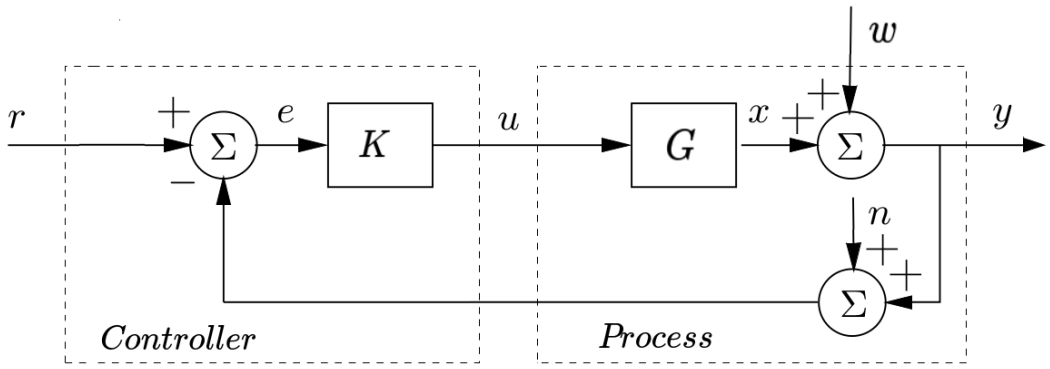


Figure 3.5: Block diagram of a basic feedback loop.

The feedback loop in Fig. 3.5 can be modeled with three inputs: the reference r, the plant disturbance w and the measurement noise n. So it is possible to write three relations between the inputs and each output signal. In the context of this work, the control is optimized for the measured signal y, that is proportional to the field resonating in the cavity, but also the tracking error e is of great interest for control. These two signals are studied as outputs of the system.

The system of Fig. 3.5 is linear, therefore the relation between inputs and outputs can be expressed in terms of the transfer functions. Let $Y(s)$, $E(s)$, $R(s)$, $D(s)$ and $N(s)$ the Laplace transforms of y, e, r, d and n, respectively. The two transfer functions are:

$$\begin{aligned} Y(s) = \frac{1}{1+K(s)G(s)}W(s) + \frac{K(s)G(s)}{1+K(s)G(s)}(R(s)-N(s)) = \\ = S(s)W(s) + T(s)(R(s)-N(s)) \end{aligned} \tag{3.9}$$

$$\begin{aligned} E(s) = \frac{1}{1+K(s)G(s)}(R(s)-N(s)-W(s)) = \\ = S(s)(R(s)-N(s)-W(s)) \end{aligned} \tag{3.10}$$

where $S(s)$ is the so called sensitivity transfer function and $T(s)$ the complementary sensitivity transfer function. Indeed:

$$T(s) + S(s) = 1 \tag{3.11}$$

Feedback control has to attenuate both the disturbance and noise signals respect to the measured signal $Y(s)$. In order to reduce the importance of the measurement error $N(s)$, $T(s)$ should be small, while in the other hand to reduce the importance of the plant disturbances $W(s)$, $S(s)$ should be

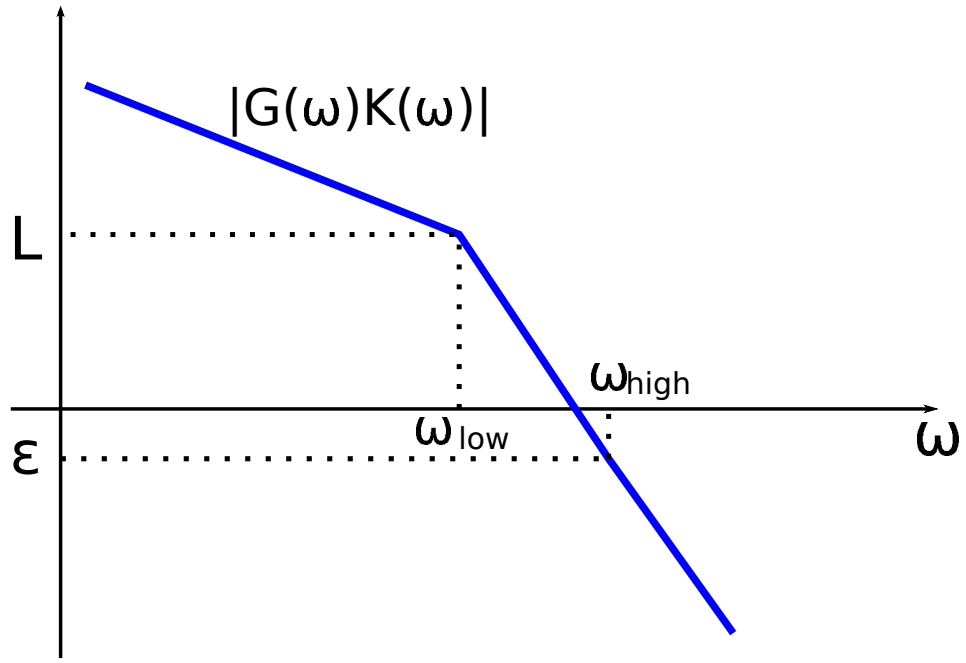


Figure 3.6: Open loop shape of the transfer function given by the cascade between controller and RF cavity model in resonance.

small. The trade-off to consider is between attenuation measurement errors and plant disturbances. Since, usually, the plant disturbances lie at low frequencies (i.e. microphonics), while measurement errors typically have higher frequencies (i.e. crosstalk in RFFE input channels, see section 7.2.4) the conflict between $T(s)$ and $S(s)$ is solved by making the former small at some frequencies and the latter small at other frequencies. The controller frequency behavior ($K(s)$) is shaped in such a way to have $S(s)$ small at low frequencies and $T(s)$ small at higher frequencies.
$|S(j\omega)|$ small implies $|K(j\omega)G(j\omega)| = L >> 1$ at low frequencies, $|T(j\omega)|$ small implies $|K(j\omega)G(j\omega)| = \varepsilon << 1$ at high frequencies. Furthermore, for a good stability margin, a rule of thumb requires a gain margin of at least 10 dB and a phase margin of at least 45 degrees. Other conditions may be required, e.g. a zero steady state error despite of step disturbances.
The cavity transfer function G(s), as defined in equation 2.29, at resonance ($\Delta\omega = 0$), it behaves like a first order low-pass filter; the shape of $|K(j\omega)G(j\omega)|$ is represented in Fig 3.6. The controller chosen is a proportional-integral PI controller.

An important parameter to consider in the design of the controller is the delay of the control ring. A delay in the time domain is transformed in

Laplace domain as $f(t-\tau) \rightarrow F(s)e^{-s\tau}$.

$$e^{-s\tau} = \frac{1}{e^{s\tau}} \approx \left(\frac{1}{1+\frac{s\tau}{n}}\right)^n \tag{3.12}$$

That is, the delay for the stability analysis can be considered as multiple poles at high frequency; this means that the delay limits the feedback gain and reduces the stability margins.

3.7 Cavity Mode of Operation

The cavities can be excited in two ways. The choice depends primarily on the cavity bandwidth and which disturbances are concerned. In the so called Generator Driven Resonator (GDR) mode, the RF field sourced by a frequency generator is fed into the cavity and there is the possibility to choose the desired magnitude and phase field in cavity.
On the other hand, in the Self Excited Loop (SEL) mode, the controller, the power amplifier and the cavity resonator form a closed loop that, under adequate conditions, oscillates at a frequency determined essentially by the cavity parameters.

Different loaded quality factors of the cavities (and so different bandwidths) make different control algorithms necessary. Superconducting cavities with an high Q, are susceptible to microphonics, that cause great fluctuations with respect to the cavity bandwidth; hence the controller has to operate much faster. This is usually accomplished with the SEL algorithm.
The GDR is normally used to control resonators where their resonance frequency keeps close to the operating frequency, that is within their bandwidth. For example, room temperature resonators like the high energy bunchers are controlled in GDR mode. The following sections describe how these algorithms work.

3.7.1 Generator Driven Resonator

In GDR mode (see Fig. 3.7) the signal picked up from the cavity is compared with the reference signal phase. The phase and amplitude signals, obtained through the in-phase and quadrature decomposition, are compared with the respective set-points. The resulting tracking errors are multiplied by

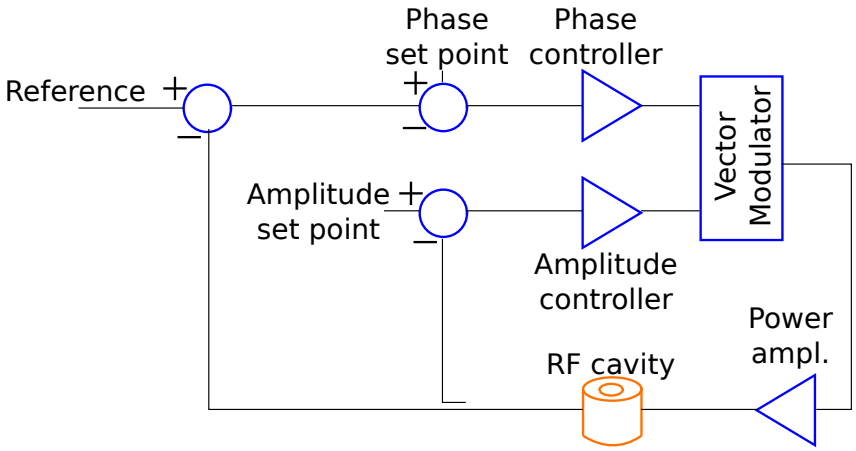


Figure 3.7: Block diagram of a cavity controlled in GDR.

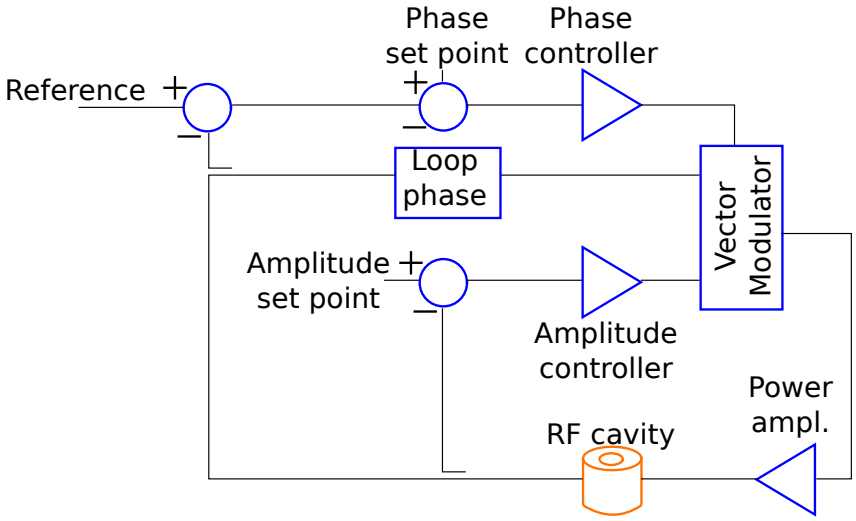


Figure 3.8: Block diagram of a cavity controlled in SEL.

appropriate control gains and the signals so obtained are used to drive the power amplifier and hence the cavity.

3.7.2 Self Excited Loop

The cavity works in a closed loop. The loop contains an amplifier, the cavity, and a phase shifter. In the presence of enough high gain and a loop phase of 2π (or multiples of it) the loop starts oscillating. The cavity acts as a narrow band-pass filter and thereby filters out everything, except the resonance frequency.
Essentially the cavity is locked to the phase of the external reference signal. If the phase between cavity output and input is modified through the phase shifter, the cavity must change its phase in order to keep the ring phase

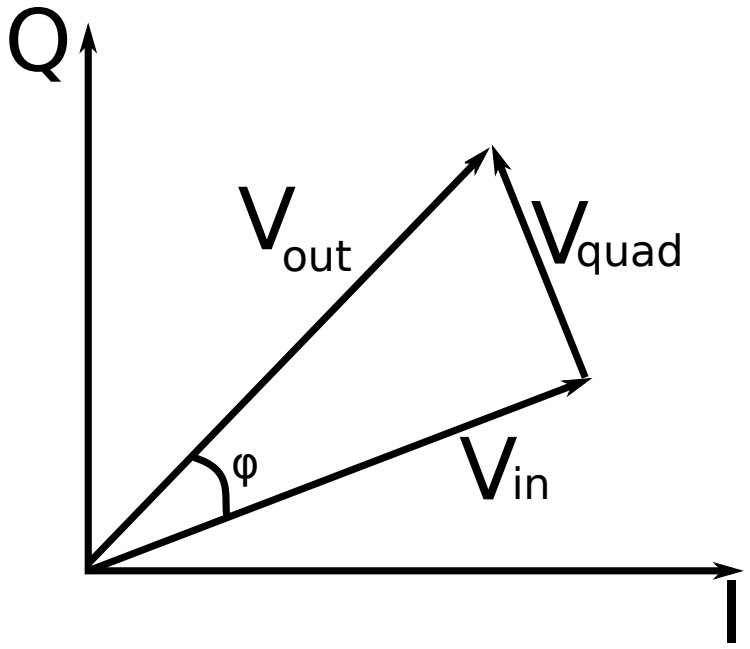


Figure 3.9: CPM working.

constant. A change in the phase means for the cavity a move of the working point along the resonance shape, that is a change of the resonance frequency. The drawback of this technique is that there is a crosstalk between the phase correction and the amplitude correction, since when the cavity moves along the resonance shape the field amplitude changes accordingly. That is why it is mandatory insert a CPM: the CPM adds a correction vector (as shown in Fig. 3.9) in quadrature to its input vector that is proportional to the phase error and therefore corrects for phase and magnitude errors caused by a detuned cavity.

3.8 Analog/Digital Conversion

The input downsampling process can be reversed to produce the RF output. Fig. 3.10 shows conceptually how the up-conversion works. In section 3.5, it was described how a Direct Down Conversion (DDC) system samples in-phase and quadrature components (I and Q) of the signal at the sampling frequency given by the equation 3.8. Similarly, digital up-conversion feeds a digital to analog converter (DAC) at the same sampling frequency of the ADC. The I and Q signals are multiplied by +1 and -1 alternately before being multiplexed and converted to the analog domain. A typical output of

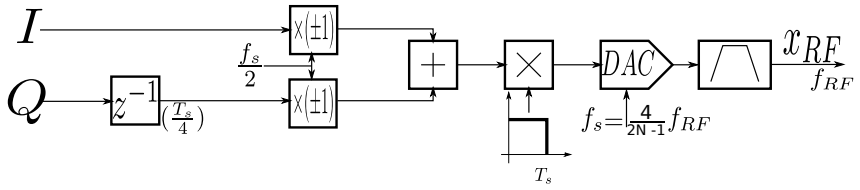


Figure 3.10: Block diagram of an I/Q modulator.

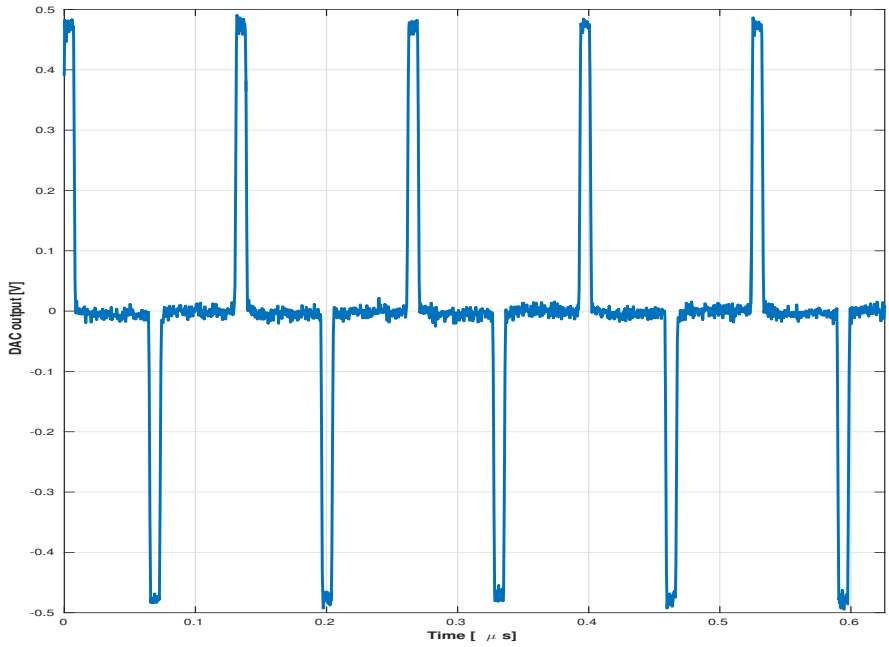


Figure 3.11: Typical DAC output in time domain.

the DAC in time domain is reported in Fig. 3.11. The quadrature components are updated at the same rate and series of harmonics are generated. The DAC generates spectral lines at $f_s/4$ and at $(2 \cdot N - 1)f_s/4$, with N = 2,3,4 ...., as shown in Fig. 3.12. The signal of interest is at frequency f_{RF} and by filtering out this frequency we get the controlled signal variable. The drawback of this technique is that the harmonic of interest has a small energy content and the filtering requirements are matched only by the use of an analog band-pass filter with narrow and sharp bandwidth.

3.9 Mechanical Tuning

In this document by mechanical tuning we refer to the frequency tuning done by slow tuners. The tuners are mechanical systems that deform the cavity walls or bottom plates forcing to resonate at the desired resonance

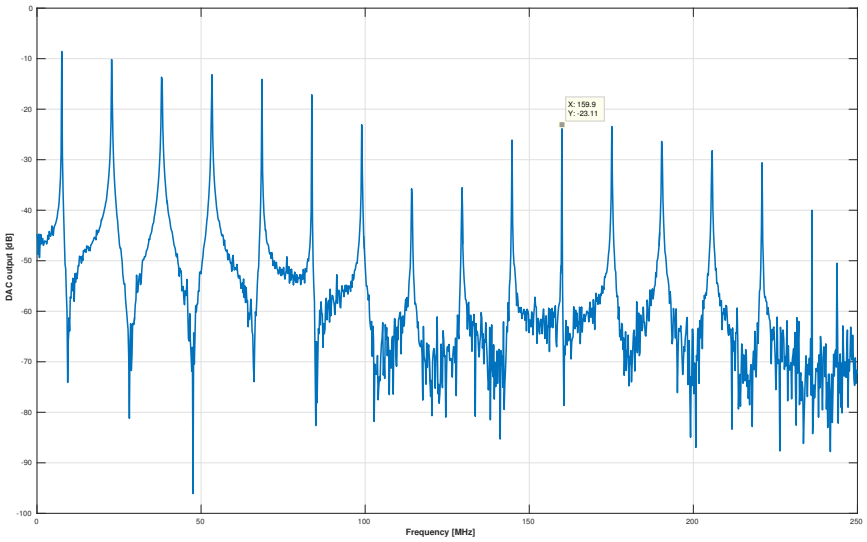


Figure 3.12: DAC output spectrum. The marker indicates the f_{RF}.

frequency f_0. When the linear accelerator operates, they guarantee the frequency compensation due to slow frequency drift. Tuners, but in general can be of different types, used in QWR cavities rely on the deformation of the lower plate of the cavity using a motor. As sketched in the previous chapter, the QWR cavity is essentially a coaxial line short-circuited at one end. The equivalent circuit, shown in Fig. 2.3, is formed by the lumped elements of a coaxial line, whose values are:

$$C = \frac{2\pi\varepsilon}{ln(r_2/r_1)} \quad L = \frac{\mu}{2\pi} ln(r_2/r_1) \quad R = \frac{R_c}{2\pi}\left(\frac{1}{r_2} + \frac{1}{r_1}\right) \tag{3.13}$$

where R_c is the surface resistivity of conductor. The circuit resonates at a frequency $f_0 = 1/2\pi\sqrt{LC}$.

At the opposite end of the short-circuited end, the cavity is closed through a plate, whose geometry can be deformed by the tuning mechanism. This plate and the central inductor form the two armatures (placed at distance d « l, as shown in Fig. 1.5) of the load capacitor C_L, which is in parallel with the capacitor C. The equivalent capacitor is then:

$$C_{eq} = \frac{C \cdot C_L}{C + C_L} \tag{3.14}$$

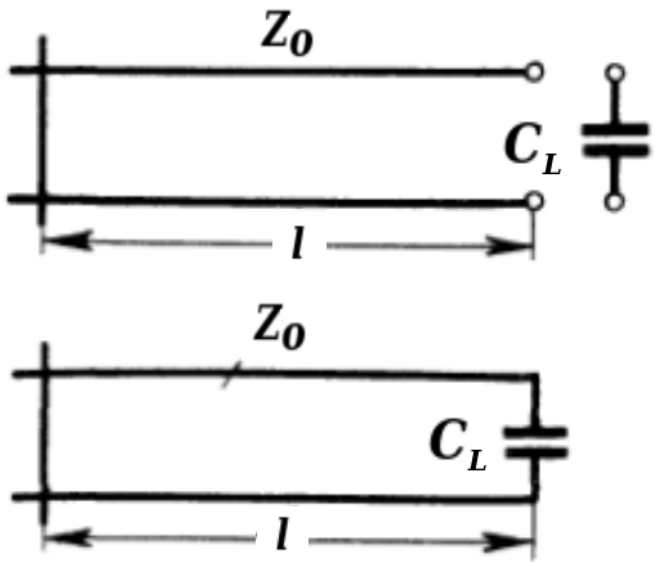


Figure 3.13: QWR line transmission capacitance with and without the load capacitance.

So that the resonance frequency of the QWR becomes:

$$f_0 = \frac{1}{2\pi} \frac{1}{\sqrt{LC_{eq}}} \tag{3.15}$$

Therefore when the slow tuner deforms the lower plate, it actually changes the loading capacitor C_L, hence the C_{eq} and finally the resonance frequency f_0. In our case the slow tuner used for low beta cavities is a lever tuner, actuated by a standard stepper motor. It is capable of a resolution better than 0.33 mm (equivalent to 1 Hz frequency steps), with a tuning range close to 30 KHz and with a very small and constant backlash.

4 The Radio Frequency Controller

4.1 Introduction

In a particle accelerator the RF controller is the core of the LLRF system. It implements the LLRF control. It processes the signal picked up from the cavity to guarantee a stable operation, besides providing the user interface to set and get live parameters. The core of the controller is a collection of analog and digital electronics boards which control the loops from the cavities to the RF amplifiers, provide constant phase and amplitude of the RF field in the gap despite the presence of perturbations coming from the external environment. The digital signal processing is performed in a field programmable gate array (FPGA), that also computes the parameters needed to control the resonance frequency of the cavities modifying their shape.
This chapter highlights the main tasks of the RF controller and of the boards composing the controller emphasizing the choices taken during the design phase. A high level outline of the boards components and connections is presented, detailing some of their main features.

4.2 Low Level Radio Frequency Functionalities

The RF controller is in charge of:

1. matching the power level of the signals picked up from the cavities to a suitable value to be sampled by RF ADCs;
2. undersampling these signals at frequency f_s (sec. 3.5) and hence extracting the in-phase and quadrature RF field components;
3. implementing the digital signal processing in according to the selected cavity driving mode (sec. 3.7) and the cavity control algorithm parameters (sec. 3.6);

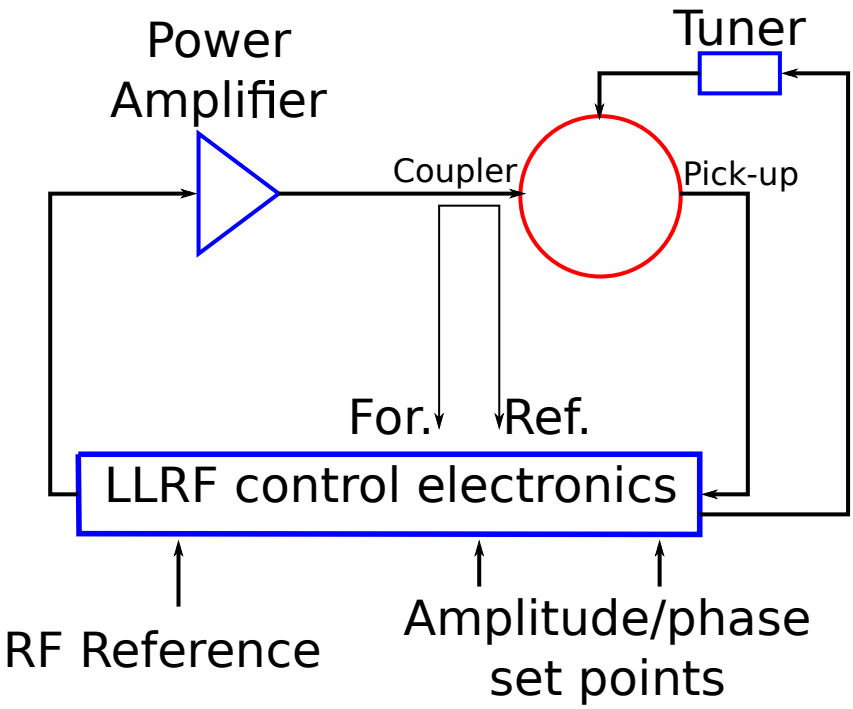


Figure 4.1: Typical LLRF control system.

4. up-converting the in-phase and quadrature components of the signal modulated through the PI controllers;
5. filtering through a narrow band-pass filter and then amplify the signals coming from the DACs (sec. 3.8);
6. distributing the clock locked with the master facility oscillator to the components that need it;
7. measuring the forward and the reflected power of the eight controlled cavities (sec. 2.6);
8. monitoring some analog signals through the inspection channels (sec. 4.4.3);
9. providing the interface for the slow control with the particle accelerator control system.

4.2.1 The Octal Resonator Controller Box

The functionalities listed above are implemented by means of several electronic boards and components. In detail points 1 and 5 are taken care by by the Radio Frequency Front End (RFFE) board (sec. 4.4) and the Helical Resonator filters (sec. 4.5), points 2, 3, 4, 6 and 9 are implemented by the

Figure 4.2: Octal Resonator Controller (front view). On top the RF IOC.

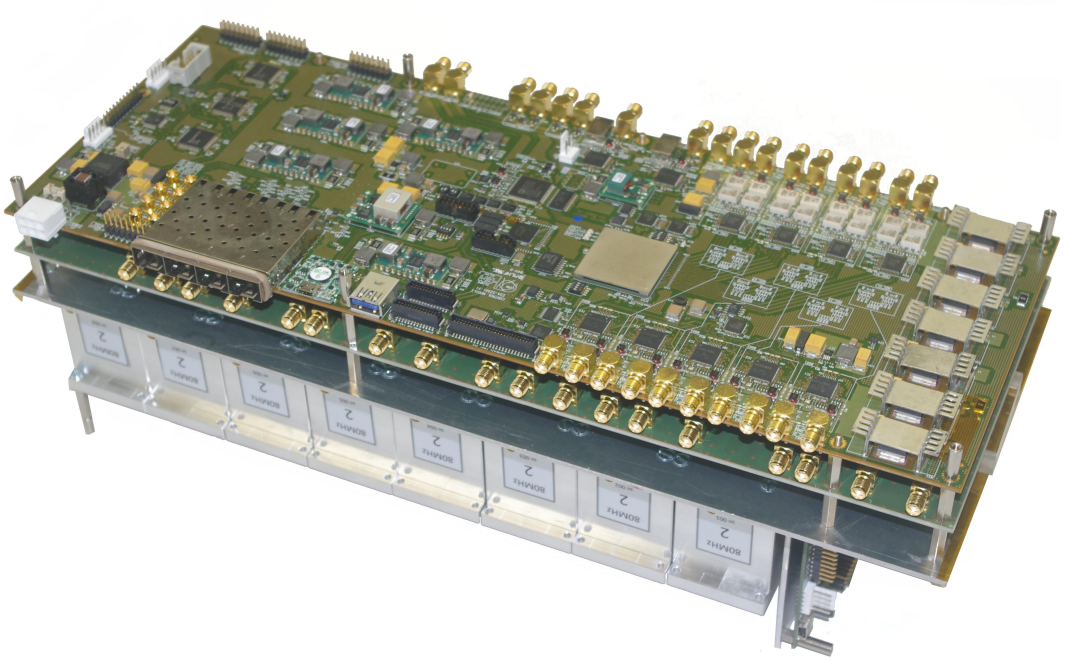


Figure 4.3: Contents of the ORC box. On top there is the RF IOC and below the RFFE.

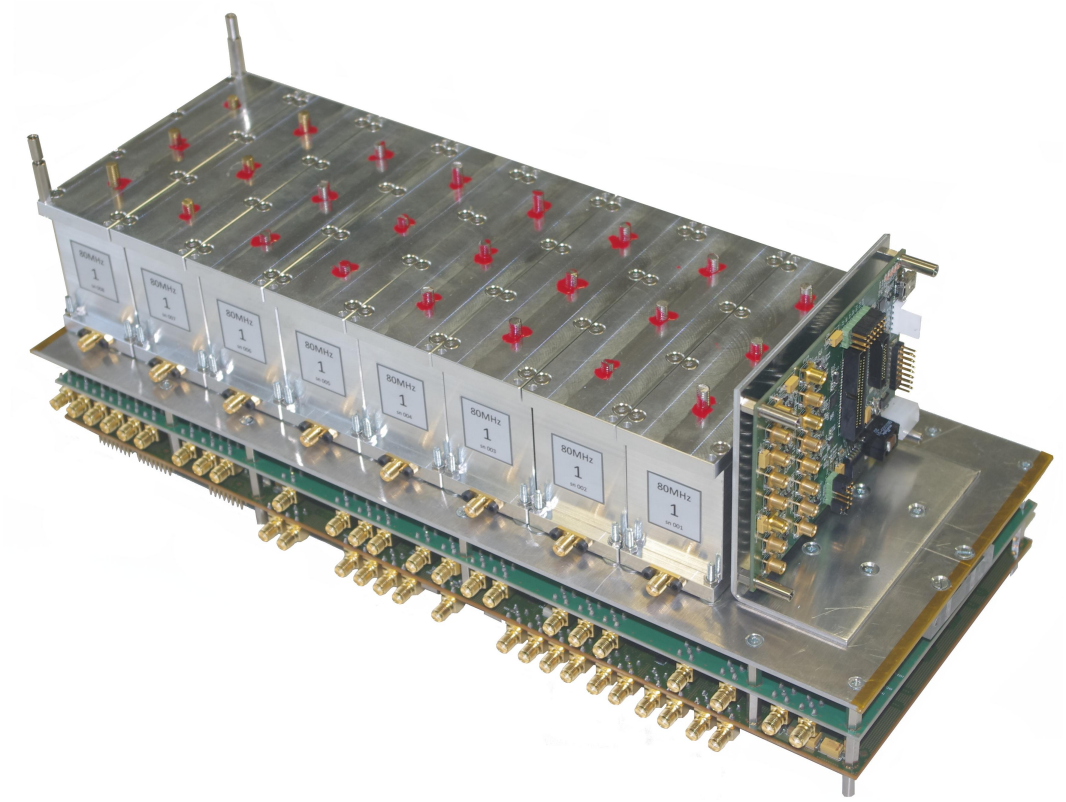


Figure 4.4: Contents of the ORC box. On top there are eight helical filters and the PM.

Radio Frequency Input/Output Controller (RF IOC) (sec. 4.3), point 7 is realized by the Power Monitor (PM) board and point 8 is achieved using two DRS4 evaluation boards [19]. All these boards and components are housed in a unique box called Octal Resonator Controller (ORC) box, Fig. 4.2. An high level outline of these components and boards and connections is represented in Fig. 4.5

4.3 The Radio Frequency I/O Control Board

The digital RF Input/Output Controller (RF IOC) is represented in Fig. 4.6. Each RF controller controls up to eight cavities at the same time. It is essentially composed of four high linearity dual channel RF ADCs, a Xilinx Kintek 7 FPGA in which the LLRF logic is implemented using VHDL code and four high speed, high performance dual channel DACs. Both ADCs and DACs support a JESD204B [20] compatible high speed serial input data interface. The clock signals are generated by two clock jitter cleaners (PLLs). ADCs, DACs and PLLs feature an SPI slave interface to access their internal

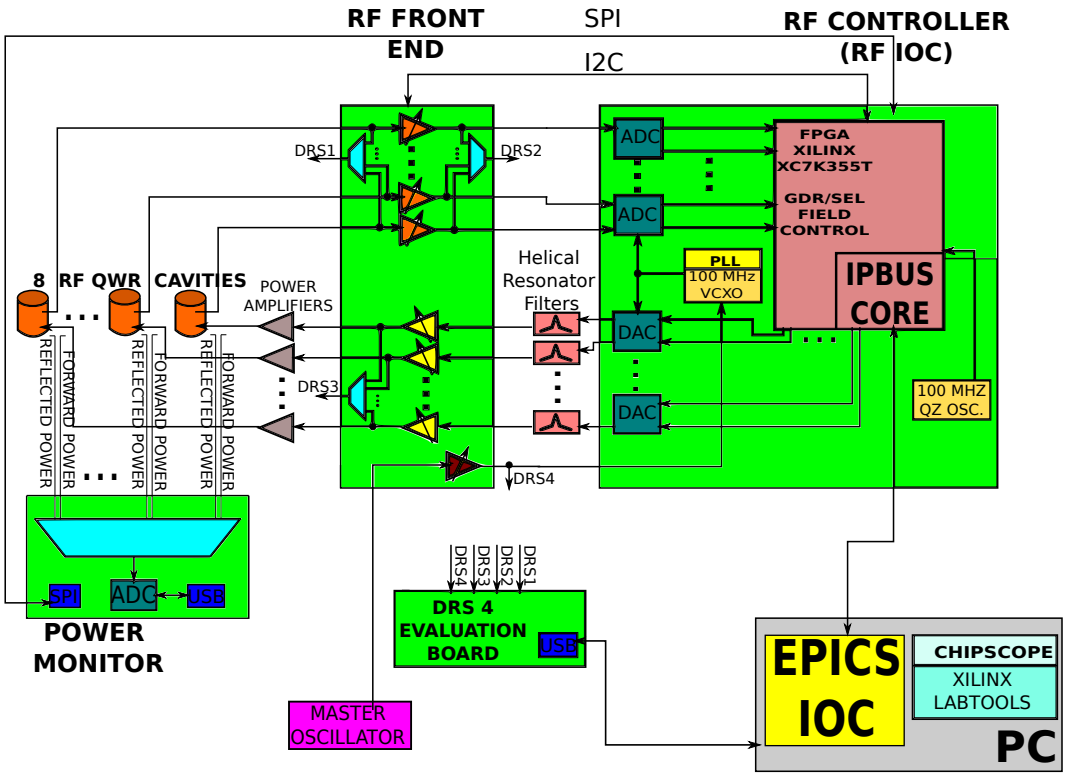


Figure 4.5: Block diagram of the ORC.

registers. Each PLL can drive up to seven JESD204B compatible converters. The slow control is realized through the IPbus protocol [21], [22]. These features of the RF IOC board are detailed in the next sections.

4.3.1 Analog Digital Converters Requirements

The ADC characteristics are mostly determined by the accuracy required in the working points of the phase and amplitude field in cavity. For a modern heavy ion Linac like ALPI, it is required a phase of at least $0.5°$ and a gradient accuracy of about 0.5% rms. From these values we can derive the specifications for signal to noise ratio (SNR) for the ADC [23].

The magnitude error holds:

$$SNR_{Mag} = -20 * \log(Err_{\text{MAGNITUDE}}) \tag{4.1}$$

while the phase error holds:

$$SNR_{Ph} = -20 * \log(\sin(45° + Err_{\text{PHASE}}) - \cos(45°)) \tag{4.2}$$

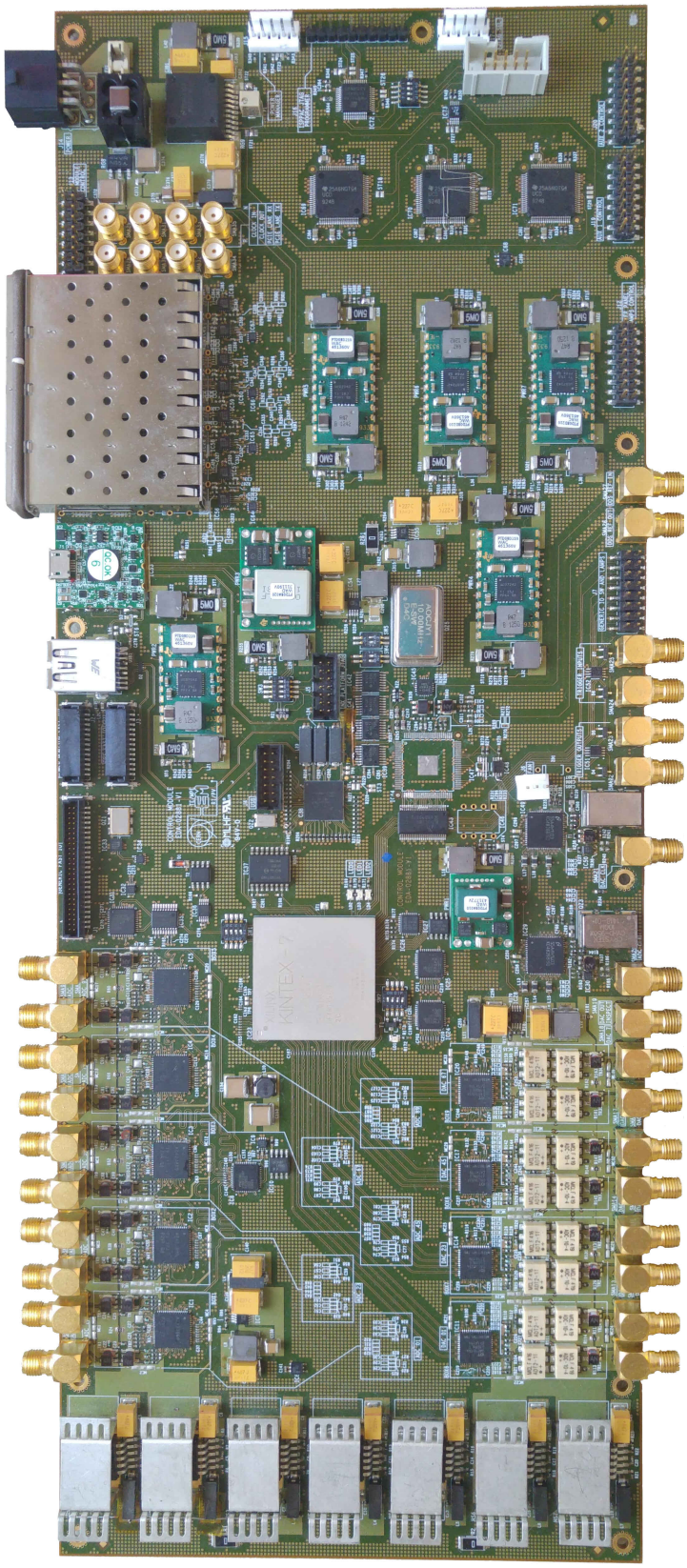


Figure 4.6: RF IOC board.

To evaluate the SNR due to the phase error, we need to derive the amplitude difference between the in-phase I and quadrature Q components, the worst case is when the magnitude of I is equal to the magnitude of Q, i.e. when the field phase is $45°$. The SNR requirement has to be kept in the whole gradient dynamic range $|E_{MIN}| \rightarrow |E_{MAX}|$, that in ALPI typical configurations is $|E_{MIN}| = 3.5$ MV/m in a low beta cavity and $|E_{MAX}| = 5$ MV/m in a medium beta cavity. Hence the ADC must have a SNR_{ADC} greater than:

$$SNR_{ADC} \geq \max(SNR_{Mag}, SNR_{Ph}) + 20 * \log(\frac{|E_{MAX}|}{|E_{MIN}|}) \tag{4.3}$$

where $20 * \log(\frac{|E_{MAX}|}{|E_{MIN}|}) \approx 3$ dB.

A gradient stability of 0.5% rms means a $SNR = -20\log(0.005) = 46$ dB. In the other hand the phase requirement is $0.5°$. This implicates for example a $SNR = -20 * \log(sin(45 + 0.5) - cos(45)) = 44.2$ dB.
The SNR of an ideal ADC is given by the following equation:

$$SNR_{ADC} = 6.02 * N + 1.76 \tag{4.4}$$

This means that our ADC has to have at least an equivalent number of bit equal to $ENOB = (SNR_{ADC} - 1.76)/6.02 = 7.9 \rightarrow 8$, with $SNR_{ADC} = 46 + 3 = 49$ dB. Furthermore, other factors are included into the SNR computation. In DDC the clock jitter is one of the most important issue, as the ADC input frequency is increased, the SNR decreases primarily because of clock jitter.
In the ultimate configuration, the RF IOC has to be able to sample RF signals spanning up to 352 MHz, hence the SNR of 49 dB must be guarantee also at this frequency.
The requirements for the DACs are not so tight as for the ADCs. Since they are in the feedforward path of the control loop, the signal errors are small in comparison to power amplifier contributions and disturbances described in the previous chapter.

4.3.2 Communication Between Converters and FPGA

The RF IOC controls at the same time eight cavities, by housing eight ADCs and eight DACs; all these converters have to communicate with a single FPGA at high speed. Moreover, to directly sampling the RF spectrum at

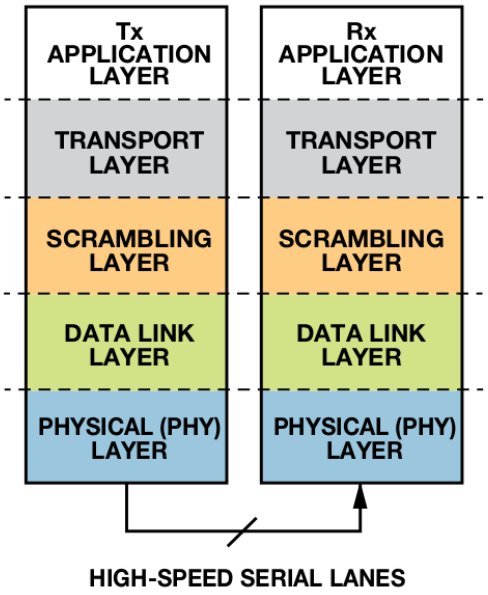


Figure 4.7: OSI model implemented by JESD204B protocol.

moderately high frequencies GSPS ADCs are necessary. The JESD204B protocol has been designed to address these issues by exploiting high speed serial links and actually the standard supports serial data rates up to 12.5 Gbps.

The use of JESD204B presents some key benefits: e.g. the reduction of the number of synchronous digital lines by serializing their activity onto high speed lanes with balanced codes and embedded clock. The reduced number of high speed differential lanes on the PCB dramatically reduces its complexity and the Simultaneous Switching Noise (SSN) due to the fast synchronous commutation of many digital signals (in our case the number of tracks has been reduced from 16 to 4 for each converter). The improvements come at the expense of increased speed of serial lanes and the forced use of complex electronics for serialization and deserialization. There are some drawbacks to this standard interface: the two most dominant are an increased link latency and an increased FPGA firmware complexity.
The JESD204B specification defines four key layers that implement the protocol data stream, as shown in Fig. 4.7. The transport layer maps the conversion between samples and framed, unscrambled octets. The optional scrambling layer scrambles/descrambles the octets, spreading the spectral peaks to reduce EMI. The data-link layer handles link synchronization, setup, maintenance and encodes/decodes the optionally scrambled octets to/from 10-bit characters. The physical layer is responsible for transmission and reception of characters at the bit rate. A logic core that implements the link

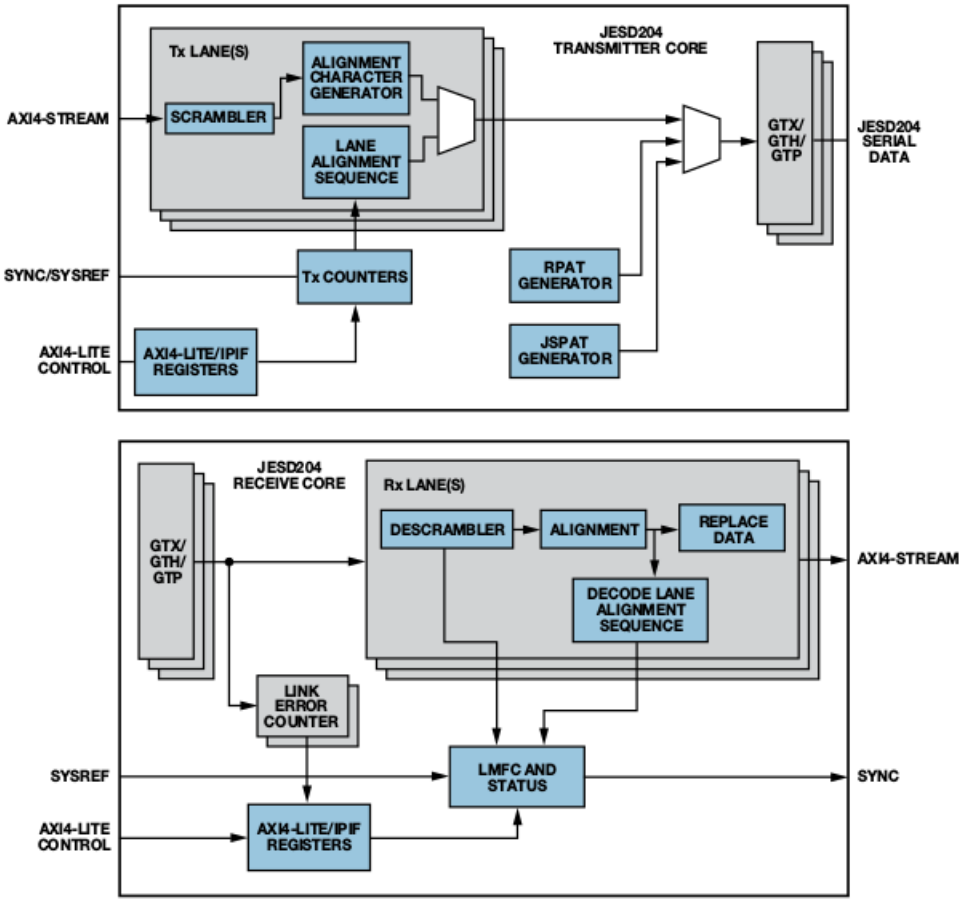


Figure 4.8: JESD204B transmitter/receiver implementation using Xilinx FPGA. [24]

layer, combined with a configurable SERDES that realizes the physical layer, forms the basis for a JESD204B link. Fig. 4.8 shows block diagrams of a JESD204B transmitter and receiver on a Xilinx FPGA. The transmitter/receiver lanes implement the scramble and link layers; the 8B/10B encoder/decoder and the physical layer are implemented in the GTX gigabit transceivers [24].

A single converter (ADC or DAC) can be mapped to a single-lane link or can be mapped to a multi-lane link (L is the number of the lanes). Multiple converters can also be mapped onto multiple lanes for M number of ADCs in the same device. In each lane are transmitted F octets and S samples per frame. The frame assembly byte representation is pictured in Fig. 4.9.

The JESD204B standard defines three different subclasses: 0, 1, and 2. The distinction between subclasses is whether to achieve a time reference alignment or not. This is a requirement for deterministic latency.

Subclass 0 does not determinate latency, whereas subclass 1 and 2 do. In subclass 1, the protocol aligns the time reference using a SYSREF signal,

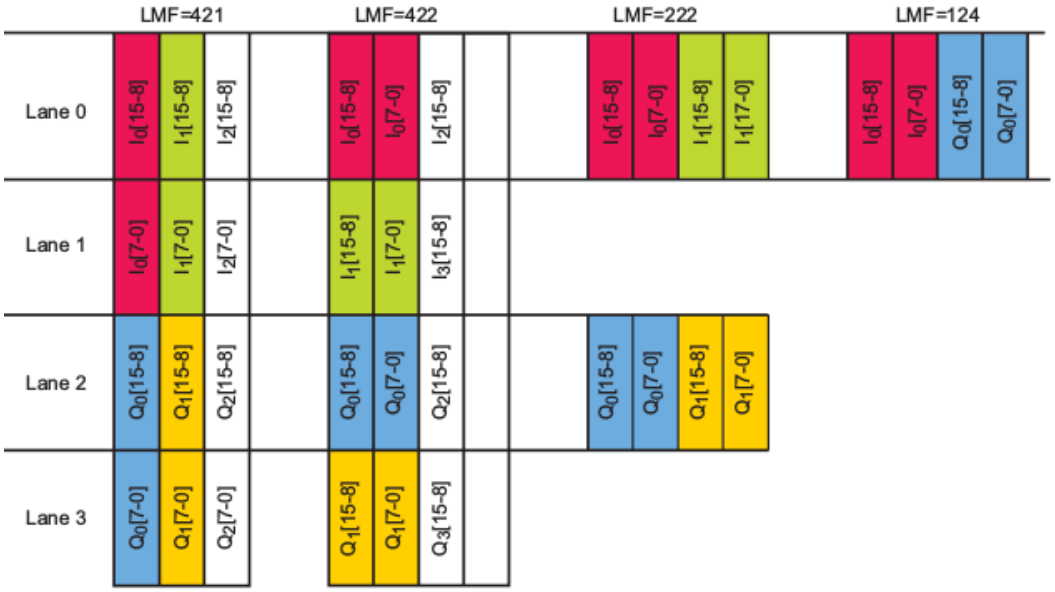


Figure 4.9: Frame assembly byte representation. [25]

whereas in subclass 2, the protocol gets the time reference alignment using a SYNC signal.
In this project we don't care about deterministic latency, hence for all the devices the subclass 0 is taken.

4.3.3 Field Programmable Gate Array

The FPGA is a programmable logic device and it constitutes the core of the control process. It is in charge of digital signal processing, the control of the cavities in according to the driving mode and the control of the parameters (see also table 5.1) chosen. The FPGA is an integrated circuit that can be configured using Hardware Description Languages (HDLs) such as VHDL or Verilog [26], [27]. The use of FPGA matches our requirement, since it can perform the control of eight cavities at the same time independently. In the RF IOC, the selected FPGA is a Kintek-7, XC7K355T manufactured by Xilinx [28], with a good performance/consumption ratio due to its manufacturing process at 28nm. The RF IOC needs 16 high speed serial transceivers for the JESD204B serial links to the converters: e.g. 4 dual ADCs and 4 dual DACs. One more serial link is necessary for the slow control link to the accelerator control system. For the communication between FPGA and the integrated circuits in the RF IOC and in other boards of the ORC box, roughly 250 GPIOs are necessary. We selected the XC7K355T model that matches our requirements.

Currently the design of control firmware for eight cavities holds on a resource usage of 35%, leaving room for future enhancement and features.

The 7 series FPGAs GTX serial transceivers [29] are power efficient transceivers, supporting line rates from 500 Mb/s to 12.5 Gb/s. Each transceiver is highly configurable and tightly integrated with the programmable logic resources of the FPGA. The main features in which we are interested are:

- 2-byte and 4-byte internal datapath to support different line rate requirements;
- 8B/10B encoding and decoding;
- comma detection and byte and word alignment;
- line rate support up to 12.5 Gb/s;

Therefore these transceivers are fully qualified to implement the physical layer of the JESD204B protocol.

4.3.4 Analog Digital Converter

The selected ADC, that satisfies the requirements outlined before, is the ADS42JB69 [30] manufactured by Texas Instrument. It is an high linearity, dual channel, 16 bit, 250 MSPS ADC. This device support the JESD204B serial interface with data rates up to 3.125 Gbps. The ADS42JB69 can be configured using a serial programming interface (SPI) and has a pipeline architecture.

The SNR of the ADC is limited by three different factors, as shown in equation 4.5. Quantization noise is typically negligible in pipeline converters and amounts to 96 dBFS for a 16 bit ADC. Thermal noise limits SNR at low input frequencies and clock jitter affects SNR for higher input frequencies.

$$SNR_{ADC}[dB] = -20\log\sqrt{\left(10^{-\frac{SNR_{QuantizationNoise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{ThermalNoise}}{20}}\right)^2 + + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \tag{4.5}$$

SNR limitation due to clock jitter can be expressed as:

$$SNR_{jitter}[dB] = -20\log(2\pi f_{IN} T_{jitter}) \tag{4.6}$$

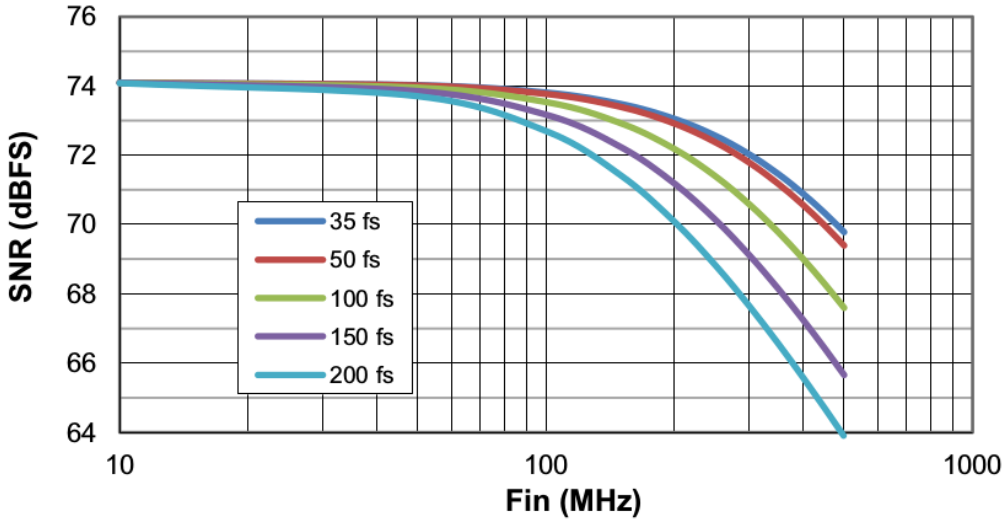


Figure 4.10: SNR versus Input Frequency and External Clock Jitter for ADS42JB69.[30]

The total clock jitter (T_{jitter}) has two components: the internal aperture jitter is set by the noise of the clock input buffer and the external clock jitter. T_{jitter} can be calculated by:

$$T_{jitter} = \sqrt{T^2_{jitter-External-Clock} + T^2_{aperture}} \tag{4.7}$$

The dependence of the SNR value on the amount of external jitter for different input frequencies, is shown in Fig. 4.10.

4.3.5 Digital Analog Converter

The DACs used in the board are the DAC1653D [25] manufactured by Integrated Device Technology (IDT). They are high speed, high performance, 16 bit, dual channels ('A' and 'B') Digital to Analog Converters DACs that integrate a JESD204B compatible high speed serial input data interface. The DAC1653D requires configuration through SPI slave interface to access the internal registers. The DAC1653D generates two complementary current outputs on pins $IOUTA_P/IOUTA_N$ and $IOUTB_P/IOUTB_N$, corresponding to channel 'A' and 'B' respectively, providing a programmable full scale output current I_{fs} of 20 mA. This is an useful feature because, as outlined in section 3.8, the up-conversion process has the drawback of generating the useful harmonic with a low energy content; the programmable gain of the final RF amplifier inside the DAC helps solving this issue. The full scale

Addr.	Register name	R/W	Bit definition								Default
Hex			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0037h	DAC_A_AGAIN_LSB	R/W	DAC_A_AGAIN[7:0]								20h
0038h	DAC_A_AGAIN_MSB	R/W	DAC_A_AGAIN_PON	-	-	-	-	DAC_A_AGAIN_X2	DAC_A_AGAIN[9:8]		83h
0039h	DAC_B_AGAIN_LSB	R/W	DAC_B_AGAIN[7:0]								20h
003Ah	DAC_B_AGAIN_MSB	R/W	DAC_B_AGAIN_PON	-	-	-	-	DAC_B_AGAIN_X2	DAC_B_AGAIN[9:8]		83h

Figure 4.11: DAC1658. Dual core block register allocation map.

Address	Register	Bit	Symbol	Access	Value	Description
0037h	DAC_A_AGAIN_LSB	7 to 0	DAC_A_AGAIN[7:0]	R/W	-	least significant 8 bits for analog gain DAC A
0038h	DAC_A_AGAIN_MSB	7	DAC_A_AGAIN_PON	R/W		Analog gain DAC A power
					0	off
					1	**on** (see Section 11.5)
		2	DAC_A_AGAIN_X2		**0**	**off**
					1	output current doubled range
		1 to 0	DAC_A_AGAIN[9:8]		-	most significant 2 bits for analog gain DAC A
0039h	DAC_B_AGAIN_LSB	7 to 0	DAC_B_AGAIN[7:0]	R/W	-	least significant 8 bits for analog gain DAC B
003Ah	DAC_B_AGAIN_MSB	7	DAC_B_AGAIN_PON	R/W	-	Analog gain DAC B power
					0	off
					1	**on** (see Section 11.5)
		2	DAC_B_AGAIN_X2		**0**	**off**
					1	output current doubled range
		1 to 0	DAC_B_AGAIN[9:8]			most significant 2 bits for analog gain DAC B

Figure 4.12: DAC1658. Analog gain control registers.

current of DAC A is setting through two parameters:

$$I_{fsA} = DAC\_A\_AGAIN\_X2 \cdot DAC\_A\_AGAIN[9:0] \cdot 25 \tag{4.8}$$

Similarly for DAC B:

$$I_{fsB} = DAC\_B\_BGAIN\_X2 \cdot DAC\_B\_BGAIN[9:0] \cdot 25 \tag{4.9}$$

These parameters are defined in the dual DAC core block. They are showed in Fig. 4.11 and in Fig. 4.12.

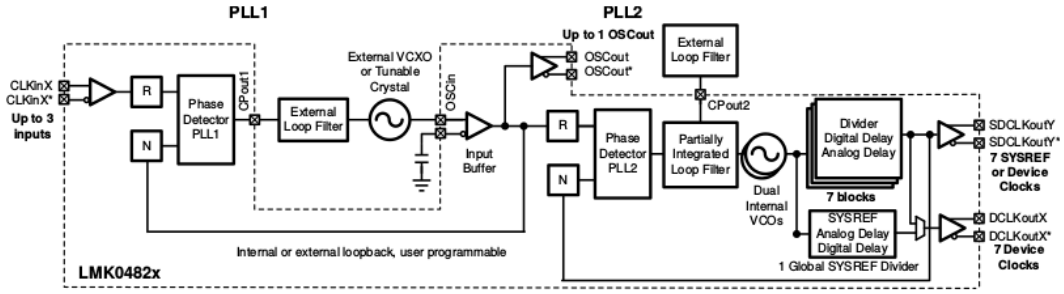


Figure 4.13: LMK04828B block diagram.

4.3.6 Clock Distribution

The timing system in ALPI Linac is based on the distribution of a unique harmonic at 160 MHz that serves both as originating frequency for the cavities resonance and as a phase reference for maximum accelerating field. The timing distribution network consists of a ovenized master oscillator distributed across the plant in a semi rigid cable and split tops at each cryostat location. At each top the master clock is fed to the resonator controller which in turn derives all its internal clocks as phase locked fractional times of the reference harmonic. These are the clocks for the GTX transceivers of the FPGA, ADCs and DACs. This work is done by two Dual/Cascade PLLs LMK04828b [31] manufactured by Texas Instruments, which provide support also for JEDEC JESD204B. Since in the design we use the JESD204B subclass 0, we don't care about the SYSREF clock outputs. The first stage of the PLL is driven by the signal coming from the ALPI master oscillator at frequency $f_{ALPI} = 160\,\mathrm{MHz}$. An external CVHD-950 VCXO [32] at 100 MHz provides the reference clock for the second stage of the PLL. The internal Voltage Controlled Oscillator (VCO) of the second stage works in the range from 2415 MHz to 2460 MHz. To provide the right sampling frequency for the ADCs and meet the VCO range condition a decimation factor D has to be inserted in eq. 3.8, that can be rewritten as:

$$f_s = D\frac{4f_{RF}}{2 \cdot N - 1}, \forall N \in Z | N \geq 1 \tag{4.10}$$

The superconducting cavities resonate at $80\,\mathrm{MHz}$ or $160\,\mathrm{MHz}$. Following equation 4.10, the sampling frequencies f_s has been chosen as to yield the smallest N and to be the same for both $f_{RF} = 80\,\mathrm{MHz}$ and for $f_{RF} = 160\,\mathrm{MHz}$. Choosing the smallest N means select the subharmonic with the highest energy content for the down/up conversion. Table 4.1 lists the parameters that

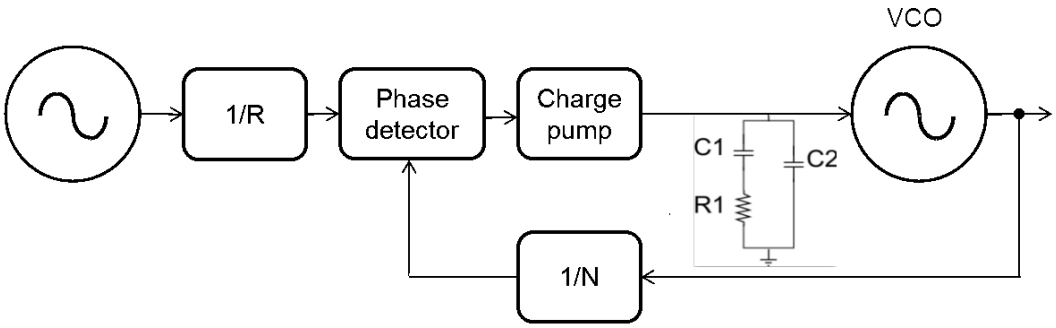


Figure 4.14: PLL block diagram with loop filter highlighted.

satisfy these requirements. Therefore the sampling frequency is:

$$f_s = D\frac{4f_{RF}}{2 \cdot N - 1} = 121.9\text{MHz}$$

Table 4.1: Values of equation 4.10.

f_{RF} [MHz]	N	D
80	11	8
160	11	4

As seen in section 4.3.4, jitter in the clock signals is a critical parameter in the design of the board. The LMK04828 PLL provides the lowest jitter figure over a wide range of output frequencies and phase noise integration bandwidths, nominally hundreds of femto seconds at f_s.

As reported in Fig. 4.14, in order to avoid stability problems at each PLL stage an external loop filter is added by means of a passive RC network. In practice a zero is added to the open loop transfer function by placing a resistor $R1$ in series with the capacitor $C1$. An extra smoothing capacitor $C2$ is often used to smooth out the rapid voltage steps which would occur from the other capacitor being charged through a resistor by means of a switch which is opening and closing. The resistance and capacitances values are computed by the following equations (a derivation of these equations and the meaning of the parameters is in appendix B):

$$R_1 = \frac{2\pi N \omega_c}{I_{CP} K_{VCO}} \frac{b}{b-1} \tag{4.11}$$

$$C_1 = \tau_2 / R_1 \tag{4.12}$$

$$C_2 = \frac{\tau_2 \tau_3}{\tau_2 - \tau_3} / R_1 \tag{4.13}$$

4.4 Radio Frequency Front End Board

Cavity pick-ups and power couplers present power levels that are not compatible with the digital circuitry of the RF IOC board. In fact these power levels are not even unique, in the sense that they depend not only on the cavity manufactured process (e.g. 80 MHz vs 160 MHz cavities, a niobium bulk vs niobium sputtered cavities) but also on the working conditions: warm or superconducting cavities, well conditioned or non conditioned cavities exhibit different input and output power levels. A flexible adaption of the power levels to/from the cavities is the task of the RF Front End (RFFE) board. The circuitry from the cavity pick-up and routed to ADC in the RF IOC board is called input channel (ICh) and from the DACs output stage to the power amplifier is called output channel (OCh). RFFE is divided in eight sections, one for each cavity controlled. Every section is formed by an input channel and an output channel. Furthermore for each section there are some inspection channels used to monitor the analog signals. Some of them are at the input of the IChs and at the output of the IChs in order to monitor the signals picked up from the cavities and the signals at the input of the ADCs.

4.4.1 Input Channels

The signals coming from the cavities, depending on their working points, are spanned in a wide power range. In conditioning operation it is estimated a -30dBm power level, while in superconducting working with zero detuning angle a 33dBm power level is estimated at the input of each input channel (ICh). The signal is then adapted to be sampled by the ADCs of the RF IOC. These ADCs can accept at their inputs an RF signal with maximum voltage of 2.5V, that is 18 dBm in 50 Ω system. Therefore the ICh has both to attenuate or amplify the signals. In typical working conditions, the signal picked up from the cavity has to pass through the RFFE encountering the smaller number of components in order to reduce added noise as much as possible. Fig. 4.16 shows the block diagram of the ICh. A 4 dB absorptive attenuator is the first component in the input chain and a digital programmable step attenuator DAT-15R5-SP+ [33], manufactured by Mini-Circuits, offers an attenuation range up 15.5 dB in step of 0.5 dB, via a 5 control bit programmable with a serial interface. At this point three paths

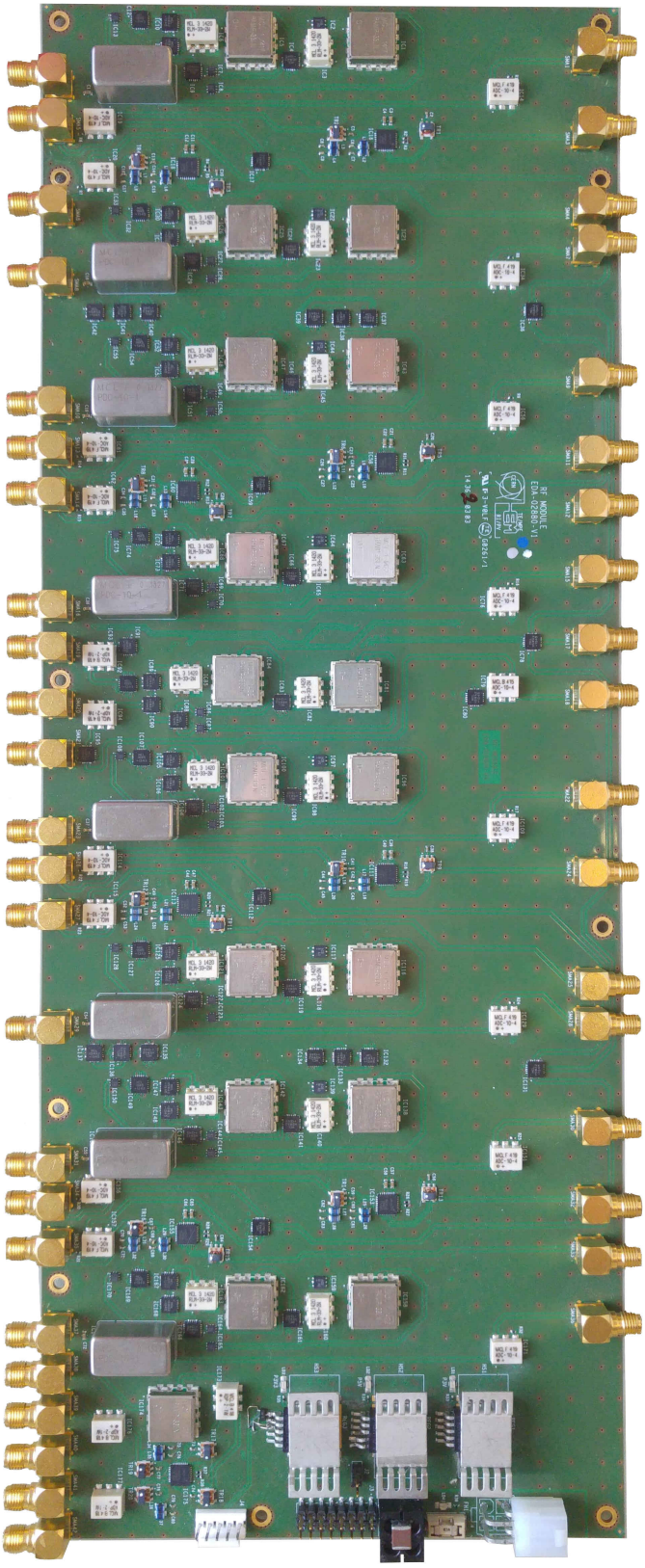


Figure 4.15: RFFE board.

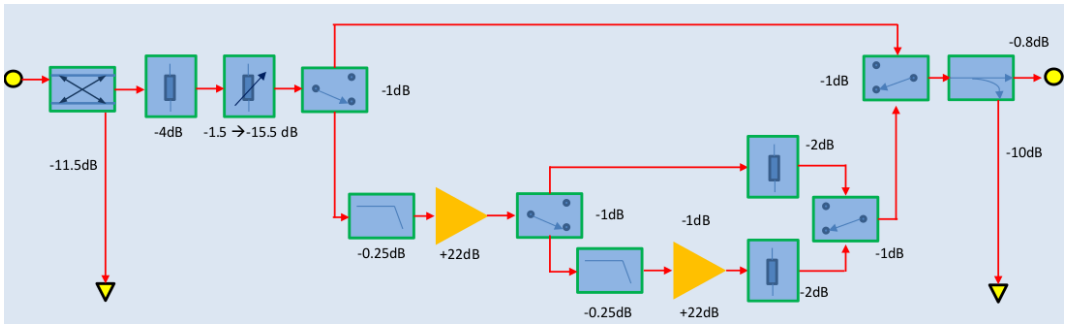


Figure 4.16: Block diagram of the input channel.

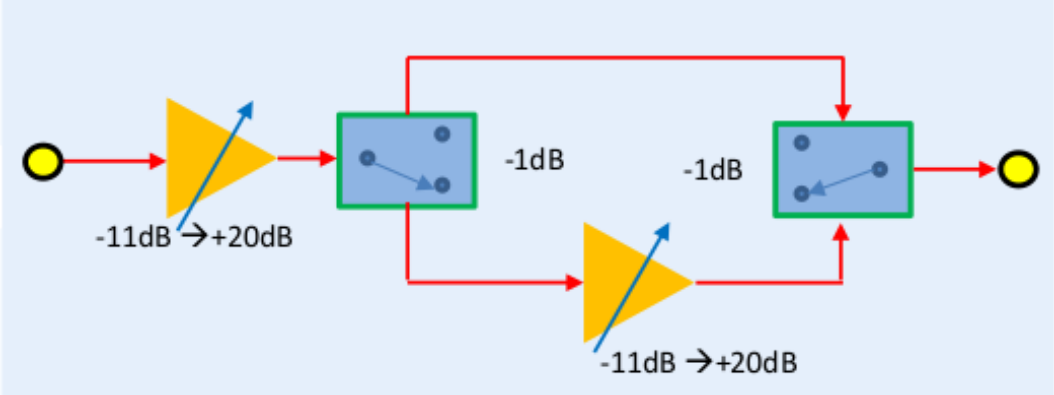


Figure 4.17: Block diagram of the output channel.

can be selected via the programmable switches HSWA2-30DR+ [34] manufactured by Mini-Circuits. In the upper path there is only a transmission line, in the middle path there is an RF amplifier with a fixed 22 dB gain reduced by a limiter and in the lower path there is an additional RF amplifier with a fixed 22 dB gain, for a total maximum input gain of 31 dB.

4.4.2 Output Channels

The output channel (OCh) is used to amplify the harmonic at the output of the helical filter, that as reported in section 3.7, has a small energy content at frequency f_{RF}. The component used for this purpose is the Variable Gain Amplifier (VGA) IDTF1240NBGI [35], a dual intermediate frequency digital variable gain amplifier, manufactured by IDT. Each VGA has a programmable variable gain from -11dB to 20 dB, with step of 0.5 dB, controlled by a 6 bit parallel interface. Since in this application we need the sensitivity of 0.5 dB, but a wider range, two VGAs have been cascaded, in order to obtain a maximum gain of 40dB.

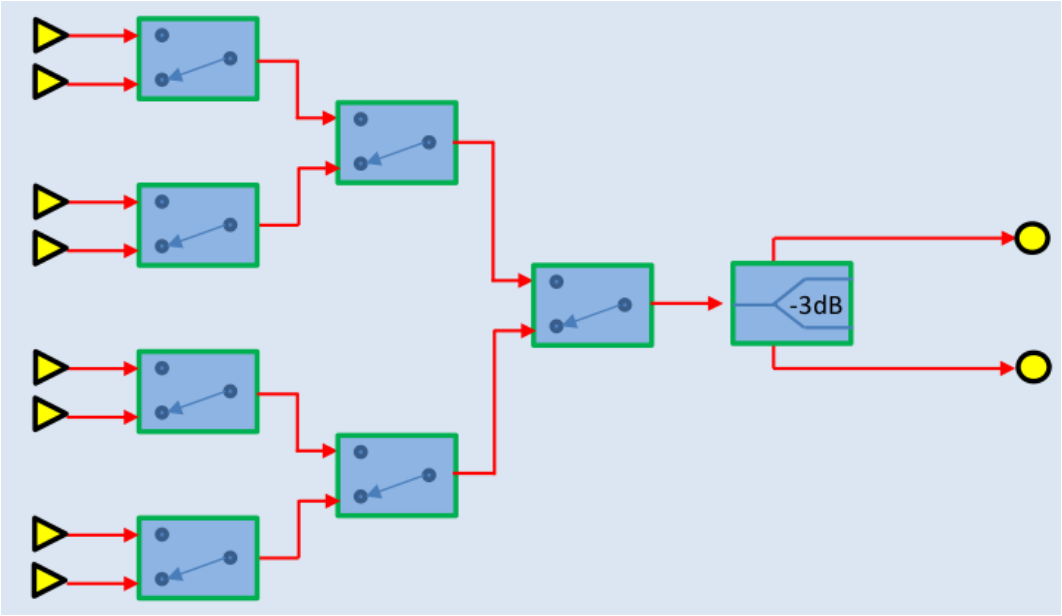


Figure 4.18: Block diagram of a 8:1 multiplexer.

4.4.3 Inspection Channels

The inspection channels are used to monitor some analog signals in each of the eight sections in the board. In the RFFE the are two inspection channels and there they are present also in the RF IOC at the output of the DACs. Directional couplers are used to pick a portion of the signal, through the coupled port. The directional couplers housed in the boards have an insertion loss lower than 1dB, a directivity higher than 40 dB and a coupling factor of 11. The coupled ports are the eight inputs of a multiplexer, as shown in Fig. 4.18, formed by 7 RF switches. It is used to select which one out of eight channels monitored. The output of each multiplexer is connected in an input of an embedded oscilloscope (DRS4 evaluation board).

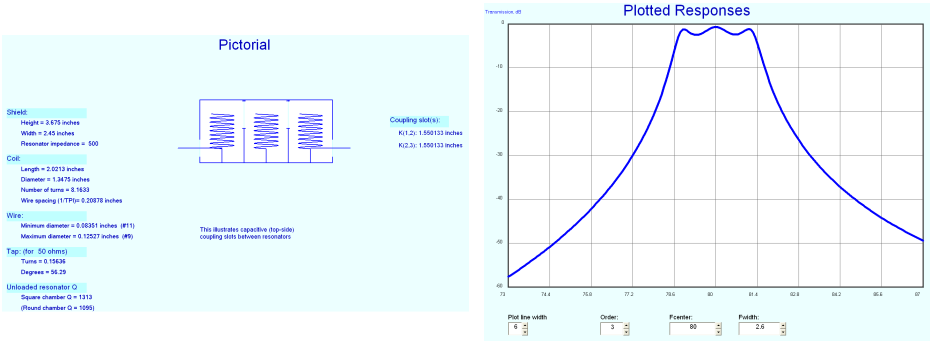
4.5 Helical Filters

The digital to analog conversion process carried out by RF IOC DACs produces an output signal with wide harmonic content due to the high speed commutation of analog levels that sum up to form the desired signal shape. It is therefore mandatory to filter out the undesired harmonics of the DACs output signal before its injection in the power amplifier and cavity power coupler. As written in section 3.7, it is crucial to filter out the harmonic

f_0 [MHz]	Insertion Loss [dB]	BW @ 3dB [MHz]	Stop Lower freq. [MHz]	Stop Higher freq. [MHz]	Att. @ stop freq. [dB]	S_{11} @ f_0 [Ω]	S_{22} @ f_0 [Ω]
80	< 4.5	< 3	73	87	> 50	$50 \pm 20\%$	$50 \pm 20\%$
160	< 4.5	< 3	145	175	> 50	$50 \pm 20\%$	$50 \pm 20\%$

Table 4.2: Helical filters main features.

containing the proper phase signal, but with a small signal content at frequency f_{RF}. For the filtering process Helical Resonator Filters have been chosen. They exhibit a reasonable Q factor and excellent performance over a wide temperature range with less volume and mass compared to conventional coaxial cavity filters operating in this band. This type of filters becomes particularly attractive as components of the new cavity radio frequency controllers of ALPI Linac and RFQ accelerators, where low volume coupled with high reliability and electrical performance is a requirement [36]. In the filter design has been carried out a trade-off between filter size,



(a) (b)

Figure 4.19: Interfaces of "Helical version 2.07" software tool.

mechanical complexity and performances. We wanted an insertion loss less than 4 dB, an attenuation in the stop band of at least of 50 dB and a size for each filter, both at 80 MHz and 160 MHz, compatible with the volume available in the ORC box. In the design process we used the "Helical version 2.07" software (Fig. 4.19). In its interfaces the input parameters were tuned in order to get the features desired, e.g. a helical resonator filters with three cavities.

So far only filters with a central frequency of $80\,\mathrm{MHz}$ and $160\,\mathrm{MHz}$ have been prototyped and manufactured. The main features of these filters are listed in table 4.2.

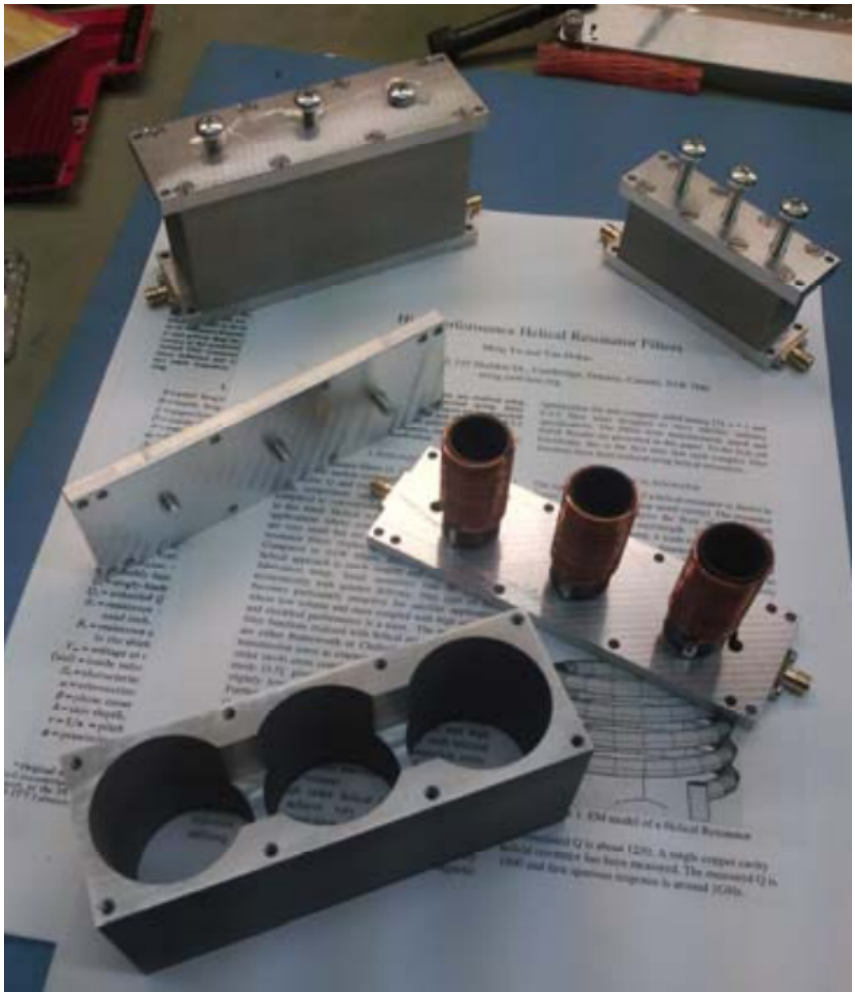


Figure 4.20: Filter prototypes under construction.

5 Firmware

5.1 Introduction

As described in chapter 4, the core element of the LLRF controller system is the RF IOC board. This board is in charge of the amplitude and phase control loops and of the communication with the accelerator control system. These functionalities are implemented through a Field Programmable Gate Array. The firmware developed for the FPGA has been written in VHDL. This chapter introduces some of choices taken in the firmware implementation and a description of the firmware structure as shown in Fig. 5.1; the different blocks correspond to VHDL modules included in the project. Each module encapsulates part of the functionalities of the board, as detailed in the following sections.

5.2 Fixed Point Arithmetic

Fixed-point arithmetic has been chosen. It has low latency and occupy not many resources in the FPGA. Fixed-point arithmetic is a variant of the typical two's complement signed fixed-point representation where a binary comma is implicitly defined. This has the advantage that the required basic arithmetic operations can be implemented in the same way as for unsigned numbers. This makes the implementation simpler and more efficient.
The fixed_pkg library is part of the VHDL standard [37]. The library defines two data types: the UFIXED for unsigned fixed point type and the SFIXED for signed fixed point type arithmetic. Methods for conversion between types are defined in the library too. When control algorithms are implemented digitally, special care has to be taken with respect to arithmetic overflows. The fixed_pkg library was written in order to make sure that overflow does not occur and defines a function for rounding the number in case of overflow or underflow; this is implemented through *resize* function. The *resize* function can be used as a rounding and saturation primitive for

adjusting the size of fixed-point operands. As inputs, it accepts a fixed-point operand, a left and a right index bound and two additional arguments that specify the rounding (underflow handling) and saturation (overflow handling) mechanisms. Different underflow (rounding to nearest and truncation) and overflow (saturation or wrap-around) schemes are supported [38]. Essentially, in digital signal processing of the cavity signals we care about two different values: the numerical representation of the magnitude field in cavity and its phase. Two approaches have been taken regarding the overflow: for the magnitude field cavity the saturation approach has been taken, while for the phase numerical representation, wrap-around was chosen.

5.3 Functionalities

The FPGA is responsible of the following tasks:

1. implementation of the data link layer and physical layer of the JESD204B protocol both in reception and transmission (Fig. 4.8); e.g. decoding the signals coming from the four dual channel ADCs and coding the signals transmitted to the DACs;
2. demodulation of the digitized signals coming from the ADCs in order to extract the I/Q components (Fig. 3.4);
3. modulation of the signals to send to the DACs, that is the first step of the up-conversion process (Fig. 3.10);
4. data transmission to the accelerator control system via Gigabit Ethernet link and reception from the accelerator control system of the control and configuration commands;
5. executing configuration commands of ICs (ADCs, DACs and PLLs) and boards (RFFE and PM board), using SPI interface and IIC interface respectively;
6. executing control commands through the internal registers;
7. application of the proportional-integral control law to the signal representing the amplitude and phase field in cavities;
8. selection of the SEL and GDR driving cavities operating modes.

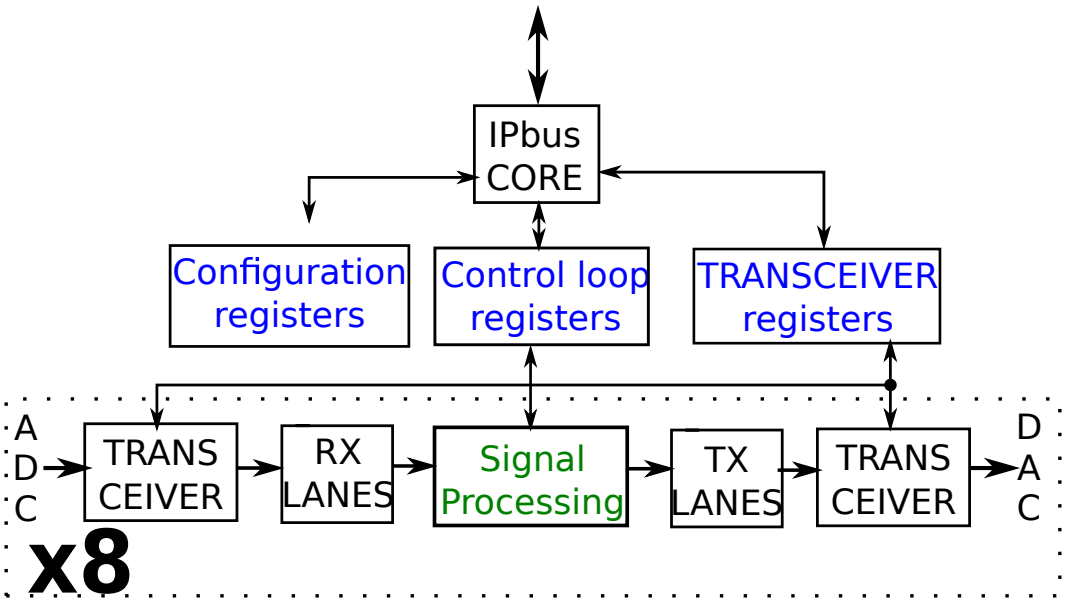


Figure 5.1: Top view of the firmware architecture.

The firmware has been written connecting entities that implement the different functionalities listed above. The top module is the higher level module that instantiates all entities and contains all FPGA I/Os. An outline of the top module is represented in Fig. 5.1. In the next sections all the modules are detailed.

5.4 The IPbus Core

The IPbus protocol is a simple control protocol for reading and modifying registers within Internet Protocol aware hardware devices which have a virtual A32/D32 bus [39]. The IPbus protocol lies in the application layer of the networking model. Each IPbus host device (in this project the RF IOC board) has an IP address and a port number through which it accepts IPbus control packets. The IPbus firmware suite has been designed for low level controls in the context of the CERN CMS experiment [21].

As shown in Fig. 5.2, the main components of the IPbus core are:

- interface to Ethernet MAC core and protocol engines for UDP, ICMP and ARP;
- SoC bus master which decodes an IPbus transaction list;

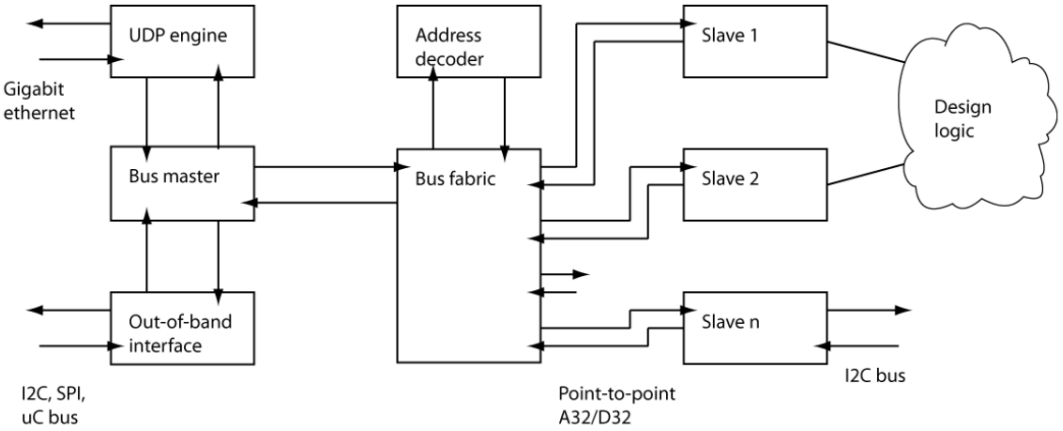


Figure 5.2: Block diagram of IPbus core. [39]

- a bus fabric allowing the attachment of multiple slaves to the SoC bus with address decoding. The bus fabric arranges for a slave to see activity on the bus when it is being addressed.
  In this project the slaves are the so called "Configuration registers", "Control loop registers" and "Transceiver registers" as shown in Fig. 5.1.

5.5 Transceiver Interface

As stated in the previous chapter, the communication between FPGA and ADCs and DACs is based on the JESD204B protocol. In the physical layer data is serialized, 8b/10b encoded, transmitted and received at line rate speeds. The physical layer of this protocol and part of the data link layer are implemented via GTX transceivers [40]. In order to utilize a GTX transceiver, it is necessary to instantiate a primitive called GTXE2. Four GTXE2 channels clustered together with one GTXE2_COMMON primitive form a Quad. The GTXE2_COMMON primitive contains a PLL. Each GTXE2_CHANNEL primitive consists of a channel PLL, a transmitter, and a receiver. Fig. 5.3 shows a single external reference clock connected to multiple transceivers within a single Quad. This is the configuration chosen in this project. The clock is generated by the same PLL and at the same frequency of the clock signals used by ADCs and DACs.

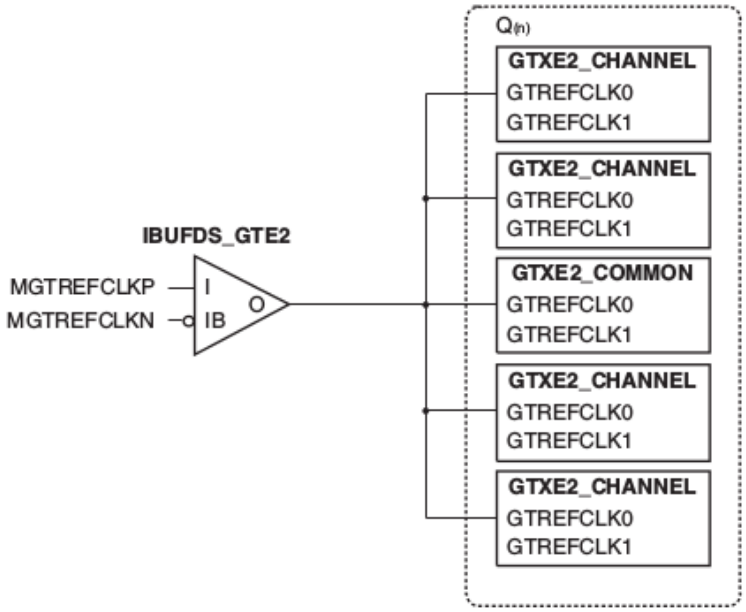


Figure 5.3: Quad outline.[40]

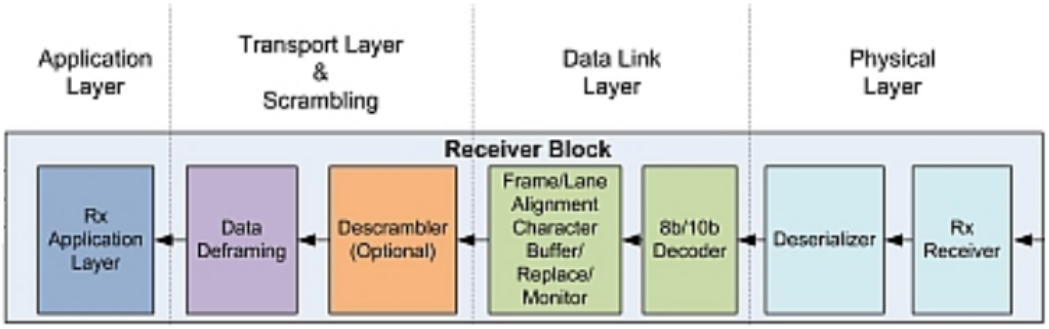


Figure 5.4: JESD204B receiver implementation. [24]

5.6 RX and TX Lanes

The "RX Lanes" entity receives the data deserialized from the transceiver and translates them in a format suitable to be processed by the following block. In this block the transport layer and part of the data link layer (Fig. 5.4) are implemented. In this project the JESD204B option for data scrambling protocol is not exploited. The scrambling can be used to reduce peak spectral emissions on the high speed serial lanes between transmitter and receiver.

The "RX Lanes" block is essentially a wrapper for the module represented in Fig. 5.5. This module is formed by three different entities. These entities basically do the Code Group Synchronization (CGS), the Initial Lane Alignment Sequence (ILAS) and the data de-framing. During the CGS, the FPGA locates comma characters in its input data stream coming from the ADCs.

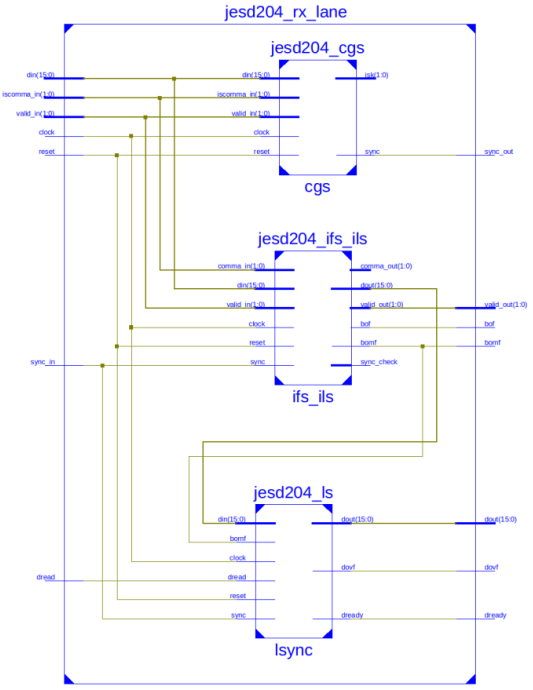


Figure 5.5: RX LANES, register transfer level (RTL) representation.

Once a certain number of consecutive comma characters have been detected on the lanes, the upper block of Fig. 5.5 de-asserts the SYNC signal to the ADCs. Then the ADCs capture the change in SYNC and starts the ILAS on the next local multiframe clock (LMFC) boundary. The other blocks in Fig. 5.5 do the ILAS and the data de-framing implemented using a procedure and a state machine written in VHDL. The ILAS aligns all the lanes of the link, verifies the parameters of the link and establishes where the frame and multi-frame boundaries are in the incoming data stream at the receiver. Data de-framing, implemented in the same state machine, maps the frames built according to the JESD204B configuration chosen, in samples available to be processed by the data processing block.

The block labeled as "TX Lanes", in Fig. 5.1, implements the transport layer and the data link layer of a JESD204B transmitter (Fig. 5.6). The firmware written for this block does the exact opposite of the receiver.

5.7 Registers

The FPGA firmware implements a set of control and status registers through which the accelerator control system can set the amplitude and phase loop parameters and the configuration parameters for the ICs on the RF IOC,

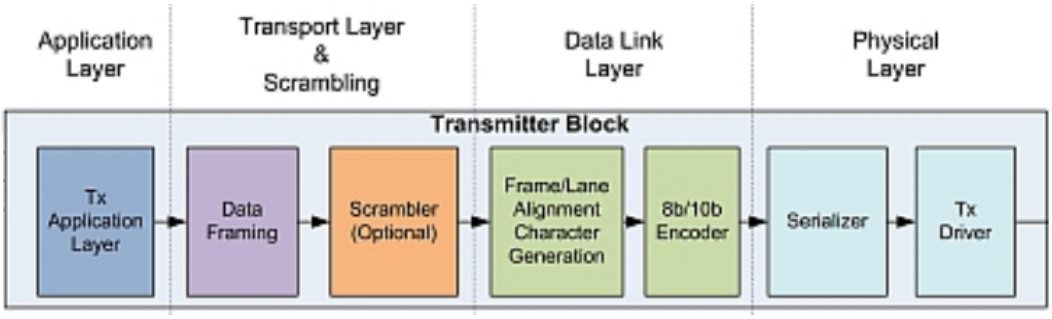


Figure 5.6: JESD204B transmitter implementation. [24]

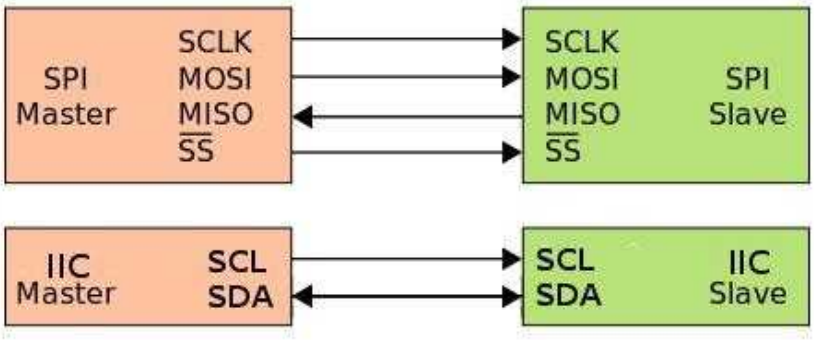


Figure 5.7: SPI (above) and IIC(under) interfaces.

RFFE and PM boards. These registers (Fig. 5.1) are labeled as "Configuration registers" and "Control loop registers". Actually the control register is formed by eight blocks: one block for each controlled cavity. These registers are the slave blocks for the IPbus core.

5.7.1 Configuration Registers

These registers are used to:

- configure the ADCs, DACs and PLLs in the RF IOC board;
- configure the digital step attenuators, the VGAs and RF switches in the RFFE board;
- read the digitized values of RF power from the PM board.

A dedicated firmware finite state machine takes care of network transactions of the IPbus protocol in SPI and IIC transactions for reading and writing IC specific registers. SPI and IIC have a master-slave architecture (Fig. 5.7) with a single master (the FPGA) that originates the frame for reading/writing transactions.

Parameter	Reg.	Off.	Wid.	R/W
Decimation factor	0	0	6	W
Phase Loop enable	0	12	1	W
Field Loop enable	0	13	1	W
Phase Locked	0	14	1	R
Field Locked	0	15	1	R
SEL/GDR	0	16	1	W
Power Enable	0	17	1	W
CIC enable	0	18	1	W
Phase shift	1	0	16	W
Quiescent power	2	0	16	W
Phase Set Point	3	0	16	W
Field Set Point	4	0	16	W
Phase Proportional Gain	5	0	16	W
Phase Integral Gain	6	0	16	W
Field Proportional Gain	7	0	16	W
Field Integral Gain	7	0	16	W
Phase Error	14	0	16	R
Field Error	14	16	16	R
Frequency Error	15	0	24	R
Phase Correction	16	0	16	R
Field Correction	17	0	16	R

Table 5.1: Parameters of the phase and amplitude field control loops.

5.7.2 Control Registers

The control registers, as said before, are used to set the parameters for amplitude and phase loops. The main parameters of control registers for each cavity controlled are listed in table 5.1.

5.8 Signal Processing

Fig. 5.8 shows the block diagram of the firmware for signal processing, implemented in VHDL. The signal from the pick-up antenna is digitized by RF ADC with a suitable sampling frequency, as described in section 3.5. The digitized signals, possibly decimated, are demodulated in in-phase and quadrature components. To accomplish this operation the CORDIC algorithm in vectoring mode is applied: from the two rectangular coordinates (in-phase and quadrature components), the phase and the amplitude (polar

coordinates) of the RF field are obtained. Since phase and amplitude/magnitude cavity field are meaningful physical properties, it is convenient to control them independently. The use of polar coordinates, allows their management with different control loops and independent proportional and integral gains.

The amplitude modulation is done by a proportional-integral (PI) controller. On the amplitude correction an offset is added (a quiescent power) whose value represents the power in the cavity when the feedback loops are open and in critical coupling condition.
The phase feedback loop depends on which operating mode of the cavity has been selected. In SEL mode the cavity phase signal is the sum of cavity phase and the phase shift imposed by the controller, while in GDR mode the phase signal represents the phase modulated by the PI block of the controller. In SEL mode a phase shift changes the length of the loops and consequently the resonance frequency. Optimizing this value brings the auto-oscillating frequency of the entire system close to the resonance frequency of the cavity and maximizes the auto-oscillating magnitude. Also in the phase feedback circuit the gain is set as high as possible, but avoiding auto-oscillation of the circuit itself. The cavity phase and the magnitude so obtained are reconverted in rectangular coordinates using the CORDIC algorithm in rotation mode. These coordinates are the inputs of the CPM block, which works by adding at the input the in-phase and quadrature components of the orthogonal correction signal. The phase correction signal is obtained by a comparison with the reference phase too; this is needed to set the phase required to optimize the transit time factor of the particles in cavities. The in-phase and quadrature signals at the output of the CPM block are modulated, fed into the digital analog converter, filtered with a narrow band-pass filter and routed to the power amplifier [41]. In the next sections the main blocks will be detailed.

5.8.1 The Demodulator

The demodulator firmware block is essentially a FSM that implements three functionalities:

- acquires the in-phase and quadrature components taking their absolute value, since the CORDIC block require only positive value at its inputs;

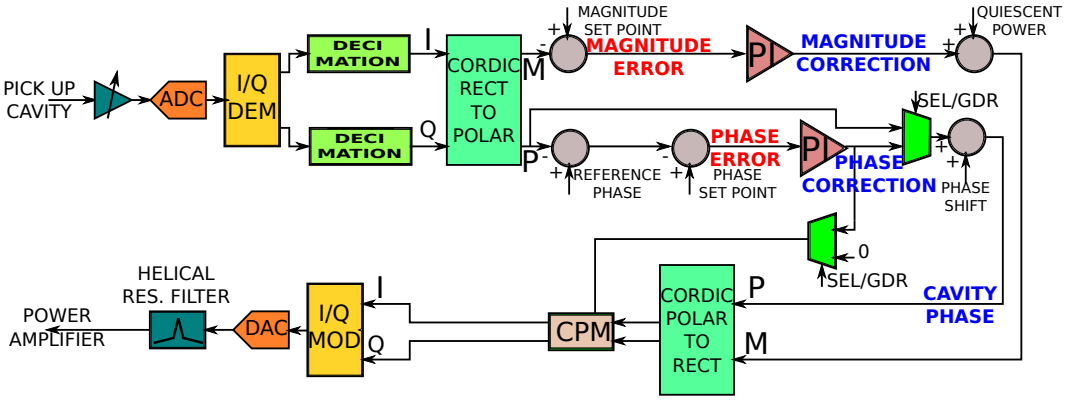


Figure 5.8: FPGA Data Flow.

- makes a moving average of subsequent samples. This functionality is almost mandatory for reducing the white noise. Therefore it is useful to increase the ADC SNR and so to reduce the impact of clock and aperture jitter. This process is very important when signals are sampled outside the first Nyquist zone;
- decimates the samples coming from the ADC in order to adhere to the sampling frequency, as per the equation 4.10. The decimation factor is D.

5.8.2 Cordic Rotation

The control algorithm uses coordinate transformations from cartesian coordinates to polar coordinates and vice-versa. Usually these transformations require trigonometric functions that are not easily implemented in a FPGA. The COordinate Rotation DIgital Computer (CORDIC) algorithm solves this problem by calculating vector rotations summing up progressively smaller pseudo rotation [14]. This algorithm is based on the rotation of the vector from position $(x_1,\ y_1)$ to position $(x_2,\ y_2)$, represented in Fig. 5.9 and by equations 5.1.

$$\begin{cases} x_2 = x_1 - y_1 \tan(\theta) \\ y_2 = y_1 + x_1 \tan(\theta) \end{cases} \tag{5.1}$$

The CORDIC algorithm makes iterative rotations of angles $\tan(\theta)^i = 2^{-i}$, using a shift instead of a multiplication by a tangent. Therefore for the i-th

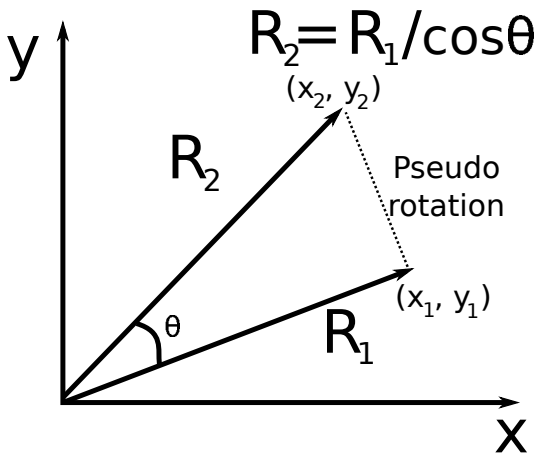


Figure 5.9: CORDIC pseudo rotation.

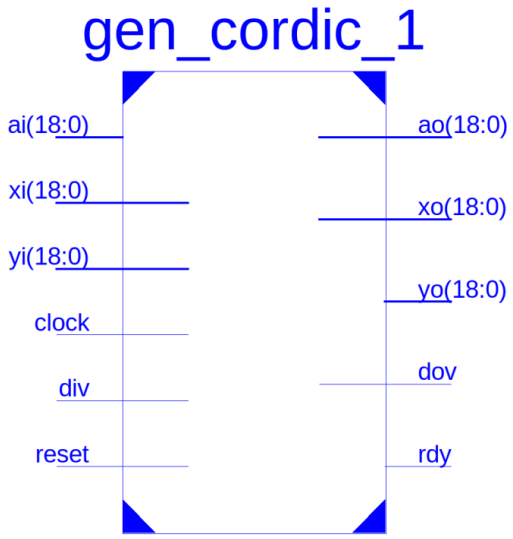


Figure 5.10: CORDIC entity, RTL representation.

rotation, equations 5.1 can be written as:

$$\begin{cases} x_{i+1} = x_i - y_i 2^{-i} d_i \\ y_{i+1} = y_i + x_i 2^{-i} d_i \\ a_{i+1} = a_i - d_i \theta_i \end{cases} \tag{5.2}$$

where d_i is ± 1 and a_i is the accumulative angle rotated at each iteration. During the i-th pseudo rotation the output term is scaled by a factor $1/\cos(\theta_i)$, so at each rotation a scaling factor has to be applied, giving a whole scaling factor equal to K_{SC}. Fig. 5.10 shows the RTL block implementing the CORDIC algorithm. As mentioned before, the algorithm can operate in two modes: in vectoring mode $d_i = -sign(x_i y_i)$, after n pseudo rotations, the

outputs of the block are:

$$\begin{cases} xo = K_{SC}\sqrt{xi^2 + yi^2} \\ yo = \text{open} \\ ao = ai + \arctan(yi/xi) \end{cases} \tag{5.3}$$

with xi,yi,ai, xo,yo and ao the inputs/outputs of the block in Fig. 5.10. In rotation mode $d_i = sign(a_i)$, after n pseudo rotations, the outputs of the block are:

$$\begin{cases} xo = K_{SC}(xi\cos(ai) - yi\sin(ai)) \\ yo = K_{SC}(yi\cos(ai) + xi\sin(ai)) \\ ao = \text{open} \end{cases} \tag{5.4}$$

5.8.3 The Proportional Integral Controller

As described in section 3.6, the PI controller has been chosen as control law for the amplitude and the phase control loops.
The controller has two branches: the proportional and the integral one. The proportional part consists in the multiplication between the error and a programmable proportional gain (see Tab. 5.1). The integral is an accumulator, that continuously sums the present error with previous errors multiplied by a programmable integral gain (see Tab. 5.1). At the end, output of the two branches are added together.

5.8.4 The Complex Phase Modulator

In SEL mode the CPM adds a correction vector in quadrature to its input vector and therefore corrects for phase and magnitude errors caused by a detuned cavity, as stated in section 3.7.2. The magnitude of the output vector from the CPM block is:

$$|\vec{v_{out}}| = |\vec{v_{in}}|\frac{1}{\cos(\varphi)} \rightarrow \frac{|\vec{v_{out}}|}{|\vec{v_{in}}|} = \frac{1}{\cos(\varphi)} \tag{5.5}$$

If this correction vector has the same value of the detuning angle of the cavity, that is:

$$cos(\varphi) = cos(\Psi) \tag{5.6}$$

the CPM (eq. 5.5) has the inverse transfer function of the cavity (eq. 2.12). With this firmware block the magnitude error and the phase error due to the cavity detuning are corrected at the same time avoiding the coupling between the two control loops.

5.8.5 The Modulator

The modulator firmware is essentially a FSM that multiplies the in-phase and quadrature components alternately by 1 and -1, to restore the negative components of the samples and then they are summed together. These operations are done taking into account the decimation factor D of equation 4.10;

5.8.6 Frequency Error

The computation of the frequency error is based on the concept of instantaneous frequency. In a discrete time domain, given an analytic signal $s(n)$ in polar form, that is $s(n) = a(n)e^{j\phi(n)}$, where $a(n)$ is the discrete magnitude and $\phi(n)$ the discrete phase [42], the discrete time instantaneous frequency is defined as the backward difference of the phase:

$$f(n) = [\phi(n) - \phi(n-1)] \text{mod}(2\pi) \tag{5.7}$$

where mod(2π) reflects the periodic nature of $\phi(n)$.
The VHDL code to compute the frequency error makes an accumulation of $f(n)$ values according to equation 5.7 where $\phi(n)$ is the phase error at the n-th instant. The mod(2π) is implemented using the wrap-around option of the *resize* function (section 5.2).

6 EPICS Based Radio Frequency Control System

6.1 Introduction

The RF control system communicates with the RF IOC board via the EPICS Channel Access and renders all its functionalities controllable from the EPICS environment. The first part of this chapter gives a brief overview of what a particle accelerator control system is, focusing in particular on the EPICS architecture and its features. The rest of the chapter is split in two sections. In the first a description of the EPICS device driver designed is given. In the last section the frequency control of the cavity is fully explored.

6.2 Particle Accelerator Control Systems

The particle accelerator control system enables users control and operate all the particle accelerator machine interactively from a unique control room. The control system can be split in several working subsystems. The main subsystems are: beam diagnostics, transport, criogenycs, vacuum, RF control system and personnel protection. The Fig. 6.1 represents a generic particle accelerator control system.

The subsystems work together to let the global control system do what it is expected. They are different and heterogeneous subsystems, therefore an upper framework to supervise them is crucial. The framework chosen is EPICS.

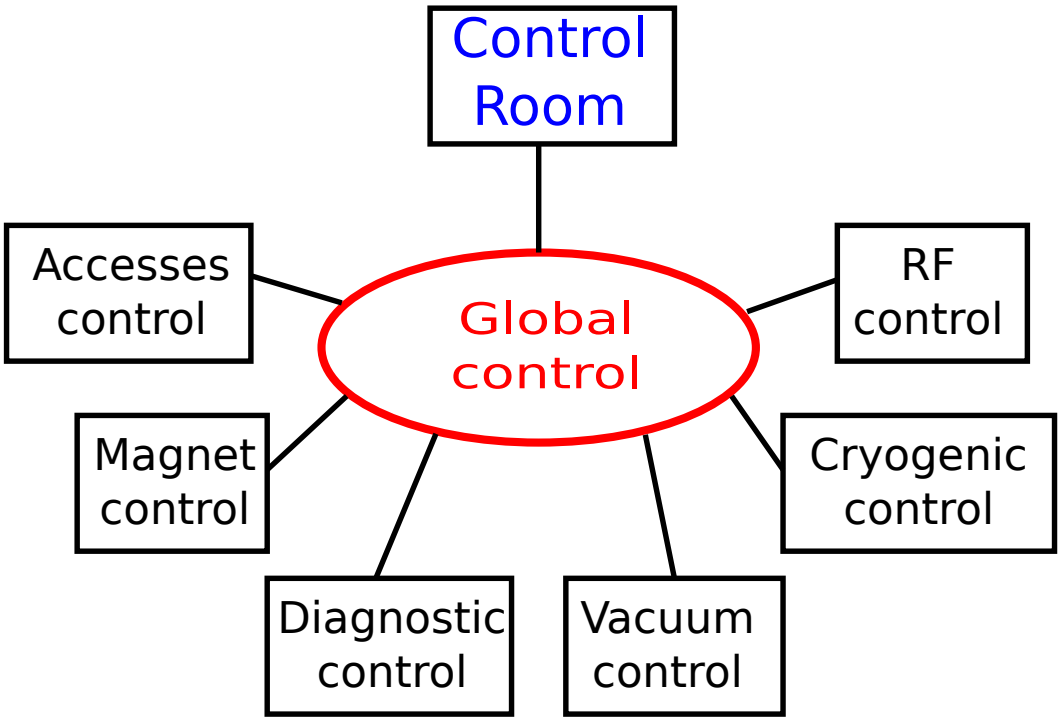


Figure 6.1: Accelerator control system architecture.

6.3 EPICS

EPICS (Experimental Physics and Industrial Control System) is a set of software tools that are key to realize control system for particle accelerators or more in general for large physical experiments. It is designed for distributed control systems with a large number of computers connected together.

EPICS has Client/Server and Publish/Subscribe model for communication between computers. This architecture is built on an efficient protocol for data transfer, the Channel Access (CA) and a real-time distributed database [18].

Fig. 6.2 shows the EPICS architecture for a particle accelerator control system. The computers, here called Input/Output controllers (IOCs), work as server pushing data from the hardware. The data published to the clients are gathered by clients using the CA network protocol. The CA protocol communication is usually done via Ethernet.

The data is published from IOCs to clients in form of Process Variables (PVs). In EPICS a PV is a named piece of data associated with the machine. The PV implementation is made through structures called records. In EPICS environment a record identifies an object with:

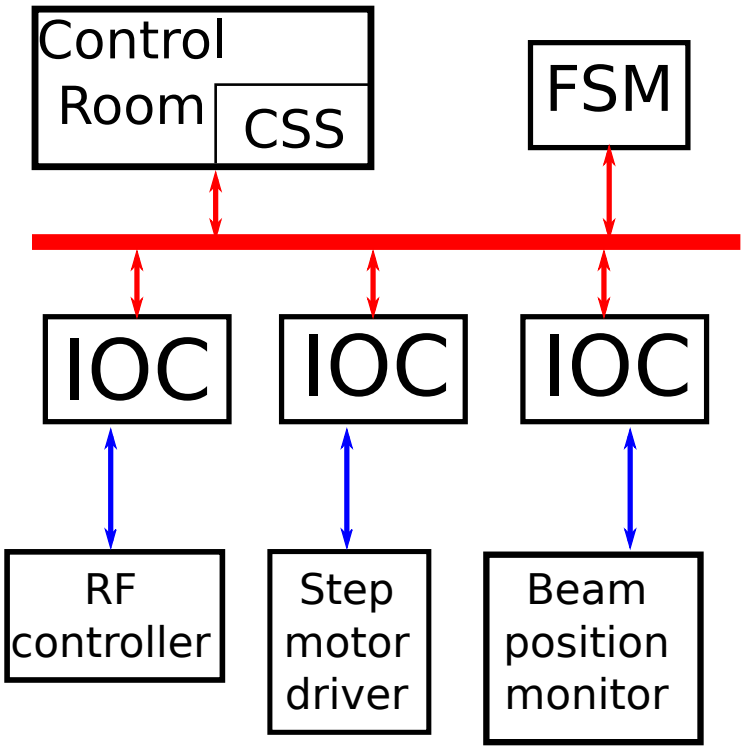


Figure 6.2: EPICS architecture of the accelerator control system.

- a unique name;
- a behavior defined by its type. For example Analog Input (ai) and Analog Output (ao) records, do input/output operations, from/to hardware, with analog values;
- multiple fields, where features are defined;
- optional links with other records;
- optional association with hardware using the device support.

Therefore, each PV is defined by a record and a list of records forms a database. The database is loaded by the IOC.

An IOC is a set of routines that defines the PVs and implements the real-time control algorithms; basically it defines the routines for the communications with the channel access and with the hardware, stores and manages the PVs. An EPICS IOC diagram, with its main blocks, is represented in Fig. 6.3.

The blocks of Fig. 6.3 have the following functionalities:

- the channel access is the software interface between the IOC and the transmission channel;

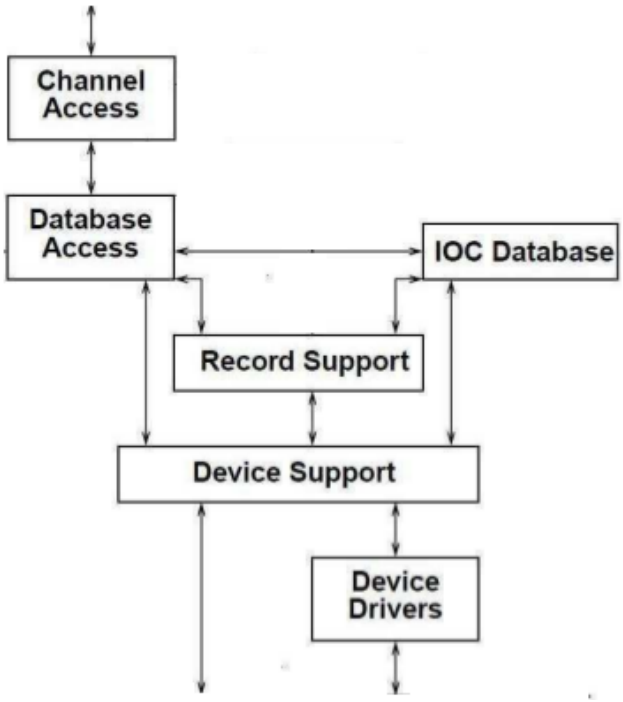


Figure 6.3: Block diagram of a EPICS IOC.

- the IOC database is the storage where the PVs are defined and available to the clients;
- the Database Access is the module in charge of manage the accesses to the database;
- the Record Support is the module to manage the records;
- the Device Support is the template used to define new modules that implement the communication with hardware devices;
- the Device Drivers are modules that interface directly with the hardware. They are provided to isolate device support routines from details of the interface to the hardware.

Among the EPICS CA clients, the Control System Studio (CSS) was chosen in the context of this thesis. CSS is a collection of tools with monitors and operating panels for large scale control systems, such as the ones in the accelerator community. Fig. 6.4 shows an example of a Graphical User Interface (GUI) developed using CSS for an EPICS control system.

Figure 6.4: Cryostat monitor interface developed with CSS.

6.4 RF Control System

The RF control system is a subsystem of the global control in charge of monitor, control and operate the boards housed in the ORC box. A great effort was devoted in the development of the EPICS device driver to support the communication with the RF IOC board by the global control system.
The remote communication from the RF IOC to the clients is implemented with the architecture shown in Fig. 6.5.

The more common software components of Fig. 6.5 have been described in the previous section, while the custom components chosen and developed in this architecture are detailed in the next sections.

6.4.1 EPICS Device Driver Support

In this section the device/driver supports developed in order to communicate with the hardware are detailed. These supports constitute a software layer written in C/C++ based on the asyn package, described in paragraph 6.4.2. Device and driver support is outlined in Fig. 6.6. Records may have special attributes that specify link fields to user-defined functions executed during record processing. Hence support is generally intended as the code snippets that allow a particular type of record to communicate with the hardware. Sometimes the device support for different types of records

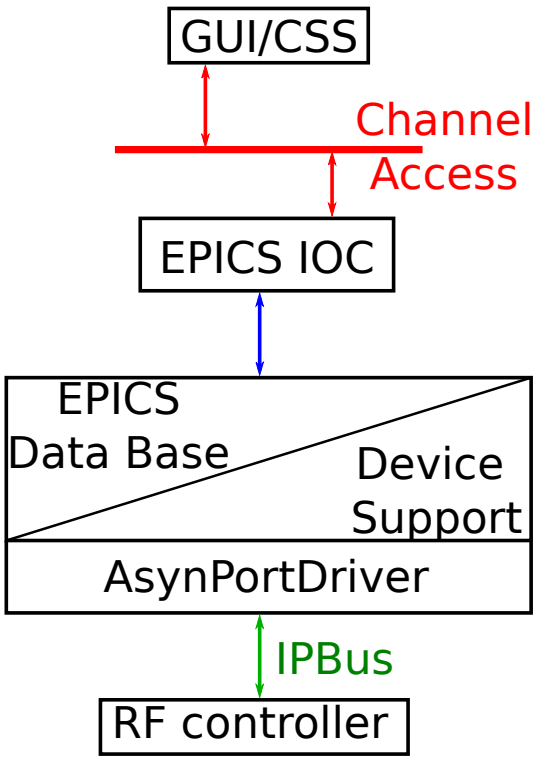


Figure 6.5: RF control system architecture.

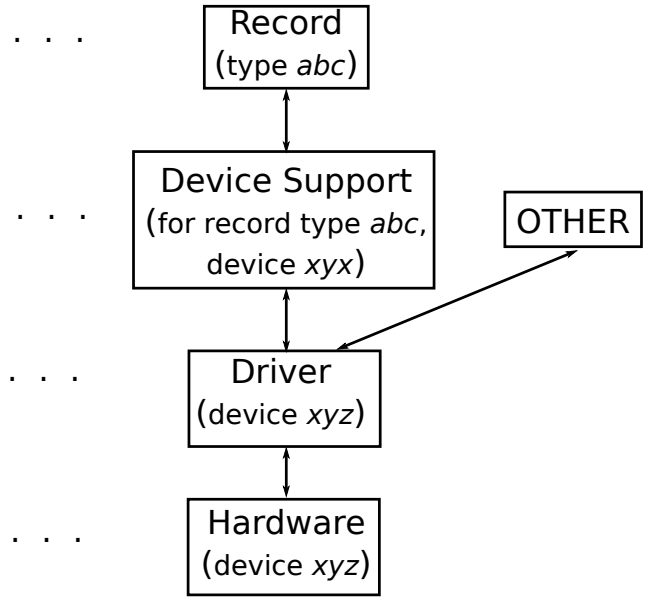


Figure 6.6: IOC-EPICS device/driver support architecture.

shares code that reflects common functionalities: this code forms a separate module called driver support. This module can be accessed also by other code non-record related, as shown in Fig. 6.6.

The driver support is referred to software layer used to perform the slow control services of the RF IOC board and the other boards in the ORC box. Basically the driver support reads and writes registers implemented in the FPGA via VHDL and described in section 5.7. In the support software the hardware is represented by interfaces and classes that mimic hardware boards and the functionalities of each integrated circuit. The object hierarchy of the driver support is presented in Fig 6.7.

The lowest-level read and write functions to the memory-mapped registers, implemented in the FPGA, are based on the read and write functions respectively, provided by the μHAL A.P.I.; e.g. a C++ library that is a component of the IPbus suite. This μHAL is shortly described in paragraph 6.4.3.

Each device driver can be used to control one or more RF controllers. To allow this, operators from a remote console set and get working parameters that can be subdivided, based on how and where they access the FPGA internal registers, in three groups:

1. amplitude and phase loop parameters;
2. configuration ICs parameters through PVs;
3. configuration ICs parameters non-record related.

The first point represents the parameters, represented in the IOC database as analog input/output records, that can access control registers (section 5.7.2). Most of these parameters are reported in table 5.1.

The second point of the previous list refers to the parameters stored in the database as "ai" or "ao" records. As reported above the C++ classes in the driver support represent the boards and their ICs. Therefore during record processing the functions of the high level classes that interact with different devices are called. As shown in Fig 6.7 these classes call lower level classes, i.e. spiMaster and i2cMasterBase classes, that through the set and get atomic methods provided by μHAL library, implement the low-level write and read functions to the memory-mapped registers. The type of low level classes involved in the record processing depends on the serial protocol provided by the integrate circuit slave.

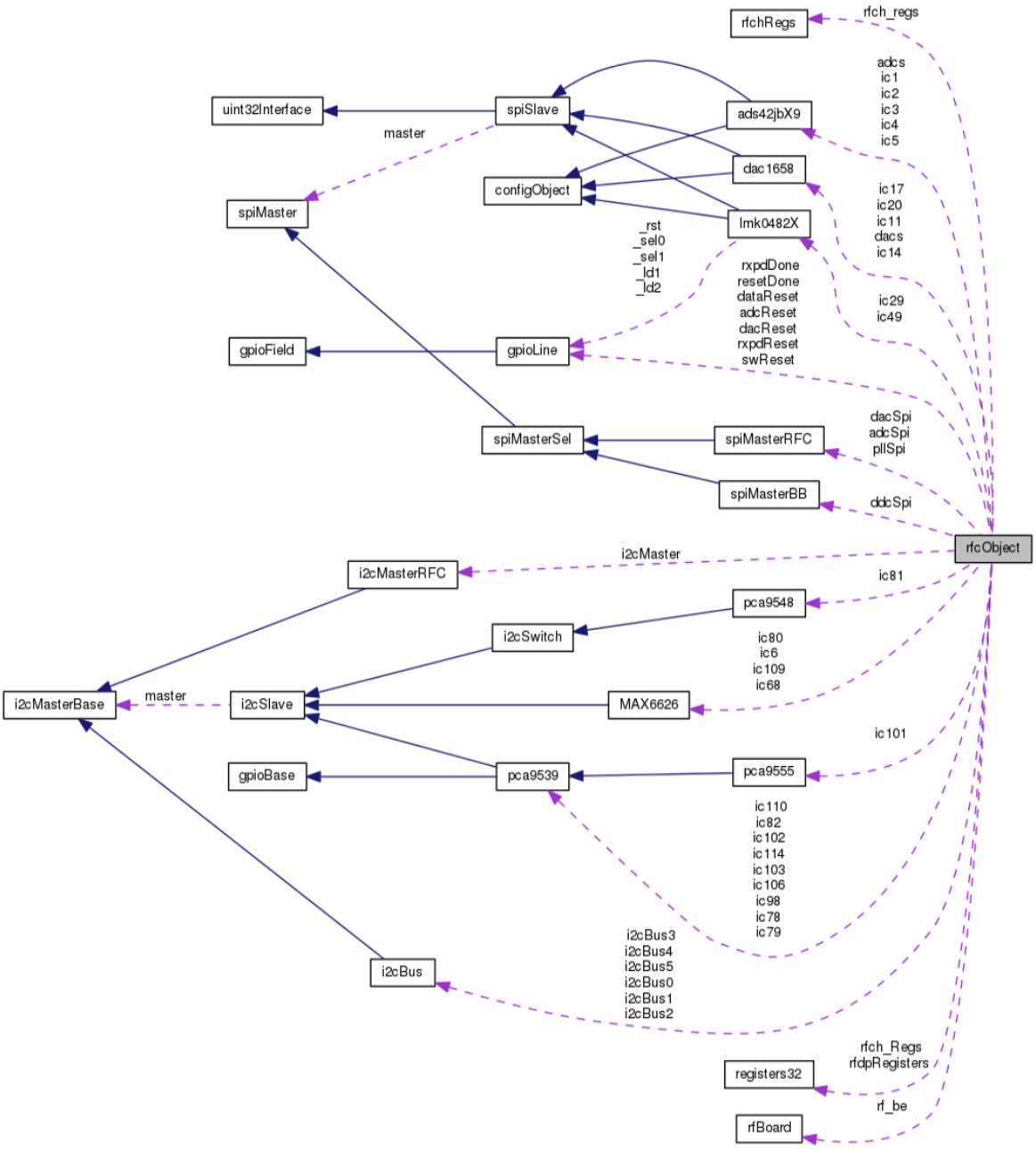


Figure 6.7: Collaboration diagram of the software classes in the driver support developed.

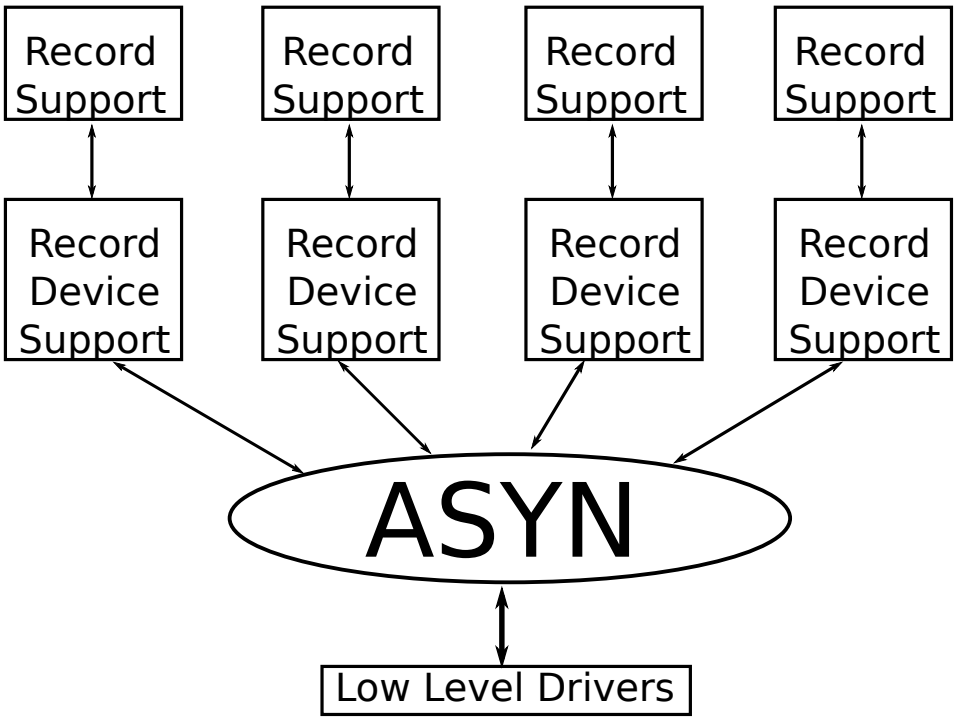


Figure 6.8: AsynPortDriver architecture.

The last point of the list represents the parameters used to configure the ADCs, DACs and PLLs in the RF IOC board. Usually this configuration happens once during the connection of the asyn process. These parameters are not record related.

6.4.2 AsynDriver

AsynDriver, or simply Asyn, is a general purpose package for interfacing device specific code to low level communication drivers. Essentially it provides a standard interface between device supports and device drivers [43].

The Asyn package is written in C/C++ and it provides the functions necessary to write servers, the port drivers and clients, such as EPICS device supports/drivers. Here is declared the method connect, used to connect to the hardware. Moreover the package provides specific I/O interfaces as asynInt32, asynOctet and asynFloat64, each one equipped with at least the two methods read() and write(). AsynPortDriver is a C++ class that is intended to make easier writing asyn port drivers as it takes care of most of the details of writing a port driver. It calls the original asynDriver functions, which are hidden from the derived classes that are based on asynPortDriver.

This device support package increases modularity avoiding the creation of a new record type for each type of device.

6.4.3 μHAL

μHAL [21] is a C++ library providing an end-user interface for IPbus reads, writes and Read-Modify-Write (RMW) operations. In μHAL the target's registers layout is specified by XML files, allowing a hierarchical address structure of register nodes. It promotes modularity by referencing other address files containing the layout of registers in common repeated modules. The XML file that maps the parameters contained in table 5.1 is listed below.

Listing 6.1: Registers layout xml file

```
<node id="rf_ch_register">
  <node id="reg_0"          address="0x00" permission = "rw"  fwinfo="endpoint;
      width=0">
<!--      <node id="dec_fact"            mask = "0x0000003f"/>  -->
<!--      <node id="downsamp_fac_exp"    mask = "0x000007c0"/>  -->
<!--      <node id="counter_clockwise"   mask = "0x00000800"/>  -->
<!--      <node id="phase_loop_en"       mask = "0x00001000"/>  -->
<!--      <node id="field_loop_en"       mask = "0x00002000"/>  -->
<!--      <node id="phase_locked"        mask = "0x00004000"/>  -->
<!--      <node id="field_locked"        mask = "0x00008000"/>  -->
<!--      <node id="cav_mode"            mask = "0x00010000"/>  -->
<!--      <node id="power_en"            mask = "0x00020000"/>  -->
<!--      <node id="cic_en"              mask = "0x00040000"/>  -->
  </node>
  <node id="ph_shift"       address="0x01" permission = "rw"  fwinfo="endpoint;
      width=0"/>
  <node id="quies_pw"       address="0x02" permission = "rw"  fwinfo="endpoint;
      width=0"/>
  <node id="ph_set_point"   address="0x03" permission = "rw"  fwinfo="endpoint;
      width=0"/>
  <node id="fld_set_point" address="0x04" permission = "rw"  fwinfo="endpoint;
      width=0"/>
  <node id="ph_P_gain"      address="0x05" permission = "rw"  fwinfo="endpoint;
      width=0"/>
  <node id="ph_I_gain"      address="0x06" permission = "rw"  fwinfo="endpoint;
      width=0"/>
  <node id="fld_P_gain"     address="0x07" permission = "rw"  fwinfo="endpoint;
      width=0"/>
  <node id="fld_I_gain"     address="0x08" permission = "rw"  fwinfo="endpoint;
      width=0"/>
  <node id="ph_lck_thrs"    address="0x09" permission = "rw"  fwinfo="endpoint;
      width=0"/>
  <node id="fld_lck_thrs"   address="0x0a" permission = "rw"  fwinfo="endpoint;
      width=0"/>
  <node id="ph_lck_wind"    address="0x0b" permission = "rw"  fwinfo="endpoint;
      width=0"/>
```

```
  <node id="fld_lck_wind"  address="0x0c" permission = "rw"  fwinfo="endpoint;
      width=0"/>
  <node id="ph_fld_err"    address="0x0d" permission = "rw"  fwinfo="endpoint;
      width=0">
<!--     <node id="ph_err"   mask = "0x0f"/>  -->
<!--     <node id="fld_err"  mask = "0xf0"/>  -->
  </node>
  <node id="freq_error"    address="0x0e" permission = "rw"  fwinfo="endpoint;
      width=0"/>
  <node id="ph_corr"       address="0x10" permission = "rw"  fwinfo="endpoint;
      width=0"/>
  <node id="fld_corr"      address="0x11" permission = "rw"  fwinfo="endpoint;
      width=0"/>
</node>
```

Transactions are queued within the transport layer payload buffers until either the dispatch method is called or the payload of the request/response packet is full. The μHAL library also has bindings for Python, which acts as a useful platform for quickly developing test scripts or control software.

6.5 RF Cavity Tuning

In section 3.9 was shown how the cavity frequency tuning system works. Basically there is a mechanical compression system which uses a deformation tuner for its operation. An automatic control system based on the stepper motors is therefore fundamental to keep the cavity resonance frequency close to its own eigenfrequency.

Stepper motors are controlled by the Beckhoff terminal KL2541 [44] (as shown in Fig. 6.9): a stepper motor driver with up to 5A/ph current, limit switches and encoder support. To interface the Beckhoff driver card with the accelerator control system an EPICS driver support was developed. This driver uses the EPICS modbus module as the low level communication channel. The KL2541 has two kinds of registers: the "process communication" registers are 6 modbus registers, whereas the "register communication" registers are 128 internal memory locations with motor parameters that can be accessed through read/write operations via modbus registers. An asynPortDriver port (motorDriver) masks this programming interface while the motor record support reads and writes to the motorDriver port.

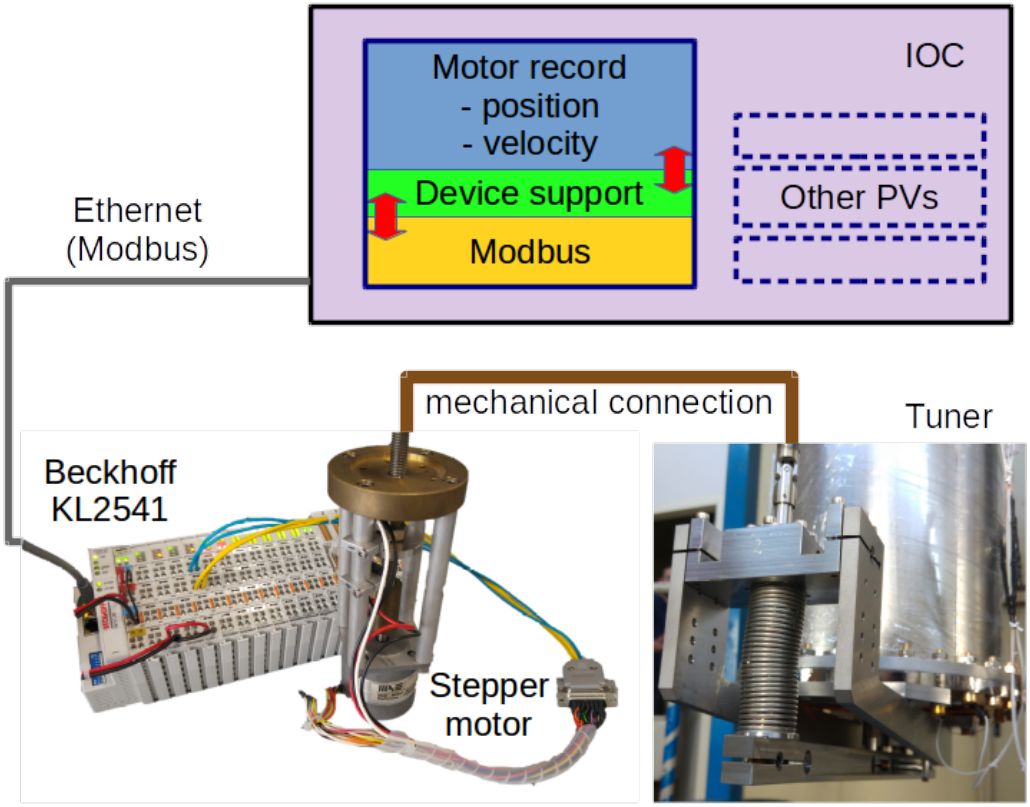


Figure 6.9: Tuner control.

6.5.1 State Machines

The automation process is easily represented as in a state diagram (see Fig. 6.10): each circle is a state. As the number of states is finite and the machine is in only one state at a time, the process can be modeled as a finite state machine (FSM) where the transition from a state to another (depicted with arrows) is triggered by external events.

In EPICS, FSM can be implemented either:

- as part of the IOC;
- as a program running in client-side.

The first approach is preferred when PVs that are the FSM inputs/outputs are stored in the same IOC.
Since the machines that we are going to build exploit PVs from heterogeneous IOCs, the second approach was preferred.

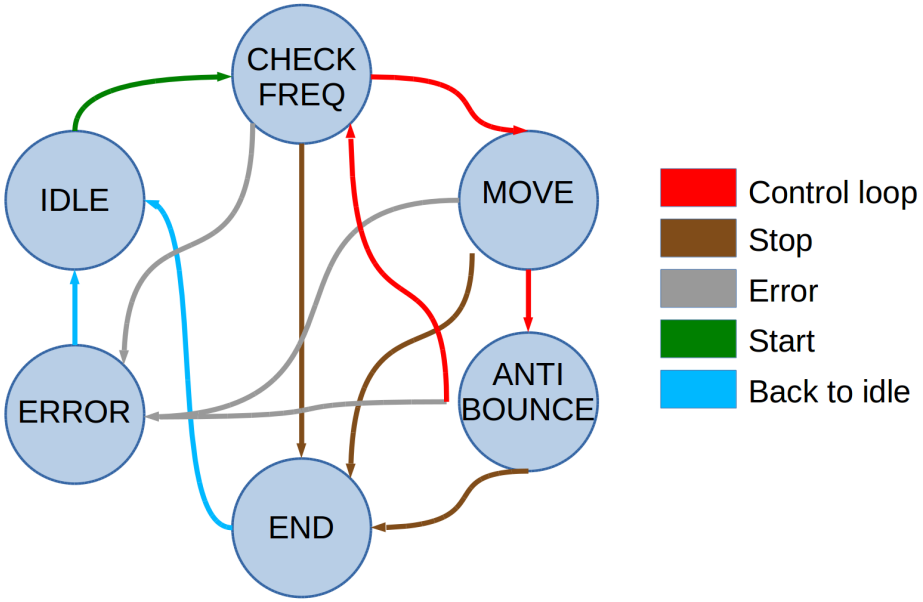


Figure 6.10: Cavity tuning state diagram.

6.5.2 Implementation

Event-driven FSMs implemented, mimic a typical operator behavior. The FSM framework is built using Python language and is centered around various classes. Some of the key objects are:

- fsmBase: it is the actual FSM. It is instantiated at the program beginning and it manages the state execution, the state transitions and it interfaces to timers and inputs. Each FSM is derived from fsmBase;
- fsmThread: for each FSM, makes a new thread operating in parallel with respect to other machines. Moreover it manages the start and the stop of the machine;
- fsmIO: represents the FSM inputs and outputs. It contains the PVs references and it manages the I/O operations with the Channel Access;
- fsmTimer: is the FSM timer. It keeps the status informations and it executes the FSM when it expires.

6.5.3 Routine for Cavity Tuning

In the new EPICS control system many FSMs have been implemented. As an example for a FSM, the process of cavity tuning will be detailed.

The FSM state diagram is represented in Fig. 6.10. At the beginning, during the "idle" state, the FSM waits for an enable input given by an operator. If the cavity is phase/field locked and the FSM is enabled, the machine changes to "checkfreq" state. In this state the frequency error described in paragraph 5.8.6 is read from the RF controller. As per equation 6.1, if the error read is greater than a programmable threshold the machine goes in "move" state, where the stepper motor acts:

$$steps = [N(1 + G(|err| - thrs)] \cdot sign(err) \cdot S \tag{6.1}$$

N is the minimum step number to do, G the controller gain, S is the sign. The sign indicates the moving direction in order to correct a positive error. The steps so computed are proportional to the frequency error exceeding a given threshold.

In "move" state the end of the movement is waited and if there are no errors the machine moves to "antiBounce" state. A timer is started and after a programmable time the machine comes back to the "checkFreq" state, to restart a new control loop. A wait period is necessary to avoid sampling the input frequency just after the motor movements which affect resonance due to mechanical vibrations. The FSM execution is interrupted when an error is detected or the enable is off: the machine changes to error or end state, respectively. [45]

7 Tests and Results

7.1 Introduction

This chapter describes the validation and qualification of the RF controller. After the development of the FPGA firmware and the essential parts of the driver support, operate the boards contained in the ORC box was possible, therefore the hardware qualification stage could begin. A set of measurements focused on determining some crucial parameters in the RF IOC board and in the RFFE board were performed. Clock jitter, the ADC ENOB and the signal integrity of the high speed serial links between FPGA and converters were assessed. In the RFFE board the crosstalk between adjacent channels and the distortion introduced by the input channels were evaluated. After completion of the EPICS architecture to control the RF controller and the hardware validation, the second stage could begin. It consisted in the installation of the new RF controller with its control system in the ALPI facility in order to operate eight cavities at the same time: four cavities (e.g. one cryostat) with a resonance frequency at 80 MHz and four at 160 MHz. The cavities were locked in SEL mode during the transport of a beam with current of tens of nA of ^{32}S. The performance of the RF control system was validated through specific measurements to make sure it meets the specifications.

This chapter contains two sections. In the first one is presented the results of the measurements carried out to validate the RF IOC and the RFFE boards. In the second section is reported the measurements carried out to validate the RF control system and its functionalities.

7.2 Hardware Validation

The hardware validation tests consisted in off-line measurements made with laboratory test benches. They are detailed in the next sections. Fig. 7.1

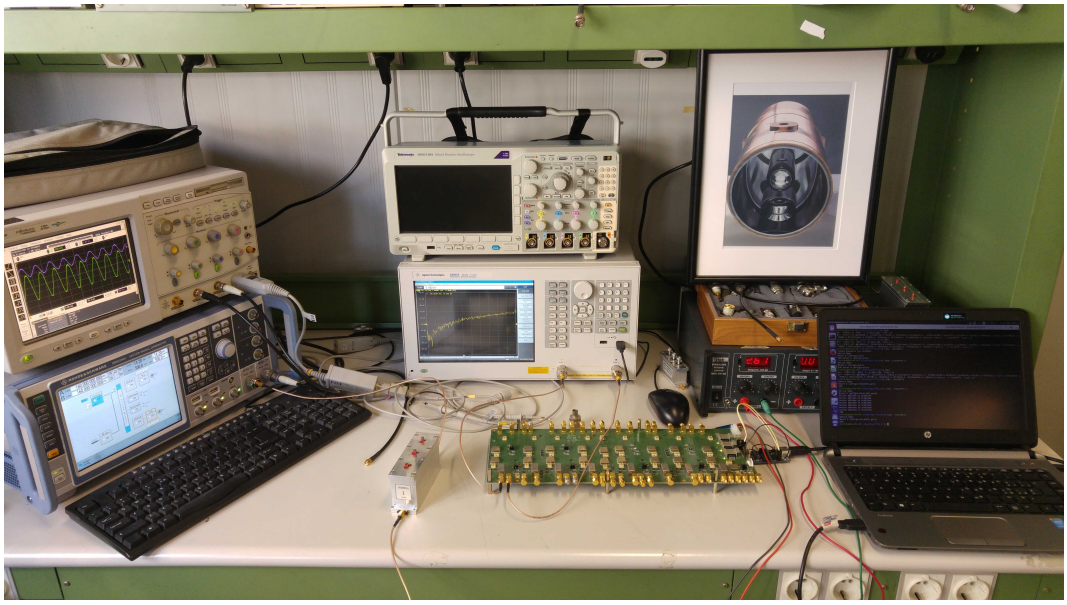


Figure 7.1: Measurement setup to validate the RFFE board.

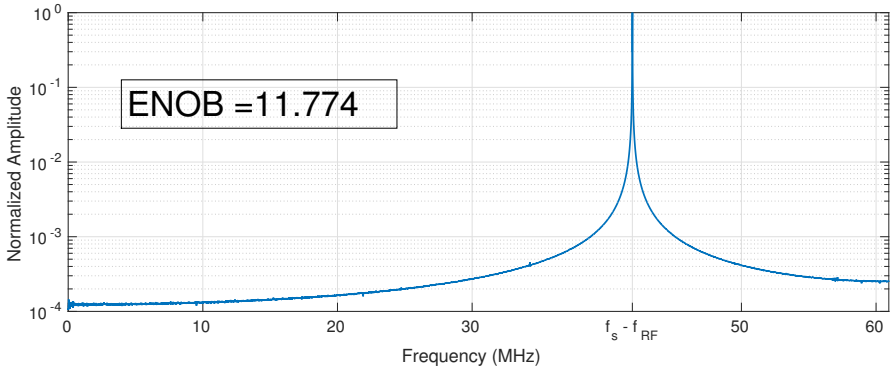


Figure 7.2: Theoretical ENOB at 80 MHz.

shows the measurement setup used to validate the RFFE board. The clock reference and the input test signals were generated using a R&S®SMW200A Vector Signal Generator [46].

7.2.1 Effective Number Of Bits

After setting the parameters of the ADCs, their inputs were shorted on a matched load. This was done in order to measure the electronic noise floor for the different channels. The digitized data were transmitted to the FPGA and here monitored using the chipscope Xilinx software tools and then processed using Matlab®.

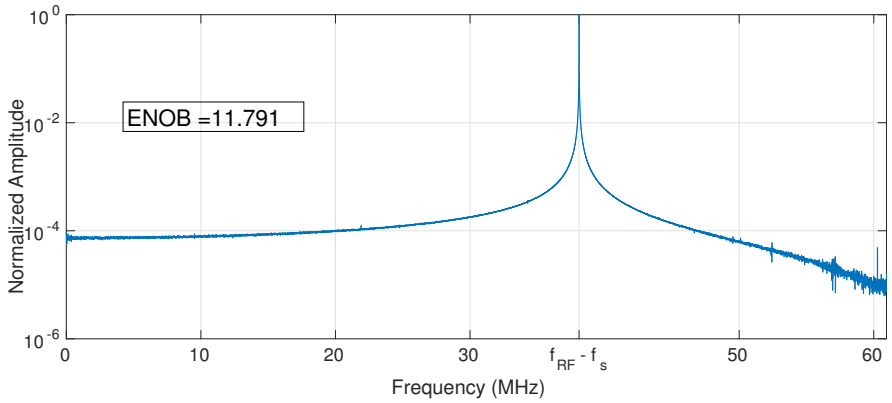


Figure 7.3: Theoretical ENOB at 160 MHz.

The upper limit of the ENOB was so obtained. A sinusoid generated via Matlab® was overlapped to a normally distributed random noise to simulate the quantization noise, in such a way that its $SNR = 6.02N + 1.76$, with $N = 16$. Adding the sampled noise floor and using the equation:

$$ENOB = \frac{SINAD - 1.76 + 20log(\frac{V_{fullscale}}{V_{input}})}{6.02} \tag{7.1}$$

the theoretical ENOB was found. Since all the tests were done in the condition $V_{fullscale} = V_{input}$, equation 7.1 can be rewritten as:

$$ENOB = \frac{SINAD - 1.76}{6.02} \tag{7.2}$$

In particular, if the sinusoid has a frequency of $80\,\mathrm{MHz}$, Fig. 7.2, ENOB= 11.77, while for frequency of $160\,\mathrm{MHz}$, Fig.7.3, ENOB= 11.79. These ENOB values are essentially identical, since they don't depend on the input frequency. These values are very close to the ENOB $\approx$ 12 reported in data sheet of the ADCs used.

Table 7.1: Ideal ENOB.

f_{RF} [MHz]	ENOB
80	11.77
160	11.79

Table 7.2: Real ENOB.

f_{RF} [MHz]	ENOB
80	10.26
160	10.11

In case of signal frequency of $80\,\mathrm{MHz}$ at the input of the ADCs, to clean the test input from undesired harmonics, a narrow band-pass filter centered at $80\,\mathrm{MHz}$ was interposed (section 4.5). The fast Fourier transform magnitude of the sampled input signal at $80\,\mathrm{MHz}$ is shown in Fig. 7.4 and the ENOB, calculated following the equation 7.2, is $\mathrm{ENOB}_{80} = 10.26$. With an input

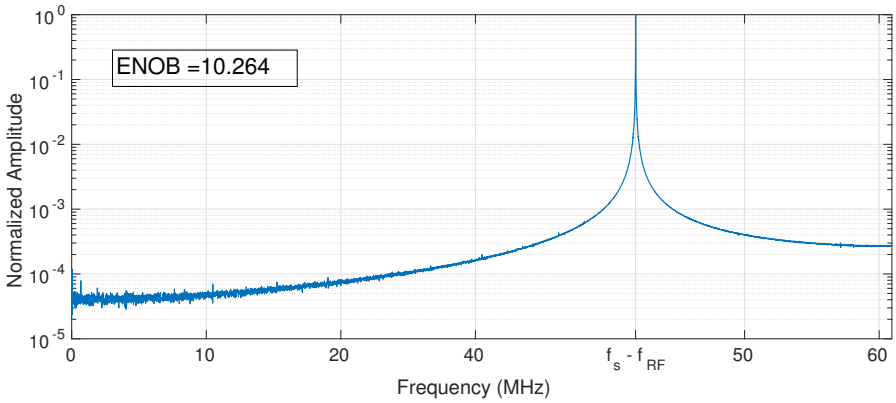


Figure 7.4: Real ENOB at 80 MHz.

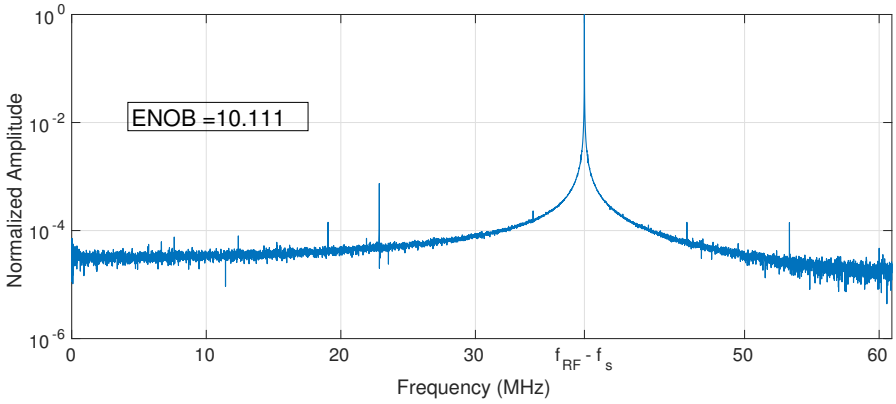


Figure 7.5: Real ENOB at 160 MHz.

frequency of $160\,\mathrm{MHz}$ an $\mathrm{ENOB}_{160} = 10.11$ is revealed, as shown in Fig. 7.5. These values of ENOB fulfill the SNR requirements taken into account in section 4.3.1.

7.2.2 Clock Performance

For the sake of clarity, here are reported the definitions of SNR, SINAD and THD taken from the ADC data sheet [30]:

$$SNR_{dB} = 10 \cdot log\left(\frac{P_s}{P_n}\right) \Rightarrow SNR^* = \frac{P_n}{P_s} = 10^{-SNR_{dB}/10}$$
$$SINAD_{dB} = 10 \cdot log\left(\frac{P_s}{P_n + Pd}\right) \Rightarrow SINAD^* = \frac{P_n + P_d}{P_s} = 10^{-SINAD_{dB}/10}$$

$$THD_{dB} = 10 \cdot log\left(\frac{P_s}{P_d}\right) \Rightarrow THD^* = \frac{P_d}{P_s} = 10^{-THD_{dB}/10} \tag{7.3}$$

where P_s, P_n and P_d represent the power of the fundamental, the power of the noise floor and the power of the first nine harmonics, respectively.

The combination of equations 7.3, holds:

$$SINAD^* = SNR^* + THD^* \tag{7.4}$$

and substituting typical values for the component chosen:

$$SINAD^* \approx SNR^* \Rightarrow SINAD_{dB} \approx SNR_{dB} \tag{7.5}$$

Therefore in this paragraph and more in general in this chapter SINAD and SNR are considered equivalent parameters.

As stated in section 3.5, the main drawback in the DDC technique adopted is that in the signal sampling the clock jitter has a large impact on the ADCs effective resolution.

Combining equations 4.6, 7.2 and 7.5:

$$T_{jitter} = \frac{1}{2\pi f_{IN}} 10^{-(6.02 \cdot ENOB + 1.76)/20} \tag{7.6}$$

Substituting in equation 7.6 the values of table 7.2, a time jitter of 1 ps rms is found. It is the upper limit in the figure of noise of the clocking system that does not deteriorate the ADC performance. Looking at the ADC data sheet the typical value of $T_{aperture}$, from equation 4.7, it is easy to assert $T_{jitter} \approx T_{jitter-External-Clock}$.

The digital oscilloscope used for quantifying the jitter is a 4-channel 20 GSa/s scope with an input bandwidth of 6 GHz, model 54855A [47] from Agilent Technologies. The period jitter measurement floor, according to the oscilloscope datasheet, is $T_{INSTR} = 2$ ps rms. Tests have been carried out using differential probe model E2675A [47] from Agilent Technologies, that has a 7 GHz bandwidth.

We performed period jitter analysis by capturing multiple clock periods using the scope deep acquisition memory. The period jitter is the difference between the measured period and the ideal period within an observation window of at least 10000 cycles [48].

This measurement was taken in order to evaluate the jitter that affects the clock signal at the ADCs inputs. The measurements gave us unexpected

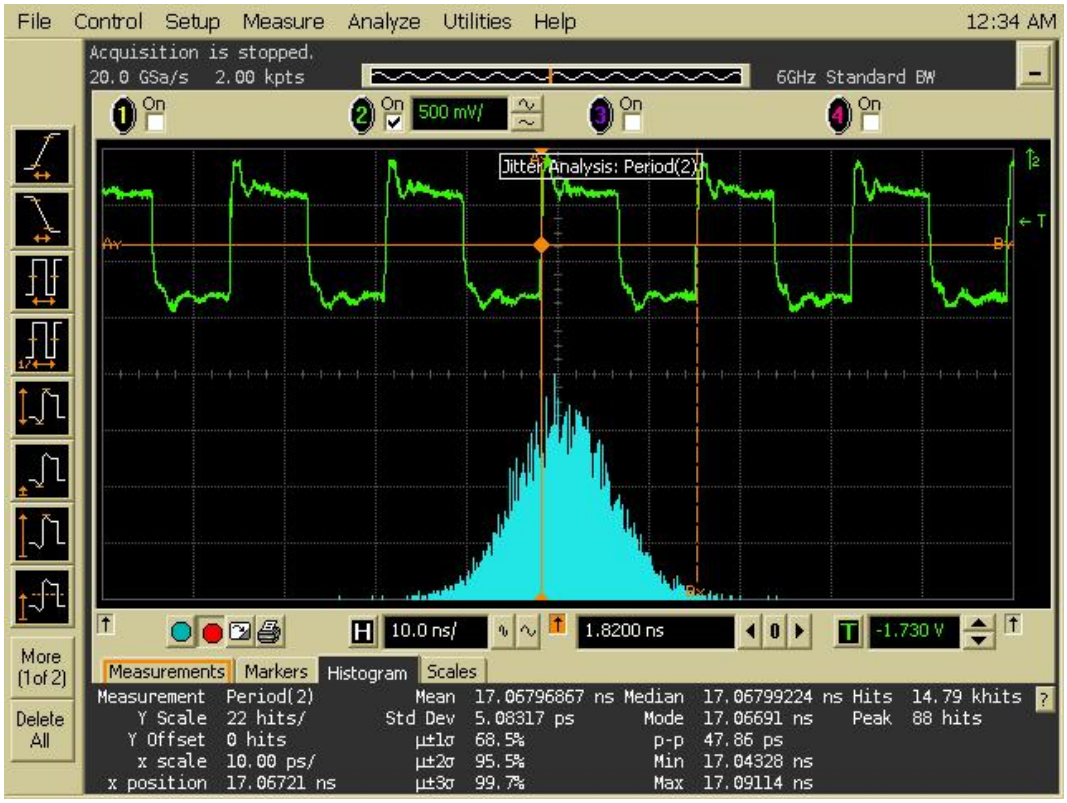


Figure 7.6: Jitter measurement in LMK04828 EVM.

results, because they were not in good accordance with equation 7.6; in particular we found a rms jitter T_{jitter} of 6 ps, instead of 1 ps as expected.

In order to quantify the performance of our measurement setup we took the same measurement with a PLL LMK04828/6 evaluation module (EVM). The EVM was setup with parameters advised by the vendor that hold a rms jitter of 87.8 fs. The measurement taken with our setup is shown in Fig. 7.6: the rms jitter so evaluated is 5.1 ps rms. This result indicates that the digital oscilloscope is uncalibrate. Since measured jitter sums up as:

$$t^2_{MEAS} = t^2_{DUT} + t^2_{INSTR} \tag{7.7}$$

where t_{MEAS}, t_{DUT} and t_{INSTR} are total measured jitter, the jitter of device under test and jitter due to instrument respectively. We have deduced that the jitter measurement floor of our setup amounts to $t_{INSTR} \approx 5$ps rms. This is an indirect confirmation that the total ADC jitter amounts to ≈ 1 ps rms as foreseen by eq. 7.6. Hence you can state that the jitter measurements taken with the measurement setup just described are not reliable.

7.2.3 Serial Links

The high speed serial links between FPGA and converters are one of the critical points in the control card design, as these signals are expected to carry digital data at frequencies in the gigahertz range. As written in 4.3.2, the serial links support the JESD204B protocol. In this section the quality of the serial links between the FPGA and the DACs is examined. Identical considerations can be done for the serial links between FPGA and ADCs.

The DAC input clock divider registers were set in order to bypass dividers. According to the table 31 of the DAC data sheet [25], the data rate of the serial links was set in such a way that:

$$DR = 10 \times F \times K \times f_s \tag{7.8}$$

where DR is the data rate, $F = 2$ is the frame number, K doesn't care since it is bypassed and $f_s = 121.9$ MHz is the sampling frequency. Therefore $DR = 10 \times 2 \times 121.9 \cdot 10^6 = 2.43$ Gbps.

The JESD204B standard defines three speed grade variants, based on OIF Optical standards (OIF-CEI-02.0) [49]. Variants differ for some parameters, a sample of which are reported in table 7.3 and in Fig. 7.7.

Table 7.3: JESD204B requirements.

Parameter	LV-OIF-Sx15	LV-OIF-6G-SR	LV-OIF-11G-SR
Data Rate Max.	3.125Gbps	6.375Gbps	12.5Gbps
Diff. Output Voltage	500-1000 mV	400-750 mV	360-770 mV
Rise/Fall time	≥ 50 ps	≥ 30 ps	≥ 24 ps

The quality of the serial links can be assessed by looking at the eye diagram at the receiving device. It was obtained by superimposing the individual bits sent from the FPGA using a digital oscilloscope. The oscilloscope used is the same described in section 7.2.2, but the probe used is a Solder-in differential probe head with 7 GHz bandwidth, model E2677A [47] manufactured by Agilent Technologies.

The eye diagram, Fig. 7.8, is used to determine the receiver's ability to extract the correct information from the incoming data stream.

The serial links data rate is less than 3.125 Gbps, that is the lower max data rate defined by the JESD204B protocol. It is easy to observe that the eye

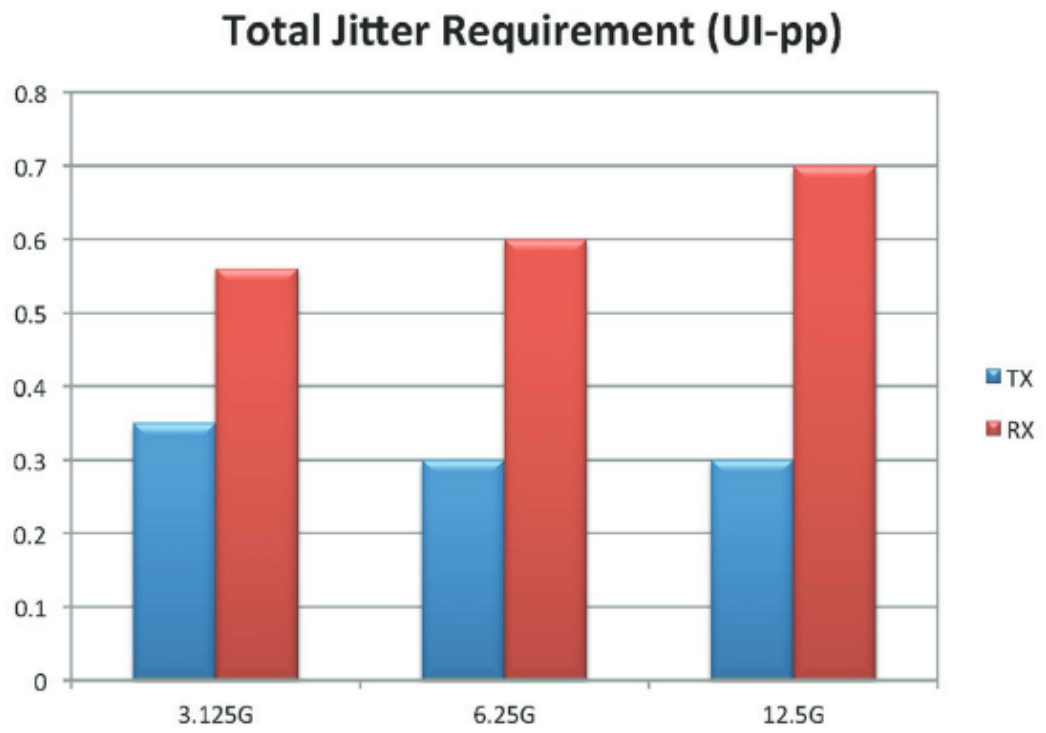


Figure 7.7: Jitter requirement comparison based on maximum link rate. [50]

diagram in Fig. 7.8 matches the requirements written in the first column of table 7.3.

In this context, the jitter is the deviation from the ideal switching point at zero voltage cross. JESD204B standard specifies the jitter requirements for both transmitter (TX) and receiver (RX) in terms of the percentage of the bit period, as shown in Fig. 7.7. The receive jitter measurement turns out to be tighter than the transmit jitter; it indicates how much jitter the receiver can tolerate while still extracting the correct information from the incoming data stream. In the eye diagram context the bit period is commonly called the Unit Interval (UI). From the eye diagram and from the DR, one can find that $UI = 1/DR \approx 411$ ps. In the eye diagram is reported also the jitter measurement done at the receiver and it has a peak-to-peak value of 71 ps. This value is less than 0.35 UI as reported in Fig. 7.7. Therefore the serial links on the RF IOC board match the requirements of a JESD204B serial link with max rate of 3.125 Gbps.

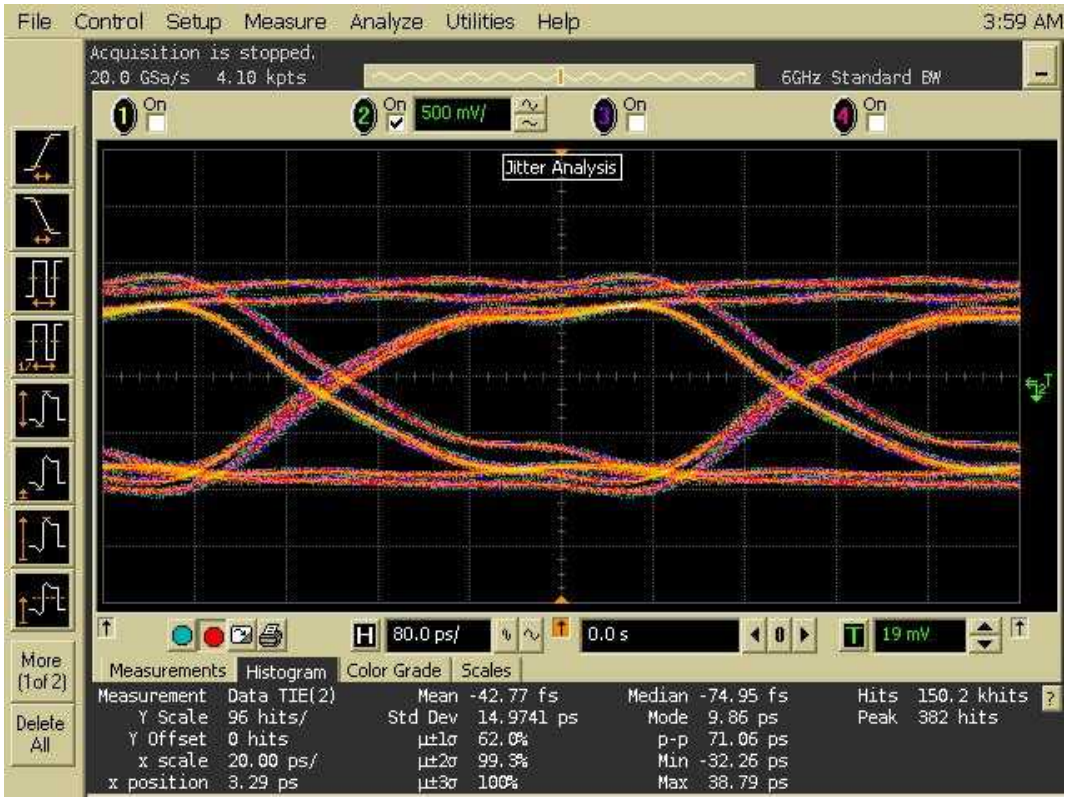


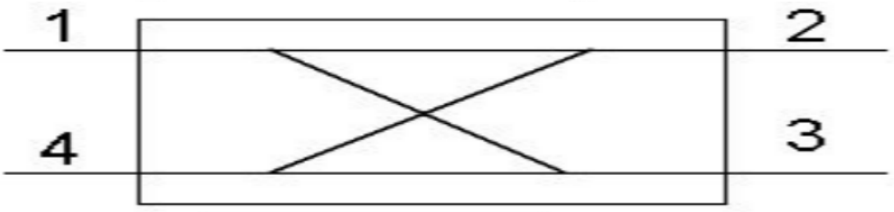
Figure 7.8: Eye diagram of a serial link between a DAC and a FPGA.

7.2.4 Characterization of RFFE Channels

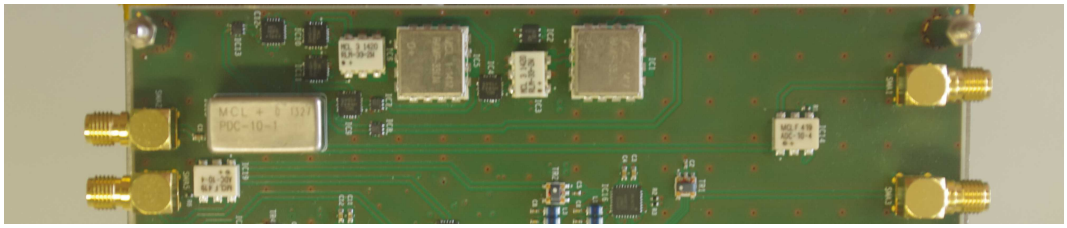
As reported in the paragraph 4.4, the RFFE board is essentially divided into eight identical sections (Fig. 7.9). Each one is formed by an input channel next to an output channel; from the point of view of EMI this can be modeled as a RF four-port network. Port 1 is the input of the ICh, port 2 is the output of the ICh, port 3 is the input of the OCh and port 4 is the output of the OCh.

The scattering parameter formalism, is a convenient way to describe the behavior of each RFFE board section at a given frequency. Every S-parameter is the ratio between a signal coming out of one end (the reflected signal) and a signal going into another end (the incident wave). A four port network is described by a 4x4 scattering matrix.

$$\mathbf{V}^- = \mathbf{S}\mathbf{V}^+ \Rightarrow \begin{bmatrix} V_1^- \\ V_2^- \\ V_3^- \\ V_4^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ V_3^+ \\ V_4^+ \end{bmatrix} \tag{7.9}$$



(a)



(b)

Figure 7.9: a) Representation of a 4 port network b) Section of a RFFE formed by one ICh and one OCh.

The S-parameter terms are: the input return losses (S_{11} and S_{33}), the output return losses (S_{22} and S_{44}), the insertion losses (S_{21} and S_{43}), the reverse isolations (S_{12} and S_{34}) and all the other terms are a measure of the crosstalk between the channels.

The study of the crosstalk is the subject of this section. When a channel is excited by a signal (the aggressor), a portion of it appears in the adjacent channel (the victim) also when there isn't a direct connection. The signal in the aggressor channel induces a noise on the victim channel through the fringe electric field and magnetic field lines between the channels. The noise on the victim channel is superimposed to the useful signal and it propagates till the end of the line.

We measured the numerical values of some scattering matrices. They were found for different frequencies of stimulus signals and for different gain settings, both for input channels and output channels. In order to accomplish these measurements a network analyzer, model E5061B [51] manufactured by Agilent Technologies, was employed. With this instrumentation we could evaluate the S_{11} and the S_{21} parameter. During the measurements the ports not connected to the network analyzer were matched with an external load.

Four scattering matrices are reported. They have been evaluated at different frequencies, 80MHz and 160MHz and for different gains of the input

and output channels. Two configurations of gains were set. In the first configuration, typical gains are set in the same way used to do the test reported in section 7.3. The second configuration represents the worst case, where all the channel gains were set at their maximum value; this configuration might be used only during the first conditioning operations, where the signal picked up from the cavity has a power level of -30 dBm.

The scattering matrix at 160 MHz, with maximum channel gains configuration:

$$\begin{bmatrix} 7.2 \cdot 10^{-3} - j1.2 \cdot 10^{-1} & 2.9 \cdot 10^{-4} + j3.0 \cdot 10^{-4} & -7.0 \cdot 10^{-6} - j3.5 \cdot 10^{-4} & 1.8 \cdot 10^{-5} - j2.6 \cdot 10^{-5} \\ -4.1 \cdot 10^{1} - j8.3 \cdot 10^{1} & -7.1 \cdot 10^{-2} - j1.3 \cdot 10^{-1} & -3.2 \cdot 10^{-3} - j3.1 \cdot 10^{-3} & 3.0 \cdot 10^{-4} - j8.6 \cdot 10^{-4} \\ 1.7 \cdot 10^{-4} - j9.5 \cdot 10^{-4} & 2.2 \cdot 10^{-5} - j1.5 \cdot 10^{-4} & 1.8 \cdot 10^{-2} + j2.3 \cdot 10^{-2} & -3.6 \cdot 10^{-4} - j1.8 \cdot 10^{-3} \\ -8.6 \cdot 10^{-2} + j5.4 \cdot 10^{-2} & -7.8 \cdot 10^{-3} - j6.9 \cdot 10^{-5} & -2.1 \cdot 10^{3} - j5.2 \cdot 10^{2} & 1.2 \cdot 10^{-1} - j3.2 \cdot 10^{-2} \end{bmatrix}$$

The scattering matrix at 160 MHz, with typical channel gains configuration:

$$\begin{bmatrix} 6.6 \cdot 10^{-2} - j3.4 \cdot 10^{-2} & -1.6 \cdot 10^{-1} + j3.0 \cdot 10^{-1} & -8.1 \cdot 10^{-4} + j1.4 \cdot 10^{-3} & -1.4 \cdot 10^{-4} - j1.7 \cdot 10^{-4} \\ 1.1 + j3.1 & -9.8 \cdot 10^{-2} - j1.9 \cdot 10^{-1} & 5.8 \cdot 10^{-3} - j3.6 \cdot 10^{-3} & 5.5 \cdot 10^{-5} + j1.8 \cdot 10^{-4} \\ 4.2 \cdot 10^{-5} - j3.8 \cdot 10^{-5} & 3.0 \cdot 10^{-5} - j1.5 \cdot 10^{-4} & -5.9 \cdot 10^{-2} + j4.0 \cdot 10^{-2} & -3.2 \cdot 10^{-4} - j2.8 \cdot 10^{-3} \\ 8.7 \cdot 10^{-4} - j2.9 \cdot 10^{-3} & -4.7 \cdot 10^{-3} - j2.6 \cdot 10^{-4} & -3.1 \cdot 10^{2} - j2.5 \cdot 10^{2} & 1.2 \cdot 10^{-1} - j5.1 \cdot 10^{-2} \end{bmatrix}$$

The scattering matrix at 80 MHz, with maximum channel gains configuration:

$$\begin{bmatrix} 1.1 \cdot 10^{-1} - j5.6 \cdot 10^{-2} & -2.9 \cdot 10^{-4} - j4.1 \cdot 10^{-4} & -7.5 \cdot 10^{-5} + j1.5 \cdot 10^{-4} & 2.4 \cdot 10^{-5} + j4.0 \cdot 10^{-6} \\ -8.2 \cdot 10^{1} + j5.1 \cdot 10^{1} & 5.3 \cdot 10^{-2} - j1.2 \cdot 10^{-1} & 6.4 \cdot 10^{-4} + j5.8 \cdot 10^{-3} & 1.6 \cdot 10^{-5} + j6.7 \cdot 10^{-4} \\ 1.8 \cdot 10^{-4} + j4.4 \cdot 10^{-4} & 7.7 \cdot 10^{-5} + j7.0 \cdot 10^{-6} & -2.7 \cdot 10^{-1} + j1.2 \cdot 10^{-1} & 1.2 \cdot 10^{-3} + j1.8 \cdot 10^{-3} \\ 4.9 \cdot 10^{-2} + j3.3 \cdot 10^{-2} & 3.4 \cdot 10^{-3} - j1.2 \cdot 10^{-3} & 2.3 \cdot 10^{3} + j1.1 \cdot 10^{3} & 2.2 \cdot 10^{-2} + j1.4 \cdot 10^{-1} \end{bmatrix}$$

The scattering matrix at 80 MHz, with typical channel gains configuration:

$$\begin{bmatrix} 5.3 \cdot 10^{-2} + j1.2 \cdot 10^{-2} & -1.7 \cdot 10^{-1} - j2.9 \cdot 10^{-1} & 4.9 \cdot 10^{-4} - j7.4 \cdot 10^{-4} & 1.2 \cdot 10^{-4} - j6.5 \cdot 10^{-5} \\ -2.7 - j1.9 & 1.0 \cdot 10^{-1} - j1.7 \cdot 10^{-1} & -2.5 \cdot 10^{-3} + j1.6 \cdot 10^{-3} & -1.0 \cdot 10^{-4} + j5.2 \cdot 10^{-5} \\ -2.5 \cdot 10^{-5} + j1.3 \cdot 10^{-5} & 6.9 \cdot 10^{-5} + j1.1 \cdot 10^{-5} & -2.7 \cdot 10^{-1} + j1.2 \cdot 10^{-1} & 1.8 \cdot 10^{-3} + j2.8 \cdot 10^{-3} \\ -6.5 \cdot 10^{-4} + j1.5 \cdot 10^{-3} & 1.7 \cdot 10^{-3} - j4.9 \cdot 10^{-4} & 3.6 \cdot 10^{2} + j2.7 \cdot 10^{2} & 4.5 \cdot 10^{-2} + j1.3 \cdot 10^{-1} \end{bmatrix}$$

An easier way to evaluate the S-parameter terms is to compute their magnitudes in decibel:

$$S_{nm}dB = 20 * \log(|S_{nm}|) \tag{7.10}$$

The main crosstalk parameters considered are the S_{41} and the S_{23}. Their values in dB, for different configurations, are representative of the crosstalk at the input of the power amplifier due to the signal picked up from the cavity (the S_{41} term) and the crosstalk at the input of the ADC due to the signal at the output of the DAC after being filtered (the S_{23} term). These values are reported in tables 7.4 and 7.5.

Table 7.4: Measurement for typical gain setting.

f_{RF} [MHz]	$S_{41}dB$	$S_{23}dB$
80	-55.6	-50.5
160	-50.3	-44.6

Table 7.5: Measurement for maximum gain setting.

f_{RF} [MHz]	$S_{41}dB$	$S_{23}dB$
80	-20.0	-46.95
160	-24.5	-43.4

Other scattering matrices were measured, taking as victim and aggressor channels that belong to different sections, also for sections placed at the opposite sides of the board. The S-parameters found with these last measurements are similar to those found before, but scaled down by a factor proportional to the distance between the channels considered for the measure.

7.2.5 Distortion of the RFFE Input Channels

Care must be taken to avoid significant distortion and noise corruption for the signals picked up from cavities, that are attenuated or amplified by the RFFE input channels, because PI loops will do their best to counteract these errors even if they do not relate to the physical process of interest. In this section the sensitivity of the input channels to these disturbances is evaluated.

As illustrated in section 4.4, the input channels have to adapt the power signal levels within a range from -30 dBm to +33 dBm. The RFFE input channel is essentially an amplifier with a programmable gain from -22.5 dB to 31 dB, formed by a common programmable attenuator and three different selectable paths: the upper path is a transmission line, the middle path has one amplification stage and the lower path two amplification stages.

The parameter chosen to evaluate the sensitivity of each input channel is the Total Harmonic Distortion (THD):

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + \cdots + V_{10}^2 + N^2}}{V_1} \tag{7.11}$$

where V_i is the RMS voltage of the i-th harmonic, $i = 1$ is the fundamental frequency and N is the rms voltage of the noise.

The measurement was performed injecting at the input a sine wave with a power from -30 dBm to +33 dBm. Therefore the corresponding output was sampled by the digital oscilloscope and so the signals were elaborated

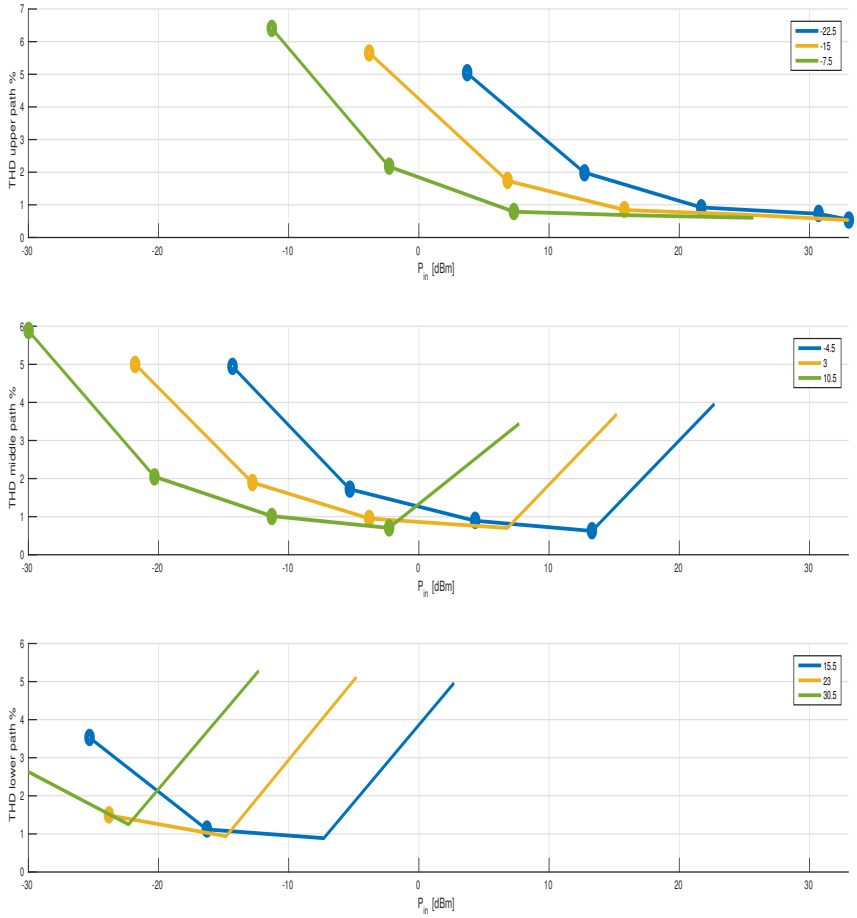


Figure 7.10: Percentage THD of the ICh for different gains at 80 MHz.

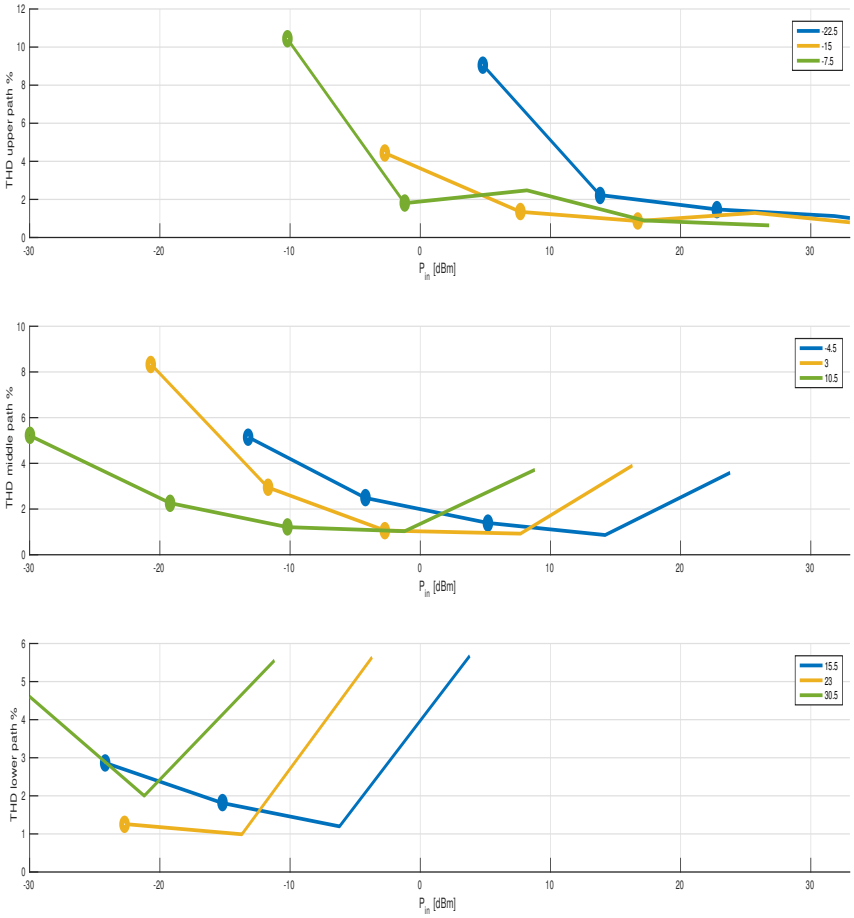


Figure 7.11: Percentage THD of the ICh for different gains at 160 MHz.

using Matlab®and its *thd()* built-in function. The number of superior harmonics taken to evaluate the THD is nine. Some plots representing the THD expressed in percentage are shown in Fig. 7.10 and in Fig. 7.11.

In this context, the THD, at a given frequency, is assessed with respect to the ENOB reported in table 7.2. The minimum signal level, expressed as peak value, that can be measured from the ADC is:

$$V_{min} = \frac{V_{fullscale}}{2^{ENOB}} \tag{7.12}$$

Therefore the channel is considered good enough if the fundamental harmonic level at the output of the channel (Vo_1), multiplied by THD is less than V_{min}, that is:

$$Vo_1 \times THD < V_{min} \tag{7.13}$$

In Fig. 7.10 and in Fig. 7.11, for a given frequency, the operating points (input power, channel gain) that fulfill the inequality 7.13 are marked with a star.

7.3 Radio Frequency Control System Validation

The evaluation of the performance of the RF control system consisted in the measurement of general parameters like stability, overshoot, settling time and steady state errors, besides of course its overall suitability for the task at hand.

During the first test the performances of the phase and amplitude feedback control loops, concerning the rejection of disturbances and the ability of following a reference signal were evaluated. In the second test the suitability of the prototype RF controller has been tested by measuring the amplitude and phase stability.

The data reported in the next sections were probed using the Integrated Logic Analyzer(ILA), one of the ChipScope Pro®tool provided by Xilinx. ILA is a customizable logic analyzer core that can be used to monitor the internal signals in the firmware of the FPGA. ILA can acquire 2^{17} samples at maximum and sample them synchronously with redefined firmware clock. During the tests, the ILA could monitor the signal for a window time of $t_w = 2.2s$ and multiple and continue acquisitions were taken. In the pictures of the next sections a maximum of 50 ms of the recorded data are shown.

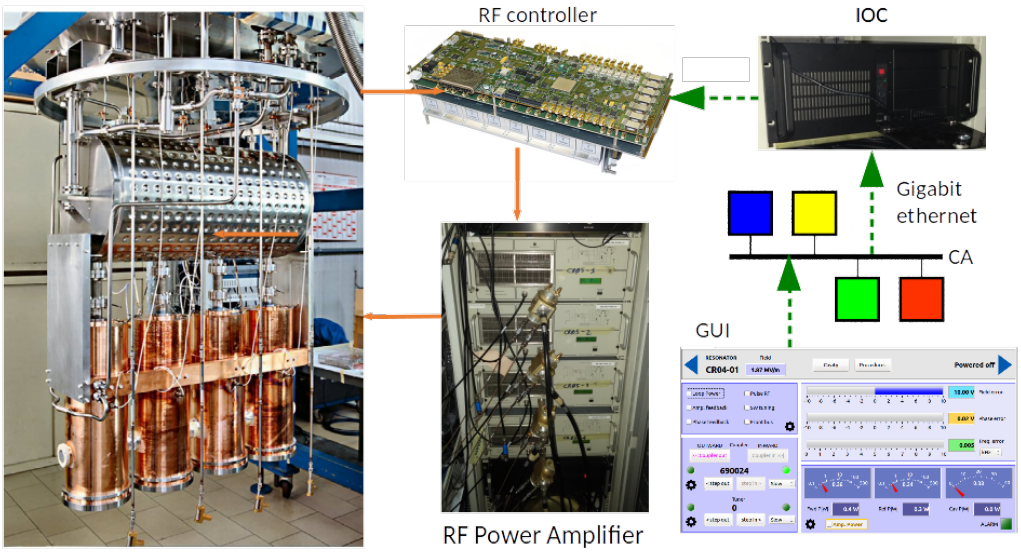


Figure 7.12: Measurement setup during the RF control system validation.

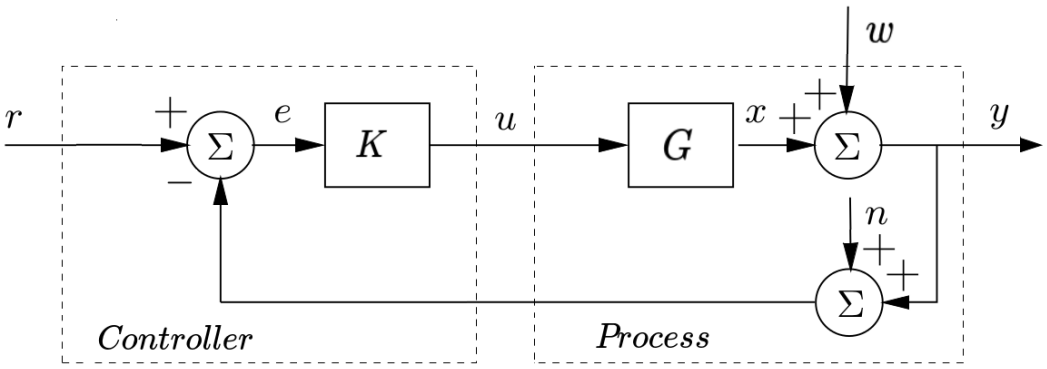


Figure 7.13: Block diagram of a basic feedback loop.

The measurement setup used is reported in Fig. 7.12.

7.3.1 Performances of the Control Loops

From equations 3.9 and 3.10 there are only two transfer functions to describe how the system reacts to plant disturbances and measurement noise and how it reacts to references changes. Since the two functions are complementary, the study of one transfer function gives insight for the other.

Looking at the Fig. 7.13, each block or signal can be assigned to a real device or signal, as:

- the plant G is formed by the chain: DAC housed in the RF IOC, helical filter, RFFE output channel, power amplfier, QWR cavity and pick-up antenna;

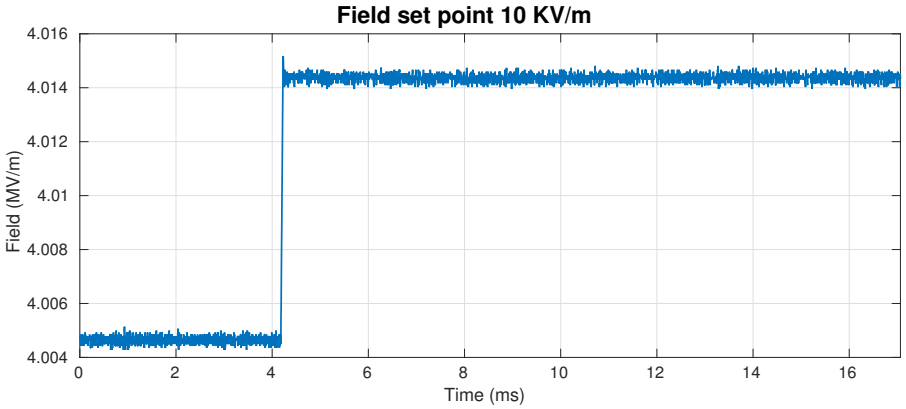


Figure 7.14: Step response of the field amplitude when its set-point is changed, for a medium beta cavity.

- the plant disturbances w are the microphonics and the slow frequency drifts described in section 3.3;
- the measurement noise n is essentially composed by the ENOB, the crosstalk between channels in the RFFE and their distortion;
- the tracking errors are referred as magnitude (or amplitude) error and phase error in Fig. 5.8;
- the controller is implemented by a PI controller in FPGA.

From tests in the field it turns out that the measurement noise is negligible with respect to the plant disturbances. Therefore it can be ignored in the block diagram, and the equations 3.9 and 3.10 become:

$$Y(s) = \frac{1}{1 + K(s)G(s)} W(s) + \frac{K(s)G(s)}{1 + K(s)G(s)} R(s) = \\ = S(s)W(s) + T(s)R(s) \tag{7.14}$$

$$E(s) = \frac{1}{1 + K(s)G(s)} (R(s) - W(s)) = \\ = S(s)(R(s) - W(s)) \tag{7.15}$$

The behavior of plant G in working condition is actually very difficult to evaluate in terms of poles, zeros or frequency response. Therefore the response of the transfer function is analyzed, by studying its step responses when the set-points of phase and amplitude are changed.

The step response can be described essentially by four parameters: the rise time, the eventual overshoot, the settling time and the ringing. The analysis

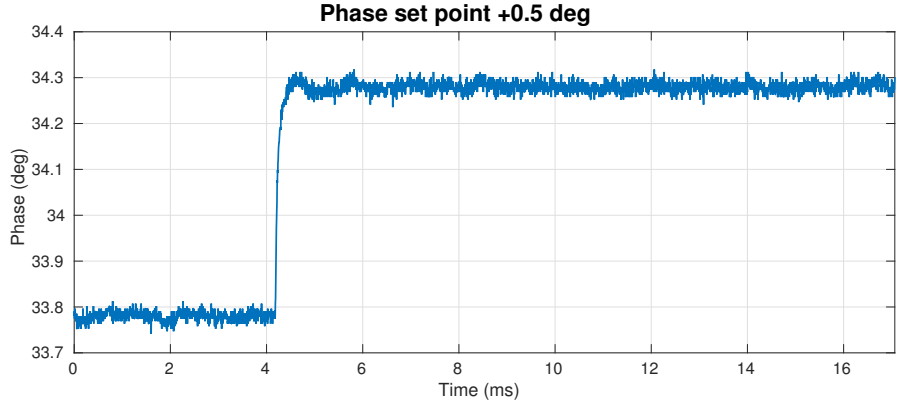


Figure 7.15: Step response of the field phase when its set-point is changed, for a medium beta cavity.

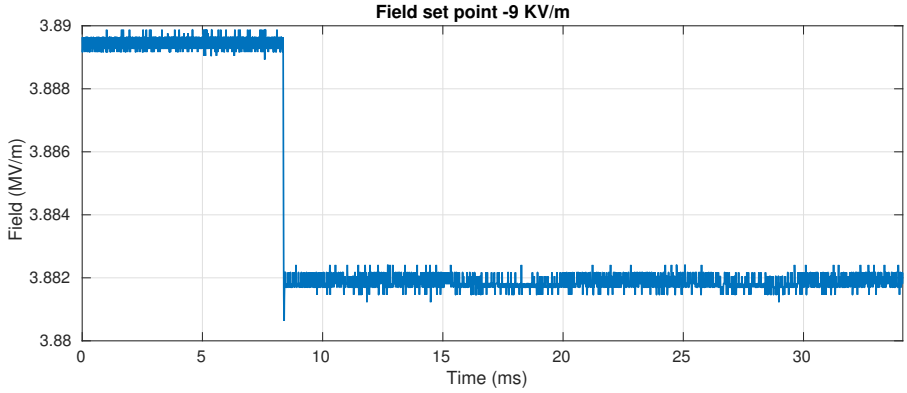


Figure 7.16: Step response of the field amplitude when its set-point is changed, for a low beta cavity.

of these parameters gives information about the system stability, the ability to reach a stationary state when starting from another state and some information about the frequency resonance.

Fig. 7.16 and 7.17 report the step response of the measured signal y when the field and phase set-points have a step discontinuity for a low beta cavity. The ringing presence in Fig. 7.17, is not an effect of the step set-point changes, but it is caused by the plant disturbances $w(t) \xrightarrow{\mathcal{L}} W(s)$. Looking at the period of the disturbance, it is likely due a mechanical vibration, propagated to the cavity by the vacuum pump mechanical setup. In fact this ringing is visible only in the step response of a low beta cavity, since its wall is thinner than that of a medium beta cavity, hence it is more susceptible to external disturbances that propagate to the cavity. Indeed of the ringing is not present in a medium beta cavity (Fig. 7.14, 7.15).

Step response is a powerful tool to understand if the proportional and integral gains of the PI controller implemented in FPGA are set properly. Since

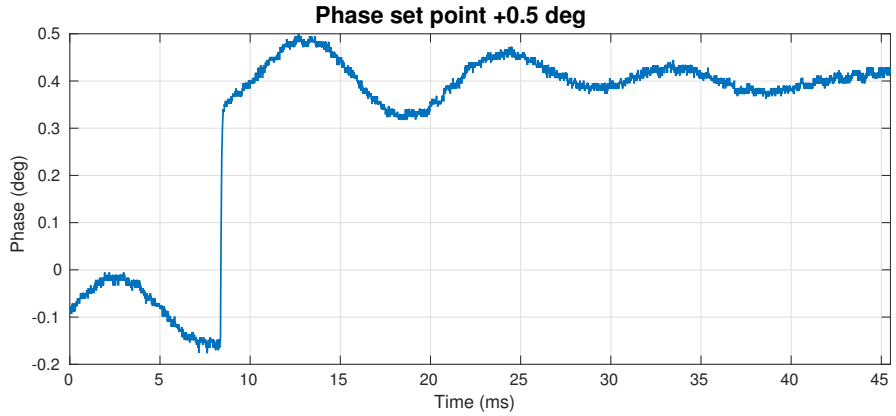


Figure 7.17: Step response of the field phase when its set-point is changed, for a low beta cavity.

the step responses, is fast both in phase and in amplitude, without overshoots or ringings and the steady state is achieved, it is easy deduce that the PI controllers have been tuned optimally. In the other hand, it is questionable if the tuning done guarantees enough stability margin.

7.3.2 Stability of the Control Loops

As stated in section 4.3.1, in order to guarantee an optimal acceleration of the beam, the stability of the electrical field into the cavities (for a heavy ion Linac like ALPI) requires a phase stability of at least $0.5°$ and a gradient stability of about 0.5% rms. Suitable indicators to validate the stability performance of the RF IOC board are the rms value of the residual errors both for phase and magnitude parameters.

Typical residual errors in time domain are given in Fig. 7.18, 7.19, 7.20 and 7.21. Concerning low beta cavity in Fig. 7.19, it presents the same ringing effect observed in the step response described in the previous paragraph. Furthermore, there is an overlapped oscillation at approximately 1500 Hz. This frequency is an high order eigenfrequency of the central conductor for this kind of cavity. From graphs on Fig. 7.20 and 7.21 it is hard to extrapolate any useful information.

A better visualization of the different frequencies perturbations affecting the cavities is achieved calculating the integrated rms detuning spectrum [18]:

$$\Delta d(f_n)_{rms} = \frac{\sqrt{\sum_1^n |\mathcal{F}[\Delta d(t)]_i|^2}}{\sqrt{2}} \tag{7.16}$$

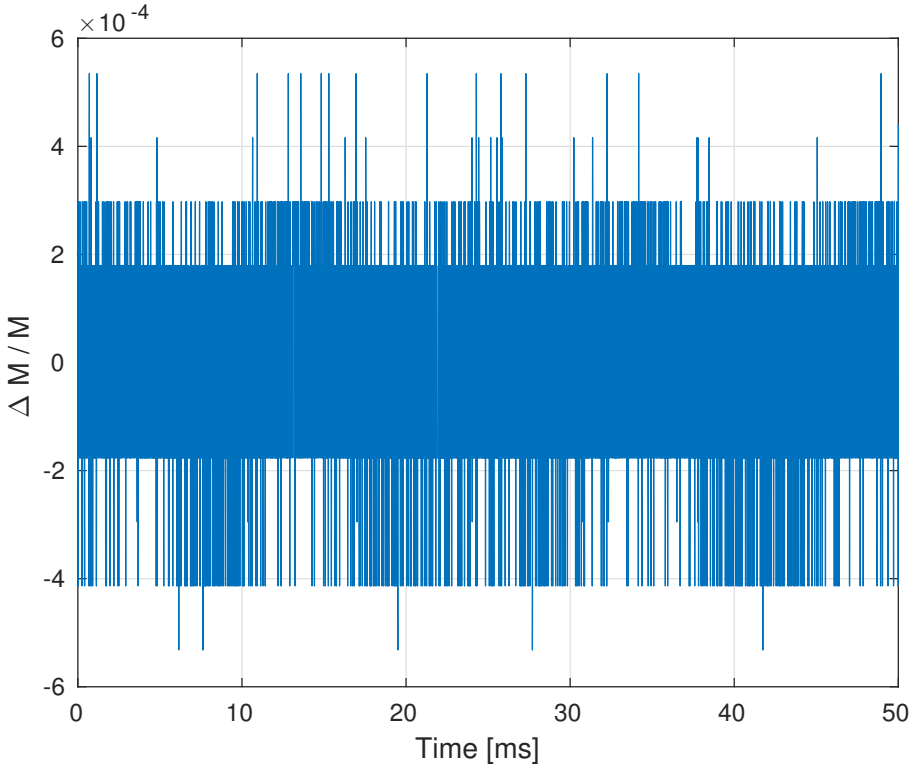


Figure 7.18: Field amplitude error for a low beta cavity operating in SEL.

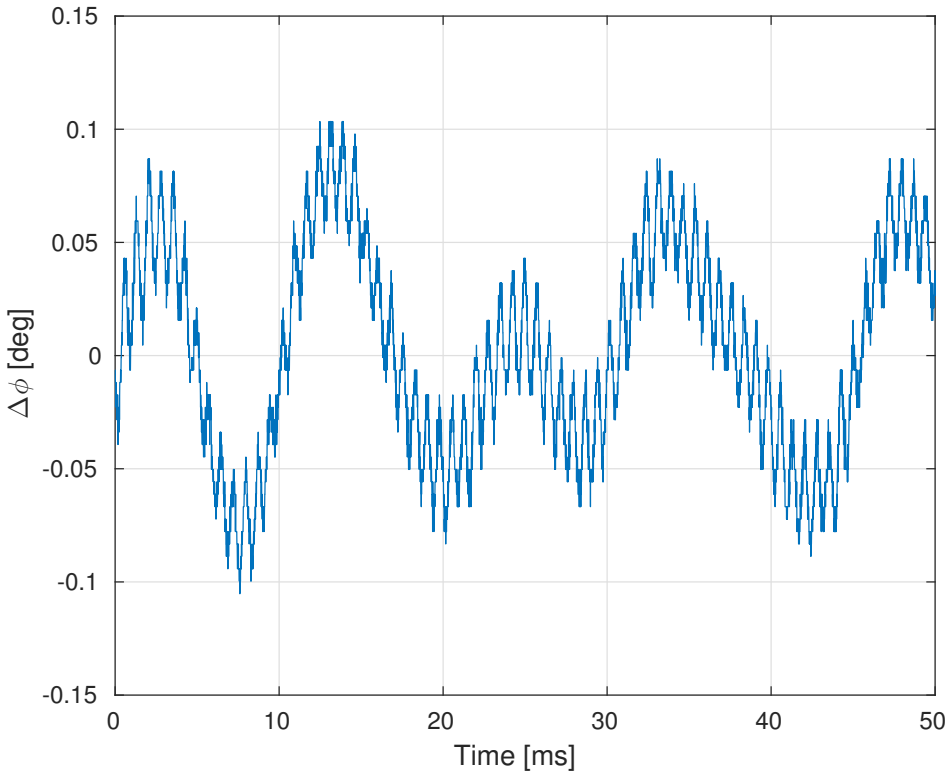


Figure 7.19: Field phase error for a low beta cavity operating in SEL.

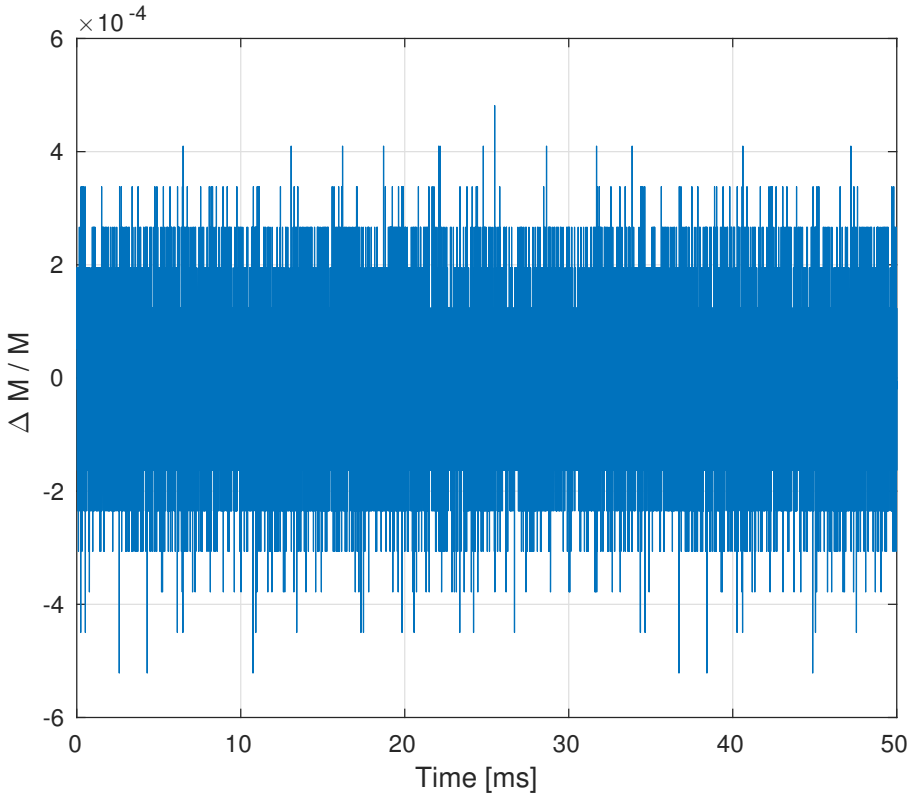


Figure 7.20: Field amplitude error for a medium beta cavity operating in SEL.

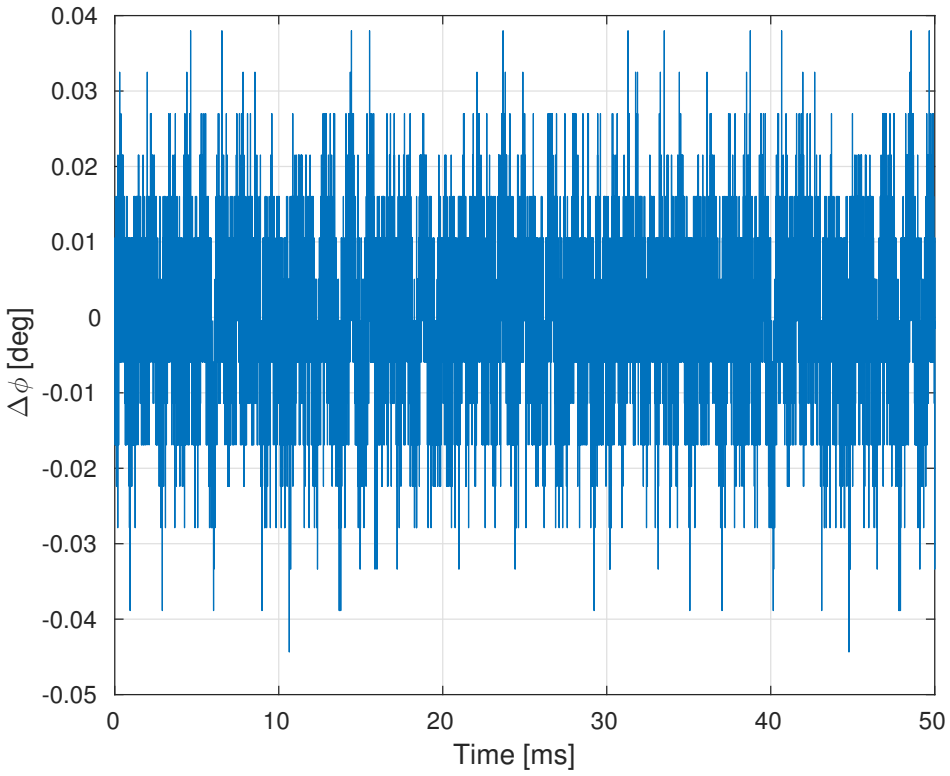


Figure 7.21: Phase amplitude error for a medium beta cavity operating in SEL.

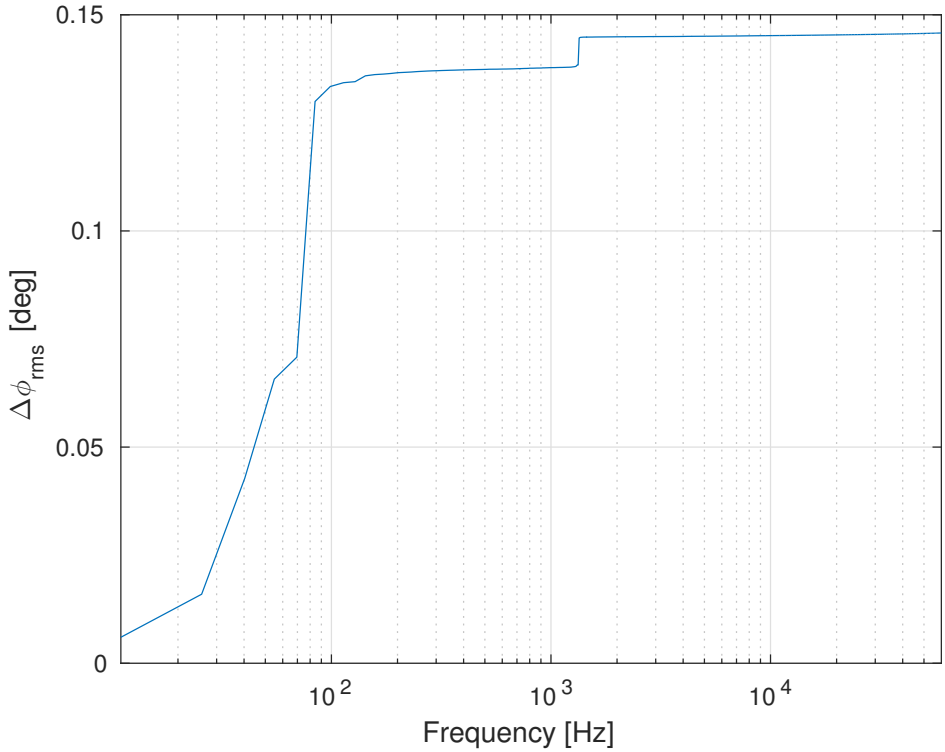


Figure 7.22: Cumulative spectrum of the phase error for a low beta cavity SEL driven.

where $\Delta d(f_n)_{rms}$ represents the spectrum of the time series collected. It is obtained accumulating the absolute squared values of the Fourier components $\mathcal{F}[\Delta d(t)]_i$, up to the perturbation frequency f_n.

Fig. 7.22 shows the integrated phase error for a low beta cavity. This graph confirms the interpretations previously done for the Fig. 7.19.
For both integrated field amplitude errors graphs Fig. 7.23 and 7.25, there is a source of noticeable amplitude error around the 10 KHz. Its origin is still unknown. The perturbation only appears in the magnitude field measurement.

From Fig. 7.22, 7.23, 7.24 and 7.25, it appears evident that the total value of the phase fluctuation is $0.145°$, while for the field fluctuation is $6.9 \cdot 10^{-4}$ rms. These values adhere to the requirements typical of a heavy ion Linac like ALPI, that is a phase stability of at least $0.5°$ and a gradient accuracy less than 0.5% rms.

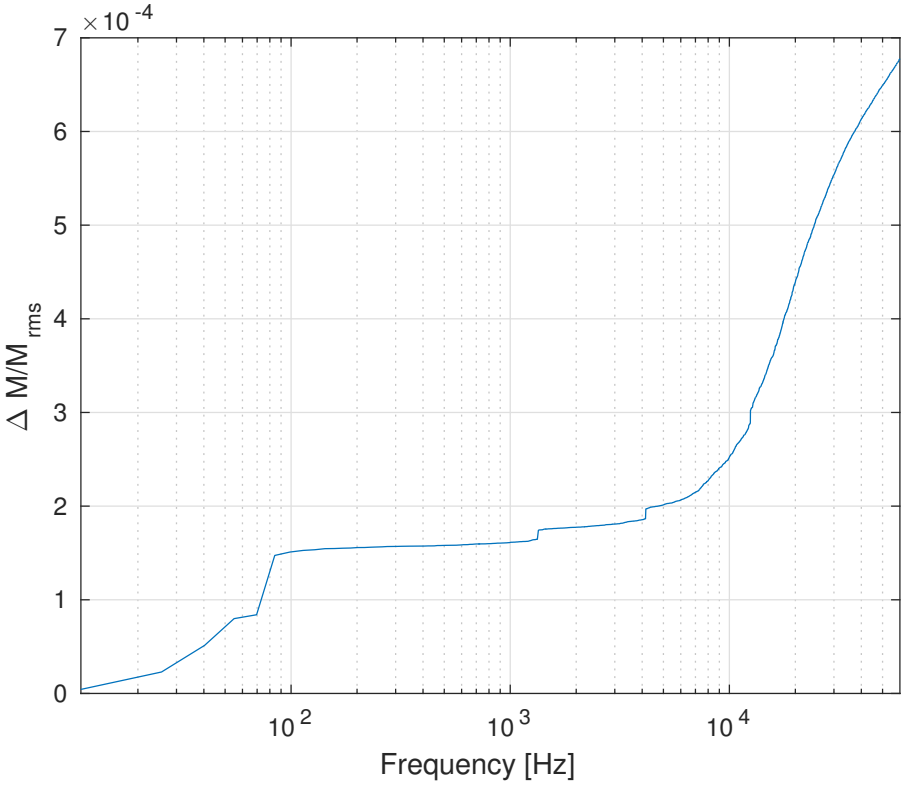


Figure 7.23: Cumulative spectrum of the amplitude error for a low beta cavity SEL driven.

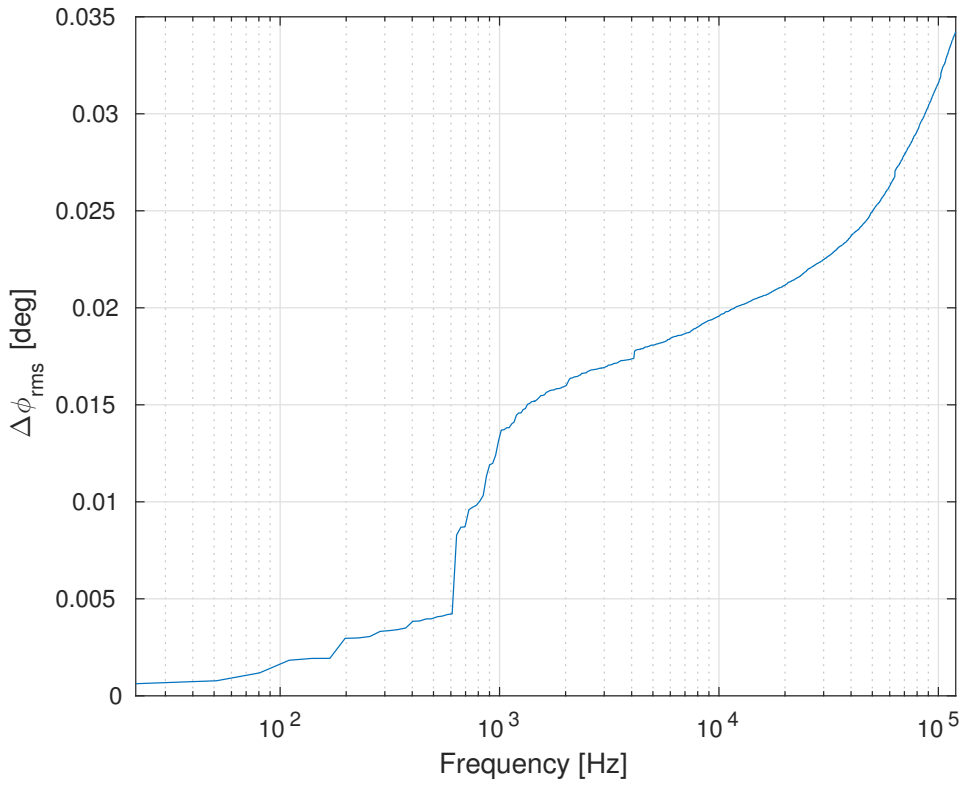


Figure 7.24: Cumulative spectrum of the phase error for a medium beta cavity SEL driven.

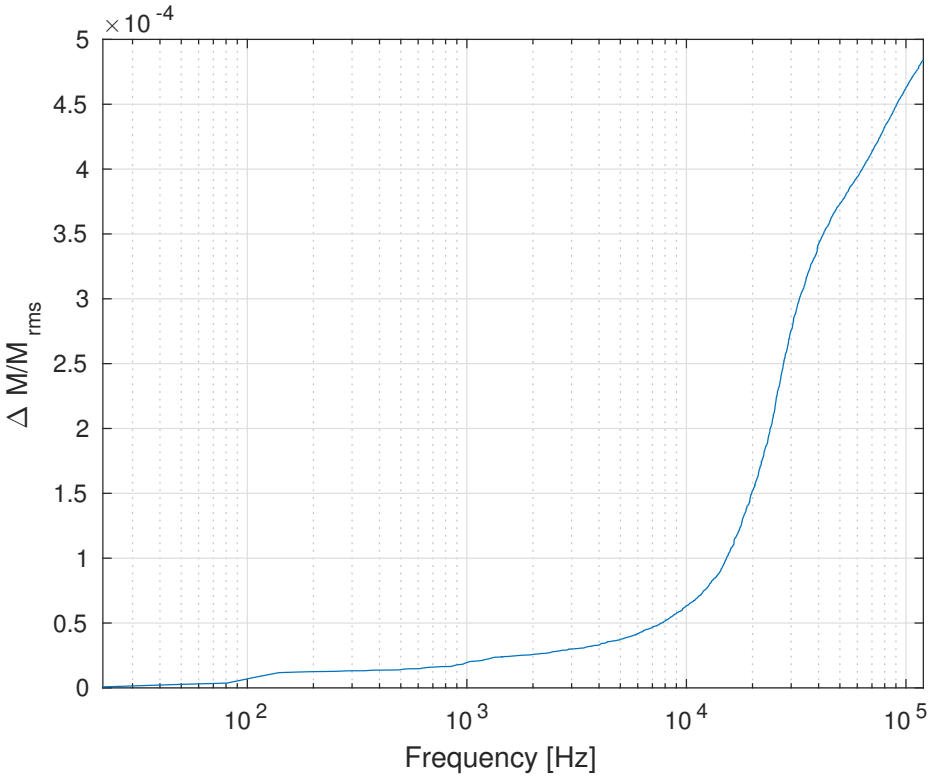


Figure 7.25: Cumulative spectrum of the amplitude error for a medium beta cavity SEL driven.

8 Conclusions

In this document was presented a new digital radio frequency controller. The system has been developed and commissioned at the LNL and has been designed to work in a wide range of frequencies, thus spanning all types of RF structures of the final SPES configuration, both in normal or superconducting conditions. It can be configured to work in generator driven resonator or in self excited loop mode. The control algorithms are implemented in a FPGA, a re-programmable hardware, increasing the adaptability and the programmability of the controller. Parameters and signals internal to the FPGA can be set and read from the particle accelerator control system, that it is designed using the EPICS framework. This architecture improves flexibility, reliability and speeds up the software development. The remarkable features of the controller are essentially two: the first is the utilization of a complex phase modulator in SEL mode to compensate the disturbances that affect cavities, thus disentangling the operations of the phase and amplitude control loops. The second is the digitalization of the signals picked up from the cavities through a DDC technique. The measurements have shown that this system guarantees a phase and an amplitude stabilization in excess of those required for a heavy ion linear accelerator as ALPI.

The RF application, in this document, has been described in its main blocks. For each block the main issues are faced and the choices taken to solve or reduce the problems are argued. All the boards housed in the ORC box have been described. Particular attention was paid for the main and more challenging boards: the RF IOC and the RFFE. For all the boards every integrated circuit hosted in them was described as well as the communication between ICs and boards. The fundamental IC is the FPGA. Hence the firmware blocks, written in VHDL, were treated in detail. Finally the software, the lower layer in EPICS architecture, necessary for the communication with the hardware was detailed. Upon completion of the hardware-firmware-software development, the boards were ready to be validated. The DDC technique demands for ADCs a low jitter clock. Therefore measurements to evaluate the jitter clock and the ENOB of the analog digital

converters were taken.
The communication between data converters and FPGA is based on JESD204B. In order to qualify these high speed serial links the signal integrity was studied. After the validation of the RF IOC board, some tests were done also for the RFFE board. The quality of its input channels has been validated in terms of signal distortion and crosstalk between channels.

The measurements done to qualify the hardware boards and to evaluate the stability and the performance of the RF control system have been accomplished through an ion beam campaign with the Linac itself during May 2016. Therefore the hardware developed is now ready for mass production in order to replace the existing analog controllers, since it has proved to have better performances.

8.1 Contributions

As introduced in the abstract, the fifth, sixth and seventh chapters collect most of my personal contributions made to the development of the novel RF control system for ALPI. I have actively contributed in many ways of the firmware and software developments, as well as to do the tests, qualification and revision of the RF controller.

Firmware development took a significant part of my time due to inherent complexity of control, configuration and operation of FPGA transceivers concerning the JESD204B protocol. I developed, qualified and implemented some digital processing blocks that are in the amplitude and phase control loops. I also carried out the implementation and integration of the ethernet based slow control centered around the IPbus software development in the EPICS framework using C++, focusing on the driver support for the distributed configuration of all the chips in the boards that make up the controller.

With a deep insight on the firmware and software ecosystem I could carry out an extensive test and qualification phase: from laboratory tests for assessing the performance of the hardware in terms of noise, ENOB, SINAD, THD and crosstalks, to in-beam tests with cold cavities in the fully operational Linac during a physics campaign.

Part of this work appears in the [41], [52] and [53].

8.2 Outlook

So far, all operations related to accelerator configuration have been done by the beam accelerator scientists. Given required species and energies they perform an off-line simulation of the accelerator complex with a theoretical model of the machine which accounts for particle interactions with machine instrumentation and space charge effects; as a result, settings for magnetic and electrostatic lenses as well as fields and phases for cavities are obtained. Unfortunately particle accelerators host lots of complex non linear physical phenomena and they involve many interacting systems with the requirement of being mostly insensitive to long term changes in individual components (beam on target could lost weeks). All the deviations of physics based simulations and system design from the installed system constitute a real challenge for the design of control systems, aiming at practical or complete automation of the timing process of a particle accelerator.

In the future we envisage to test an approach that stems from the adoption of a matrix-based theoretical model of the machine instrumentation: this model has fast computation times and can be deployed almost in real-time. We will use the model in sections corresponding to machine sections that during the tuning process are operated sequentially and we will feed the on-line model with data sampled from the field via beam diagnostic instrumentations. We hope to be able to compare theoretical and field results so to devise a control strategy for at least partial automatic tuning operation. In the process the RF controller will be augmented with firmware and software to support the process.

Automated tools for optimal cavity setting up can now be studied: link LLRF variables to beam longitudinal dynamics metrics and quantify their impact on beam acceleration is crucial for a correct acceleration. Furthermore the flexibility given us from a digital control system, based on FPGA, gives us the opportunity to implement more advanced control methods in order to reach better performances.

A Beam Loading

A.1 Introduction

The next pages report the dissertation done by Sergey Belomestnykh during the Superconducting RF School 2017 [13].

S. Belomestnykh
August 2002

Formulae for the waves in a waveguide terminated by a beam-loaded cavity

Waveguide impedance transformed to cavity is

$$Z_{\mathrm{WG}} = R/Q \cdot Q_{\mathrm{ext}},$$

where *R/Q* is the cavity specific impedance and Q_{ext} is the external quality factor. The cavity coupling factor is then defined by the ratio of cavity intrinsic quality factor Q_0 and its external *Q*:

$$\beta = \frac{Q_0}{Q_{\mathrm{ext}}},\ \beta + 1 = \frac{Q_0}{Q_{\mathrm{L}}},$$

here Q_{L} is the cavity loaded quality factor. The waveguide is terminated by the cavity with impedance

$$Z_{\mathrm{c}} = R_{\mathrm{c}} + X_{\mathrm{c}} = \frac{R/Q \cdot Q_0}{1 + i\tan\psi},\ \tan\psi = 2Q_0\frac{\Delta\omega}{\omega},$$

where ψ is the cavity tuning angle and $\Delta\omega$ is the cavity resonance detuning from the RF frequency, and in parallel by the beam with admittance

$$Y_{\mathrm{b}} = G_{\mathrm{b}} + B_{\mathrm{b}} = \frac{I_{\mathrm{b}}}{V_{\mathrm{c}}} e^{i\varphi_0},$$

ϕ_0 is the beam phase. Then the total load is

$$G = \frac{1}{R/Q \cdot Q_0} + \frac{I_{\mathrm{b}}}{V_{\mathrm{c}}}\cos\varphi_0,$$
$$B = \frac{\tan\psi}{R/Q \cdot Q_0} + \frac{I_{\mathrm{b}}}{V_{\mathrm{c}}}\sin\varphi_0,$$
$$Y = G + B = \frac{1}{Z}.$$

The reflection coefficient for such load is

$$\Gamma_{\mathrm{V}} = \frac{V_{\mathrm{refl}}}{V_{\mathrm{forw}}} = \frac{Z/Z_{\mathrm{WG}} - 1}{Z/Z_{\mathrm{WG}} + 1} = \frac{1 - Y \cdot Z_{\mathrm{WG}}}{1 + Y \cdot Z_{\mathrm{WG}}} = \frac{1 - \tilde{Y}}{1 + \tilde{Y}},$$

The cavity voltage is determined by the forward and reflected waves at the load:

$$V_{\mathrm{c}} = V_{\mathrm{forw}} + V_{\mathrm{refl}} = V_{\mathrm{forw}}\left(1 + \Gamma_{\mathrm{V}}\right) = \frac{2}{1 + \tilde{Y}} \cdot V_{\mathrm{forw}},$$

One can now get following expressions for the forward and reflected waves:

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August 2002

$$V_{\text{forw}} = \frac{V_c}{2}\cdot\left(1+\tilde{Y}\right) = \frac{V_c}{2}\left[1+\frac{1}{\beta}+\frac{I_b\,R/Q\cdot Q_{ext}}{V_c}\cos\varphi_0 + i\frac{\tan\psi}{\beta}+i\frac{I_b\,R/Q\cdot Q_{ext}}{V_c}\sin\varphi_0\right] =$$
$$= \frac{I_b\,R/Q\cdot Q_{ext}}{2}\left(\cos\varphi_0+i\sin\varphi_0\right)+\frac{V_c}{2}\left(\frac{\beta+1}{\beta}+i\frac{\tan\psi}{\beta}\right) =$$
$$= \frac{I_b\,R/Q\cdot Q_{ext}}{2}\left(\cos\varphi_0+i\sin\varphi_0\right)+\frac{V_c}{2}\frac{\beta+1}{\beta}\left(1+i\tan\psi'\right)$$

$$V_{\text{refl}} = \frac{V_c}{2}\cdot\left(1-\tilde{Y}\right) = \frac{V_c}{2}\left[1-\frac{1}{\beta}-\frac{I_b\,R/Q\cdot Q_{ext}}{V_c}\cos\varphi_0 - i\frac{\tan\psi}{\beta}-i\frac{I_b\,R/Q\cdot Q_{ext}}{V_c}\sin\varphi_0\right] =$$
$$= -\frac{I_b\,R/Q\cdot Q_{ext}}{2}\left(\cos\varphi_0+i\sin\varphi_0\right)+\frac{V_c}{2}\left(\frac{\beta-1}{\beta}-i\frac{\tan\psi}{\beta}\right) =$$
$$= -\frac{I_b\,R/Q\cdot Q_{ext}}{2}\left(\cos\varphi_0+i\sin\varphi_0\right)+\frac{V_c}{2}\frac{\beta+1}{\beta}\left(\frac{\beta-1}{\beta+1}-i\tan\psi'\right)$$

$$P_{\text{forw}} = \frac{\left|V_{\text{forw}}\right|^2}{Z_{WG}} = \frac{{V_c}^2}{4\,R/Q\cdot Q_{ext}}\cdot\left|1+\frac{1}{\beta}+\frac{I_b\,R/Q\cdot Q_{ext}}{V_c}\cos\varphi_0 + i\frac{\tan\psi}{\beta}+i\frac{I_b\,R/Q\cdot Q_{ext}}{V_c}\sin\varphi_0\right|^2 =$$
$$= \frac{{V_c}^2}{4\,R/Q\cdot Q_{ext}}\cdot\left\{\left[\frac{\beta+1}{\beta}+\frac{I_b\,R/Q\cdot Q_{ext}}{V_c}\cos\varphi_0\right]^2+\left[\frac{\tan\psi}{\beta}+\frac{I_b\,R/Q\cdot Q_{ext}}{V_c}\sin\varphi_0\right]^2\right\} =$$
$$= \frac{{V_c}^2}{4\,R/Q\cdot Q_{ext}}\cdot\frac{(\beta+1)^2}{\beta^2}\cdot\left\{\left[1+\frac{I_b\,R/Q\cdot Q_L}{V_c}\cos\varphi_0\right]^2+\left[\tan\psi'+\frac{I_b\,R/Q\cdot Q_L}{V_c}\sin\varphi_0\right]^2\right\}$$

$$\tan\psi' = 2Q_L\frac{\Delta\omega}{\omega}\ .$$

To compensate the reactive part of the beam impedance, the cavity has to be detuned so that

$$I_b\,R/Q\cdot Q_{ext}\sin\varphi_0 + V_c\frac{\beta+1}{\beta}\tan\psi' = 0$$

$$\tan\psi' = -\frac{I_b\,R/Q\cdot Q_L\sin\varphi_0}{V_c}$$

or

$$\Delta\omega = -\frac{I_b\,R/Q\cdot\omega\cdot\sin\varphi_0}{2V_c}\ .$$

Then matched or reflection-free condition will be reached at the beam current

$$I_b \, R/Q \cdot Q_{ext} \cos\varphi_0 = V_c \cdot \frac{\beta - 1}{\beta}$$

$$I_b = \frac{V_c}{R/Q \cdot Q_{ext} \cos\varphi_0} \frac{\beta - 1}{\beta} \quad .$$

This corresponds to forward power

$$P_{forw} = \frac{{V_c}^2}{R/Q \cdot Q_{ext}} \quad .$$

B PLL Parameters

B.1 Introduction

The RF IOC board houses two LMK04848 PLLs manufactured by Texas Instruments (TI). TI provides to the developers a Clock Design Tool to facilitate the loop filter design and the device configuration. This tool was not used, though.
In this appendix the formulas used to design the loop filter are reported.

B.2 Loop Filter Design

The minimum loop filter configuration contains a smoothing capacitor in parallel to the RC section. So the loop filter impedance is:

$$Z_f(s) = \frac{1}{s(C_1+C_2)} \frac{1+sR_1C_1}{1+sR_1(\frac{C_1C_2}{C_1+C_2})} = \frac{k}{s}\frac{1+s\tau_2}{1+s\tau_3} = \frac{k}{s}\frac{1+s\tau_2}{1+s\tau_2/b} \tag{B.1}$$

Where τ_2 is the time constant of the zero, τ_3 is the time constant of the pole and $b = \tau_2/\tau_3 = 1 + C_1/C_2$.
Since a PLL can hardly be estimated to a second order system, it is not possible use the theory based on the natural frequency and damping factor concepts typical in a second order system analysis. So to dimension the loop filter parameters, it will make use of the open loop bandwidth and phase margin concepts.
To ease explanation here it is reported the linear phase model of a PLL .

The open loop transfer function is expressed as:

$$G(s) = \frac{\varphi_{OUT}(s)}{\varphi_{REF}(s)} = \frac{I_{CP}}{2\pi} Z_f(s) \frac{K_{VCO}}{s} \frac{1}{N} \tag{B.2}$$

The open loop bandwidth $f_c = \omega_c/2\pi$ is the frequency when $|G(j\omega_c)| = 1(or = 0dB)$. The phase margin is defined as $\phi_m = \angle(G(j\omega_c)) + \pi$.

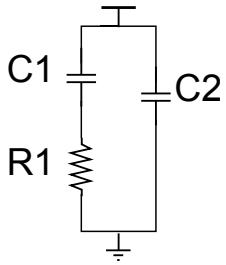

Figure B.1: Loop Filter $Z_f(s)$.

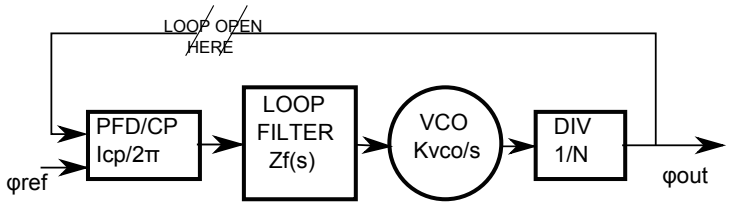

Figure B.2: Linear model of a PLL.

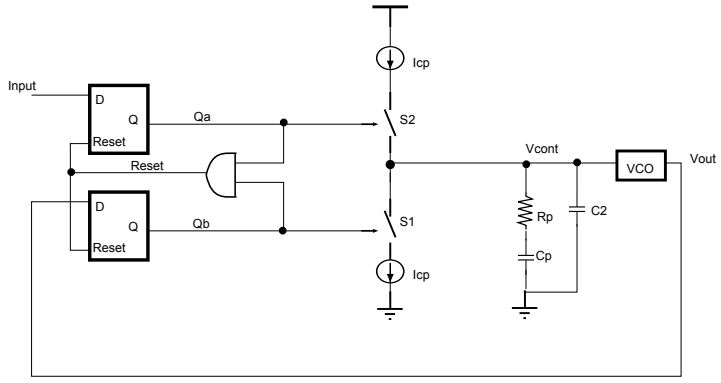

Figure B.3: PLL with a third order loop filter.

The open loop transfer function at ω_c from (B.2) yields:

$$|G(j\omega_c)| = \frac{I_{CP}K_{VCO}k}{2\pi N}\frac{1}{\omega_c^2}\frac{|1+j\omega_c\tau_2|}{|1+j\omega_c\tau_3|} = \frac{I_{CP}K_{VCO}k}{2\pi N}\frac{1}{\omega_c^2}\frac{\sqrt{1+(\omega_c R_1 C_1)^2}}{\sqrt{1+(\omega_c R_1 \frac{C_1C_2}{C_1+C_2})^2}} = 1 \tag{B.3}$$

The phase of $G(j\omega)$ from (B.2) is denoted as:

$$\Psi(j\omega) = -\pi + \angle(1+j\omega\tau_2) - \angle(1+j\omega\tau_3) = -\pi + tan^{-1}(\omega\tau_2) - tan^{-1}(\omega\tau_3) \tag{B.4}$$

The point of zero derivative of the phase response will be ω_{MAX}, this frequency corresponding to the maximum value of $\Psi(j\omega)$ for given values of τ_2 and τ_3. It becomes:

$$\omega_{MAX} = \sqrt{\frac{1}{\tau_2\tau_3}}. \tag{B.5}$$

Using the last two equations we compute the value of the maximum phase advance:

$$\phi_{MAX} = \Psi(j\omega_{MAX}) + \pi = tan^{-1}\left(\frac{\tau_2-\tau_3}{2\sqrt{\tau_2\tau_3}}\right) = tan^{-1}\left(\frac{b-1}{2\sqrt{b}}\right) \tag{B.6}$$

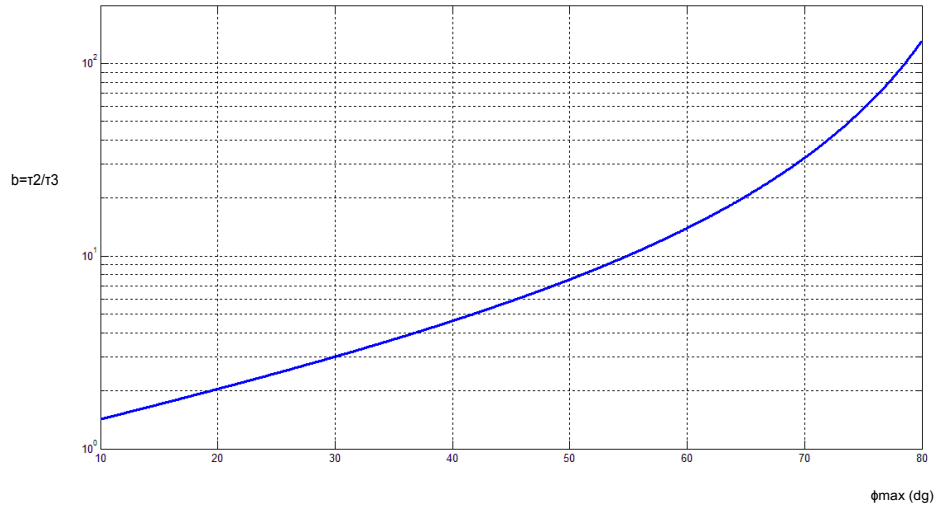

Figure B.4: Value of the ratio of the time constant $b = \tau_2/\tau_3$ as a function of the $G(j\omega)$ phase.

Solving the equation for b as a function of ϕ_{MAX} yields:

$$b = \frac{1}{(-tan\phi_{MAX} + 1/cos\phi_{MAX})^2} \tag{B.7}$$

The numerical values of b as a function of ϕ_{MAX} are plotted in Fig. B.4.

Assuming $\omega_c = \omega_{MAX}$ then $\phi_m = \phi_{MAX}$. From equation B.6 and knowing that $b = \tau_2/\tau_3$ results:

$$\tau_2 = \frac{\sqrt{b}}{\omega_c} \tag{B.8}$$

$$\tau_3 = \frac{1}{\sqrt{b}\omega_c}. \tag{B.9}$$

Replacing the equations (B.8) and (B.9) into (B.3) yields:

$$\omega_c = \frac{I_{CP}K_{VCO}k}{2\pi N\omega_c}\sqrt{\frac{1+\sqrt{b}^2}{1+\sqrt{1/b}^2}} = \frac{I_{CP}K_{VCO}}{2\pi N}R_1\frac{b-1}{b} \tag{B.10}$$

The value of the loop filter components can be calculated. The results are:

$$R_1 = \frac{2\pi N\omega_c}{I_{CP}K_{VCO}}\frac{b}{b-1} \tag{B.11}$$

$$C_1 = \tau_2/R_1 \tag{B.12}$$

$$C_2 = \frac{\tau_2\tau_3}{\tau_2-\tau_3}/R_1 \tag{B.13}$$

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