Suppression of Second-Order Harmonic Current for Droop-Controlled Distributed Energy Resource Converters in DC Microgrids

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***Abstract*—Droop-controlled distributed energy resource converters in dc microgrids usually show low output impedances. When coupled with ac systems, second-order harmonics typically appear on the dc-bus voltage, causing significant harmonic currents at the converters resource side. This paper shows how to reduce such undesired currents by means of notch filters and resonant regulators included in the converters control loops. The main characteristics of these techniques in terms of harmonic attenuation and stability are systematically investigated. In particular, it is shown that the voltage control-loop bandwidth is limited to be below twice the line frequency to avoid instability. Then, a modified notch filter and a modified resonant regulator are proposed, allowing to remove the constraint on the voltage loop bandwidth. The resulting methods (i.e., the notch filter, the resonant regulator, and their corresponding modified versions) are evaluated in terms of output impedance and stability. Experimental results from a dc microgrid prototype composed of three dc-dc converters and one dc-ac converter, all with a rated power of $5\,\mathrm{kW}$, are reported.**

***Index Terms*—dc microgrids, droop-controlled converter, notch filter, resonant regulator, second-order ripple.**

I. Introduction

DISTRIBUTED energy resource (DER) and local customer loads can be integrated in the form of dc microgrids, improving system reliability and distribution efficiency [1], [2]. In general, dc microgrids can be linked to the ac utility mains or ac microgrids through grid-interface converters (GIC), to allow power balancing flexibility and energy trading [3], [4]. The layout of a representative dc microgrid is displayed in Fig. 1.

Droop control is a common control strategy for dc microgrids, with the main merit of allowing voltage-controlled converters to operate in parallel without requiring communication

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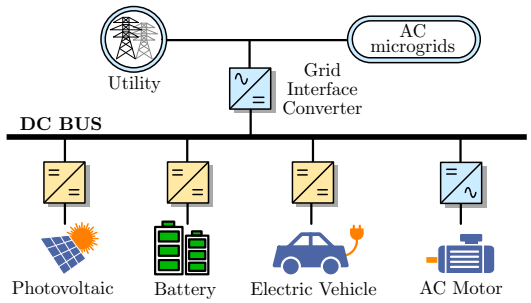

Fig. 1. Typical structure of a dc microgrid.

[5]. By the droop control, the DER converters and the GIC contribute in regulating the dc-bus voltage, all behaving as grid-supporting units. On top of the droop loop, other control loops can be added to achieve various control targets. For instance, to obtain seamless transitions between power flow control and the droop control, an external power loop can be employed [6]. However, as long as the droop loops are included, DER converters have low output (i.e., dc-bus side) impedances at twice the line frequency $2\omega_g$ [7].

In a small-scale dc microgrid, a single-phase bidirectional converter can be used as GIC [8]. In this case, when the GIC operates at unity power factor, a second-order ripple inevitably appears in the dc bus voltage. This ripple also occurs with three-phase GIC under unbalanced voltages [9]. Due to the limited output impedance of DER converters, such a second-order voltage perturbation causes large current fluctuations at the resource side of the converters, which is an unwanted effect. In some applications (e.g., fuel cells, batteries), the corresponding second-order harmonic current is detrimental, because it may shorten devices lifetime [10].

The issue of second-order harmonic current can be addressed by means of both hardware and control solutions. Hardware solutions, like increasing the bus capacitance [11], using different GIC topologies [12], and installing active power decoupling circuits [13]–[15], aim at eliminating the bus voltage harmonic ripple with hardware modifications. As a consequence, the second-order harmonic currents in DER converters are also reduced. It is worth mentioning that nonlinear control approaches are adopted in [14], [15]. While these nonlinear methods rely on the prior knowledge of the controlled system to obtain high performance, the linear ones, including the methods proposed in this paper, show

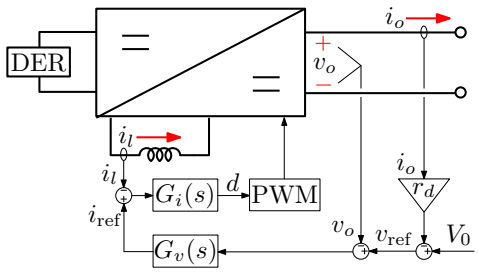

Fig. 2. A generic droop-controlled DER converter.

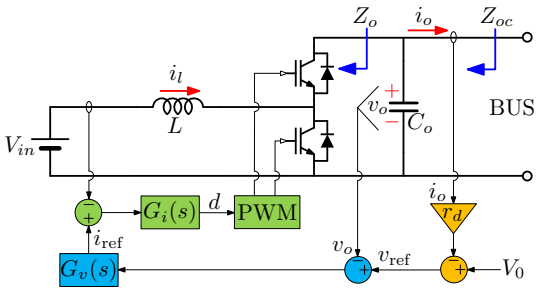

Fig. 3. An example droop-controlled boost converter.

the favorable feature of being more tolerant to the varying conditions that are typical of the addressed microgrid scenario. Moreover, without additional components, H-bridge rectifiers integrated with the active power decoupling function were proposed recently [16], [17]. In this converter, one half-bridge is responsible for active power transmission, while the other one is used for power decoupling. This converter serves as a good interface between 380 V dc microgrids and 110 V ac utility grid. However, interfacing with 230 V ac grids, a commonly used voltage level in Europe, would require dc bus voltages higher than 380 V (e.g., 500 V). Differently, techniques at the converters control level, which are addressed herein, allow to selectively mitigate harmonic currents at the resource side of DER converters in a flexible and effective way without requiring higher dc bus voltages or hardware modifications [18].

In [19], knowing the bus capacitance and the GIC output power, the bus voltage second-order ripple is calculated and then compensated by adding a ripple cancellation term on the duty cycle of the GIC. However, this method hardly supports the plug-and-play connection of converters, which makes the dc bus capacitance to vary unpredictably.

Second-order harmonic current suppression can be attained also by shaping the converters output impedance to be high at $2\omega_g$. To this end, the bandwidth of the output voltage loops can be set well below $2\omega_g$ [20], which though sacrifices the dynamic performance of the DER converters. In [21] the mean value of the bus voltage, rather than its instantaneous value, is calculated and taken as the feedback signal to eliminate the second-order harmonic in the voltage loops. For the same purpose, a notch filter based on the second-order generalized integrator (SOGI) is added in the output voltage feedback path in [22]. In these approaches, frequency-adaptive notch filters can be used to obtain more precise performances under fluctuating line frequency [23], [24], and multiple notch filters can be adopted to cope with multiple harmonic frequencies [25]. However, since notch filters introduce $-\pi/2$ phase lag around the characteristic frequency (i.e., $2\omega_g$), the bandwidth of the voltage loop is limited to be below $2\omega_g$ to avoid instability. In order to improve the dynamic performance of converters with low-bandwidth (less than $2\omega_g$) voltage loops, a load current feedforward path consisting of a notch filter is adopted in [26], and a virtual impedance in parallel with the dc bus capacitor is introduced in [18]. Both the load current feedforward method and the parallel virtual impedance method should be calculated based on the inverse of the converters transfer functions, which complicates the design.

This paper extends [7], presenting additional current suppression methods, improved analyses, design principles, and additional experimental results. In particular, four different methods for second-order harmonic currents reduction are discussed herein: adoption of a notch filter, a modified notch filter, a resonant regulator, and a modified resonant regulator. The implementations called *modified notch filter* and *modified resonant regulator* are proposed herein. The modified schemes can be simply inserted into high-bandwidth loops, without specific concerns about stability. Hence, the proposed approaches give an efficient way to tackle the second-order harmonic current issue and to achieve good dynamic performance, concurrently. The remainder of the paper is organized as follows. Sec. II gives the small-signal model of a DER converter. Sec. III investigates the method using a notch filter, focusing on the converter output impedance and stability. Sec. IV introduces the modified notch filter and compares its performance with the notch filter; the design of the filter is reported in this section too. Sec. V briefly discusses the resonant regulator and the modified resonant regulator methods. Sec. VI summarizes and compares the obtained results. Finally, Sec. VII reports the experimental verification of the presented theoretical results and the methods.

II. Droop-controlled converter model

A generic droop-controlled DER converter is displayed in Fig. 2. The control scheme is composed of three loops: the inductor current loop, the voltage loop, and the droop loop. $G_i(s)$ and $G_v(s)$ are controllers used to regulate the inductor current i_l and the output voltage v_o, respectively. The droop loop is closed on top of the current and voltage loops. The parameter r_d is the droop coefficient, V_0 is the voltage set point under no load condition. Typically, step-up dc-dc converters are utilized as DER converters [27], [28]. Without loosing generality, a droop-controlled bidirectional boost converter, shown in Fig. 3, is referred to in the following analysis.

The linearized circuit equations of the boost converter around an operation point are [29]:

$$sL \cdot \hat{i}_l = -(1 - D_p) \cdot \hat{v}_o + V_{op} \cdot \hat{d} \tag{1}$$

$$sC_o \cdot \hat{v}_o = (1 - D_p) \cdot \hat{i}_l - I_{lp} \cdot \hat{d} - \hat{i}_o \tag{2}$$

where the diacritic mark $\hat{}$ indicates the ac small-signal, V_{op} is the static output voltage, I_{lp} is the static inductor current, and D_p is the static duty-cycle. In steady-state, the input voltage

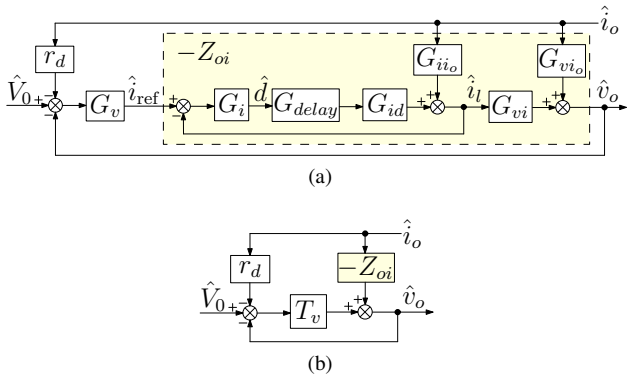

Fig. 4. Linearized model of the droop-controlled boost converter. (a) Control block diagram; (b) Equivalent transformation.

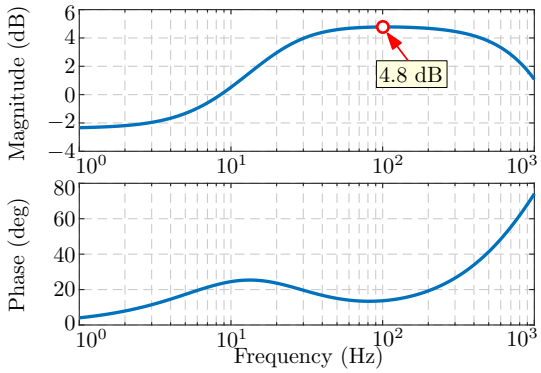

Fig. 5. Bode diagram of the converter output impedance $Z_o(s)$ in (10) with all the three loops closed.

V_{in} equals $(1-D_p)\cdot V_{op}$, and the static output current I_{op} equals $(1-D_p)\cdot I_{lp}$. Then, by combining (1) and (2), the state variables $\hat{i}_l$ and $\hat{v}_o$ can be expressed as:

$$\hat{i}_l = \underbrace{\frac{sC_oV_{op}+I_{op}}{s^2LC_o+(1-D_p)^2}}_{G_{id}(s)}\cdot\hat{d} + \underbrace{\frac{1-D_p}{s^2LC_o+(1-D_p)^2}}_{G_{ii_o}(s)}\cdot\hat{i}_o \quad (3)$$

$$\hat{v}_o = \underbrace{\frac{-sLI_{lp}+V_{in}}{sC_oV_{op}+I_{op}}}_{G_{vi}(s)}\cdot\hat{i}_l + \underbrace{\frac{-V_{op}}{sC_oV_{op}+I_{op}}}_{G_{vi_o}(s)}\cdot\hat{i}_o \quad (4)$$

The power stage of the boost converter can be described by the transfer functions $G_{id}(s)$, $G_{ii_o}(s)$, $G_{vi}(s)$, and $G_{vi_o}(s)$. The final block diagram of the linearized droop-controlled boost converter is displayed in Fig. 4a.

When the inductor current loop is closed and the other two loops are open, the output impedance $Z_{oi}(s)$ can be calculated as:

$$Z_{oi}(s) = -\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{i}_{\text{ref}}=0} = -\left[G_{vi_o}(s)+\frac{G_{ii_o}(s)G_{vi}(s)}{1+T_i(s)}\right] \quad (5)$$

where $T_i(s)$ is the open-loop transfer function of the inductor current loop:

$$T_i(s) = G_i(s)\cdot G_{delay}(s)\cdot G_{id}(s) \quad (6)$$

By including $Z_{oi}(s)$ in the block diagram, the equivalent model shown in Fig. 4b can be obtained. $T_v(s)$ is the open-loop transfer function of the voltage loop:

$$T_v(s) = G_v(s)\cdot T_{iCL}(s)\cdot G_{vi}(s) \quad (7)$$

where $T_{iCL}(s)$ is the closed-loop transfer function of the inductor current loop:

$$T_{iCL}(s) = T_i(s)/\left[1+T_i(s)\right] \quad (8)$$

Then, the output impedance with all the three loops closed is:

$$Z_{oc}(s) = -\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{V}_0=0} = \frac{Z_{oi}(s)+r_d\cdot T_v(s)}{1+T_v(s)} \quad (9)$$

$Z_o(s)$ can be further derived by decoupling the output capacitance $1/sC_o$ from $Z_{oc}(s)$:

$$Z_o(s) = Z_{oc}(s)/\left[1-sC_oZ_{oc}(s)\right] \quad (10)$$

As an example, Fig. 5 shows the bode diagram of $Z_o(s)$ that refers to the system in Fig. 3, with $V_{in} = 200\,\text{V}$, $V_{bus} = 380\,\text{V}$, $L = 0.5\,\text{mH}$, $C_o = 220\,\mu\text{F}$, $V_0 = 380\,\text{V}$, $r_d = 0.76\,\text{V/A}$. The current loop and voltage loop bandwidths are equal to 2 kHz and 650 Hz, respectively. Notably, $|Z_o(s)|$ is about 4.8 dB (i.e., 1.7 Ω) at twice the line frequency $2\omega_g$ (i.e., 100 Hz), which means that even a relatively small second-order harmonic voltage ripple would lead to a large associated current flowing at the resource side of the converter. Actually, if the voltage control bandwidth is high enough, the output impedance at $2\omega_g$ can be as low as r_d, producing an even higher second-order harmonic current.

III. Adoption of a Notch Filter

To mitigate the second-order harmonic current, a common way is to decrease the voltage loop gain at twice the line frequency, that is, to reduce the second-order fluctuations in the current reference i_{ref}. A notch filter $G_{nf}(s)$ can be adopted to this purpose:

$$G_{nf}(s) = \frac{(s/\omega_c)^2+2\xi_1\cdot s/\omega_c+1}{(s/\omega_c)^2+2\xi_2\cdot s/\omega_c+1} \quad (11)$$

where ω_c is the center frequency of the notch, ξ_1 and ξ_2 are two coefficients related to the filter bandwidth and the notch depth. With the decrease of the ratio ξ_1/ξ_2, the notch at ω_c gets deeper (i.e., higher attenuation). The filter bandwidth becomes wider as ξ_1 decreases or ξ_2 increases. An instance of $G_{nf}(s)$ is displayed in Fig. 6. The bandwidth of this notch filter is 100 Hz and the notch depth is −60 dB. By inserting $G_{nf}(s)$ into the forward path of the voltage loop, that is, in series with the voltage regulator $G_v(s)$, the voltage loop gain at ω_c can be reduced to a low level and i_{ref} is free from the ripple at ω_c. The resulting control scheme adopting a notch filter is displayed in Fig. 7.

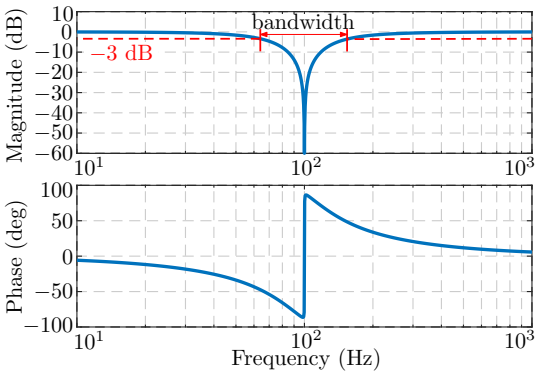

Fig. 6. Bode diagram of a representative notch filter $G_{nf}(s)$ in (11) using $\omega_c = 2\pi \cdot 100\,\text{rad/s}$, $\xi_1 = 5.0 \times 10^{-4}$, and $\xi_2 = 5.0 \times 10^{-1}$.

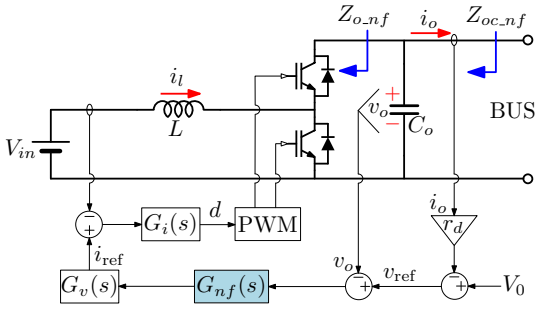

Fig. 7. Control scheme of the second-order harmonic current provision by adopting a notch filter $G_{nf}(s)$ [defined in (11)]. $G_{nf}(s)$ can be replaced by the modified notch filter $G_{mnf}(s)$ [defined in (16)].

A. Output impedance

According to Fig. 7, the converter output impedance $Z_{oc\_nf}(s)$ with $G_{nf}(s)$ inserted is:

$$Z_{oc\_nf}(s) = \frac{Z_{oi}(s) + r_d \cdot T_{v\_nf}(s)}{1 + T_{v\_nf}(s)} \tag{12}$$

where $T_{v\_nf}(s)$ is the open-loop transfer function of the voltage loop with $G_{nf}(s)$ inserted:

$$T_{v\_nf}(s) = T_v(s) \cdot G_{nf}(s) \tag{13}$$

As $G_{nf}(s)$ shows a high attenuation at $2\omega_g$, $|T_{v\_nf}(j2\omega_g)|$ is small. Hence, $Z_{oc\_nf}(j2\omega_g)$ can be approximated as:

$$Z_{oc\_nf}(j2\omega_g) \approx Z_{oi}(j2\omega_g) \tag{14}$$

and $Z_{o\_nf}(s)$ can be expressed as:

$$Z_{o\_nf}(s) = Z_{oc\_nf}(s) / \left[1 - sC_o Z_{oc\_nf}(s)\right] \tag{15}$$

The bode diagram of $Z_{o\_nf}(s)$ is displayed in Fig. 8. The notch filter $G_{nf}(s)$ used here has a bandwidth of 10 Hz and a notch depth of −60 dB, with $\omega_c = 2\pi \cdot 100\,\text{rad/s}$, $\xi_1 = 5.0 \times 10^{-5}$, and $\xi_2 = 5.0 \times 10^{-2}$. It can be noticed that $Z_{o\_nf}(j2\omega_g)$ has a magnitude of 22 dB (i.e., 12.6 Ω), which is 7.4 times $Z_o(j2\omega_g)$. Consequently, with $G_{nf}(s)$, the second-order harmonic current is notably reduced.

B. Stability analysis

It should be noted that if the crossover frequency of the voltage loop is above $2\omega_g$, which is typically the case in practice, $G_{nf}(s)$ brings two additional zero crossings: one below $2\omega_g$, the other above $2\omega_g$. Notably, $G_{nf}(s)$ introduces large phase lags at frequencies below $2\omega_g$, reducing the phase margin at the corresponding zero crossing and weakening significantly the stability of the voltage loop. Fig. 9 shows the bode diagram of the open-loop transfer functions $T_{v\_nf}(s)$ and $T_v(s)$ of the voltage loop. Without $G_{nf}(s)$, $T_v(s)$ has a magnitude of 14 dB and a phase of −80° at 100 Hz. By employing $G_{nf}(s)$, $T_{v\_nf}(s)$ has two additional zero crossing points around 100 Hz. At the zero crossing below 100 Hz, the phase margin is drastically reduced to 22°. To maintain the system stability, the voltage control bandwidth should be redesigned to fall below 100 Hz, resulting in a slow dynamic response.

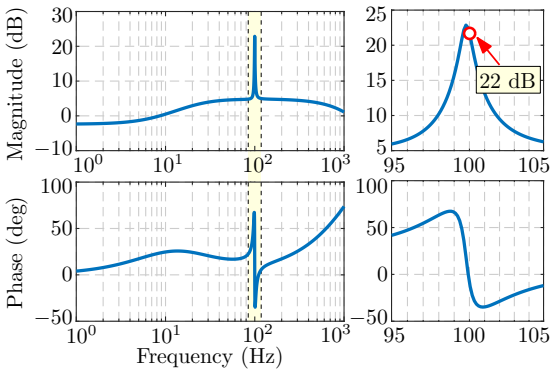

Fig. 8. Bode diagram of the output impedance $Z_{o\_nf}(s)$ [see (15)] resulting by adopting the notch filter $G_{nf}(s)$.

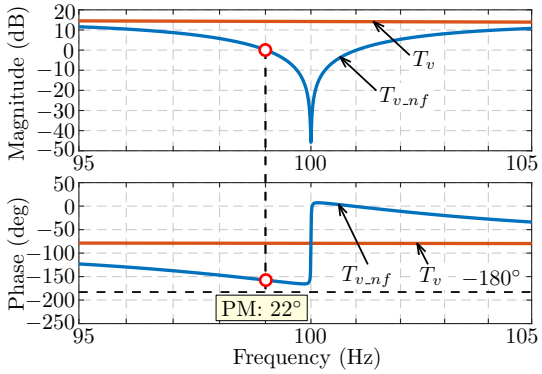

Fig. 9. Impact of $G_{nf}(s)$ on the stability: bode diagram of the open-loop transfer function $T_{v\_nf}(s)$ [see (13)] of the voltage loop with $G_{nf}(s)$ adopted and the transfer function $T_v(s)$ [see (7)] of the same loop without $G_{nf}(s)$.

IV. Adoption of a Modified Notch Filter

In order to concurrently achieve fast dynamic response and good stability margin, a modified notch filter $G_{mnf}(s)$ is proposed herein in place of $G_{nf}(s)$ in Fig. 7:

$$G_{mnf}(s) = \frac{1}{\alpha^2} \frac{(s/\omega_c)^2 + 2\xi_1 \cdot s/\omega_c + 1}{\left[s/(\alpha\omega_c)\right]^2 + 2\xi_2 \cdot s/(\alpha\omega_c) + 1} \tag{16}$$

where α, which is larger than 1, is the deviation factor; if $\alpha = 1$, $G_{mnf}(s)$ corresponds to $G_{nf}(s)$. The bode diagram of $G_{mnf}(s)$ with different values of α is displayed in Fig. 10. By increasing α, the two poles of $G_{mnf}(s)$ move to higher

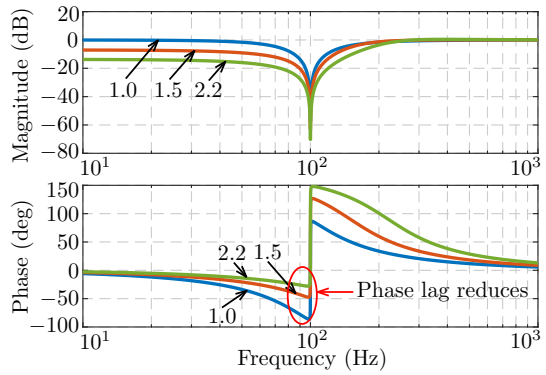

Fig. 10. Bode diagram of the modified notch filter $G_{mnf}(s)$ in (16) with different α, using $\omega_c = 2\pi \cdot 100\,\mathrm{rad/s}$, $\xi_1 = 5.0 \times 10^{-4}$, and $\xi_2 = 5.0 \times 10^{-1}$.

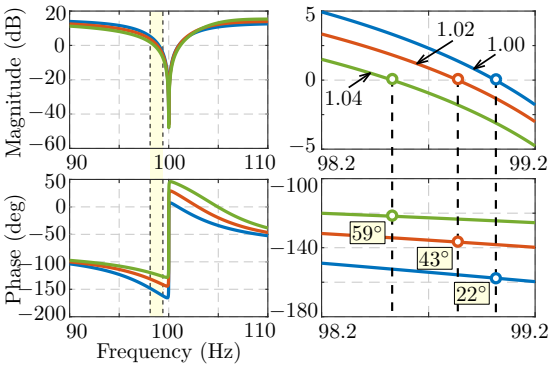

Fig. 11. Stability improvement by using $G_{mnf}(s)$ in (16) with different α: bode diagram of the open-loop transfer function $T_{v\_mnf}(s)$ of the voltage loop.

frequencies. Consequently, the phase lag below ω_c reduces, while keeping a high attenuation at ω_c. The term $1/\alpha^2$ is used to correct the gains to 1 at high frequency, so that $G_{mnf}(s)$ does not change the original crossover frequency of the voltage loop. However, by doing so, the static gain of $G_{mnf}(s)$ is less than 1.

A. Stability improvement

To investigate the effect of $G_{mnf}(s)$ on the converter stability, the open-loop transfer function $T_{v\_mnf}(s)$ of the voltage loop with $G_{mnf}(s)$ inserted is considered:

$$T_{v\_mnf}(s) = T_v(s) \cdot G_{mnf}(s) \tag{17}$$

The bode diagram of $T_{v\_mnf}(s)$ is displayed in Fig. 11. The $G_{mnf}(s)$ reported here have different α, but the other parameters are kept constant (i.e., $\omega_c = 2\pi \cdot 100\,\mathrm{rad/s}$, $\xi_1 = 5.0 \times 10^{-5}$, and $\xi_2 = 5.0 \times 10^{-2}$). Remarkably, the phase margin rises from 22° to 59°, with a light increase of α from 1.00 to 1.04, showing a significant stability improvement. Since the instability is avoided, the voltage control bandwidth can be kept at the original value, that is, 650 Hz. Compared to the case with the traditional notch filter, the converter dynamic response is much faster.

It is worth observing that the phase improvement induced by $G_{mnf}(s)$ is determined only by the filter parameters, and it is not influenced by physical system variations. Clearly, to always ensure an adequate phase margin also in the presence

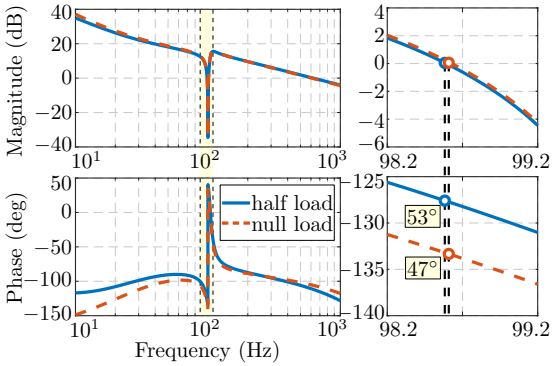

Fig. 12. Voltage loop stability under different operation points while $G_{mnf}(s)$ is employed, with α equal to 1.04.

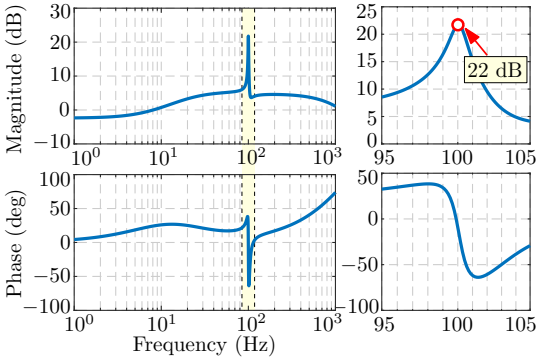

Fig. 13. Bode diagram of the output impedance $Z_{o\_mnf}(s)$ [see (19)] resulting by adopting the modified notch filter $G_{mnf}(s)$.

of a wide range of operating conditions, $G_{mnf}(s)$ should be designed by referring to the operation point showing the worst (i.e., minimum) phase at $2\omega_g$. From this perspective, Fig. 12 shows the voltage loop stability under different operation points using $G_{mnf}(s)$ with α equal to 1.04. Notably, the phase margin is always higher than 45°.

B. Output impedance

By replacing $G_{nf}(s)$ with $G_{mnf}(s)$ in Fig. 7, the output impedance $Z_{oc\_mnf}(s)$ can be expressed as:

$$Z_{oc\_mnf}(s) = \frac{Z_{oi}(s) + r_d \cdot T_{v\_mnf}(s)}{1 + T_{v\_mnf}(s)} \tag{18}$$

$Z_{o\_mnf}(s)$ can be calculated by decoupling $1/sC_o$ from $Z_{oc\_mnf}(s)$:

$$Z_{o\_mnf}(s) = Z_{oc\_mnf}(s) / \left[1 - sC_o Z_{oc\_mnf}(s)\right] \tag{19}$$

The bode diagram of $Z_{o\_mnf}(s)$ is shown in Fig. 13. $G_{mnf}(s)$ adopted here uses $\alpha = 1.04$. Since $G_{mnf}(s)$ also brings $|Z_{o\_mnf}(j2\omega_g)|$ to 22 dB (i.e., 12.6 Ω), it has the same performance as $G_{nf}(s)$ (see Fig. 8) in rejecting second-order harmonic current.

C. Filter design

A modified notch filter $G_{mnf}(s)$ has one additional parameter (i.e., α) compared to the notch filter $G_{nf}(s)$. The selection of α is discussed below.

The deviation factor α is utilized to increase the phase margin of the voltage loop. As compared to $G_{nf}(s)$, $G_{mnf}(s)$

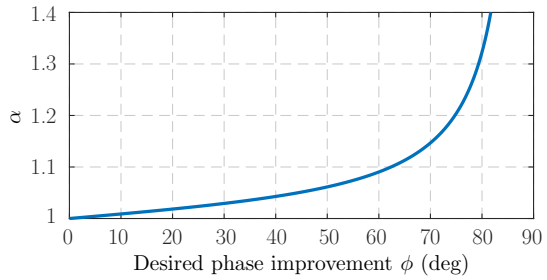

Fig. 14. Relationship (21) between the desired phase improvement ϕ and α, using $\xi_2 = 5.0 \times 10^{-2}$.

gives a high phase gain at $2\omega_g$, and the phase gain reduces as the frequency strays from $2\omega_g$ (see Fig. 10). In different application cases, voltage loops with $G_{mnf}(s)$ inserted may have different crossover frequencies around $2\omega_g$, so the phase margin improvements brought by $G_{mnf}(s)$ differ from case to case. Fortunately, as long as the implemented $G_{mnf}(s)$ has a narrow notch, the crossover frequency locates in the vicinity of $2\omega_g$ (see Fig. 11). In this case, the phase gain of $G_{mnf}(s)$ at the crossover frequency is approximately equal to the phase gain at $2\omega_g$, that is, $\angle G_{mnf}(j2\omega_g)$. This estimation makes the selection of α independent from the specific application case, simplifying the design procedure. The phase gain of $G_{mnf}(s)$ at $2\omega_g$ can be calculated as:

$$\angle G_{mnf}(j2\omega_g) = \frac{\pi}{2} - \arctan\left(\frac{2\alpha\xi_2}{\alpha^2 - 1}\right) \tag{20}$$

The value of α for a desired phase gain ϕ ($0 < \phi < \pi/2$) is:

$$\alpha = \left(\xi_2 + \sqrt{{\xi_2}^2 + \tan^2\left(\frac{\pi}{2} - \phi\right)}\right) \Big/ \tan\left(\frac{\pi}{2} - \phi\right) \tag{21}$$

Fig. 14 displays the relationship between ϕ and α. Notably, the larger the required phase improvement, the larger the required value of α.

As an example, let us consider the choice of α to reach a phase margin of 60° in the case of Fig. 9, where the phase margin is displayed to decrease to 22° after inserting the notch filter. Being the necessary phase lead equal to 38°, by referring to (21) or Fig. 14, it is possible to find that the desired phase margin improvement can be achieved if α is set to 1.04. In Fig. 11 the final result by employing a modified notch filter with $\alpha = 1.04$, showing an obtained phase margin of 59°.

V. Adoption of a Resonant Regulator and a Modified Resonant Regulator

An alternative way to suppress the second-order harmonic current is to actively regulate it to zero. A resonant regulator $G_{rr}(s)$ can be adopted to this end as shown in Fig. 15. The expressions of $G_{rr}(s)$ is:

$$G_{rr}(s) = \frac{\lambda_1 \cdot s/\omega_r}{(s/\omega_r)^2 + \lambda_2 \cdot s/\omega_r + 1} + 1 \tag{22}$$

where ω_r is the resonant frequency, λ_1 and λ_2 are two coefficients. $G_{rr}(s)$ not only provides the unity gain, but also amplifies the error between 0 and i_l at $2\omega_g$. The final outcome of this approach is determined by the gain of $G_{rr}(s)$ at $2\omega_g$: the higher the gain, the smaller the second-order harmonic

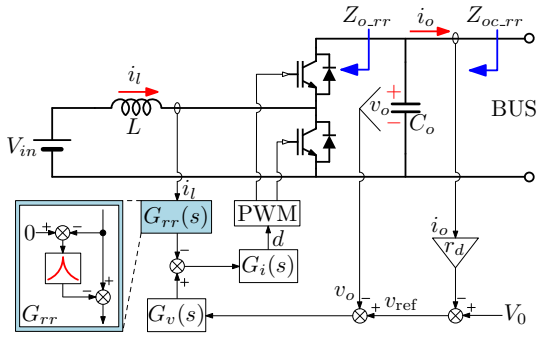

Fig. 15. Second-order harmonic current provision by adopting a resonant regulator $G_{rr}(s)$ [defined in (22)]. $G_{rr}(s)$ can be replaced by the modified resonant regulator $G_{mrr}(s)$ [defined in (23)].

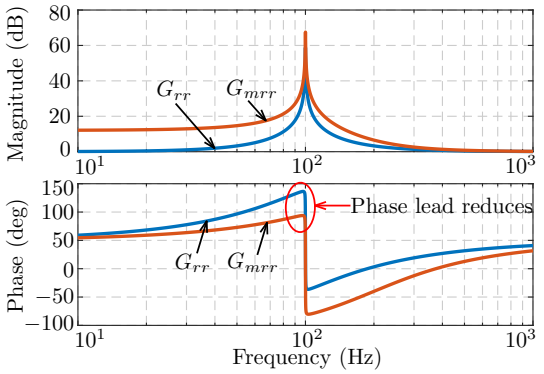

Fig. 16. Bode diagram of the resonant regulator $G_{rr}(s)$ in (22) and the modified resonant regulator $G_{mrr}(s)$ in (23).

current. Particularly, if the gain is infinite, the second-order harmonic current can be totally compensated.

A modified resonant regulator $G_{mrr}(s)$, constructed in a way similar to $G_{mnf}(s)$, can be used in place of $G_{rr}(s)$ in Fig. 15. Its transfer function is:

$$G_{mrr}(s) = \beta^2 \frac{[s/(\beta\omega_r)]^2 + (\lambda_1 + \lambda_2) \cdot s/(\beta\omega_r) + 1}{(s/\omega_r)^2 + \lambda_2 \cdot s/\omega_r + 1} \tag{23}$$

where β, which is larger than 1, is the deviation factor. If $\beta = 1$, $G_{mrr}(s)$ is equivalent to $G_{rr}(s)$. The zeros of $G_{mrr}(s)$ are moving to higher frequencies by increasing β. To keep the original crossover frequencies of the current and the voltage loops, the gains at high frequencies are set to 1 by the term β^2. It should be noted that, since the static feedback gain of the current loop is β^2 instead of 1, the output limitations of the voltage regulator $G_v(s)$ should be changed correspondingly.

The bode diagram of an instance of $G_{rr}(s)$ and $G_{mrr}(s)$ is displayed in Fig. 16, using $\omega_r = 2\pi \cdot 100\,\text{rad/s}$, $\lambda_1 = 1.6$, $\lambda_2 = 1.6 \times 10^{-3}$, and $\beta = 2.0$. $G_{rr}(s)$ and $G_{mrr}(s)$ all have high gains at $2\omega_g$. Notably, $G_{mrr}(s)$ shows less phase lead below $2\omega_g$ than $G_{rr}(s)$.

A. Output impedance

Fig. 17 shows the bode diagram of $Z_{o\_rr}(s)$ and $Z_{o\_mrr}(s)$. The $G_{rr}(s)$ and $G_{mrr}(s)$ employed here use $\omega_r = 2\pi \cdot 100\,\text{rad/s}$, $\lambda_1 = 1.6 \times 10^{-1}$, $\lambda_2 = 1.6 \times 10^{-4}$, and $\beta = 1.12$. At 100 Hz, $Z_{o\_rr}(s)$ exactly matches $Z_{o\_mrr}(s)$,

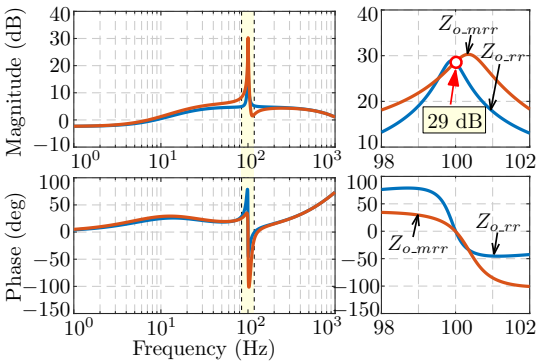

Fig. 17. Bode diagram of the output impedance $Z_{o\_rr}(s)$ and $Z_{o\_mrr}(s)$, resulting by adopting $G_{rr}(s)$ and $G_{mrr}(s)$ [see Fig. 15], respectively.

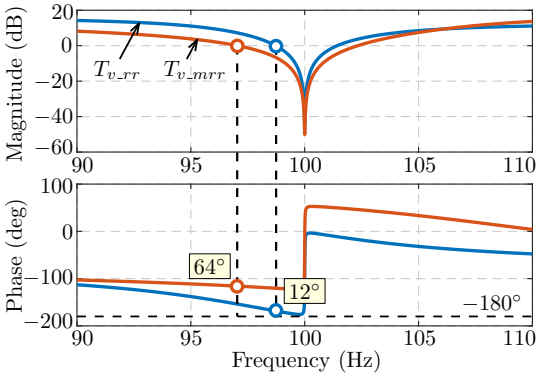

Fig. 18. Effect of $G_{rr}(s)$ and $G_{mrr}(s)$ on voltage loop stability: bode diagram of the voltage loop gains $T_{v\_rr}(s)$ and $T_{v\_mrr}(s)$.

with a magnitude of 29 dB (i.e., 28.2 Ω), indicating a high rejection of the second-order harmonic current ripple in i_l.

B. Stability analysis

To investigate the influence of $G_{rr}(s)$ and $G_{mrr}(s)$ on the stability, the bode diagram of the open-loop transfer functions $T_{v\_rr}(s)$ and $T_{v\_mrr}(s)$ of the voltage loop is reported in Fig. 18. It is possible to notice that $T_{v\_rr}(s)$ has two additional zero crossings around $2\omega_g$, and the phase margin is only 12° below $2\omega_g$. Hence, the converter stability worsens considerably after inserting $G_{rr}(s)$. On the contrary, $T_{v\_mrr}(s)$ has a phase margin of 64°, and the system stability is significantly improved by adopting $G_{mrr}(s)$. Accordingly, the voltage loop bandwidth can be kept at 650 Hz by adopting $G_{mrr}(s)$, while it must be reduced to fall below 100 Hz with $G_{rr}(s)$. As a consequence, the converter shows a better dynamic performance if $G_{mrr}(s)$ is employed.

C. Regulator design

It can be observed from (23) and (16) that $G_{mrr}(s)$ resembles $G_{mnf}(s)$ in terms of structure. Therefore, the design methodology of $G_{mnf}(s)$ described in Sec. IV-C can be adopted also to $G_{mrr}(s)$. Since β is used to enhance the voltage loop stability, β should be chosen on the basis of the desired phase margin improvement. Note that $G_{mrr}(s)$ introduces a phase lag in the current loop, which turns out

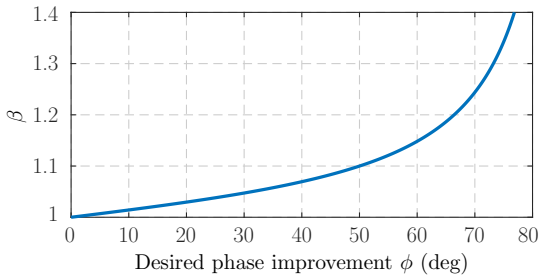

Fig. 19. Relationship (24) between the desired phase improvement ϕ and β, using $\lambda_1 = 1.6 \times 10^{-1}$ and $\lambda_2 = 1.6 \times 10^{-4}$.

TABLE I
COMPARISON OF HARMONIC CURRENT SUPPRESSION METHODS

Method	Harmonic current suppression	Influence on converter stability
G_{nf} in (11) and Fig. 7	good	easily cause instability
G_{mnf} in (16) and Fig. 7	good	stability ensured
G_{rr} in (22) and Fig. 15	excellent	easily cause instability
G_{mrr} in (23) and Fig. 15	excellent	stability ensured

to be a phase lead in the voltage loop. Actually, the phase margin improvement is roughly equal to the phase gain of $1/G_{mrr}(j2\omega_g)$. In practice, in order to simplify the design process, β can be selected according to the phase change of $1/G_{mrr}(j2\omega_g)$, which can be expressed as:

$$\angle\left(1/G_{mrr}(j2\omega_g)\right) = \frac{\pi}{2} - \arctan\left(\frac{\beta(\lambda_1+\lambda_2)}{\beta^2-1}\right) \qquad (24)$$

Fig. 19 displays the relationship between the desired phase improvement ϕ and β. Notably, for a phase improvement from 0° to 50°, the value of β varies from 1 to 1.1.

VI. Summary and Comparisons

Table I summarizes the performances of the suppression methods analyzed in Sec. III to Sec. V. The methods are compared by considering *i*) effectiveness in suppressing second-order harmonic currents and *ii*) impact on converter stability.

Regarding the reduction of the second-order harmonic current, the notch filter $G_{nf}(s)$ and the modified notch filter $G_{mnf}(s)$ are able to remove the second-order ripple in the current reference, whereas the approach using the resonant regulator $G_{rr}(s)$ and the one employing the modified resonant regulator $G_{mrr}(s)$ are capable of canceling the second-order ripple in the measured actual current. Hence, $G_{rr}(s)$ and $G_{mrr}(s)$ are expected to have better suppression performances than $G_{nf}(s)$ and $G_{mnf}(s)$.

Regarding the impact on converter stability, $G_{nf}(s)$ and $G_{rr}(s)$ drastically deteriorate the system stability if the voltage loop has a control bandwidth above $2\omega_g$. In contrast, $G_{mnf}(s)$ and $G_{mrr}(s)$ allow higher phase margins for the control system and, consequently, stable voltage control loops with wider control bandwidths.

VII. Experimental Results

The laboratory-scale experimental testbed represented in Fig. 20, constituted of one full-bridge GIC and three boost

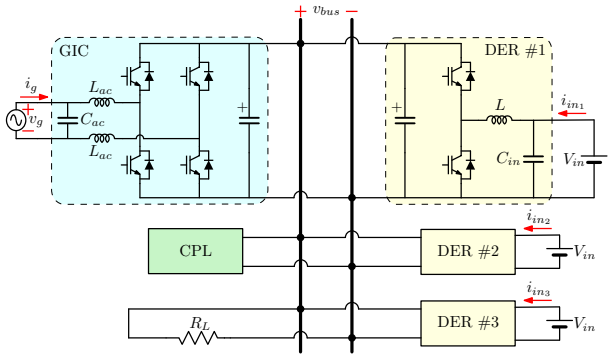

Fig. 20. Schematic of the experimental testbed.

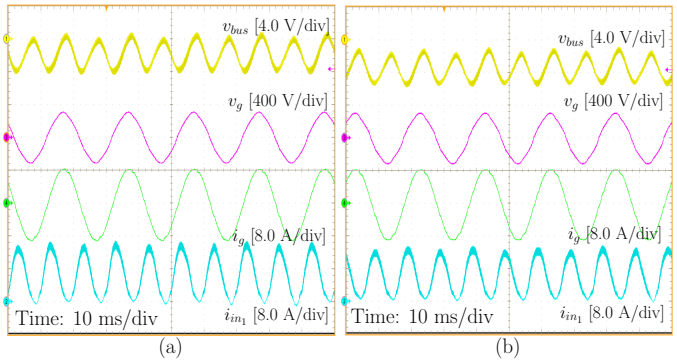

Fig. 21. Steady-state experimental results without any second-order harmonic current suppression provision: an undesired second-order harmonic ripple in i_{in_1} is visible. Droop coefficient r_d: (a) $0.76\,\mathrm{V/A}$; (b) $1.52\,\mathrm{V/A}$. v_{bus} offset: $380\,\mathrm{V}$.

TABLE II
EXPERIMENTAL SYSTEM PARAMETERS

Parameter	Symbol	Value
Grid RMS voltage	V_g	220 V
Grid frequency	f_g	50 Hz
AC side inductance	L_{ac}	1.6 mH
AC side capacitance	C_{ac}	20 µF
Nominal bus voltage	V_{bus}	380 V
Total dc bus capacitance	C_b	2.2 mF
DER input voltage	V_{in}	200 V
Boost inductance	L	1.6 mH
DER input capacitance	C_{in}	110 µF
Switching frequency	f_{sw}	12.5 kHz
Voltage set point	V_0	380 V
Droop coefficient	r_d	0.76 V/A
Current regulator	$G_i(s)$	$0.027 + 5/s$
Voltage regulator	$G_v(s)$	$3.7 + 103/s$

DER converters, is considered to evaluate the methods discussed herein. Constant power load and resistive load are both installed in the prototype. System parameters, unless otherwise specified, are reported in Table II. The total bus capacitance C_b is the sum of all the capacitances connected to the bus. The input of the boost converters are connected to a dc source. The GIC and DER converters are controlled in droop, with the same droop coefficient r_d. The dc bus voltage is set to range between $360\,\mathrm{V}$ and $400\,\mathrm{V}$. The bandwidths of the inductor current loop and the output voltage loop of the DER converters are set to $1\,\mathrm{kHz}$ and $150\,\mathrm{Hz}$, respectively, without including notch filters or resonant controllers. These control parameters are reasonable and aligned with those found in other microgrid implementations [30], [31].

A. Operation with no harmonic suppression provisions

In this test, the GIC and DER #1 are in operation. A basic droop controller (see Fig. 3) is implemented on DER #1, without any second-order harmonic current suppression technique. The experimental result is given in Fig. 21. Measured signals are marked in Fig. 20. The dc bus voltage v_{bus} is measured in DC coupling mode of the oscilloscope, with an offset of $380\,\mathrm{V}$.

In Fig. 21a, default value of the droop coefficient r_d is used, that is, $0.76\,\mathrm{V/A}$. Due to the second-order power generated by the single-phase GIC, there is a second-order bus voltage ripple with a peak-to-peak value of about $4\,\mathrm{V}$. An associated current ripple with amplitude of about $6.7\,\mathrm{A}$ is measured in i_{in_1}. In this case, the second-order harmonic ripple amounts to about 27% the nominal value. Further, r_d is doubled and the corresponding experimental result is presented in Fig. 21b. v_{bus} shows a larger dc deviation from the nominal value and has a similar second-order harmonic ripple of $4\,\mathrm{V}$. The harmonic current ripple is reduced to around $5.6\,\mathrm{A}$ but still accounts for a significant portion (22%) of the nominal value.

B. Evaluation of steady-state performances

The steady-state performances of the analyzed suppression methods are now considered.

1) Notch filters: a notch filter $G_{nf}(s)$ and a modified notch filter $G_{mnf}(s)$, with $\omega_c = 2\pi \cdot 100\,\mathrm{rad/s}$, $\xi_1 = 5.0 \times 10^{-5}$, $\xi_2 = 5.0 \times 10^{-2}$, and $\alpha = 1.06$, are included in the controller of DER #1, separately. The obtained results are shown in Fig. 22a and Fig. 22b, respectively. Although v_{bus} shows a ripple with a peak-to-peak value of $5\,\mathrm{V}$, the corresponding ripple in i_{in_1} is effectively reduced.

2) Resonant regulators: the steady-state experimental results of the methods adopting the resonant regulator $G_{rr}(s)$ and the modified resonant regulator $G_{mrr}(s)$ are presented in Fig. 22c and Fig. 22d, respectively. The implemented $G_{rr}(s)$ and $G_{mrr}(s)$ use $\omega_r = 2\pi \cdot 100\,\mathrm{rad/s}$, $\lambda_1 = 1.6 \times 10^{-1}$, $\lambda_2 = 1.6 \times 10^{-4}$, and $\beta = 1.06$. Notably, the second-order harmonic ripple in i_{in_1} is well eliminated.

The second-order harmonic component in the inductor current is also extracted by performing a discrete Fourier transform (DFT) over a time window of $2.5\,\mathrm{s}$ sampled at $200\,\mathrm{kS/s}$. The results are reported in Table III. Compared to the cases using $G_{nf}(s)$ or $G_{mnf}(s)$, the current ripple is better rejected by solutions $G_{rr}(s)$ or $G_{mrr}(s)$. It should be also noticed that, as the inductor current has a dc component of $5.5\,\mathrm{A}$, the ripple differences between these four methods are relatively small.

Fig. 22a to Fig. 22d display an increase in the bus voltage ripple when harmonic suppression methods are applied. This is due to the larger magnitude of $Z_o(s)$ at twice the line frequency attained by the suppression techniques, which prevents the DER converters from draining the second-order harmonic power affecting the dc bus.

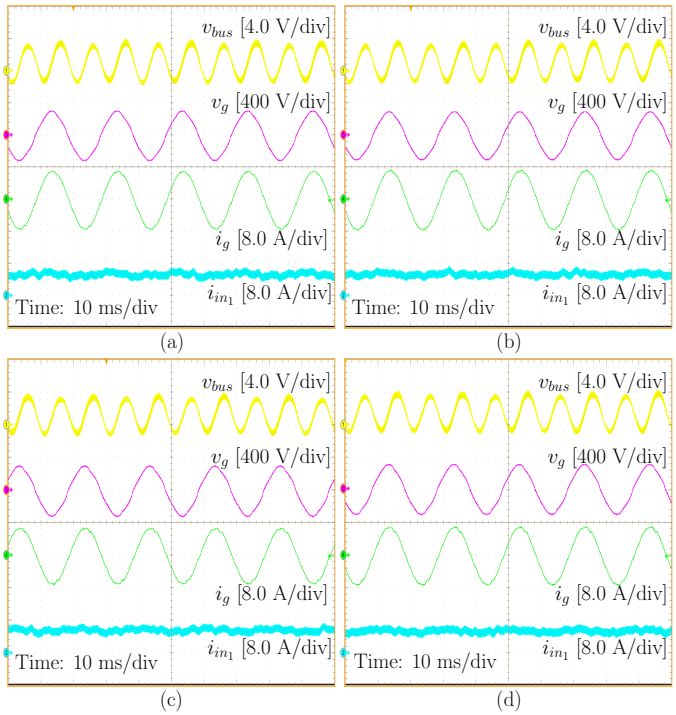

Fig. 22. Steady-state experimental results with different methods. (a) $G_{nf}(s)$; (b) $G_{mnf}(s)$; (c) $G_{rr}(s)$; (d) $G_{mrr}(s)$. v_{bus} offset: 380 V.

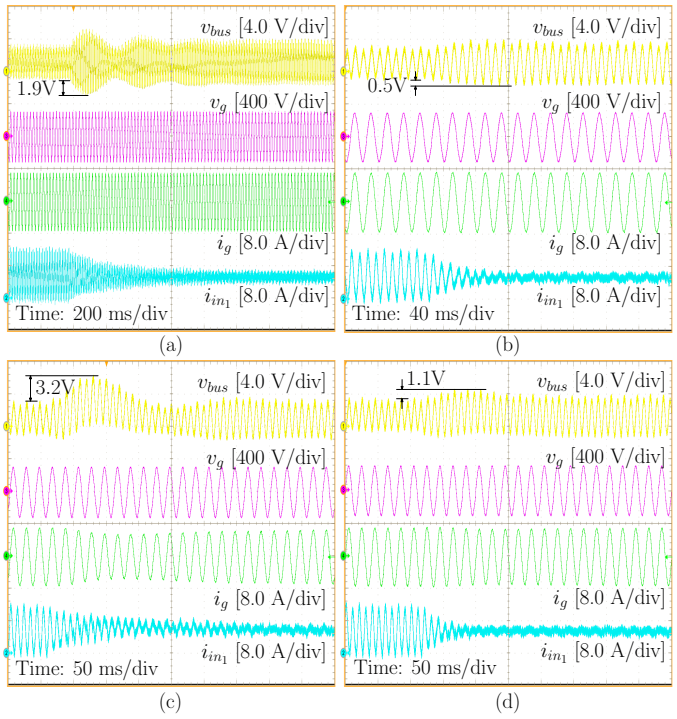

Fig. 23. Dynamic experimental results of activating: (a) $G_{nf}(s)$; (b) $G_{mnf}(s)$; (c) $G_{rr}(s)$; (d) $G_{mrr}(s)$. v_{bus} offset: 380 V.

TABLE III
AMPLITUDE OF SECOND-ORDER HARMONIC CURRENT RIPPLE

Methods	No provision	$G_{nf}(s)$	$G_{mnf}(s)$	$G_{rr}(s)$	$G_{mrr}(s)$
Ripple	6.75 A	0.11 A	0.14 A	0.03 A	0.01 A

C. Evaluation of stability performances

The dynamic processes of activating the second-order harmonic current suppression methods are now reported to show the stability performances of the considered approaches.

1) Notch filters: Fig. 23a shows the experimental result of activating $G_{nf}(s)$. In the dynamic process, an oscillation can be observed in the bus voltage. Looking at the envelope, v_{bus} shows a peak of 1.9 V in the first oscillation cycle and reaches steady state after 3 cycles, which indicates poor a stability margin. Fig. 23b refers to the activation of $G_{mnf}(s)$. As compared to $G_{nf}(s)$, the bus voltage oscillation spike becomes smaller, indicating a better system stability, which shows the advantage of the proposed modified notch filter $G_{mnf}(s)$.

2) Resonant regulators: Fig. 23c and Fig. 23d show the experimental results of activating $G_{rr}(s)$ and $G_{mrr}(s)$, respectively. After activating $G_{rr}(s)$, v_{bus} shows an oscillation with an overshoot of 3.2 V. Whereas, if $G_{mrr}(s)$ is considered, the bus voltage oscillation overshoot reduces to 1.1 V. This shows that the proposed modified resonant regulator $G_{mrr}(s)$ is able to improve the system stability.

D. Evaluation of dynamic performances

The transient processes of load step are presented herein to assess the dynamic speed of DER converters with the modified approaches. In this test, the GIC and three DER converters are all activated. For the purpose of comparison, a low-bandwidth (corresponding to 50 Hz voltage loop bandwidth) voltage regulator, whose transfer function is $1.2 + 153/s$, is also implemented.

1) Notch filters: Fig. 24a shows the experimental result of load change, with the 50 Hz voltage regulator and $G_{mnf}(s)$. Because of the low-bandwidth voltage loop, v_{bus} shows a significant drop during the transient. On the other hand, Fig. 24b shows the experimental result of the same load change, with the default 150 Hz voltage regulator and $G_{mnf}(s)$. Thanks to the increase of the voltage control bandwidth, v_{bus} smoothly transit to the new steady state. Therefore, a high-bandwidth (over $2\omega_g$) voltage loop, which is the benefit brought by the proposed $G_{mnf}(s)$, enables better dynamic performance and tighter dc bus voltage regulation.

2) Resonant regulators: Fig. 24c and Fig. 24d report the experimental results about the dynamic speed with $G_{mrr}(s)$ employed. Performing a load step in the dc microgrid, v_{bus} dips notably in Fig. 24c, with the 50 Hz voltage regulator. On the contrary, the bus voltage drop is not observed with the 150 Hz voltage regulator in Fig. 24d, validating the advantage of the proposed $G_{mrr}(s)$.

VIII. CONCLUSION

This paper presents four second-order harmonic current suppression methods for droop-controlled distributed energy resource converters in dc microgrids coupled with ac power systems. The methods are based on the adoption of *a notch filter*, *a modified notch filter*, *a resonant regulator*, and *a modified resonant regulator*. They all allow converters connected to dc buses presenting a significant second-order harmonic voltage ripple to be free from corresponding current fluctuations

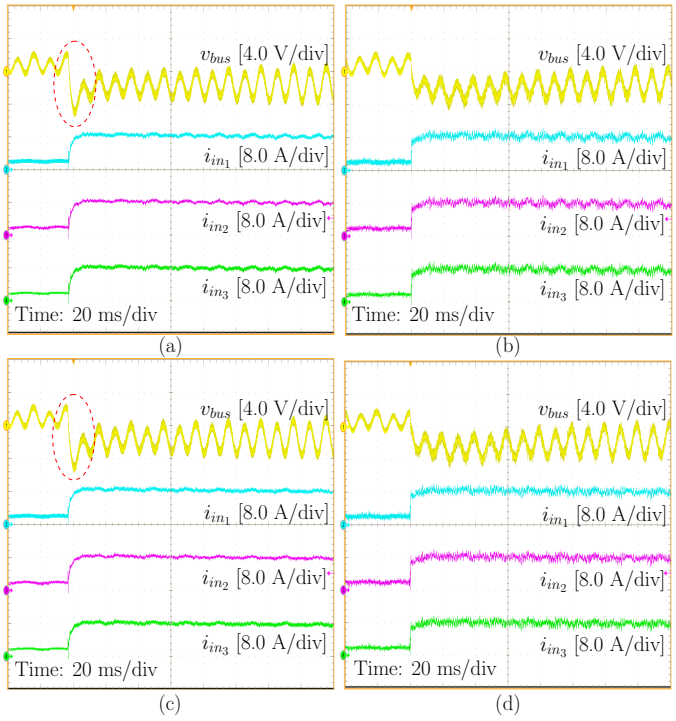

Fig. 24. Dynamic experimental results under load change. (a) Low-bandwidth (i.e., 50 Hz) voltage controller + $G_{mnf}(s)$; (b) high-bandwidth (i.e., 150 Hz) voltage controller + $G_{mnf}(s)$; (c) low-bandwidth voltage controller + $G_{mrr}(s)$; (d) high-bandwidth voltage controller + $G_{mrr}(s)$. v_{bus} offset: 380 V.

at resource side. It is shown that, for the method adopting a notch filter and the one employing a resonant regulator, the voltage control bandwidth is limited to be below $2\omega_g$ to ensure stability, because these methods introduce large phase lags and high attenuation below $2\omega_g$ in the voltage control loop. Instead, in the case of the modified methods proposed in this paper, voltage control bandwidth can be designed to be above $2\omega_g$, while preserving stability and improving the converters dynamics. These four methods are verified experimentally on a prototype composed of three DER converters and one single-phase grid-interface converter.

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