The New Beam Diagnostic Data Readout and Signal Processing System at LNL

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***Abstract*—The ongoing upgrade campaign at the INFN National Laboratories of Legnaro, required to accommodate the SPES facility, demands for a new beam diagnostic system that outperforms the legacy VME based current and beam position monitor. The beam diagnostic is an essential component without whom the operator would blindly attempt to setup all accelerator parameters in order to transport the beam from the source to the target experiment. The paper provides a complete overview of the diagnostic data readout chain inclusive of custom hardware solutions, signal processing, and data management. Each diagnostic point, installed along the beam pipe, consists of a Faraday cup and a beam profile monitor. The frontend electronics is based on a custom general purpose motherboard endowed with an FPGA that handles the data sampling, data filtering and data buffering and with a computer on module that runs an EPICS IOC application and bridges the beam diagnostic information to the control network for remote visualization. The custom hardware platform at the heart of the diagnostic system, is able to perform real time tasks and allows for hardware standardization and modularity, then being the base for embedding the control of several different appliances in our accelerators complex. A precise beam current and position measurement is required by the SPES project that foresees a radioactive ion beam in a wide range of intensities and energies. The prototypes of the new electronics have shown good performance improvements and the beam current resolution has been extended to few pA.**

***Index Terms*—beams, diagnostics, data acquisition, front-end electronics, data processing, FPGAs, charge collection.**

I. Introduction

SELECTIVE Production of Exotic Species (SPES) is a second generation Isotope Separation On-Line (ISOL) Radioactive Ion Beam (RIB) facility in construction at the National Laboratory of Legnaro, Italy [1]. The primary proton beam generated by a 70 MeV cyclotron collides with an uranium carbide (UCx) target and the reaction products, properly extracted, selected and ionized, will be reaccelerated and transported to the experimental halls using the existing LINAC accelerator (ALPI). Hardware and software must be upgraded to accommodate the requirements of the SPES project [2]. In particular, the upgrade campaign of ALPI involves the the beam diagnostic system [3] and the Radio Frequency (RF) control system [4]. The diagnostic system has particular importance since the neutron-rich beams foreseen by SPES project will be characterized by a wide range of intensities and energies moving along the vacuum chamber from the RIB source to the experimental halls. Therefore, the diagnostic boxes and the readout electronics currently used in ALPI, must be upgraded in order to extend the beam profile and current measurements resolution to few pA. The document describes the diagnostic instruments, diagnostic data acquisition and the digital signal processing of such system. The core of the new beam diagnostic readout system is a custom general purpose Input Output Controller (IOC) board that acts as a local intelligent node in the distributed control network and replaces legacy VME crates by providing computational power and a large number of I/O functions all integrated in a compact module [5]. The diagnostic application highlights the advantages of this embedded controller with respect to low cost commercial microprocessor boards in terms of:

- Flexibility. The IOC board is general enough to be exploited in several different applications spanning from simple slow control tasks to complex data processing operations requiring an high level of computational power.
- Modularity. The controller functionality can be easily extended with commercial solutions in PCIe or FMC Low Pin Count (LPC) form factors.
- The on board FPGA provides support for fast peripherals control and real time tasks.
- Standardization. The IOC board is based on the COM Express standard [6] and the IOC concept will be the base for hardware standardization at LNL.
- The possibility to boot a standard Linux distribution and the x86_64 architecture makes software development independent from the underlying hardware layer and facilitates the software portability between platforms. The integration of the new hardware in the control system is straightforward.

II. Beam Diagnostic Instruments

Part of the SPES facility is completely new, while for the rest exploits the existing linear accelerator ALPI, whose layout is shown in Figure 1. The beam transport system accelerates, focuses and shapes the beam while guiding it from the source to the experimental halls. It mainly consists in a series of three components: lenses (both magnetic and electrostatic) that bend and focus the beam in the vacuum chamber, accelerating

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RF cavities, bunchers and beam diagnostic instruments that provide a feedback to the operator while transporting the beam.

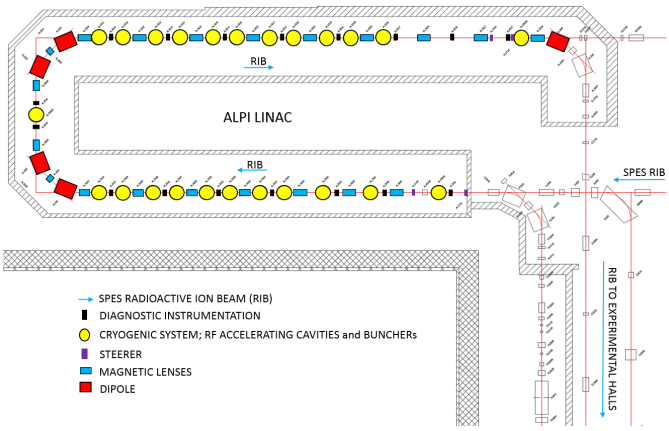

Fig. 1. ALPI Superconducting Linear Accelerator Layout

All these devices are integrated in the distributed control network and their relevant process variables should be remotely accessible in view of an automatic beam transport system. To accomplish this, a big effort was required to develop and integrate custom and commercial hardware and software solutions to embed the control of all the devices involved in the beam transport operations. The main concept underlying the beam diagnostic system upgrade process is that the diagnostic instruments and their readout electronics must provide support for a wide range of beams. Indeed ALPI must be backward compatible with previously projects that accelerate stable single-charged beams of single species from ^{28}Si to ^{197}Au, with intensities up to mA, and, at the same time, must accommodate the new SPES requirements. The SPES project foresees the usage of Cs, Xe, Rb, Ba, Br, Sn and many others neutron-rich ion beams, that, in same cases, may have intensities as low as 10^4 ions per second (fA range); in this contest the usage of a stable pilot beam is mandatory. The desired atom species will be selected by an High-Resolution Mass Separator (HRMS) that removes isobar ions prior the injection in ALPI. Regardless of the accelerated species, the beam diagnostic system should help the understanding of the beam behavior under normal and abnormal conditions, providing the operator with a monitor on the beam losses along the accelerator pipe and allowing the improvement of the transport efficiency. Some of the main parameters to be measured and that characterize the beam are the intensity, the transverse centroid and the transverse beam profile.

A. Beam Intensity

The intensity can be measured via destructive or non destructive methods. Non destructive measurements allow the monitoring of online beam intensity fluctuation. Those techniques are usually complex and their accuracy rarely reaches the nA range, therefore are not treated in this paper since their usage is limited. In SPES, several Faraday cup monitors are used to measure beam intensities from few pA to hundreds of µA.

B. Vertical and Horizontal Beam Profiles

Profile measurements yield information about the 2D projection of the beam as well as the position of the beam centroid. Extensive experience at LNL confirms the possibility to use a grid of wires as Beam Profile Monitor (BPM) for accelerators with beam size in the cm or sub-cm range [7]. We investigated the beam intensity sensitivity achievable using the grid as BPM when accelerating low intensity beams since online and semi-interceptive methods are of particular interest for radioactive ion beams facilities. Conversely, dealing with high intensity beams, the robustness of BPM is the main concern since a long term exposure to the beam, may damage the thin wires losing the measurement resolution.

III. Diagnostic Box

The diagnostic box is an extension of the vacuum chamber that accommodates all the instruments necessary to determine the beam position, profile and current intensity. The 3D section view is shown in Figure 2.

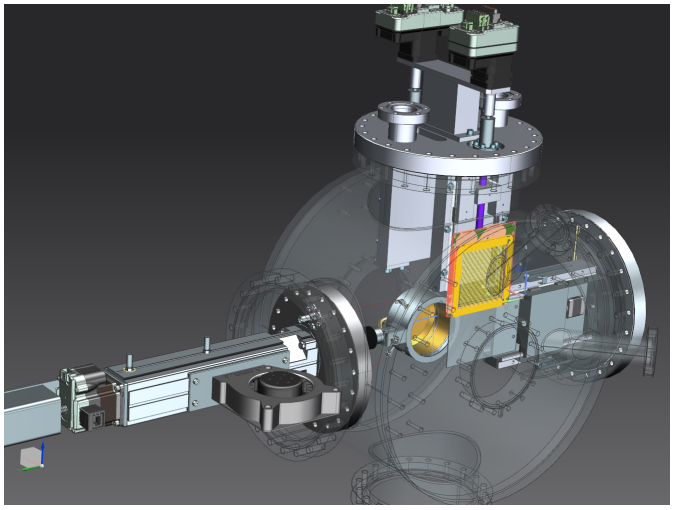

Fig. 2. Diagnostic Box

The diagnostic box, the Faraday cup and the BPM (both highlighted in yellow) have been entirely designed at LNL. The custom BPM consists of a carrier board plus a top board which holds a mesh of thin wires (forty horizontal and forty vertical) made of gold plated tungsten (50 µm diameter) equally spaced. This grid is produced in different spacings (250 µm, 500 µm, 1 mm and 2 mm) for beams with size ranging from 1 cm up to 8 cm. The grid prototypes have been manufactured with a dielectric (Rogers RO3003™) that ensures excellent electrical and mechanical properties over a wide temperature range [8]. Furthermore, this ceramic-filled PTFE composite suits high vacuum applications. Profile grids can be used with DC as well as bunched beams; the relevant information being the average charge deposited on the wire.

The Faraday cup consists of a copper cup that intercepts the beam and the resulting current is measured and used to determine the number of ions hitting the cup per second. The electric current measured is proportional to the number of ions trapped in the cup according to (1):

$$\frac{N}{t} = \frac{I}{e} \tag{1}$$

where N is the number of ions observed in a time t, assuming each ion with a single charge, I is the measured current and e the elementary charge. Cooling is ensured by a heat pipe connected to the copper cup via a Shapal™ ceramic tablet which ensures high thermal conductivity and excellent electrical insulation at the same time [9]. The main source of error is represented by the emission of secondary electrons from the copper surface struck by incident ions, and, by the back scattering of incident particles. For this purpose an electron-suppressor plate kept at high voltage prevents the escape of secondary electrons from the cup and reduces the back scattering problem. Previous installations demonstrate that the Faraday cup suits well to measure low intensity beams and that the current sensitivity is independent from the ions mass and therefore from the type of RIB.

IV. Diagnostic Data Readout Chain

The sensitivity to low intensity beams can be achieved thanks to very sensitive diagnostic devices and improving the quality of the readout electronics to enhance the signal to noise ratio (SNR). An overview of the new diagnostic data readout chain is given in Figure 3. Each diagnostic point consists of a BPM and a Faraday cup as described previously. Beam profile information is first elaborated by an analogue frontend board. This preamplifier board converts the charge deposited by the beam on the wire in a proper voltage signal through a transimpedance amplifier (TIA) built with a very low bias current Operational Amplifier (OpAmp). The TIA presents a very low input impedance to the current source thanks to the high open loop gain which is in the order of 10^8 since the load resistance of the OpAmp is tens of MΩ in our configuration. The feedback network, digitally selectable by the end user, is composed by a resistor whose value is reasonably high to increase the current sensitivity, and a capacitor. The DC gain of the current to voltage converter can be set to 10^6, 10^7, 10^8 or 10^9, depending on the beam current sensitivity to be achieved. The low pass filter behavior is also imposed by the RC feedback network and the bandwidth is 10 Hz for all the gain configurations. The voltage offset of the OpAmp is negligible in our measurements due to the high value of the feedback resistor and the high impedance of the grid wire that behaves like an ideal current source. Whereas the bias current is the main source of error of this stage, it is very important to choose an OpAmp with a very low bias current to avoid complex calibrations. The preamplifier board hosts 40 TIAs and multiplexes the 40 input channels to a single voltage output channel, subsequently digitized inside the IOC board. In the case of beam current information, the analogue signal is fed to a commercial 4-channels FMC picoampere meter directly coupled with an FPGA. The custom IOC board is the core of the readout system. The FPGA ensures a good level of hardware abstraction and performs real time tasks like the BPM scan, the ADC conversions, data buffering and data transfer to the processor. The COM

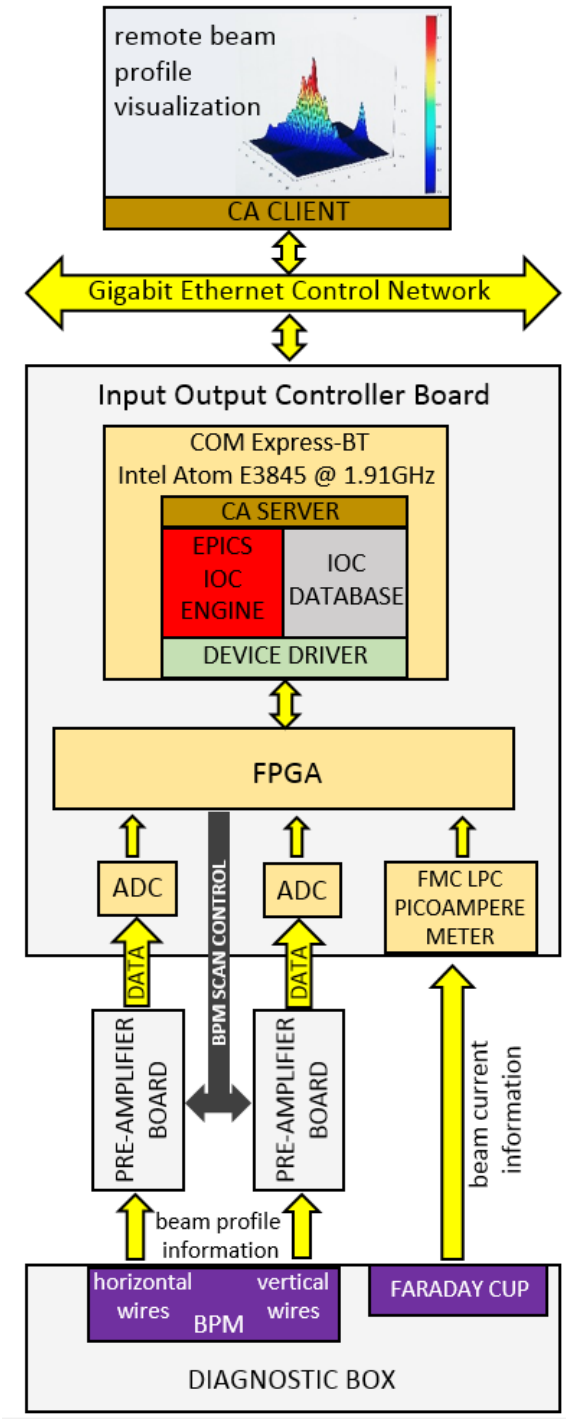

Fig. 3. Diagnostic Data Readout Chain Overview

Express module implements an EPICS database and channel access server making the diagnostic data remotely available. A single IOC board serves up to 4 diagnostic points exploiting the 4-channels mezzanine card and eight on board Analogue to Digital Converters (ADC). The preamplifier boards and IOC board will be installed in a diagnostic rack located tens of meters away from the beam line in order to avoid worries about damage or malfunction caused by ionizing radiation. In this configuration, the electronic cards will be accessible during the

run of the experiment for maintenance. The test performed on the field demonstrate that cables leakage currents do not affect the DC current sensitivity using a very low input impedance TIA stage. The noise introduced by inductive coupling on the cables is mitigated using shielded cables and a suitable low pass filter, digitally implemented inside the FPGA.

V. Input Output Controller Board

The IOC board is a custom COM Express carrier board [10] that provides a wide variety of interfaces and connectivity options, being general enough to become the basis for hardware standardization at the LNL. Alongside the generic PC functionalities that are readily available in the computer on module, the custom motherboard, has been endowed with more application specific features, not commonly found in a desktop PC, linked to the on board FPGA. The end user can deal with a general purpose PC, or it may exploit the FPGA potentialities in terms of fast peripherals control, data acquisition, data buffering and fast data preprocessing, to perform real time tasks. The modularity and functionality extension is ensured by three PCIe 1.0 slots and the FMC LPC connector. A bidirectional optical link, Power Over Ethernet (PoE), CAN bus interface, eight RS422 serial interfaces and the high number of digital and analogue general purpose input and output channels are all added values that make the board particularly suitable for embedding the control of several appliances in our facility. A first production lot of twenty boards has been carried out and fully tested. The beam diagnostic readout system is the first integration of the IOC board in the control system of the SPES accelerators complex. The COM Express module chosen for the diagnostic application is the compact Express-BT which exploits an Intel Atom E3845 @ 1.91 GHz processor and boots a standard Linux distribution. The module supports a Gigabit Ethernet connection. Figure 4 shows the IOC box and the preamplifier box assembled.

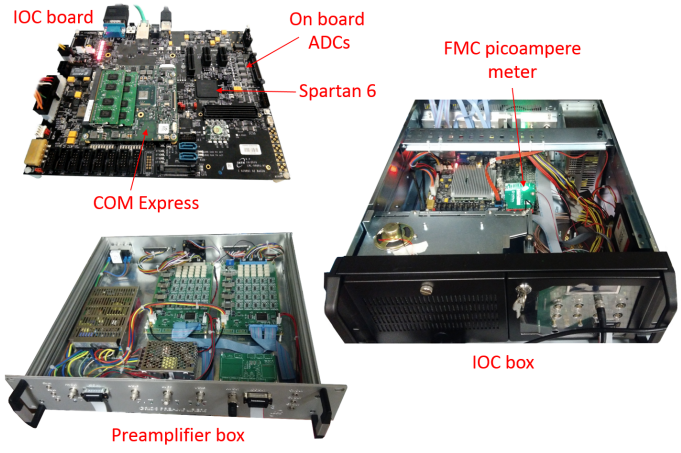

Fig. 4. IOC Board, IOC Box, Preamplifier Box

The preamplifier box contains two preamplifier boards that scan and multiplex the 40 horizontal and 40 vertical BPM wires. The wire scan and multiplexing are an example of real time tasks requiring an hardware support. These operations are readily implemented in VHDL, in the Spartan-6 FPGA of the carrier board, and the sampled values made available to the local Linux operating system.

VI. FPGA Digital Data Processing

The primary task of the register-transfer level (RTL) design is to provide a local management and transparent mapping of the process variables of the peripherals under control. This highlights the importance of establishing a reliable link between the processor and the FPGA. This is accomplished through a USB bridge that, together with the FPGA firmware, virtualizes a 32-bits parallel bus between the FPGA and the processor. In the processor, an user space Application Programming Interface (API) provides the user with all the necessary calls to perform read and write operations. The Cypress bridge transfers these read and write operations to the FPGA where the *usb interface core* acts as a parallel port end point. This IP foresees multiple memory busses in order to route the read and write requests to the correct memory slave. An overview of the flow of the digital signals and the main logical operations performed in the diagnostic readout system is given in Figure 5.

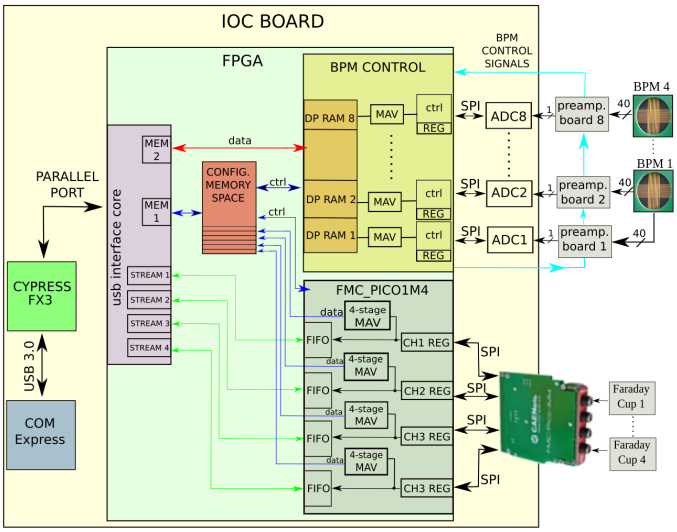

Fig. 5. RTL Design

The communication between host and hardware takes place through the exchange of frames containing address, data and header fields. The header specifies the source ID, destination port, direction, type of interface, data size, error codes. The *usb interface core* encodes and decodes these packets routing the information from/to the correct stream or memory port. The supported transfer types are:

- memory: single register (double word) read and write operations.
- stream: block read and write operations (similar to a Direct Memory Access (DMA) data transfer).

Hardware interrupt is also supported by the core. For example, the interrupt routine may be used as a back-pressure signal indicating that the internal FIFO memory is almost full.

The memory port 1 is reserved for the configuration space that is a stack of control and status registers with all the relevant device variables mapped here. Some of these registers are used to store the DC beam current measurements. The memory port 2 is attached to 8 consecutive banks of dual port RAM. Each bank is composed of 40 registers, one register for each horizontal or vertical wire of the BPM. The FMC picoampere meter control core, *FMC_PICO1m4*, interfaces the mezzanine card and controls the conversion and data acquisition from four Faraday cups. The user can select the continuously sampling mode and readout raw data streams, or, access the beam current value filtered by a Moving Average (MAV) filter [11]. The digital MAV filter reduces random noise while retaining a sharp step response and is the ideal solution to get DC current information from the Faraday cup or BPM. The MAV implemented is a multiple-pass filter and the user can remotely set the number of stages and the number of samples per stage via the configuration space. The adoption of MAV filters leads to a sensible improvement of the DC beam current sensitivity with respect to the present situation. The *BPM CONTROL* core generates the digital outputs necessary to control the digitization of the vertical and horizontal beam position signals generated by the BPM. These BPM control signals, shown in Figure 6, are connected in a daisy chain topology of up to 8 preamplifier boards, and back to the IOC board.

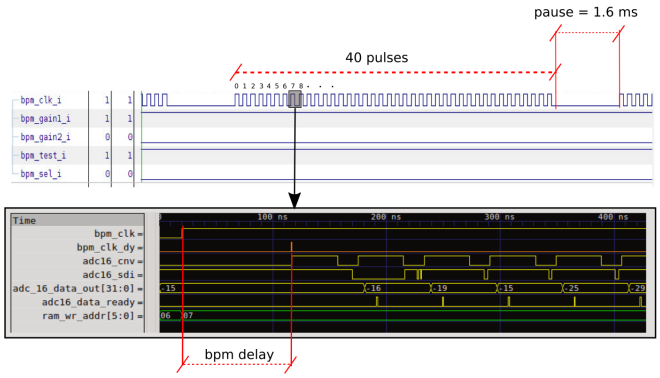

Fig. 6. BPM Control Signals

The grid scan is synchronized with the BPM clock signal enabled by the reception of a start command from the operator, and alternates bunches of forty consecutive pulses with pause intervals. Each clock pulse lasts for 200 µs and schedules the charge acquisition from the corresponding wire in all the grids of the daisy chain, e.g., during the seventh clock period, the seventh horizontal and vertical wires of each BPM in the chain are multiplexed to the corresponding ADC in the IOC board. Since the 8 ADCs are forced to operate simultaneously, it was necessary to introduce a delay (*bpm delay*) to wait for the last preamplifier board in the daisy chain to receive the clock edge and output the right value, before starting the acquisition. Since the interesting value is the DC current of the wires, during each clock pulse we average 64 consecutive samples with a single stage MAV filter.

VII. Current Sensitivity Characterization

The test results proposed in this section demonstrate that the current sensitivity has been extended to few pA.

A. BPM Readout Sensitivity

The noise floor of beam profile monitors was evaluated with the forty preamplifier's input channels unconnected, and therefore virtually grounded by the transimpedance amplifier. Each single point in Figure 7 is computed from the average of 64 consecutive samples as explained previously. The noise

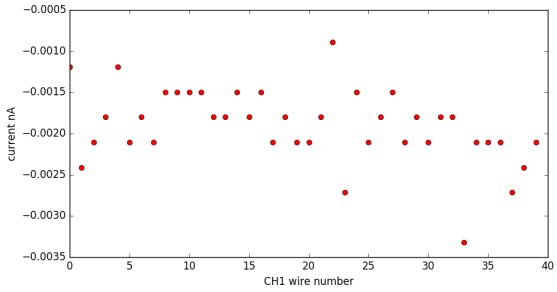

Fig. 7. BPM Readout Noise Floor

introduced by the electronics processing leads to an error of about 3 pA. This value can be considered as the best case: readout resolution on the field will be affected by cabling, connectors, grounding and current source stability [12]. In lab tests the current on the wire has been emulated with the Keithley 6430 sub femtoampere, low noise, high stability DC current source, using a triaxial probe to inject the current to one out of 51 poles of the shielded cable connected to the preamplifier board. The test setup is shown in Figure 8.

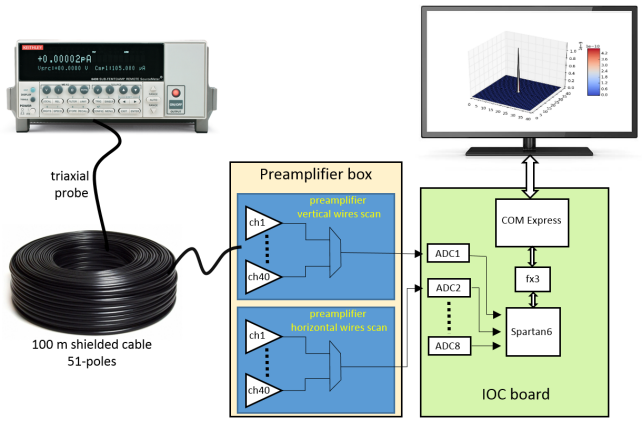

Fig. 8. BPM Current Sensitivity Characterization Setup

A BPM scan lasting 10 seconds at 10 Hz rate has been performed with the current injected in one of the forty vertical wires first, and in the corresponding horizontal wire after and the scanned data have been processed offline using Python Matplotlib. The virtual BPM matrix be reconstructed from the 10 seconds averaged horizontal and vertical vectors. The test was repeated decreasing the injected current and the results are shown in Figure 9, in 3D surface plots and 2D plots.

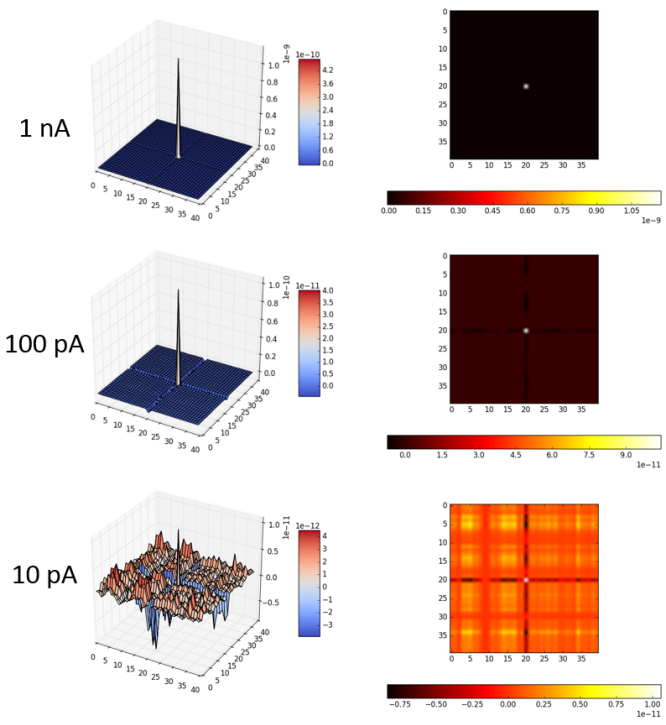

Fig. 9. BPM Readout Sensitivity

These results validate the proposed BPM readout method, and confirm that the BPM current resolution has been extended to 10 pA per wire. The test confirms also that the preamplifier boxes can be located 100 m away from the beam pipe without affecting the current sensitivity. A key point is preserving the electronics from radiation during RIB transport, and the accessibility of the readout modules during beam time.

B. Faraday Cup Readout Sensitivity

A similar approach was adopted for testing the Faraday cup readout sensitivity as shown in Figure 10.

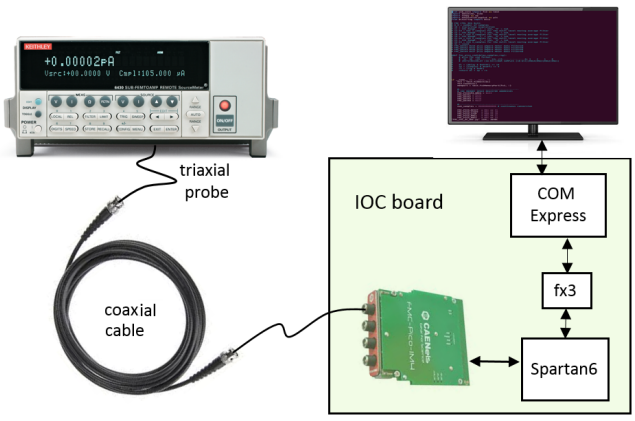

Fig. 10. Faraday Cup Current Sensitivity Characterization Setup

The precise current source injects the current in a coaxial cable connected to the mezzanine picoampere meter hosted in the IOC board. The four channels have two measuring ranges of ±1 mA and ±1 µA, customizable by the user. The 20-bits resolution ADCs in the µA range, ideally, yield a resolution of 1.9 pA. The measurements shown in Figure 11 refer to a sampling rate of about 864 Ksps, continuous conversion mode. Samples are continuously gathered into the multistage MAV filter whose latency, in number of samples, is given by (2).

$$(samples\_per\_stage)^{number\_of\_stages} \tag{2}$$

The red dots in the plots represent 100 consecutive software read operations executed at 10 Hz rate. To readout smaller currents the number of samples per stage of the MAV filter has been increased with the consequent bandwidth reduction from ten Hz to sub Hz (e.g., with 64 samples and 4 stages, the filter latency is about 20 seconds). The software access rate should decrease accordingly. The experimental results confirm the need to average the samples through a multiple-pass MAV filter in order to decrease the input noise and to extend the resolution to the least significant bit (2 pA).

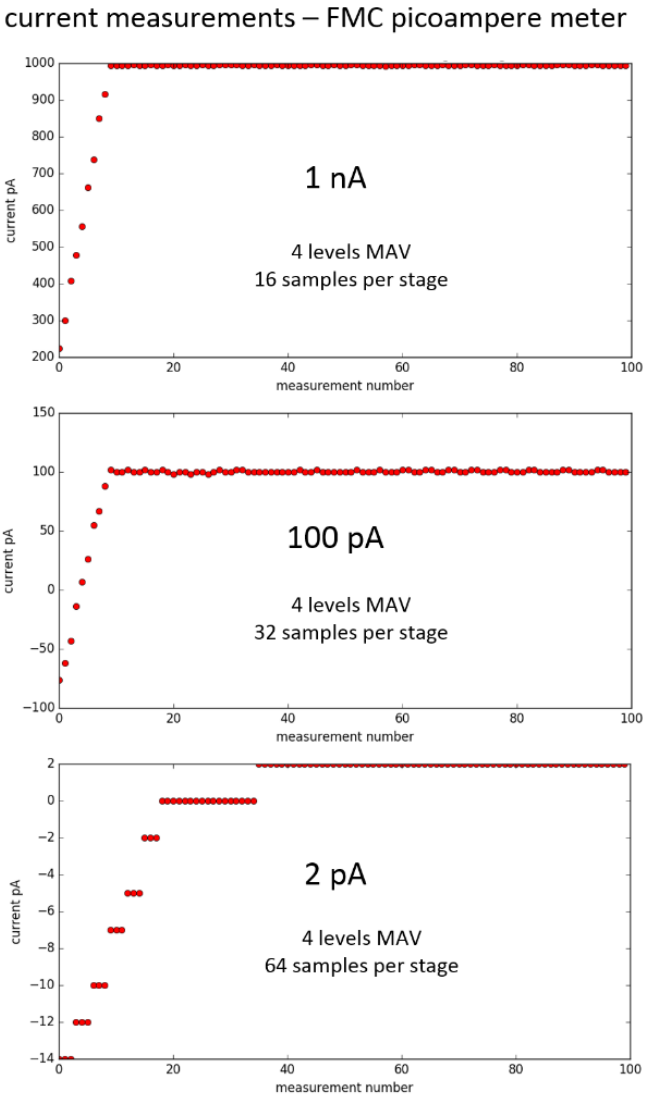

Fig. 11. Faraday Cup Readout Sensitivity

VIII. Beam Profile Measurement

The measurements reported above are a candidate proposal for the replacement of the legacy VME based diagnostic system [13]. Tests performed under real beam conditions in the SPES frontend laboratory confirmed this possibility. The SPES frontend laboratory, used to emulate the target-ion source chamber and RIB extractor, is endowed with a low energy ion source, magnetic lenses, a vacuum system (about 10^{-6} mbar) and three diagnostic points exploited to test the new diagnostic readout and signal processing system. The first beam profile measure was made with a 25 keV, 13.5 nA, N_2^+ beam. The BPM installed in that diagnostic station was a grid of 400 µm diameter steel wires, 1 mm step. Figure 12 shows the vertical and horizontal beam profiles and the 2D and 3D beam intensity reconstructions.

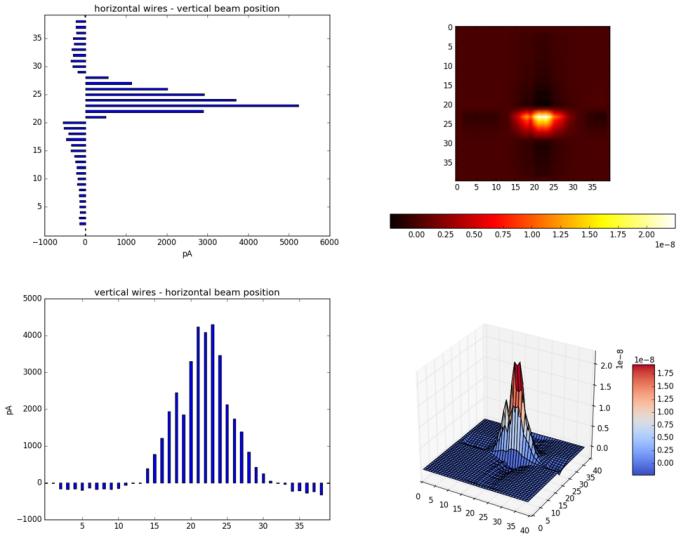

Fig. 12. Beam Profile Measure. 25 keV, 13.5 nA, N_2^+ beam

The impact of the secondary electrons is relevant and appreciable on the beam profile measurement since it amplifies the positive charge of the wires hit by the beam while generating a negative current on neighboring wires. The beam current has been monitored during the tests with a Faraday cup. Switching the voltage on the secondary electron suppressor of the Faraday cup, it was possible to quantify the contribution of the secondary electrons on the beam current measurements by a factor 4.6. Moreover measuring the beam current with the BPM inserted in the vacuum chamber in front of the Faraday cup we could estimate the transparency of the grid used that is about 33%. Beam profile measurements were repeated under different beam current intensities and the new readout electronics outperforms the old one being able to successfully characterize beams with currents as low as 250 pA. Figure 13 refers to a 250 pA, 25 keV, N_2^+ beam: tens of pA per wire is well in the range of the new diagnostic system.

The integration of the new hardware in the control system is straightforward and is based on the EPICS framework concept [14]. The software architecture has been easily ported from the old hardware and the EPICS IOC application runs in the COM

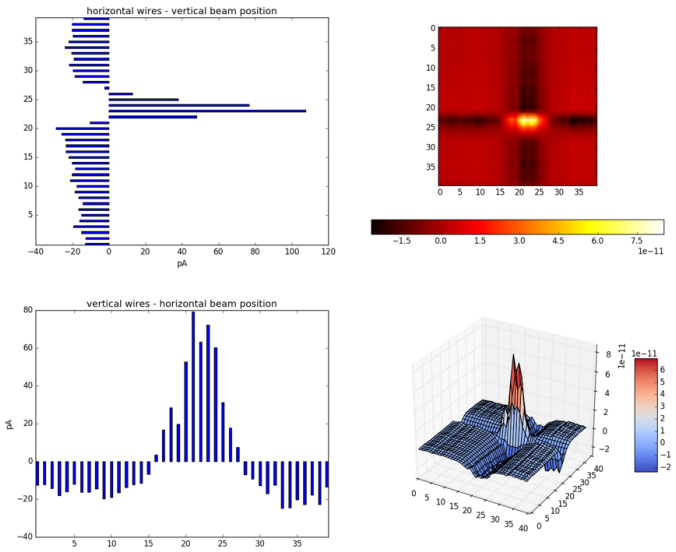

Fig. 13. Beam Profile Measure. 25 keV, 250 pA, N_2^+ beam

Express module providing remote access to all the relevant process variables mapped in the memory configuration space inside the FPGA. In the superconducting linear accelerator ALPI, in operation at LNL, the new diagnostic readout system has been successfully integrated in the diagnostic station DI9. Figure 14 shows a screenshot of the beam profile in DI9 during a test with a 7.7 MeV, ^{15}N beam of charge 2^+. The

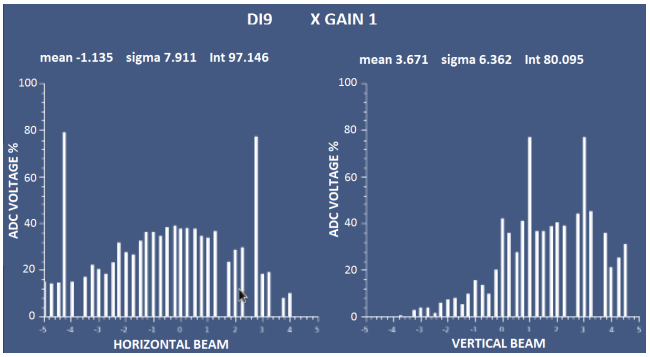

Fig. 14. Beam Profile Measure in ALPI DI9. 7.7 MeV, 110 nA, ^{15}N beam

beam current was set to 110 nA for the whole duration of the measurements. The beam has been intercepted with a standard mesh of wires of diameter 50 µm and step 1 mm: saturated wires or absent are due to damaged grids due to mechanical shocks or long exposure to beam. Figure 15 shows the measured beam current versus the voltage applied to the secondary electrons suppressor; due to the large radius of the tested Faraday cup, the potential needed to suppress secondary electrons was as high as few kV [15].

IX. Conclusion

The Input Output Controller designed is proving to be a reliable solution to standardize the control of several appliances in the SPES accelerators complex. This custom universal controller is the core of the new diagnostic readout

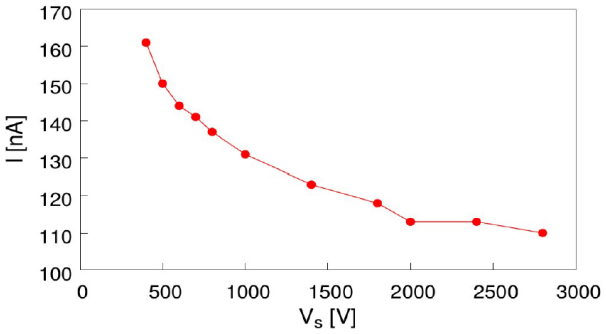

Fig. 15. Current vs Secondary Electrons Suppressor Voltage

system that extends the beam profile sensitivity and current resolution to the pA range. The integration of the new hardware in the control network is straightforward thanks to the IOC architecture which makes the software development and portability independent from the hardware layer. Real time applications are now completely supported by the on board FPGA freeing the Operating System from complex time-critical tasks. The experimental measurements validate the extensive work done developing the diagnostic frontend electronics hereby presented, and show improvements on the beam profile characterization, essential for the transport of the low intensity RIB foreseen by SPES project.

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